



## A422604 Series

### 4M X 4 CMOS DYNAMIC RAM WITH EDO PAGE MODE

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#### Document Title

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#### Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue	July 23, 2003	
1.0	Remove 24/26-pin TSOP type II package	March 26, 2009	Final



# A422604 Series

## 4M X 4 CMOS DYNAMIC RAM WITH EDO PAGE MODE

### Features

- Organization: 4,194,304 words X 4 bits
- Part Identification
  - A422604 (2K Ref.)
- Single 5.0V power supply/built-in VBB generator
- Low power consumption
  - Operating: 120mA (-50 max)
  - Standby: 1.0mA (TTL), 0.5mA (CMOS), 0.5mA (Self-refresh current)
- High speed
  - 50/60 ns  $\overline{\text{RAS}}$  access time
  - 22/27 ns column address access time
  - 13/15 ns  $\overline{\text{CAS}}$  access time
  - 20/24 ns EDO Page Mode Cycle Time
- Fast Page Mode with Extended Data Out
- 2K Refresh Cycle in 32ms
- Read-modify-write,  $\overline{\text{RAS}}$ -only,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ , Hidden refresh capability
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 300mil, 24/26-pin SOJ

### General Description

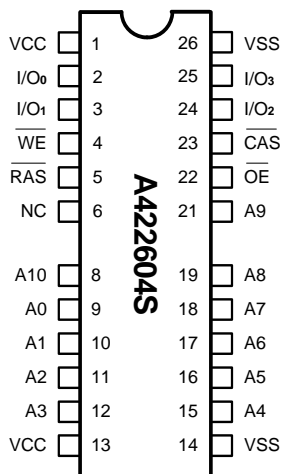
The A422604 is a new generation randomly accessed memory for graphics, organized in a 4,194,304-word by 4-bit configuration. This product can execute Write and Read operation via  $\overline{\text{CAS}}$  pin.

The A422604 offers an accelerated Fast Page Mode cycle with a feature called Extended Data Out (EDO).

This allow random access of up to 2048(2K Ref.) words within a row at a 50/42 MHz EDO cycle, making the A422604 ideally suited for graphics, digital signal processing and high performance computing systems.

### Pin Configuration

#### ■ SOJ



### Pin Descriptions

Symbol	Description
A0 - A10	Address Inputs (2K product)
I/O <sub>0</sub> - I/O <sub>3</sub>	Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
VCC	5.0V Power Supply
VSS	Ground
NC	No Connection

**Selection Guide**

Symbol	Description	-50	-60	Unit
t <sub>RAC</sub>	Maximum $\overline{\text{RAS}}$ Access Time	50	60	ns
t <sub>AA</sub>	Maximum Column Address Access Time	22	27	ns
t <sub>CAC</sub>	Maximum $\overline{\text{CAS}}$ Access Time	13	15	ns
t <sub>OE</sub>	Maximum Output Enable ( $\overline{\text{OE}}$ ) Access Time	13	15	ns
t <sub>rc</sub>	Minimum Read or Write Cycle Time	84	100	ns
t <sub>pc</sub>	Minimum EDO Cycle Time	20	24	ns

**Functional Description**

The A422604 reads and writes data by multiplexing an 22-bit address into a 11-bit(2K) row and column address.  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are used to strobe the row address and the column address, respectively.

A Read cycle is performed by holding the  $\overline{\text{WE}}$  signal high during  $\overline{\text{RAS}}/\overline{\text{CAS}}$  operation. A Write cycle is executed by holding the  $\overline{\text{WE}}$  signal low during  $\overline{\text{RAS}}/\overline{\text{CAS}}$  operation; the input data is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs later. The data inputs and outputs are routed through 4 common I/O pins, with  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{OE}}$  controlling the in direction.

EDO Page Mode operation all 2048(2K) columns within a selected row to be randomly accessed at a high data rate. A EDO Page Mode cycle is initiated with a row address latched by  $\overline{\text{RAS}}$  followed by a column address latched by  $\overline{\text{CAS}}$ . While holding  $\overline{\text{RAS}}$  low,  $\overline{\text{CAS}}$  can be toggled to strobe changing column addresses, thus achieving shorter cycle times.

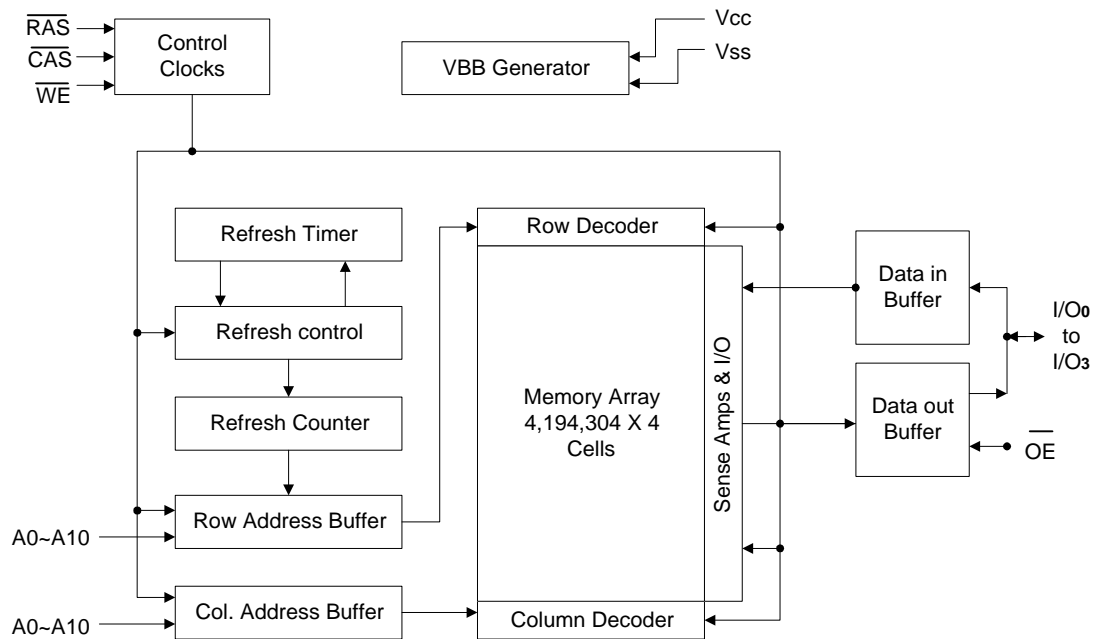
The A422604 offers an accelerated Fast Page Mode cycle through a feature called Extended Data Out, which keeps the output drivers on during the  $\overline{\text{CAS}}$  precharge time (t<sub>cp</sub>). Since data can be output after  $\overline{\text{CAS}}$  goes high, the user is not required to wait for valid data to appear before starting the

next access cycle. Data-out will remain valid as long as  $\overline{\text{RAS}}$  and  $\overline{\text{OE}}$  are low, and  $\overline{\text{WE}}$  is high; this is the only characteristic which differentiates Extended Data Out operation from a standard Read or Fast Page Read.

A memory cycle is terminated by returning both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  high. Memory cell data will retain its correct state by maintaining power and accessing all 2048(2K) combinations of the 11-bit(2K) row addresses, regardless of sequence, at least once every 32ms through any  $\overline{\text{RAS}}$  cycle (Read, Write) or  $\overline{\text{RAS}}$  Refresh cycle ( $\overline{\text{RAS}}$ -only, CBR, or Hidden). The CBR Refresh cycle automatically controls the row addresses by invoking the refresh counter and controller.

**Power-On**

The initial application of the VCC supply requires a 200  $\mu\text{s}$  wait followed by a minimum of any eight initialization cycles containing a  $\overline{\text{RAS}}$  clock. During Power-On, the VCC current is dependent on the input levels of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with VCC or be held at a valid V<sub>IH</sub> during Power-On to avoid current surges.

**Block Diagram**

**Recommended Operating Conditions** (Ta = 0°C to +70°C)

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	4.5	5.0	5.5	V
VSS	Input High Voltage	0.0	0.0	0.0	V
V <sub>IH</sub>	Input High Voltage	2.4	-	VCC + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5	-	0.8	V

**Truth Table**

Function	RAS	CAS	$\overline{WE}$	$\overline{OE}$	Address	I/Os
Standby	H	H	X	X	X	High-Z
Read: Word	L	L	H	L	Row/Col.	Data Out
Read	L	L	H	L	Row/Col.	Data Out
Write: Word (Early)	L	L	L	X	Row/Col.	Data In
Write (Early)	L	L	L	X	Row/Col.	Data In
Read-Write	L	L	H→L	L→H	Row/Col.	Data Out → Data In
EDO-Page-Mode Read: Hi-Z						
-First cycle	L	H→L	H	H→L	Row/Col.	Data Out
-Subsequent Cycles	L	H→L	H	H→L	Col.	Data Out
EDO-Page-Mode Write(Early)						
-First cycle	L	H→L	L	X	Row/Col.	Data In
-Subsequent Cycles	L	H→L	L	X	Col.	Data In
EDO-Page-Mode Read-Write						
-First cycle	L	H→L	H→L	L→H	Row/Col.	Data Out → Data In
-Subsequent Cycles	L	H→L	H→L	L→H	Col.	Data Out → Data In
Hidden Refresh Read	L→H→L	L	H	L	Row/Col.	Data Out
Hidden Refresh Write	L→H→L	L	L	X	Row/Col.	Data In → High-Z
$\overline{RAS}$ -Only Refresh	L	H	X	X	Row	High-Z
CBR Refresh	H→L	L	X	X	X	High-Z
Self Refresh	H→L	L	H	X	X	High-Z

**Absolute Maximum Ratings\***

Input Voltage (Vin) . . . . .	-1.0V to 7.0V
Output Voltage (Vout) . . . . .	-1.0V to 7.0V
Power Supply Voltage (VCC) . . . . .	-1.0V to 7.0V
Operating Temperature (TOPR) . . . . .	0°C to +70°C
Storage Temperature (TSTG) . . . . .	-55°C to +150°C
Soldering Temperature X Time (TSOLDER) . . . . .	260°C X 10sec
Power Dissipation (Pd) . . . . .	1W
Short Circuit Output Current (Iout) . . . . .	50mA
Latch-up Current . . . . .	200mA

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics (VCC = 5.0V ± 10%, VSS = 0V, Ta = 0°C to +70°C)**

Symbol	Parameter	-50		-60		Unit	Test Conditions	Notes
		Min.	Max.	Min.	Max.			
IIL	Input Leakage Current	-5	+5	-5	+5	μA	0V ≤ Vin ≤ Vin + 0.2V Pins not under Test = 0V	
IoL	Output Leakage Current	-5	+5	-5	+5	μA	DOUT disabled, 0V ≤ Vout ≤ + VCC	
Icc1	Operating Power Supply Current	-	120	-	115	mA	$\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS}$ Address cycling; trc = min.	1, 2
Icc2	TTL Standby Power Supply Current	-	1.0	-	1.0	mA	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IH}$	
Icc3	Average Power Supply Current, RAS Refresh Mode	-	120	-	115	mA	$\overline{RAS}$ cycling, $\overline{UCAS} = \overline{LCAS} = V_{IH}$ , trc = min.	1
Icc4	EDO Page Mode Average Power Supply Current	-	90	-	85	mA	$\overline{RAS} = V_{IL}$ , $\overline{UCAS}$ , $\overline{LCAS}$ Address cycling; tpc = min.	1, 2
Icc5	$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Power Supply Current	-	120	-	115	mA	$\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS}$ cycling; trc = min.	1
Icc6	CMOS Standby Power Supply Current	-	0.5	-	0.5	mA	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} =$ VCC - 0.2V	
Icc7	Self Refresh Mode Current	-	0.5	-	0.5	mA	$\overline{RAS} = \overline{CAS} \leq VSS + 0.2V$ All other input high levels are VCC-0.2V or input low levels are VSS +0.2V	
VOH	Output Voltage	2.4	-	2.4	-	V	Iout = -5.0mA	
VOL		-	0.4	-	0.4	V	Iout = 4.2mA	

**AC Characteristics** ( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ C$  to  $+70^\circ C$ )

## Test Conditions:

 Input timing reference level:  $V_{IH}/V_{IL} = 2.4V/0.8V$ 

 Output reference level:  $V_{OH}/V_{OL} = 2.0V/0.8V$ 

Output Load: 2TTL gate + CL (50pF)

 Assumed  $t_r = 2ns$ 

#	Std Symbol	Parameter	-50		-60		Unit	Notes
			Min.	Max.	Min.	Max.		
	$t_r$	Transition Time (Rise and Fall)	1	50	1	50	ns	4, 5
1	$t_{RC}$	Random Read or Write Cycle Time	84	-	100	-	ns	
2	$t_{RP}$	$\overline{RAS}$ Precharge Time	30	-	36	-	ns	
3	$t_{RAS}$	$\overline{RAS}$ Pulse Width	50	10K	60	10K	ns	
4	$t_{CAS}$	$\overline{CAS}$ Pulse Width	8	10K	10	10K	ns	
5	$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11	37	13	45	ns	6
6	$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	9	28	11	33	ns	7
7	$t_{RSH}$	$\overline{CAS}$ to $\overline{RAS}$ Hold Time	8	-	10	-	ns	
8	$t_{CSH}$	$\overline{CAS}$ Hold Time	37	-	41	-	ns	
9	$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	
10	$t_{ASR}$	Row Address Setup Time	0	-	0	-	ns	
11	$t_{RAH}$	Row Address Hold Time	8	-	10	-	ns	
12	$t_{CLZ}$	$\overline{CAS}$ to Output in Low Z	3	-	3	-	ns	8
13	$t_{RAC}$	Access Time from $\overline{RAS}$	-	50	-	60	ns	6,7
14	$t_{CAC}$	Access Time from $\overline{CAS}$	-	13	-	15	ns	6, 12
15	$t_{AA}$	Access Time from Column Address	-	22	-	27	ns	7, 12
16	$t_{OEA}$	Access Time from $\overline{OE}$	-	13	-	15	ns	
17	$t_{AR}$	Column Address Hold Time from $\overline{RAS}$	45	-	55	-	ns	
18	$t_{RCS}$	Read Command Setup Time	0	-	0	-	ns	
19	$t_{RCH}$	Read Command Hold Time	0	-	0	-	ns	9
20	$t_{RRH}$	Read Command Hold Time Reference to $\overline{RAS}$	0	-	0	-	ns	9

**AC Characteristics (continued)** (VCC = 5.0V ±10%, VSS = 0V, Ta = 0°C to +70°C)

Test Conditions:

Input timing reference level: VIH/VIL=2.4V/0.8V

Output reference level: VOH/VOL=2.0V/0.8V

Output Load: 2TTL gate + CL (50pF)

Assumed tr=2ns

#	Std Symbol	Parameter	-50		-60		Unit	Notes
			Min.	Max.	Min.	Max.		
21	tRAL	Column Address to $\overline{\text{RAS}}$ Lead Time	22	-	27	-	ns	
22	tCOH	Output Hold After $\overline{\text{CAS}}$ Low	3	-	4	-	ns	
23	tOFF	Output Buffer Turn-Off Delay Time	-	3	-	5	ns	8, 10
24	tASC	Column Address Setup Time	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	8	-	10	-	ns	
26	tOES	$\overline{\text{OE}}$ Low to $\overline{\text{CAS}}$ High Set Up	10	-	10	-	ns	
27	twCS	Write Command Setup Time	0	-	0	-	ns	11
28	twCH	Write Command Hold Time	8	-	10	-	ns	11
29	twCR	Write Command Hold Time to $\overline{\text{RAS}}$	45	-	55	-	ns	
30	tWP	Write Command Pulse Width	8	-	10	-	ns	
31	trWL	Write Command to $\overline{\text{RAS}}$ Lead Time	13	-	15	-	ns	
32	tcWL	Write Command to $\overline{\text{CAS}}$ Lead Time	8	-	10	-	ns	
33	tDS	Data-in setup Time	0	-	0	-	ns	
34	tDH	Data-in Hold Time	8	-	10	-	ns	
35	tDHR	Data-in Hold Time to $\overline{\text{RAS}}$	45	-	55	-	ns	
36	trWC	Read-Modify-Write Cycle Time	114	-	135	-	ns	
37	trWD	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time (Read-Modify-Write)	65	-	78	-	ns	11
38	tcWD	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time (Read-Modify-Write)	28	-	33	-	ns	11
39	tAWD	Column Address to $\overline{\text{WE}}$ Delay Time (Read-Modify-Write)	37	-	45	-	ns	11
40	tOEH	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	8	-	10	-	ns	

**AC Characteristics (continued)** (VCC = 5.0V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

Test Conditions:

Input timing reference level: VIH/VIL=2.4V/0.8V

Output reference level: VOH/VOL=2.0V/0.8V

Output Load: 2TTL gate + CL (50pF)

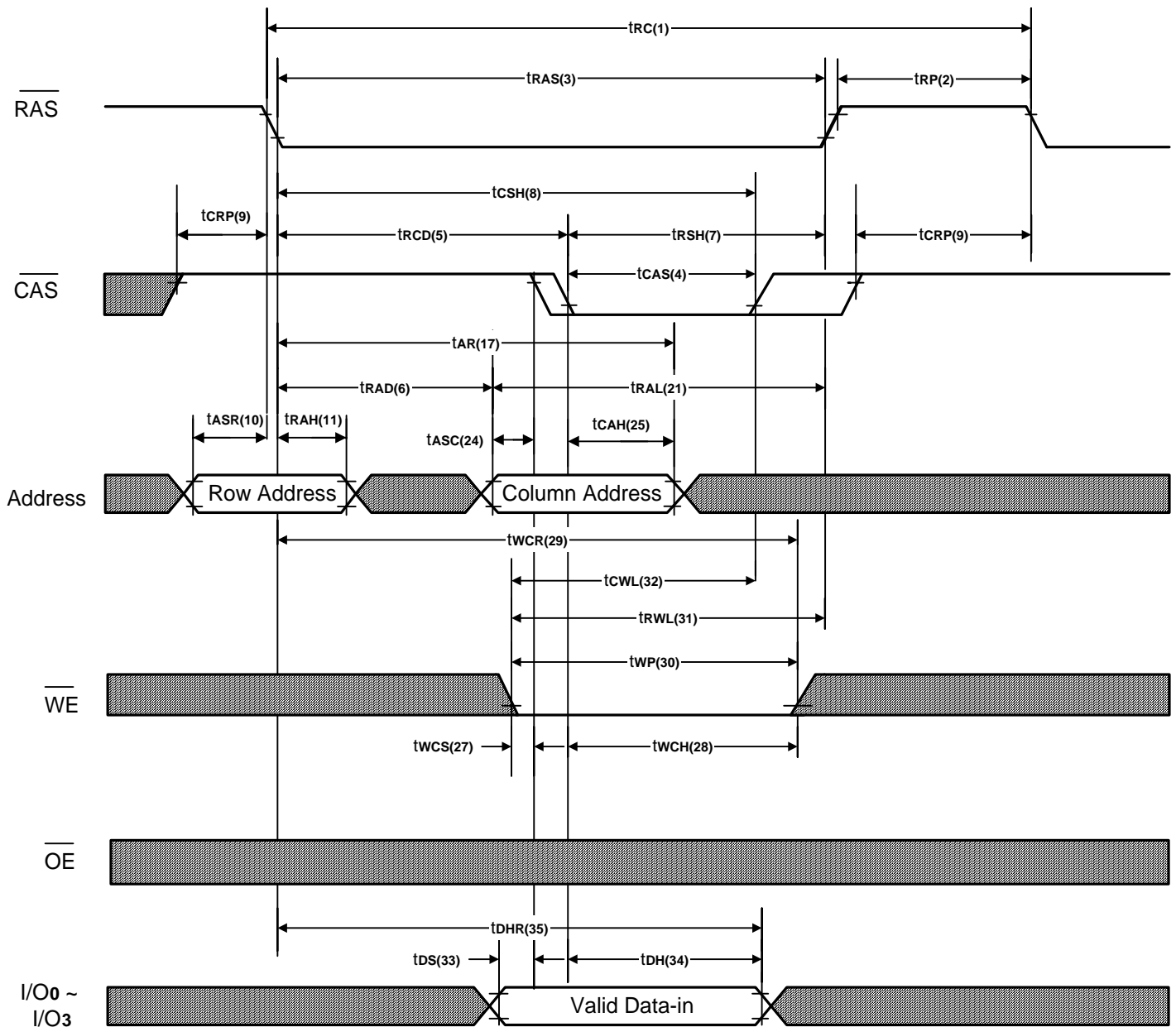
Assumed tr=2ns

#	Std Symbol	Parameter	-50		-60		Unit	Notes
			Min.	Max.	Min.	Max.		
41	toEP	$\overline{OE}$ High Pulse Width	5	-	5	-	ns	
42	tpC	Read or Write Cycle Time (EDO Page)	20	-	24	-	ns	13
43	tCPA	Access Time from $\overline{CAS}$ Precharge (EDO Page)	-	23	-	27	ns	12
44	tCP	$\overline{CAS}$ Precharge Time (EDO Page)	8	-	10	-	ns	
45	tpCM	EDO Page Mode RMW Cycle Time	50	-	59	-	ns	
46	tCRW	EDO Page Mode $\overline{CAS}$ Pulse Width (RMW)	38	-	45	-	ns	
47	tRASP	$\overline{RAS}$ Pulse Width (EDO Page)	50	100K	60	100K	ns	
48	tCSR	$\overline{CAS}$ Setup Time ( $\overline{CAS}$ -before- $\overline{RAS}$ )	5	-	5	-	ns	3
49	tCHR	$\overline{CAS}$ Hold Time ( $\overline{CAS}$ -before- $\overline{RAS}$ )	10	-	10	-	ns	3
50	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time ( $\overline{CAS}$ -before- $\overline{RAS}$ )	5	-	5	-	ns	
51	toEZ	Output Buffer Turn-off Delay from $\overline{OE}$	-	3	-	5	ns	8
52	tRASS	$\overline{RAS}$ pulse width ( $\overline{C}$ -B- $\overline{R}$ self-refresh)	100	-	100	-	μs	
53	tRPS	$\overline{RAS}$ precharge time ( $\overline{C}$ -B- $\overline{R}$ self-refresh)	84	-	100	-	ns	
54	tCHS	$\overline{CAS}$ hold time ( $\overline{C}$ -B- $\overline{R}$ self-refresh)	-50	-	-50	-	ns	

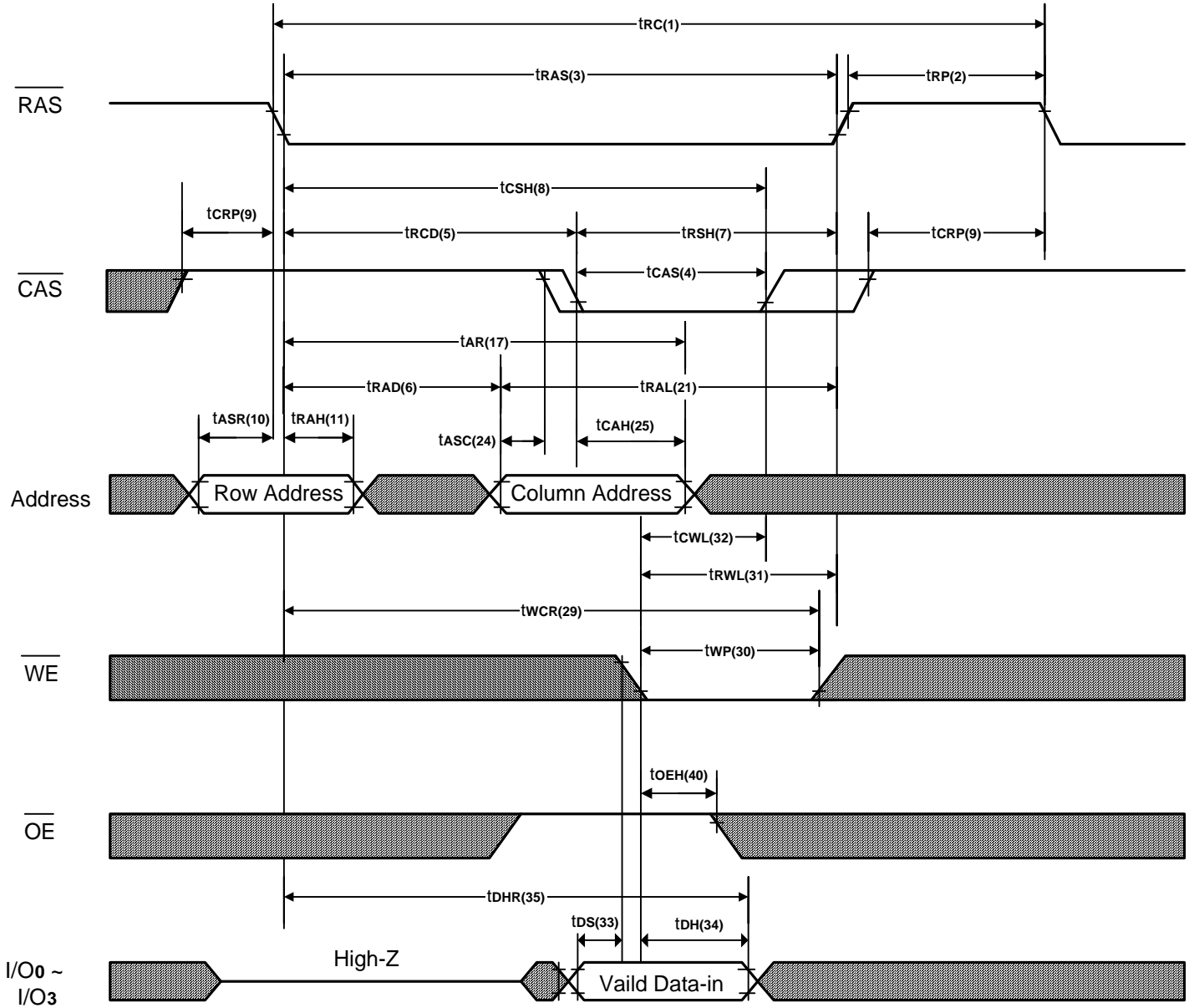
**Notes:**

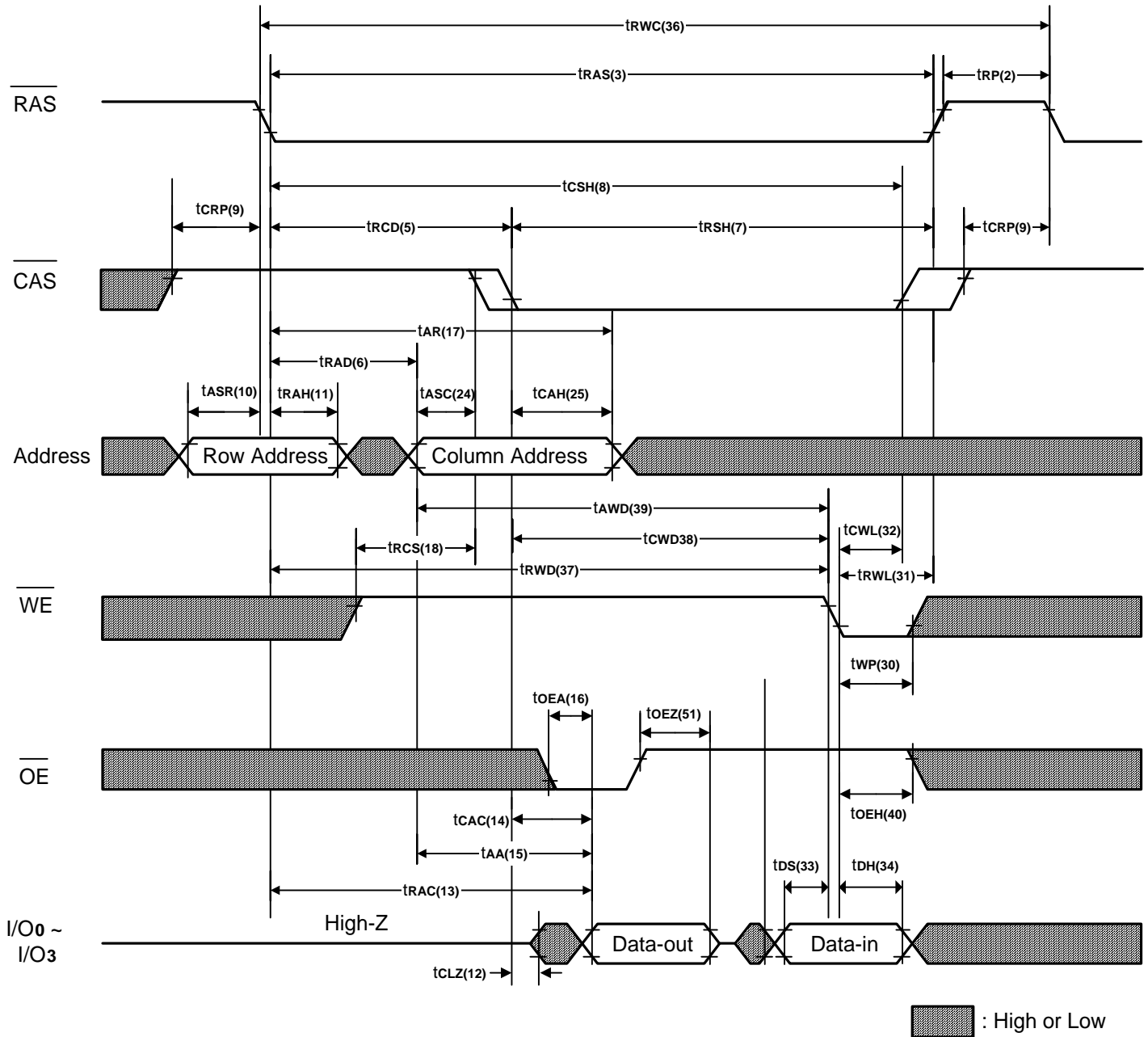
1.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC5}$  depend on cycle rate.
2.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the outputs open.
3. An initial pause of 200 $\mu$ s is required after power-up followed by any 8 RAS cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$ -before-RAS initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required. 8 initialization cycles are required after extended periods of bias without.
4. AC Characteristics assume  $t_r = 2$ ns. All AC parameters are measured with a load equivalent to two TTL load and 50pF,  $V_{IL}(\text{min.}) \geq \text{GND}$  and  $V_{IH}(\text{max.}) \leq V_{CC}$ .
5.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
6. Operation within the  $t_{RCO}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCO}(\text{max.})$  is specified as a reference point only. If  $t_{RCO}$  is greater than the specified  $t_{RCO}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
7. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
8. Assumes three state test load (5pF and a 500 $\Omega$  Thevenin equivalent).
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
10.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
11.  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$  and  $t_{WCH} \geq t_{WCH}(\text{min.})$ , the cycle is an early write cycle and data-out pins will remain open circuit, high impedance, throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12. Access time is determined by the longer of  $t_{AA}$  or  $t_{CAC}$  or  $t_{CPA}$ .
13.  $t_{ASC} \geq t_{CP}$  to achieve  $t_{PC}(\text{min.})$  and  $t_{CPA}(\text{max.})$  values.

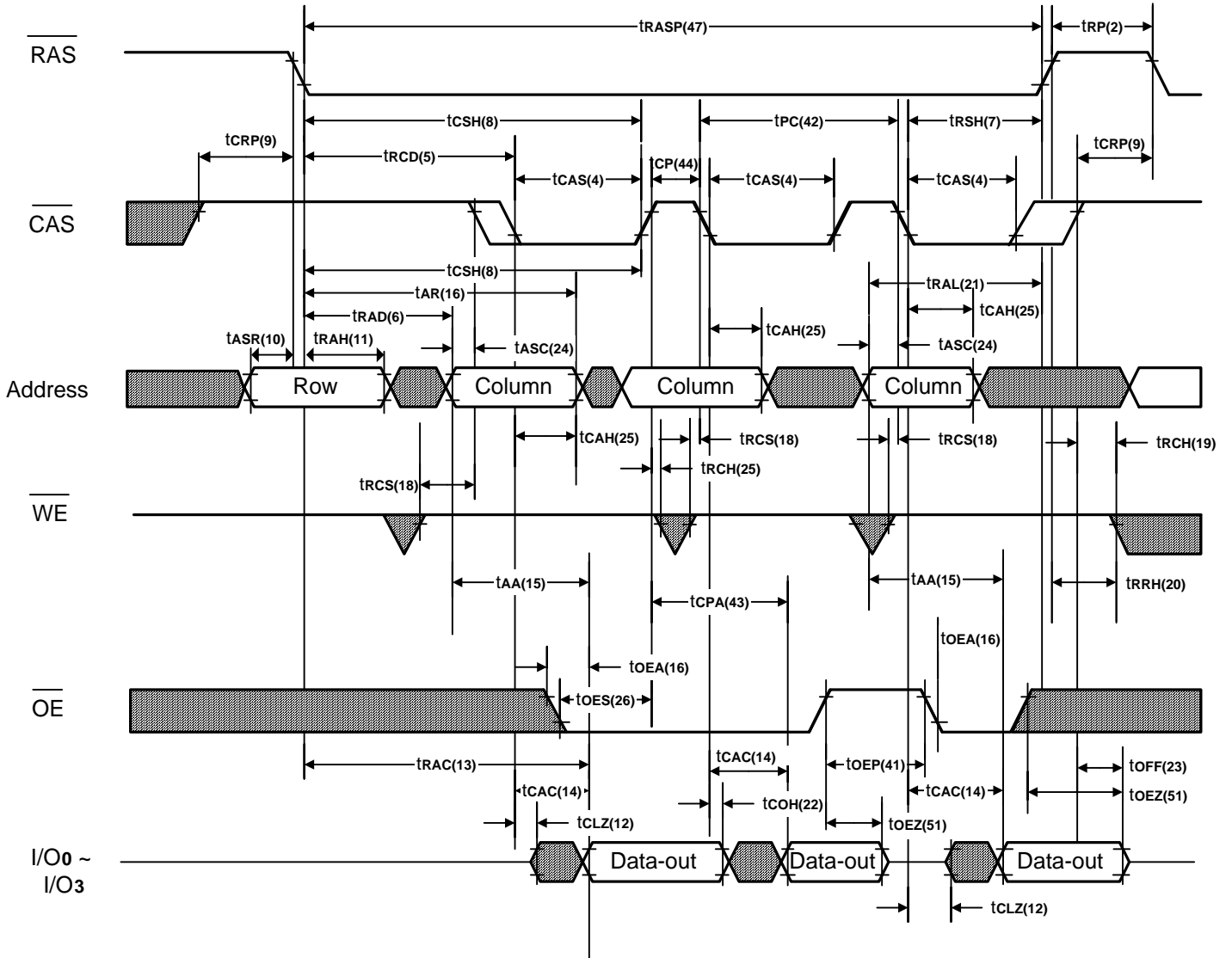


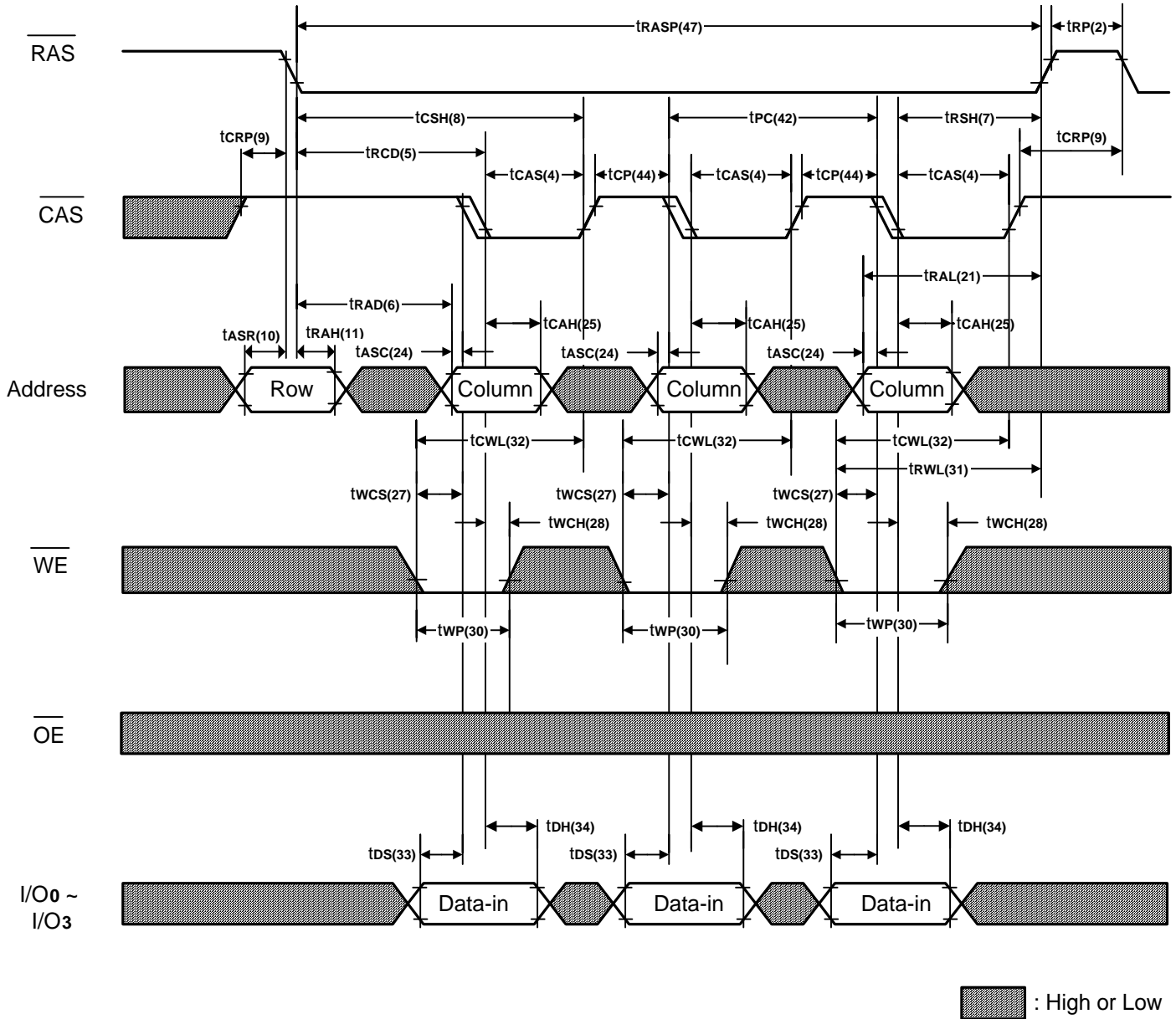
**Word Write Cycle (Early Write)**


 : High or Low

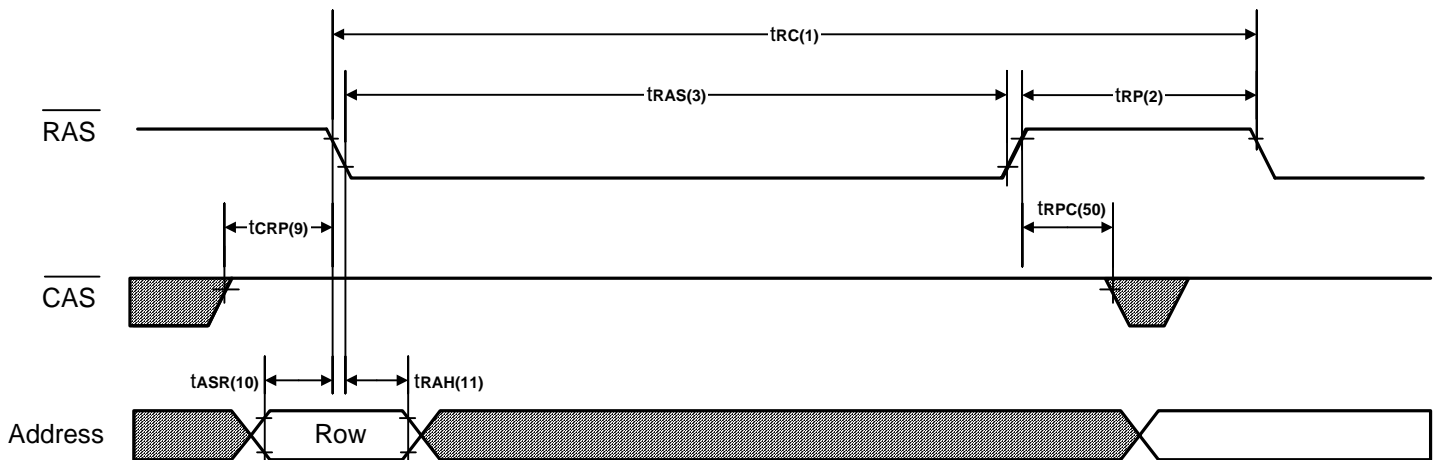
**Word Write Cycle (Late Write)**


**Word Read-Modify-Write Cycle**


**EDO Page Mode Word Read Cycle**

 : High or Low

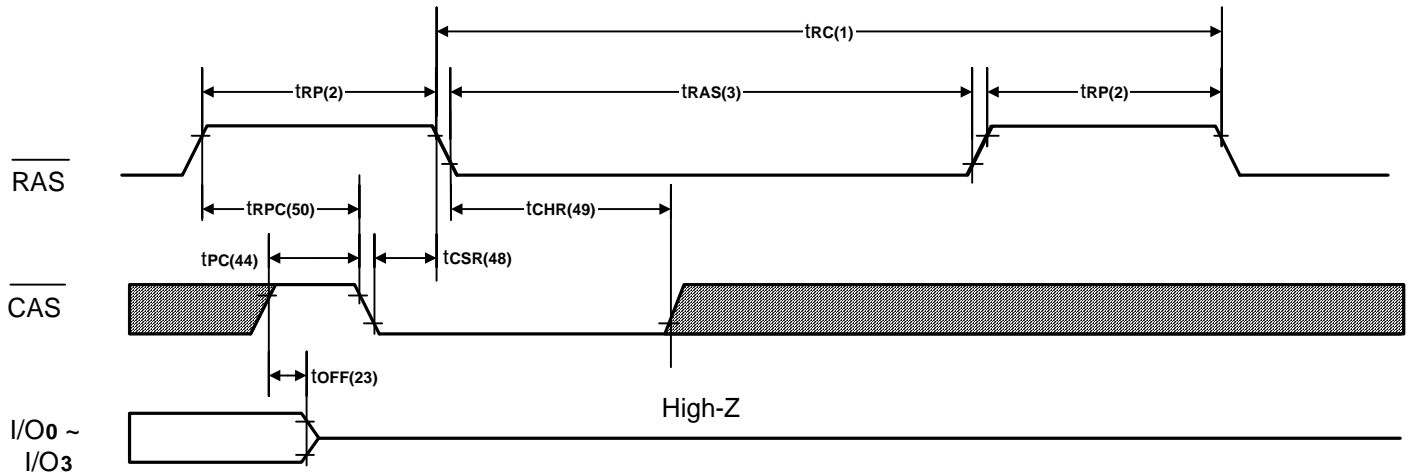
**EDO Page Mode Early Word Write Cycle**




**RAS Only Refresh Cycle**


Note:  $\overline{WE}$ ,  $\overline{OE}$  = Don't care.

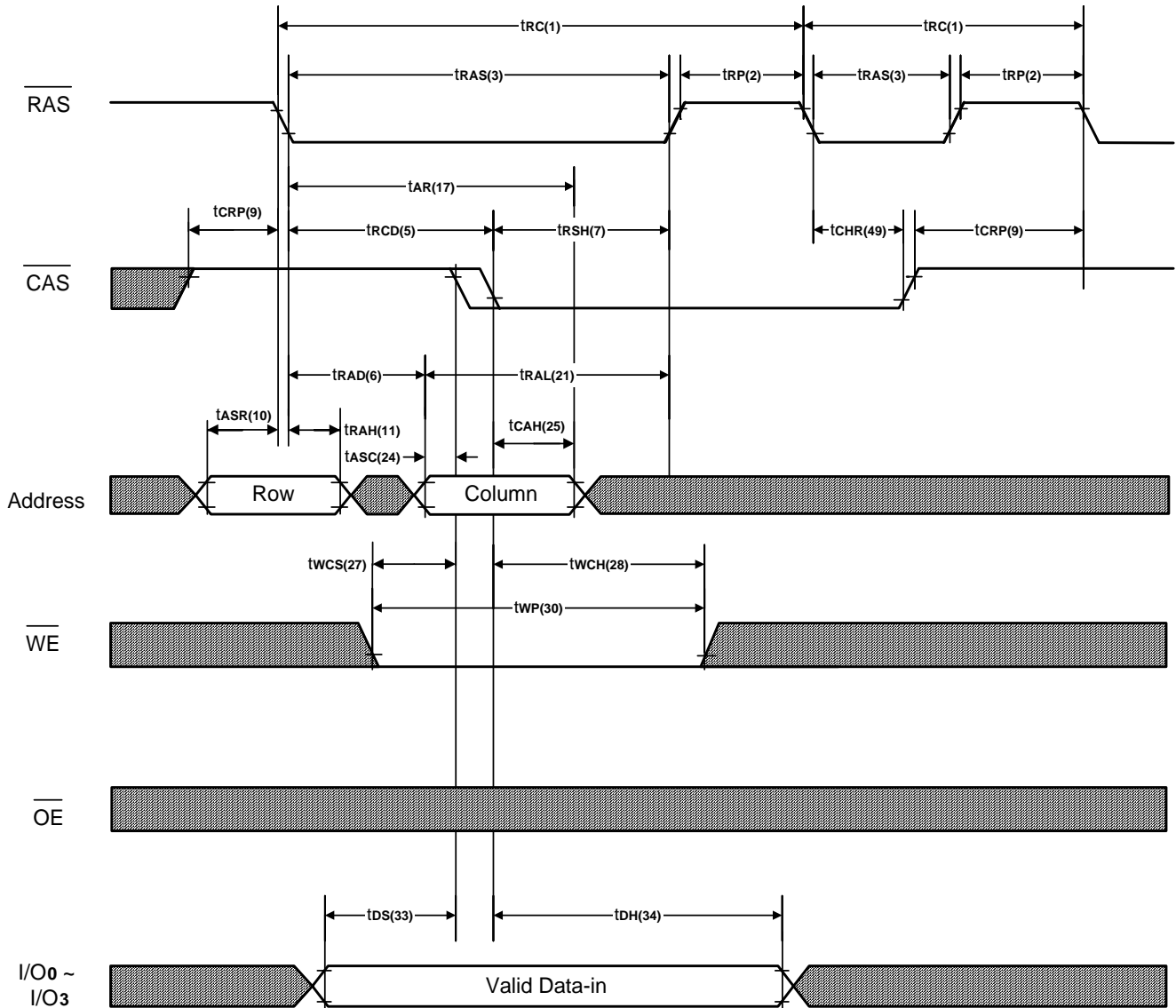
 : High or Low


**CAS Before RAS Refresh Cycle**


Note:  $\overline{WE}$ ,  $\overline{OE}$ , Address = Don't care.

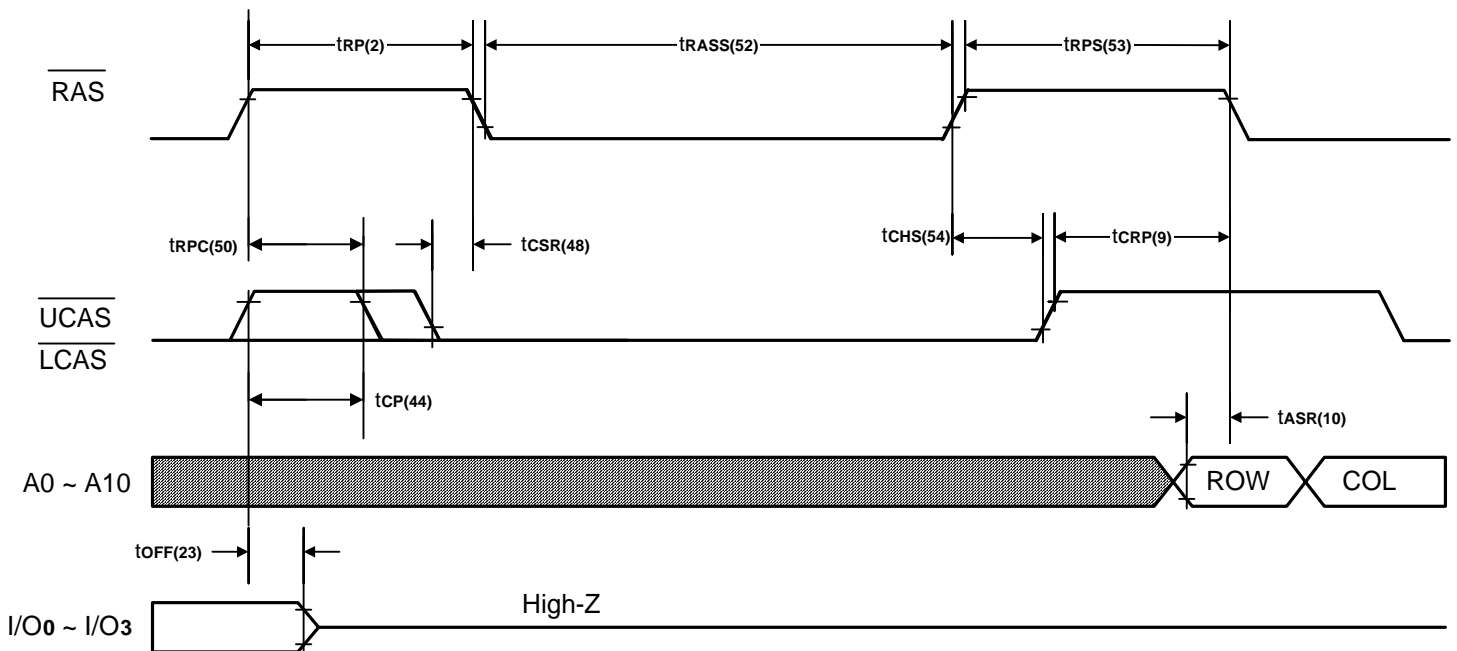
 : High or Low



**Hidden Refresh Cycle (Early Word Write)**


 : High or Low



**Self Refresh Mode**


Note:  $\overline{WE}$ ,  $\overline{OE}$  = Don't care.

 : High or Low

**Self Refresh Mode.**
**a. Entering the Self Refresh Mode:**

The A422604 Self Refresh Mode is entered by using  $\overline{CAS}$  before  $\overline{RAS}$  cycle and holding  $\overline{RAS}$  and  $\overline{CAS}$  signal "low" longer than 100 $\mu$ s.

**b. Continuing the Self Refresh Mode:**

The Self Refresh Mode is continued by holding  $\overline{RAS}$  "low" after entering the Self Refresh Mode.

It does not depend on  $\overline{CAS}$  being "high" or "low" after entering the Self Refresh Mode continue the Self Refresh Mode.

**c. Exiting the Self Refresh Mode:**

The A422604 exits the Self Refresh Mode when the  $\overline{RAS}$  signal is brought "high".

**Capacitance** (Ta = Room Temperature, VCC = 5.0V ± 10%)

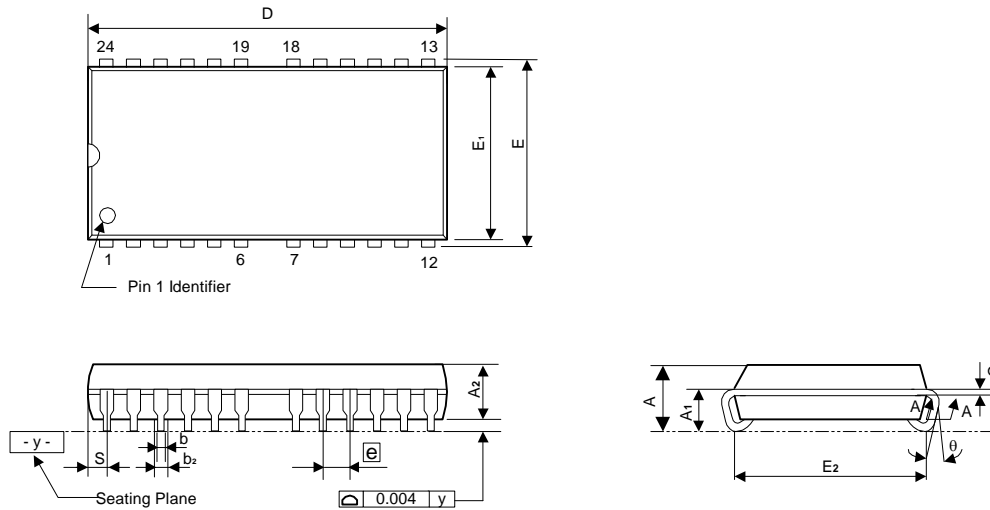
Symbol	Signals	Parameter	Max.	Unit	Test Conditions
C <sub>IN1</sub>	A0 - A10	Input Capacitance	5	pF	V <sub>in</sub> = 0V
C <sub>IN2</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$		7	pF	V <sub>in</sub> = 0V
C <sub>I/O</sub>	I/O <sub>0</sub> - I/O <sub>3</sub>	I/O Capacitance	10	pF	V <sub>in</sub> = V <sub>out</sub> = 0V

**Ordering Codes**

Package $\overline{\text{RAS}}$ Access Time	60ns	Refresh Cycle	Self-Refresh
SOJ 24/26L (300mil)	A422604S-60	2K	Yes

**Package Information**
**SOJ 24/26L (300mil) Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.140	-	-	3.56
A1	0.070	0.080	0.090	1.78	2.03	2.29
A2	0.095	0.100	0.105	2.41	2.54	2.67
b	0.016	0.018	0.022	0.41	0.46	0.56
b2	0.026	0.028	0.032	0.66	0.71	0.81
C	0.008	0.010	0.014	0.20	0.25	0.36
D	-	0.675	0.686	-	17.15	17.42
E	0.327	0.337	0.347	8.31	8.56	8.81
E1	0.295	0.300	0.305	7.49	7.62	7.75
E2	0.245	0.265	0.285	6.22	6.73	7.24
e	0.044	0.050	0.056	1.12	1.27	1.42
S	-	-	0.048	-	-	1.22
θ	0°	-	10°	0°	-	10°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E<sub>1</sub> does not include resin fins.
3. Dimension E<sub>2</sub> is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.