3.3 Volt Synchronous x 80 First-In/First-Out Queue

Memory Configuration	Device	Memory Configuration	Device
65,536 x 80	FQV80100	4,096 x 80	FQV8060
32,768 x 80	FQV8090	2,048 x 80	FQV8050
16,384 x 80	FQV8080	1,024 x 80	FQV8040
8,192 x 80	FQV8070	512 x 80	FQV8030

Key Features

- **Industry leading First-In/First-Out Queues (up to 166 MHz)**
- **Write cycle time of 6.0ns independent of Read cycle time (Data Setup time = 2.0ns)**
- **Read cycle time of 6.0ns independent of Write cycle time (Data Access time = 4.0ns)**
- **User selectable input and output bus-sizing**
- **Big Endian/Little Endian user selectable byte representation**
- **3.3V power supply**
- **5V input tolerant on all control and data input pins**
- **5V output tolerant on all flags and data output pins**
- **Master Reset clears all previously programmed configurations including Write and Read pointers**
- **Partial Reset clears Write and Read pointers but maintains all previously programmed configurations**
- **First Word Fall Through (FWFT) and Standard Timing modes**
- **Presets for eight different Almost Full and Almost Empty offset values**
- **Parallel/Serial programming of $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ offset values**
- **Programmable 8-bit or 10-bit parallel programming modes for offset values**
- **Full, Empty, Almost Full, Almost Empty, and Half Full indicators**
- **$\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ operate in either synchronous or asynchronous modes**
- **Asynchronous output enable tri-state data output drivers**
- **Synchronous Read Chip Select**
- **Data retransmission with programmable zero or normal latency modes**
- **Boundary Scan (JTAG)**
- **Available package: 256 - pin Fine Pitch Ball Grid Array (BGA)**
- **(0°C to 70°C) Commercial operating temperature available for cycle time of 6.0ns and above**
- **(-40°C to 85°C) Industrial operating temperature available for cycle time of 7.5ns and above**

Product Description

HBA's FlexQ™ III Plus offers industry leading FIFO queuing bandwidth (up to 12.0 Gbps) with a wide range of memory configurations (from 512 x 80 to 65,536 x 80). System designer has full flexibility of implementing deeper and wider queues using FWFT mode and width expansion features. Full, Empty, and Half-Full indicators allow easy handshaking between transmitters and receivers. User programmable Almost Full and Almost Empty (Parallel/Serial) indicators allow implementation of virtual queue depths.

5V tolerant on all input and output pins allow easy interfacing with devices operating at higher voltage levels. Asynchronous Output Enable pin configures the tri-state data output drivers. In addition, synchronous read chip select is also available to control the state of data output drivers. Independent Write and Read controls provide rate-matching capability.

Master Reset clears all previous programmed configurations by providing a low pulse on $\overline{\text{MRST}}$ pin. In addition, Write and Read pointers to the queue are initialized to zero. Partial Reset will not alter previously programmed configurations but will initialize Write and Read pointers to zero.

In FWFT mode, first data written into the queue appears on output data bus after the specified latency period at the low to high transition of RCLK. Subsequent reads from the queue will require asserting $\overline{\text{REN}}$. This feature is useful when implementing depth expansion functions. In this mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ are used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ respectively.

Product Description (Continued)

In Standard mode, always assert $\overline{\text{REN}}$ for a read operation. $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ are used instead of $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ respectively.

Bus matching feature is available with the following configurations:

Input Bus Width	Output Bus Width
x20	x80
x40	x80
x80	x80
x80	x40
x80	x20

In addition, Endian Select is available for implementing byte re-ordering on data outputs.

Eight different default offset values are available for Almost Full ($\overline{\text{PRAF}}$) and Almost Empty ($\overline{\text{PRAE}}$) flags. Parallel and Serial programming of these offset values provide total flexibility other than the pre-defined default values. Both 8-bit and 10-bit parallel programming modes for offset values can be selected for convenience.

$\overline{\text{PRAF}}$, $\overline{\text{PRAE}}$, and $\overline{\text{HALF}}$ are available in either FWFT or Standard mode. In addition, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ can operate in either synchronous or asynchronous modes.

At any time, data previously read from the queue can be retransmitted by asserting $\overline{\text{RET}}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero), location of the queue. Both zero and normal latency timing modes available for retransmit operation.

These FlexQ™ III Plus devices have low power consumption, hence minimizing system power requirements. In addition, industry standard 256 - pin BGA is offered to save system board space.

These queues are ideal for applications such as data communication, telecommunication, graphics, multiprocessing, test equipment, network switching, etc.

Block Diagram of Single Synchronous Queue
65,536 x 80 / 32,768 x 80 / 16,384 x 80 / 8,192 x 80 / 4,096 x 80 / 2,048 x 80 / 1,024 x 80 / 512 x 80

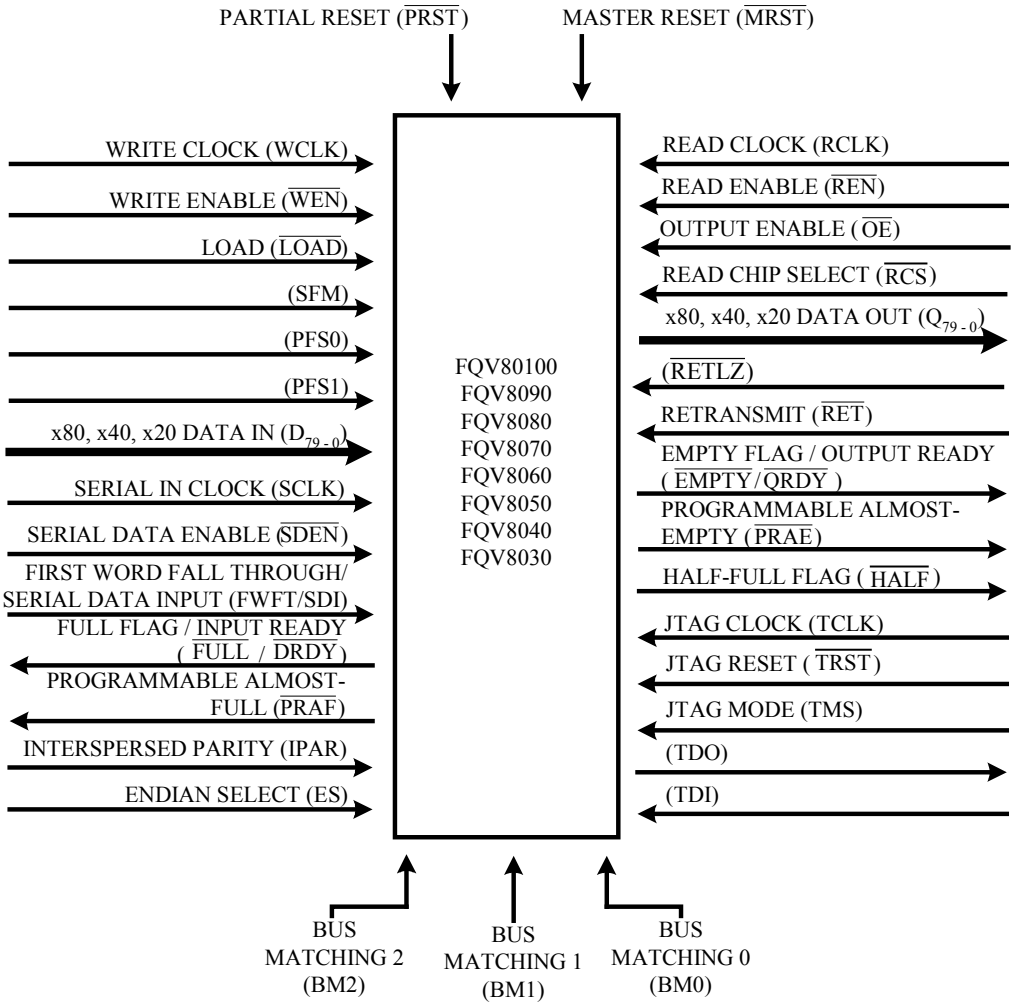


Figure 1. Single Device Configuration Signal Flow Diagram

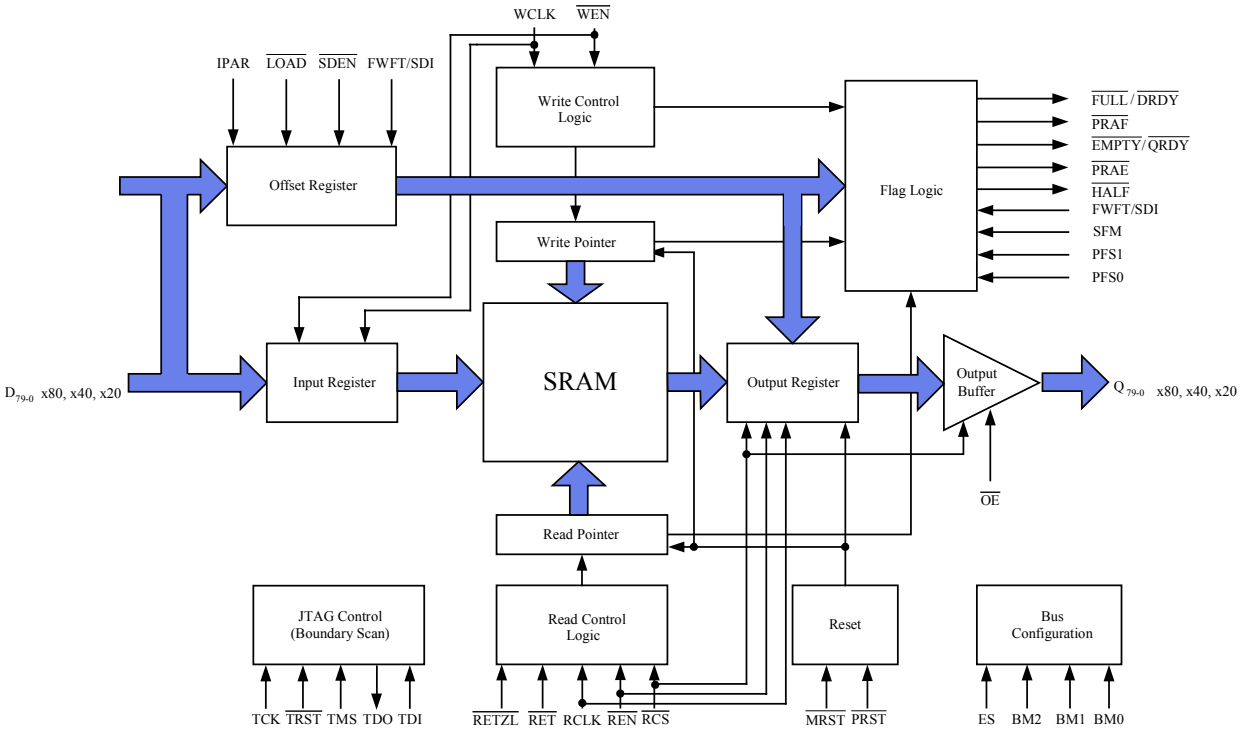
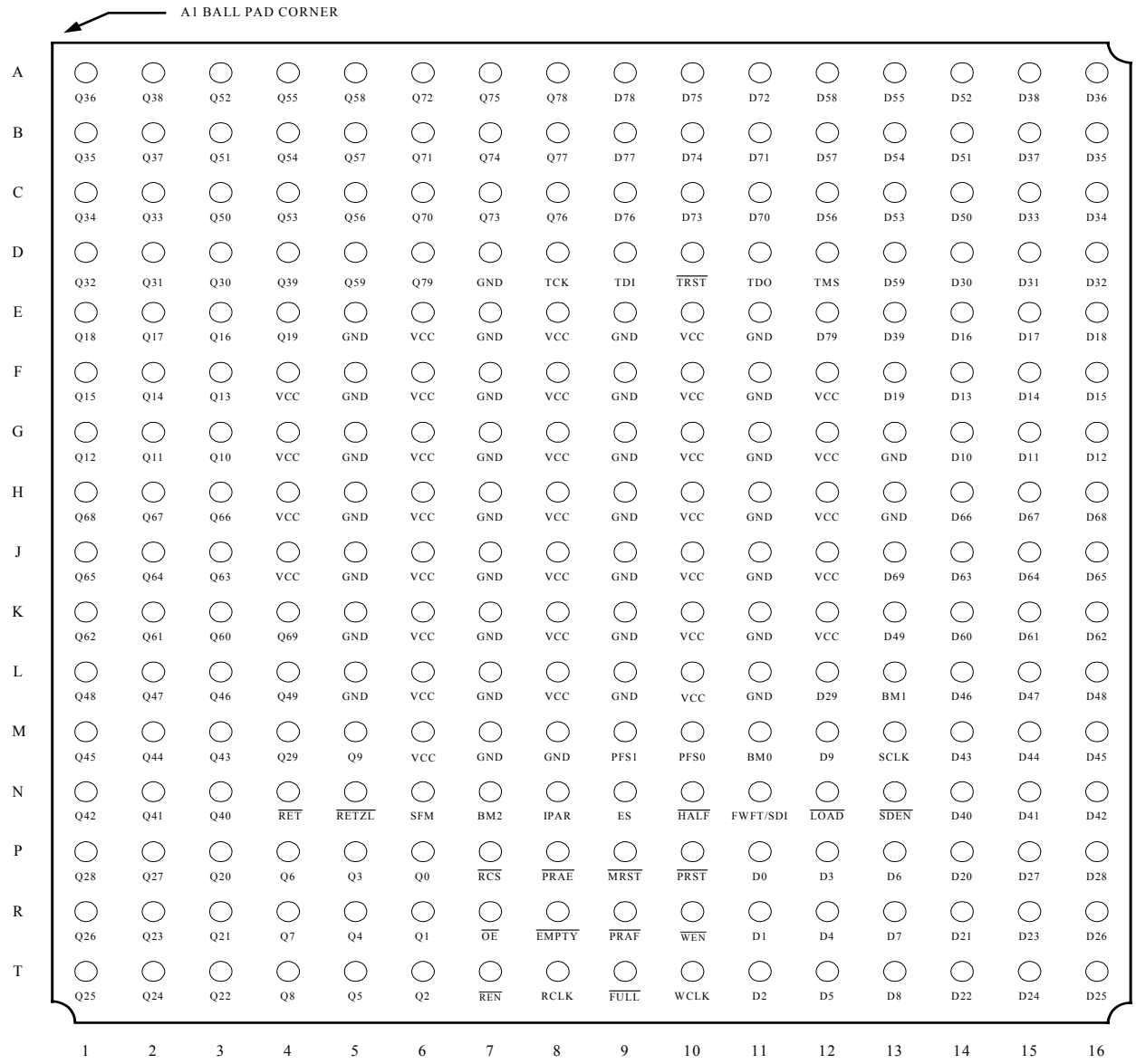


Figure 2. Device Architecture



PBGA -256 (Drw No: BB-01A; Order code: BB)
Top View
Figure 3. Device Pin Out

Pin #	Pin Name	Pin Symbol	Input/Output	Description
P9	Master Reset	$\overline{MRST}$	Input	Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{MRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will not be maintained.
P10	Partial Reset	$\overline{PRST}$	Input	Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{PRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will be maintained.
T10	Write Clock	WCLK	Input	Writes data into queue during low to high transitions of WCLK if $\overline{WEN}$ is set to low.
R10	Write Enable	$\overline{WEN}$	Input	Controls write operation into queue or offset registers during low to high transition of WCLK.
N12	Load Enable	$\overline{LOAD}$	Input	During Master Reset, set $\overline{LOAD}$ low to select parallel programming or one of eight default offset values. Set $\overline{LOAD}$ high to select serial programming or one of eight default offset values. After Master Reset, $\overline{LOAD}$ controls write/read to/from offset registers during low to high transition of WCLK/RCLK respectively. Use in conjunction with $\overline{WEN}$ / $\overline{REN}$.
M9	Default Programming 1	PFS1	Input	During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{LOAD}$ and PFS0.
M10	Default Programming 0	PFS0	Input	During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{LOAD}$ and PFS1.
A9, A10, A11, A12, A13, A14, A15, A16, B9, B10, B11, B12, B13, B14, B15, B16, C9, C10, C11, C12, C13, C14, C15, C16, D13, D14, D15, D16, E12, E13, E14, E15, E16, F13, F14, F15, F16, G14, G15, G16, H14, H15, H16, J13, J14, J15, J16, K13, K14, K15, K16, L12, L14, L15, L16, M12, M14, M15, M16, N14, N15, N16, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16	Data Inputs	D_{79-0}	Input	80 - bit wide input data bus.
T8	Read Clock	RCLK	Input	Reads data from queue during low to high transitions of RCLK if $\overline{REN}$ is set to low.

Table 1. Pin Descriptions

Pin #	Pin Name	Pin Symbol	Input/Output	Description
T7	Read Enable	$\overline{REN}$	Input	Controls read operation from queue or offset registers during low to high transition of RCLK.
P7	Read Chip Select	$\overline{RCS}$	Input	Setting $\overline{RCS}$ low during the low to high transition of RCLK activates the data output drivers. Setting $\overline{RCS}$ high during the low to high transition of RCLK deactivates the data output drivers. $\overline{OE}$ must be set low when using $\overline{RCS}$ to control the state of the drivers.
R7	Output Enable	$\overline{OE}$	Input	Setting $\overline{OE}$ low activates the data output drivers. Setting $\overline{OE}$ high deactivates the data output drivers (High-Z).
A1, A2, A3, A4, A5, A6, A7, A8, B1, B2, B3, B4, B5, B6, B7, B8, C1, C2, C3, C4, C5, C6, C7, C8, D1, D2, D3, D4, D5, D6, E1, E2, E3, E4, F1, F2, F3, G1, G2, G3, H1, H2, H3, J1, J2, J3, K1, K2, K3, K4, L1, L2, L3, L4, M1, M2, M3, M4, M5, N1, N2, N3, P1, P2, P3, P4, P5, P6, R1, R2, R3, R3, R4, R5, R6, T1, T2, T3, T4, T5, T6	Data Outputs	Q_{79-0}	Output	80 - bit wide output data bus.
N11	First Word Fall Through/Serial Data Input	FWFT/SDI	Input	Selects FWFT timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{LOAD}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{SDEN}$.
M13	Serial Clock	SCLK	Input	During serial programming, SCLK is used to program offset values through SDI.
N13	Serial Data Input Enable	$\overline{SDEN}$	Input	If serial programming is selected, setting $\overline{SDEN}$ and $\overline{LOAD}$ low enables serial data input to be written into offset registers during the low to high transition of SCLK.
N7	Bus Matching 2	BM2	Input	During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM1 and BM0.
L13	Bus Matching 1	BM1	Input	During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM2 and BM0.
M11	Bus Matching 0	BM0	Input	During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM2 and BM1.
N9	Endian Select	ES	Input	During Master Reset, set ES high to select byte re-ordering on data outputs or ES low to select no byte re-ordering on data outputs.
N4	Retransmit	$\overline{RET}$	Input	Data previously read from the queue can be retransmitted by asserting $\overline{RET}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue.

Table 1. Pin Descriptions (Continued)

Pin #	Pin Name	Pin Symbol	Input/Output	Description
N5	Zero Latency Retransmit	$\overline{\text{RETZL}}$	Input	During Master Reset, set $\overline{\text{RETZL}}$ low to select zero latency retransmit or $\overline{\text{RETZL}}$ high to select normal latency retransmit.
T9	Full/Data Input Ready Flag	$\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$	Output	Queue is full when $\overline{\text{FULL}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue. In FWFT mode, queue is full when $\overline{\text{DRDY}}$ goes high during low to high transition of WCLK. This prohibits further writes into the queue.
R8	Empty/Data Output Ready Flag	$\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$	Output	Queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue. In FWFT mode, queue is empty when $\overline{\text{QRDY}}$ goes high during the low to high transition of RCLK. This prohibits further reads from the queue.
N8	Interspersed Parity	IPAR	Input	During Master Reset, set IPAR low to select 10-bit parallel programming mode or IPAR high to select 8-bit parallel programming mode.
N6	Synchronous Partial Flag Mode	SFM	Input	During Master Reset, set SFM high to select Synchronous Partial Flag mode or SFM low to select Asynchronous Partial Flag mode.
R9	Almost Full	$\overline{\text{PRAF}}$	Output	Queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{\text{PRAF}}$.
P8	Almost Empty	$\overline{\text{PRAE}}$	Output	Queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty+offset) or programmed offset values determine the status of $\overline{\text{PRAE}}$.
N10	Half Full	$\overline{\text{HALF}}$	Output	Queue is more than half full when $\overline{\text{HALF}}$ goes low. Triggered by both WCLK and RCLK.
E6, E8, E10, F4, F6, F8, F10, F12, G4, G6, G8, G10, G12, H4, H6, H8, H10, H12, J4, J6, J8, J10, J12, K6, K8, K10, K12, L6, L8, L10, M6	Power	Vcc	N/A	3.3V power supply.
D7, E5, E7, E9, E11, F5, F7, F9, F11, G5, G7, G9, G11, G13, H5, H7, H9, H11, H13, J5, J7, J9, J11, K5, K7, K9, K11, L5, L7, L9, L11, M7, M8	Ground	GND	N/A	0V Ground.

Table 1. Pin Description (Continued)

Pin #	Pin Name	Pin Symbol	Input/Output	Description
D8	JTAG Clock	TCK	Input	Clock for JTAG function. TMS and TDI are loaded during low to high transitions of TCK. TDO is loaded during high to low transitions of TCK. When JTAG is not used, tie TCK to $\overline{\text{MRST}}$.
D10	JTAG Reset	$\overline{\text{TRST}}$	Input	Reset control for JTAG function. An asynchronous input for the JTAG controller.
D12	JTAG Mode Selection	TMS	Input	Mode select for JTAG function. TMS bits are loaded serially during low to high transitions of the TCK.
D9	Test Data Input	TDI	Input	Serial data input for JTAG function. TDI is loaded during low to high transitions of the TCK.
D11	Test Data Output	TDO	Output	Serial data output for JTAG function. TDO is unloaded during high to low transitions of the TCK. During SHIFT-DR and SHIFT-IR operations, TDO bus will be tri-stated.

Table 1. Pin Description (Continued)

Symbol	Rating	Com'l & Ind'l	Unit
VTERM	Terminal Voltage with respect to GND	-0.5 to + 4.5	V
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	-50 to +50	mA

NOTES:
Absolute Max Ratings are for reference only. Permanent damage to the device may occur if extended period of operation is outside this range. Standard operation should fall within the Recommended Operating Conditions.

Table 2. Absolute Maximum Ratings

		FQV80100, FQV8090, FQV8080, FQV8070, FQV8060, FQV8050, FQV8040, FQV8030						
		Commercial Clock = 6ns, 7.5ns, 10ns			Industrial Clock = 7.5ns, 10ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Recommended Operating Conditions								
Vcc	Supply Voltage Com'l / Ind'l	3.15	3.3	3.45	3.15	3.3	3.45	V
GND	Supply Voltage	0	0	0	0	0	0	V
VIH	Input High Voltage Com'l / Ind'l	2.0	-	5.5	2.0	-	5.5	V
VIL	Input Low Voltage Com'l / Ind'l	-	-	0.8	-	-	0.8	V
TA	Operating Temperature Commercial	0	-	70	0	-	70	°C
TA	Operating Temperature Industrial	-40	-	85	-40	-	85	°C
DC Electrical Characteristics								
ILI(1)	Input Leakage Current (any input)	-10	-	10	-10	-	10	µA
ILO	Output Leakage Current	-10	-	10	-10	-	10	µA
VOH	Output Logic "1" Voltage, IOH=-2mA	2.4	-	-	2.4	-	-	V
VOL	Output Logic "0" Voltage, IOL = 8mA	-	-	0.4	-	-	0.4	V
Power Consumption								
Icc1(2,3)	Active Power Supply Current	-	-	40	-	-	40	mA
Icc2(4)	Standby Current	-	-	15	-	-	15	mA

Table 3. DC Specifications

Capacitance at 100MHz Ambient Temperature (25°C)				
Symbol	**Parameter**	**Conditions**	**Max.**	**Unit**
C_{IN}[2]	Input Capacitance	V_{IN}= 0V	10	pF
C_{OUT}[2,4]	Output Capacitance	V_{OUT}= 0V	10	pF

NOTES:
1. Measurement with 0.4<=VIN<=Vcc
2. With output tri-stated ($\overline{OE}$ = High)
3. Icc(1,2) is measured with WCLK and RCLK at 20 MHz
4. Design simulated, not tested.

Table 3. DC Specifications (Continued)

		Commercial		Commercial & Industrial				
		FQV80100-6 FQV8090-6 FQV8080-6 FQV8070-6 FQV8060-6 FQV8050-6 FQV8040-6 FQV8030-6		FQV80100-7.5 FQV8090-7.5 FQV8080-7.5 FQV8070-7.5 FQV8060-7.5 FQV8050-7.5 FQV8040-7.5 FQV8030-7.5		FQV80100-10 FQV8090-10 FQV8080-10 FQV8070-10 FQV8060-10 FQV8050-10 FQV8040-10 FQV8030-10		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Clock Cycle Frequency	-	166	-	133	-	100	MHz
t_A	Data Access Time	1	4	2	5	2	6.5	ns
t_{WCLK}	Write Clock Cycle Time	6	-	7.5	-	10	-	ns
t_{WCLKH}	Write Clock High Time	2.5	-	3.5	-	4.5	-	ns
t_{WCLKL}	Write Clock Low Time	2.5	-	3.5	-	4.5	-	ns
t_{RCLK}	Read Clock Cycle Time	6	-	7.5	-	10	-	ns
t_{RCLKH}	Read Clock High Time	2.5	-	3.5	-	4.5	-	ns
t_{RCLKL}	Read Clock Low Time	2.5	-	3.5	-	4.5	-	ns
t_{DS}	Data Set-up Time	2.0	-	2.5	-	3.5	-	ns
t_{DH}	Data Hold Time	0.5	-	0.5	-	0.5	-	ns
t_{ENS}	Enable Set-up Time	2.0	-	2.5	-	3.5	-	ns
t_{ENH}	Enable Hold Time	0.5	-	0.5	-	0.5	-	ns
t_{RST}	Reset Pulse Width[1]	8	-	10	-	10	-	ns
t_{RSTS}	Reset Set-up Time	10	-	15		15	-	ns
t_{RSTR}	Reset Recovery Time	10	-	10	-	10	-	ns
t_{RSTF}	Reset to Flag and Output Time	-	10	-	15	-	15	ns
t_{OLZ}	Output Enable to Output in Low-Z[1]	0	-	0	-	0	-	ns
t_{OE}	Output Enable to Output Valid	2	4	2	6	2	6	ns
t_{OHZ}	Output Enable to Output in High-Z[1]	2	4	2	6	2	6	ns
t_{FULL}	Write Clock to Full Flag	-	4	-	5	-	6.5	ns
t_{EMPTY}	Read Clock to Empty Flag	-	4	-	5	-	6.5	ns
t_{PRAFS}	Write Clock to Synchronous Almost-Full Flag	-	4	-	5	-	6.5	ns
t_{PRAES}	Read Clock to Synchronous Almost-Empty Flag	-	4	-	5	-	6.5	ns
t_{RCSS}	RCS Setup Time	2	-	3.5	-	3.5	-	ns
t_{RCSH}	RCS Hold Time	0.5	-	0.5	-	0.5	-	ns
t_{RCSLZ}	RCLK to Active from High-Z	1	4	1	6.5	1	6.5	ns
t_{RCSHZ}	RCLK to High-Z	1	4	1	6.5	1	6.5	ns

Table 4. AC Electrical Characteristics

		Commercial		Commercial & Industrial				
		FQV80100-6 FQV8090-6 FQV8080-6 FQV8070-6 FQV8060-6 FQV8050-6 FQV8040-6 FQV8030-6		FQV80100-7.5 FQV8090-7.5 FQV8080-7.5 FQV8070-7.5 FQV8060-7.5 FQV8050-7.5 FQV8040-7.5 FQV8030-7.5		FQV80100-10 FQV8090-10 FQV8080-10 FQV8070-10 FQV8060-10 FQV8050-10 FQV8040-10 FQV8030-10		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{SKEW1}	Skew time between Read Clock & Write Clock for Full Flag / Empty Flag	4	-	5	-	7	-	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for $\overline{PRAE}$ & $\overline{PRAF}$	6	-	7	-	10	-	ns
t_{LOADS}	Load Setup Time	2.0	-	2.5	-	3.5	-	ns
t_{LOADH}	Load Hold Time	0.5	-	0.5	-	0.5	-	ns
t_{RETS}	Retransmit Setup Time	2.5	-	3.5	-	3.5	-	ns
t_{HALF}	Clock to $\overline{HALF}$	-	12	-	12.5	-	16	ns
t_{PRAFA}	Write Clock to Asynchronous Programmable Almost-Full Flag	-	12	-	12.5	-	16	ns
t_{PRAEA}	Read Clock to Asynchronous Programmable Almost-Empty Flag	-	12	-	12.5	-	16	ns

NOTES:
1. Design simulated, not tested.

Table 4. AC Electrical Characteristics (Continued)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns(1)
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load, clock = 6ns, 7.5ns, 10ns	Refer to Figure 4

NOTES:
1. For 166 MHz and 133 MHz operations, input rise/fall times are 1.5ns

Table 5. AC Test Condition

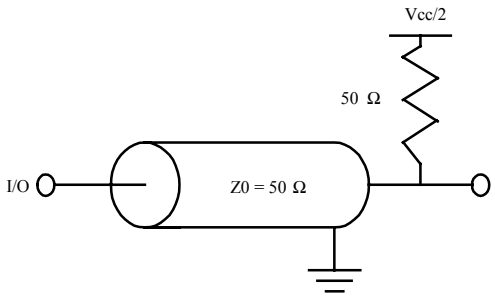


Figure 4. AC Test Load
for clock = 6ns, 7.5ns, 10ns

Pin Functions

$\overline{\text{MRST}}$ Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{MRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high, $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low, and previous programmed configurations will not be maintained.

$\overline{\text{PRST}}$ Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{PRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high. $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low, and previously programmed configurations will be maintained.

WCLK Writes data into queue during low to high transitions of WCLK if $\overline{\text{WEN}}$ is activated. Synchronizes $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ and $\overline{\text{PRAF}}$ flags. WCLK and RCLK are independent of each other.

$\overline{\text{WEN}}$ Controls write operation into queue or offset registers during low to high transition of WCLK.

$\overline{\text{LOAD}}$ During Master Reset, set $\overline{\text{LOAD}}$ low to select parallel programming or one of eight default offset values. Set $\overline{\text{LOAD}}$ high to select serial programming or one of eight default offset values. After Master Reset, $\overline{\text{LOAD}}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively for parallel programming. Use in conjunction with $\overline{\text{WEN}}$ / $\overline{\text{REN}}$. During programming of offset registers, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flag status are invalid. For Serial programming, $\overline{\text{LOAD}}$ is used to enable serial loading of offset registers together with $\overline{\text{SDEN}}$. Refer to Figure 5 for details.

PFS1 During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{\text{LOAD}}$ and PFS0. Refer to Table 11 for details.

PFS0 During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{\text{LOAD}}$ and PFS1. Refer to Table 11 for details.

$D_{79..0}$ 80 - bit wide input data bus.

RCLK Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN}}$ is set low. Synchronizes the $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ and $\overline{\text{PRAE}}$ flags. RCLK and WCLK are independent of each other.

$\overline{\text{REN}}$ Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN}}$ is set to low. This also advances the Read pointer of the queue.

$\overline{\text{RCS}}$ Setting $\overline{\text{RCS}}$ low during the low to high transition of RCLK activates the data output drivers. Setting $\overline{\text{RCS}}$ high during the low to high transition of RCLK deactivates the data output drivers. $\overline{\text{OE}}$ must be set low when using $\overline{\text{RCS}}$ to control the state of the drivers.

$\overline{\text{OE}}$ Setting $\overline{\text{OE}}$ low activates the data output drivers. Setting $\overline{\text{OE}}$ high deactivates the data output drivers (High-Z). $\overline{\text{OE}}$ does not control advancement of Read pointer.

$Q_{79..0}$ 80 - bit wide output data bus.

FWFT/SDI Selects First Word Fall Through timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{\text{LOAD}}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{\text{SDEN}}$. In FWFT mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ are used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ are used instead of $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$. Refer to Table 8 & 9 for all flags status.

SCLK During serial programming, SCLK is used to program offset values through SDI.

Pin Functions (Continued)

$\overline{\text{SDEN}}$ — If serial programming is selected, setting $\overline{\text{SDEN}}$ and $\overline{\text{LOAD}}$ low enables serial data to be written into offset registers during the low to high transition of SCLK. During serial programming, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flags status are invalid. Refer to Figure 5 for details.

BM2 — During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM1 and BM0. Refer to Table 10 for details.

BM1 — During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM2 and BM0. Refer to Table 10 for details.

BM0 — During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM2 and BM1. Refer to Table 10 for details.

ES — During Master Reset, set ES high to select byte re-ordering on data outputs or set ES low to select no byte re-ordering on data outputs. ES must be static throughout device operation. Refer to Table 10 for details.

$\overline{\text{RET}}$ — Data previously read from the queue can be retransmitted by asserting $\overline{\text{RET}}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue. Refer to Diagram 9 & 10 for details.

$\overline{\text{RETZL}}$ — During Master Reset, set $\overline{\text{RETZL}}$ low to select zero latency retransmit. Set $\overline{\text{RETZL}}$ high to select normal latency retransmit.

$\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ — In Standard mode, queue is full when $\overline{\text{FULL}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. In FWFT mode, queue is full when $\overline{\text{DRDY}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. Refer to Table 8 & 9 for behavior of $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$.

$\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ — In Standard mode, queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. In FWFT mode, queue is empty when $\overline{\text{QRDY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. Refer to Table 8 & 9 for behavior of $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$.

IPAR — During Master Reset, set IPAR low to select 10-bit parallel programming mode or set IPAR high to select 8-bit parallel programming mode. In 10-bit mode, 10-bit wide data input / output bus width is used for storing / fetching offset values. In 8-bit mode, 8-bit wide data input / output bus is used for storing / fetching offset values.

SFM — During Master Reset, set SFM high to select Synchronous Partial Flag mode or set SFM low to select Asynchronous Partial Flag mode. In Synchronous mode, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ are synchronous to WCLK and RCLK respectively. In Asynchronous mode, WCLK synchronizes the assertion of $\overline{\text{PRAF}}$ and de-assertion of $\overline{\text{PRAE}}$. RCLK synchronizes the assertion of $\overline{\text{PRAE}}$ and de-assertion of $\overline{\text{PRAF}}$.

$\overline{\text{PRAF}}$ — Queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{\text{PRAF}}$. Refer to Table 8 & 9 for behavior of $\overline{\text{PRAF}}$.

$\overline{\text{PRAE}}$ — Queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty+offset) or programmed offset values determine the status of $\overline{\text{PRAE}}$. Refer to Table 8 & 9 for behavior of $\overline{\text{PRAE}}$.

Pin Functions (Continued)

$\overline{\text{HALF}}$	Queue is more than half full when $\overline{\text{HALF}}$ goes low during the low to high transition of WCLK. Queue is less than half full when $\overline{\text{HALF}}$ goes high during low to high transition of RCLK when. Refer to Table 8 & 9 for details.

$\overline{\text{LOAD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	$\overline{\text{SDEN}}$	WCLK	RCLK	SCLK	FQV80100 FQV8090 FQV8080 FQV8070 FQV8060 FQV8050 FQV8040 FQV8030 Selection / Sequence
0	0	1	1	↑	X	X	Parallel write to offset registers: Empty Offset Full Offset Parallel write to registers: 1. $\overline{\text{PRAE}}$ 2. $\overline{\text{PRAF}}$
0	1	0	1	X	↑	X	Parallel read from offset registers: Empty Offset Full Offset Parallel read from registers: 1. $\overline{\text{PRAE}}$ 2. $\overline{\text{PRAF}}$
0	1	1	0	X	X	↑	Serial shift into registers: 32 bits for the FQV80100 30 bits for the FQV8090 28 bits for the FQV8080 26 bits for the FQV8070 24 bits for the FQV8060 22 bits for the FQV8050 20 bits for the FQV8040 18 bits for the FQV8030 1 bit for each rising SCLK edge Starting with Empty Offset (Low Byte) Ending with Full Offset (High Byte)
X	1	1	1	X	X	X	No Operation
1	0	X	X	↑	X	X	Write Memory
1	X	0	X	X	↑	X	Read Memory
1	1	1	X	X	X	X	No Operation

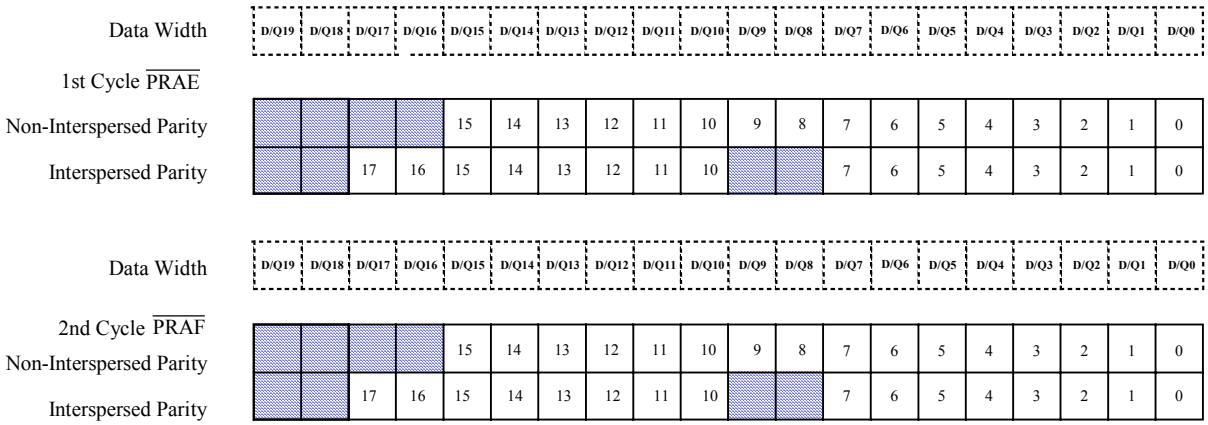
Figure 5. Programmable Flag Offset Programming Sequence
(FQV80100, FQV8090, FQV8080, FQV8070, FQV8060, FQV8050, FQV8040 and FQV8030)

Device	$\overline{PRAF}$ Programming (bits)		$\overline{PRAE}$ Programming (bits)	
FQV80100	D/Q_{15-0}	Non-IPAR	D/Q_{15-0}	Non-IPAR
	D/Q_{17-10} & D/Q_{7-0}	IPAR	D/Q_{17-10} & D/Q_{7-0}	IPAR
FQV8090	D/Q_{14-0}	Non-IPAR	D/Q_{14-0}	Non-IPAR
	D/Q_{16-10} & D/Q_{7-0}	IPAR	D/Q_{16-10} & D/Q_{7-0}	IPAR
FQV8080	D/Q_{13-0}	Non-IPAR	D/Q_{13-0}	Non-IPAR
	D/Q_{15-10} & D/Q_{7-0}	IPAR	D/Q_{15-10} & D/Q_{7-0}	IPAR
FQV8070	D/Q_{12-0}	Non-IPAR	D/Q_{12-0}	Non-IPAR
	D/Q_{14-10} & D/Q_{7-0}	IPAR	D/Q_{14-10} & D/Q_{7-0}	IPAR
FQV8060	D/Q_{11-0}	Non-IPAR	D/Q_{11-0}	Non-IPAR
	D/Q_{13-10} & D/Q_{7-0}	IPAR	D/Q_{13-10} & D/Q_{7-0}	IPAR
FQV8050	D/Q_{10-0}	Non-IPAR	D/Q_{10-0}	Non-IPAR
	D/Q_{12-10} & D/Q_{7-0}	IPAR	D/Q_{12-10} & D/Q_{7-0}	IPAR
FQV8040	D/Q_{9-0}	Non-IPAR	D/Q_{9-0}	Non-IPAR
	D/Q_{11-10} & D/Q_{7-0}	IPAR	D/Q_{11-10} & D/Q_{7-0}	IPAR
FQV8030	D/Q_{8-0}	Non-IPAR	D/Q_{8-0}	Non-IPAR
	D/Q_{10} & D/Q_{7-0}	IPAR	D/Q_{10} & D/Q_{7-0}	IPAR

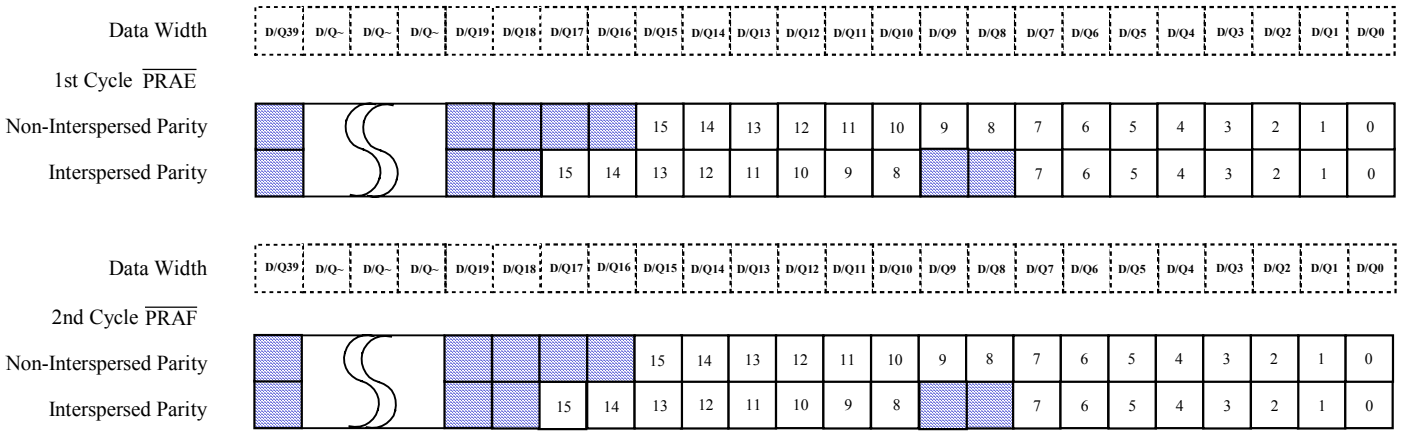
Table 6. Parallel Offset Register Data Mapping Table for x80 & x40& x20

Device	Standard Mode	FWFT Mode
FQV80100	65,536 x 80	65,537 x 80
FQV8090	32,768 x 80	32,769 x 80
FQV8080	16,384 x 80	16,385 x 80
FQV8070	8,192 x 80	8,193 x 80
FQV8060	4,096 x 80	4,097 x 80
FQV8050	2,048 x 80	2,049 x 80
FQV8040	1,024 x 80	1,025 x 80
FQV8030	512 x 80	513 x 80

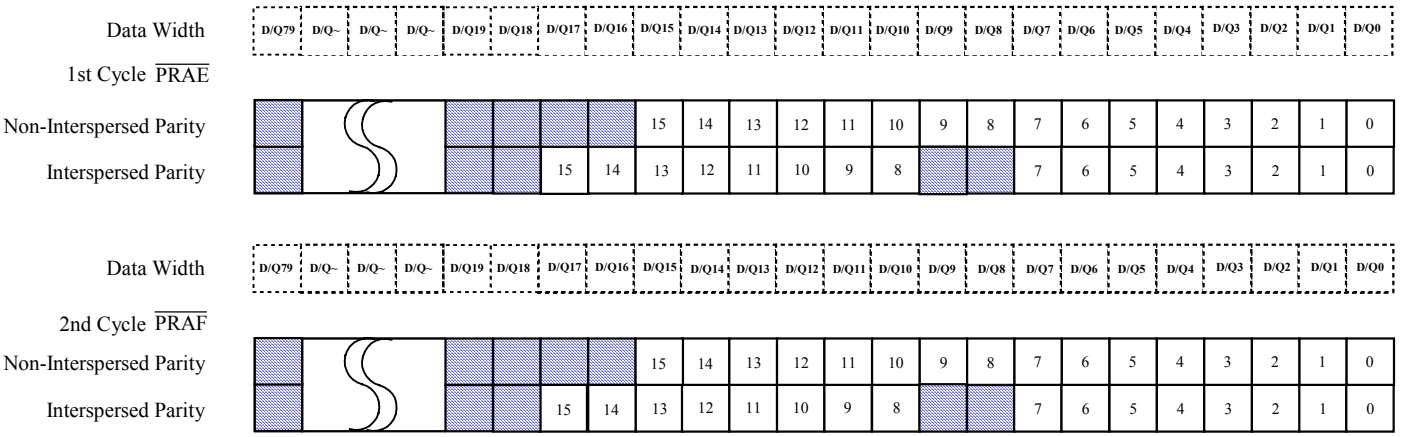
Table 7. Maximum Depth of Queue for Standard and FWFT Mode



FQV80100, FQV8090, FQV8080, FQV8070, FQV8060, FQV8050, FQV8040, FQV8030
Parallel Offset Write/Read Cycles for x20 Bus Width



FQV80100, FQV8090, FQV8080, FQV8070, FQV8060, FQV8050, FQV8040, FQV8030
Parallel Offset Write/Read Cycles for x40 Bus Width



FQV80100, FQV8090, FQV8080, FQV8070, FQV8060, FQV8050, FQV8040, FQV8030
Parallel Offset Write/Read Cycles for x80 Bus Width

Figure 6. Parallel Offset Write/Read Cycles Diagram

# of Bits for Offset Registers
16 bits for FQV80100 15 bits for FQV8090 14 bits for FQV8080 13 bits for FQV8070 12 bits for FQV8060 11 bits for FQV8050 10 bits for FQV8040 9 bits for FQV8030
Note: Don't Care applies to all unused bits

Figure 6. Parallel Offset Write/Read Cycles Diagram (Continued)

FQV80100	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0	H	H	H	L	L
1 to y[1]	H	H	H	L	H
(y+1) to 32,768	H	H	H	H	H
32,769 to [65,536-(x+1)]	H	H	L	H	H
(65,536 –x[1]) to 65,535	H	L	L	H	H
65,536	L	L	L	H	H

FQV8090	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0	H	H	H	L	L
1 to y	H	H	H	L	H
(y+1) to 16,384	H	H	H	H	H
16,385 to [32,768-(x+1)]	H	H	L	H	H
(32,768 –x) to 32,767	H	L	L	H	H
32,768	L	L	L	H	H

FQV8080	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0	H	H	H	L	L
1 to y	H	H	H	L	H
(y+1) to 8,192	H	H	H	H	H
8,193 to [16,384-(x+1)]	H	H	L	H	H
(16,384 –x) to 16,383	H	L	L	H	H
16,384	L	L	L	H	H

FQV8070	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0	H	H	H	L	L
1 to y	H	H	H	L	H
(y+1) to 4,096	H	H	H	H	H
4,097 to [8,192-(x+1)]	H	H	L	H	H
(8,192 -x) to 8,191	H	L	L	H	H
8,192	L	L	L	H	H

FQV8060	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0	H	H	H	L	L
1 to y	H	H	H	L	H
(y+1) to 2,048	H	H	H	H	H
2,049 to [4,096-(x+1)]	H	H	L	H	H
(4,096 –x) to 4,095	H	L	L	H	H
4,096	L	L	L	H	H

FQV8050	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0	H	H	H	L	L
1 to y	H	H	H	L	H
(y+1) to 1,024	H	H	H	H	H
1,025 to [2,048-(x+1)]	H	H	L	H	H
(2,048 -x) to 2,047	H	L	L	H	H
2,048	L	L	L	H	H

Table 8. Status Flags (Standard Mode)

FQV8040	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y	H	H	H	L	H
(y+1) to 512	H	H	H	H	H
513 to [1,024-(x+1)]	H	H	L	H	H
(1,024 –x) to 1,023	H	L	L	H	H
1,024	L	L	L	H	H

FQV8030	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y	H	H	H	L	H
(y+1) to 256	H	H	H	H	H
257 to [512-(x+1)]	H	H	L	H	H
(512 –x) to 511	H	L	L	H	H
512	L	L	L	H	H

NOTES:
1. See Table 11 for values x, y.

Table 8. Status Flags (Standard Mode)(Continued)

FQV80100	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1	L	H	H	L	L
(y+2) to 32,769	L	H	H	H	L
32,770 to [65,537-(x+1)]	L	H	L	H	L
(65,537 –x) to 65,536	L	L	L	H	L
65,537	H	L	L	H	L

FQV8090	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1	L	H	H	L	L
(y+2) to 16,385	L	H	H	H	L
16,386 to [32,769-(x+1)]	L	H	L	H	L
(32,769 –x) to 32,768	L	L	L	H	L
32,769	H	L	L	H	L

FQV8080	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1	L	H	H	L	L
(y+2) to 8,193	L	H	H	H	L
8,194 to [16,385-(x+1)]	L	H	L	H	L
(16,385 -x) to 16,384	L	L	L	H	L
16,385	H	L	L	H	L

FQV8070	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1	L	H	H	L	L
(y+2) to 4,097	L	H	H	H	L
4,098 to [8,193-(x+1)]	L	H	L	H	L
(8,193-x) to 8,192	L	L	L	H	L
8,193	H	L	L	H	L

FQV8060	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1	L	H	H	L	L
(y+2) to 2,049	L	H	H	H	L
2,050 to [4,097-(x+1)]	L	H	L	H	L
(4,097 -x) to 4,096	L	L	L	H	L
4,097	H	L	L	H	L

FQV8050	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1	L	H	H	L	L
(y+2) to 1,025	L	H	H	H	L
1,026 to [2,049-(x+1)]	L	H	L	H	L
(2,049 -x) to 2,048	L	L	L	H	L
2,049	H	L	L	H	L

Table 9. Status Flags (FWFT Mode)

FQV8040	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1	L	H	H	L	L
(y+2) to 513	L	H	H	H	L
514 to [1,025-(x+1)]	L	H	L	H	L
(1,025 -x) to 1,024	L	L	L	H	L
1,025	H	L	L	H	L

FQV8030	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1	L	H	H	L	L
(y+2) to 257	L	H	H	H	L
258 to [513-(x+1)]	L	H	L	H	L
(513 -x) to 512	L	L	L	H	L
513	H	L	L	H	L

Table 9. Status Flags (FWFT Mode)(Continued)

ES	BM2	BM1	BM0	I/O	Width	D/Q_{79-60}	D/Q_{59-40}	D/Q_{39-20}	D/Q_{19-0}	Sequence
X	0	X	X	I	80	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	80	Byte 4	Byte 3	Byte 2	Byte 1	1st Read
0	1	0	0	I	80	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	40	X	X	Byte 4	Byte 3	1st Read
						X	X	Byte 2	Byte 1	2nd Read
0	1	0	1	I	80	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	20	X	X	X	Byte 4	1st Read
						X	X	X	Byte 3	2nd Read
						X	X	X	Byte 2	3rd Read
						X	X	X	Byte1	4th Read
0	1	1	0	I	40	X	X	Byte 4	Byte 3	1st Write
						X	X	Byte 2	Byte 1	2nd Write
				O	80	Byte 4	Byte 3	Byte 2	Byte 1	1st Read
0	1	1	1	I	20	X	X	X	Byte 4	1st Write
						X	X	X	Byte 3	2nd Write
						X	X	X	Byte 2	3rd Write
						X	X	X	Byte1	4th Write
				O	80	Byte 4	Byte 3	Byte 2	Byte 1	1st Read
1	1	0	0	I	80	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	40	X	X	Byte 2	Byte 1	1st Read
						X	X	Byte 4	Byte 3	2nd Read
1	1	0	1	I	80	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	20	X	X	X	Byte 1	1st Read
						X	X	X	Byte 2	2nd Read
						X	X	X	Byte 3	3rd Read
						X	X	X	Byte4	4th Read
1	1	1	0	I	40	X	X	Byte 4	Byte 3	1st Write
						X	X	Byte 2	Byte 1	2nd Write
				O	80	Byte 2	Byte 1	Byte 4	Byte 3	1st Read
1	1	1	1	I	20	X	X	X	Byte 4	1st Write
						X	X	X	Byte 3	2nd Write
						X	X	X	Byte 2	3rd Write
						X	X	X	Byte1	4th Write
				O	80	Byte 1	Byte 2	Byte 3	Byte 4	1st Read

Table 10. Bus-Matching Table

$\overline{LOAD}$	PFS1	PFS0	FQV8040 FQV8030 Default Offsets x, y(1)
0	0	0	127
0	0	1	255
0	1	0	511
0	1	1	63
1	0	0	31
1	0	1	7
1	1	0	15
1	1	1	3

$\overline{LOAD}$	PFS1	PFS0	FQV8040 FQV8030 Program Mode
1	X	X	Serial
0	X	X	Parallel

$\overline{LOAD}$	PFS1	PFS0	FQV8080 FQV8070 FQV8060 FQV8050 Default Offsets x, y(1)
0	0	0	127
0	0	1	255
0	1	0	511
0	1	1	63
1	0	0	1,023
1	0	1	15
1	1	0	31
1	1	1	7

$\overline{LOAD}$	PFS1	PFS0	FQV8080 FQV8070 FQV8060 FQV8050 Program Mode
1	X	X	Serial
0	X	X	Parallel

NOTES:

1. y = $\overline{PRAE}$ offset, x = $\overline{PRAF}$ offset

Table 11. Default Programmable Flag Offsets

$\overline{LOAD}$	PFS1	PFS0	FQV80100 FQV8090 Default Offsets x, y(1)
0	0	0	127
0	0	1	8,191
0	1	0	16,383
0	1	1	4,095
1	0	0	1,023
1	0	1	511
1	1	0	2,047
1	1	1	255

$\overline{LOAD}$	PFS1	PFS0	FQV80100 FQV8090 Program Mode
1	X	X	Serial
0	X	X	Parallel

NOTES:

1. y = $\overline{PRAE}$ offset, x = $\overline{PRAF}$ offset

Table 11. Default Programmable Flag Offsets (Continued)

JTAG Interface

Standard JTAG interface is used for boundary scan purposes. For a complete description, please refer to the IEEE Standard Test Access Port Specification (IEEE STD.1149.1 – 1990)

JTAG TIMING SPECIFICATIONS

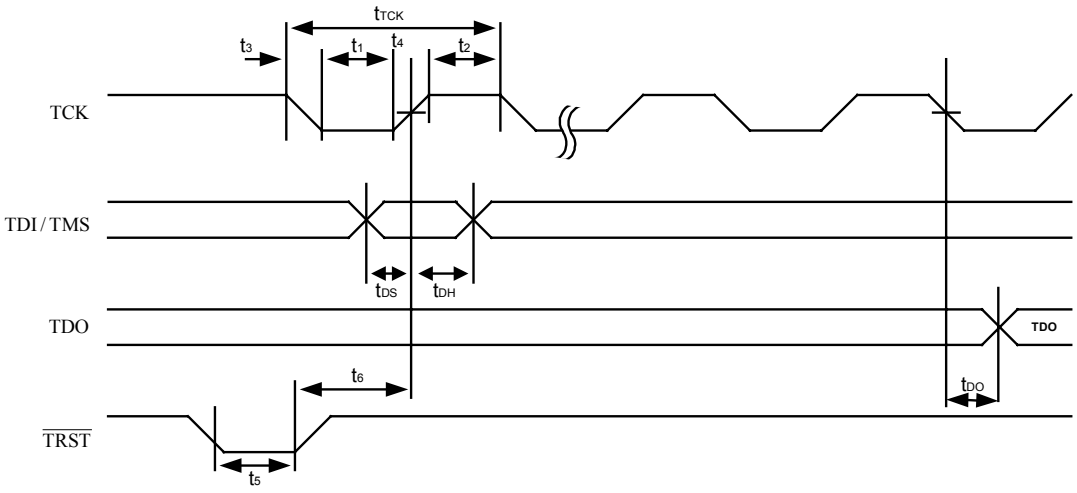


Figure 7. Standard JTAG Timing

Parameter	Symbol	Test Conditions	FQV80100 FQV8090 FQV8080 FQV8070 FQV8060 FQV8050 FQV8040 FQV8030 Min.	Max.	Units
System Interface Parameters					
Data Output	t_{DO} = Max	-	5	50	ns
Data Output Hold	t_{DOH}	-	5	-	ns
Data Input	t_{DS}	trise = 3ns	30	-	ns
	t_{DH}	tfall = 3ns	30	-	
JTAG AC Electrical Characteristics					
JTAG Clock Input Period	t_{TCK}	-	100	-	ns
JTAG Clock HIGH	$t_{TCKHIGH}$ (t_2)	-	40	-	ns
JTAG Clock Low	t_{TCKLOW} (t_1)	-	40	-	ns
JTAG Clock Rise Time	$t_{TCKRise}$ (t_4)	-	-	5	ns
JTAG Clock Fall Time	$t_{TCKFall}$ (t_3)	-	-	5	ns
JTAG Reset	t_{RST} (t_5)	-	50	-	ns
JTAG Reset Recovery	t_{RSR} (t_6)	-	50	-	ns

Table 12. JTAG AC Electrical Characteristics

JTAG BLOCK DIAGRAM

HBA's FlexQ™ offers IEEE Std. 1149.1-1990 standard JTAG interface to facilitate system debugging in all PBGA packages.

STANDARD JTAG INTERFACE ELEMENTS:

1. TAP – TEST ACCESS PORT
2. TAPCNTL – TAP CONTROLLER
3. IR – INSTRUCTION REGISTER
4. DR – DATA REGISTER

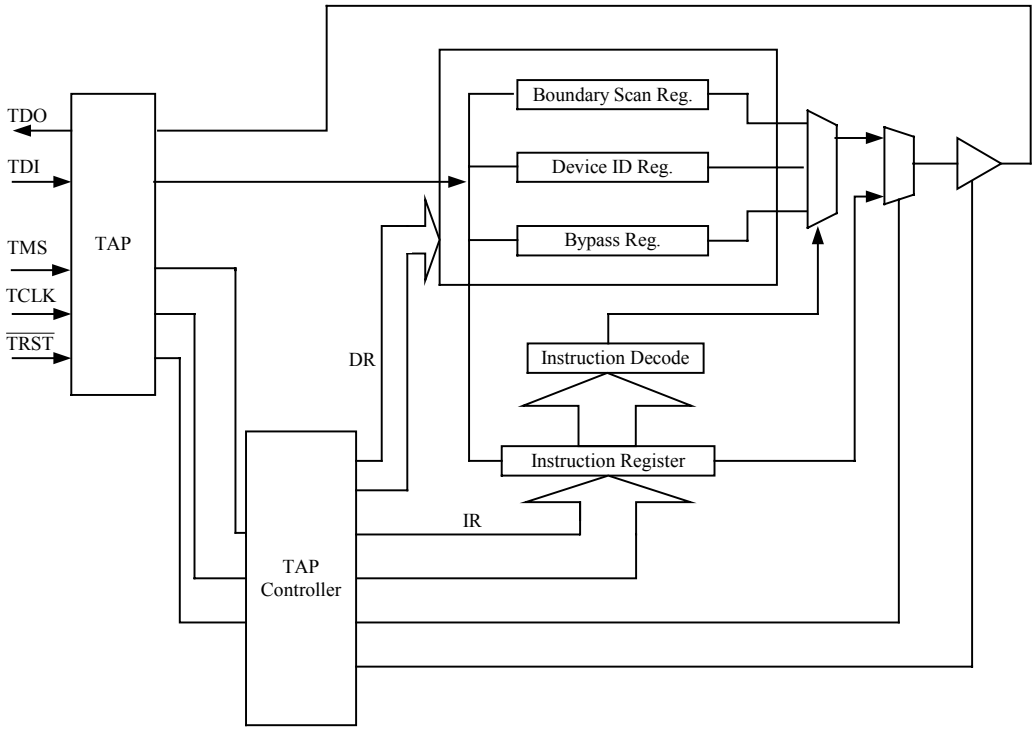


Figure 8. Boundary Scan Architecture Diagram

1. TAP

The basic ports to access the JTAG function. That includes four general input ports: $\overline{\text{TRST}}$, TCK, TMS, and TDI, and one general output port: TDO.

2. TAPCNTL

A finite state machine that provides instructions to the Instruction and Data Registers for data capture and update. Individual states are explained below.

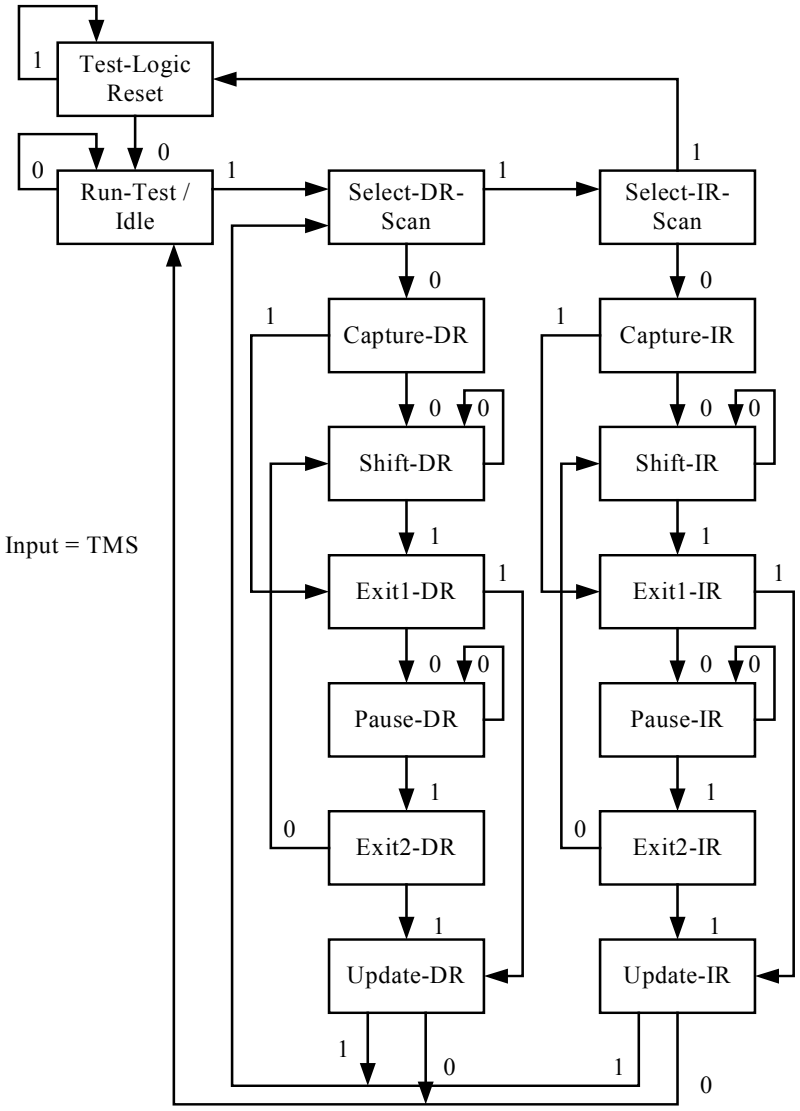


Figure 9. TAP Controller State Diagram

- **Capture-IR** Data are captured in parallel into the instruction register.
- **Capture-DR** Data are captured in parallel into the data register.
- **SHIFT-IR** LSB of the instruction register is shift in serially during a low to high transition of the TCK through TDI/TDO path
- **SHIFT-DR** LSB of the data register is shift in serially during a low to high transition of the TCK through TDI/TDO path.

- **UPDATE-IR** To shift Instruction Register Data to the parallel outputs. Instruction Register Data can be accessed through the internal bus.
- **UPDATE-DR** To shift Data Register Data to the parallel outputs. Data Register Data can be accessed through the internal bus.
- **EXIT1-IR/ EXIT2-IR** A transition state that terminates the scanning process. All Instruction Register data selected will retain their previous instruction state.
- **EXIT1-DR/ EXIT2-DR** A transition state that terminates the scanning process. All Data Register data selected will retain their previous data state.
- **PAUSE-IR** The temporary state to halt all serial shifting process between TDI and TDO. All data will retain their previous instruction state.
- **PAUSE-DR** The temporary state to halt all serial shifting process between TDI and TDO. All data will retain their previous data state.

3. INSTRUCTION REGISTER

A 4 - bit instruction register that is shifted serially at the rising edge of TCLK. The instruction is latched through the least significant bits of the nearest serial OUTPUT.

Hex Value	Instruction	Function
0 x 00	EXTEST	Select Boundary Scan Register
0 x 02	IDCODE	Select Chip Identification data register
0 x 01	SAMPLE/PRELOAD	Select Boundary Scan Register
0 x 03	HI-Z	JTAG
0 x 0F	BYPASS	Select Bypass Register

Table 13. JTAG Instruction Register Decoding Table

- **EXTEST** An instruction to facilitate external circuitry and board level interconnection verification.
- **IDCODE** An instruction to read out manufacture's identification, part number and version number.
- **SAMPLE/ PRE-LOAD** An instruction to allow snapshots of data flowing through the system pins. SAMPLE instruction MUST be executed prior to the selection of Boundary Scan test.
- **HIGH Z** An Instruction to place all output pins to high impedance state.
- **BYPASS** An Instruction to allow direct serial data shifting through TDI and TDO without any device operation.

4. DATA REGISTER

There are three data registers, Device ID register, BYPASS register, and Boundary Scan register. These parallel-connected registers are access through the common serial input and the common serial output.

- **Device ID Register** A 32-bit register that contains the specific manufacturer, part number and version number.

31(MSB) 28	27 12	11 1	0(LSB)
Version (4 bits) 0x0	Part Number (16-bit)	Manufacturer ID (11-bit) 0x16E	1

Device	Part # Field
FQV80100	0 x 8050
FQV8090	0 x 8056
FQV8080	0 x 8055
FQV8070	0 x 8054
FQV8060	0 x 8053
FQV8050	0 x 8052
FQV8040	0 x 8051
FQV8030	0 x 8057

Table 14. Device ID Register Decode Table

- **BYPASS Register** The data register that allows direct serial data shifting through TDI and TDO without any device operation.
- **BOUNDARY SCAN Register** The data register that allows the serial writes and read through TDI and TDO.

Timing Diagrams

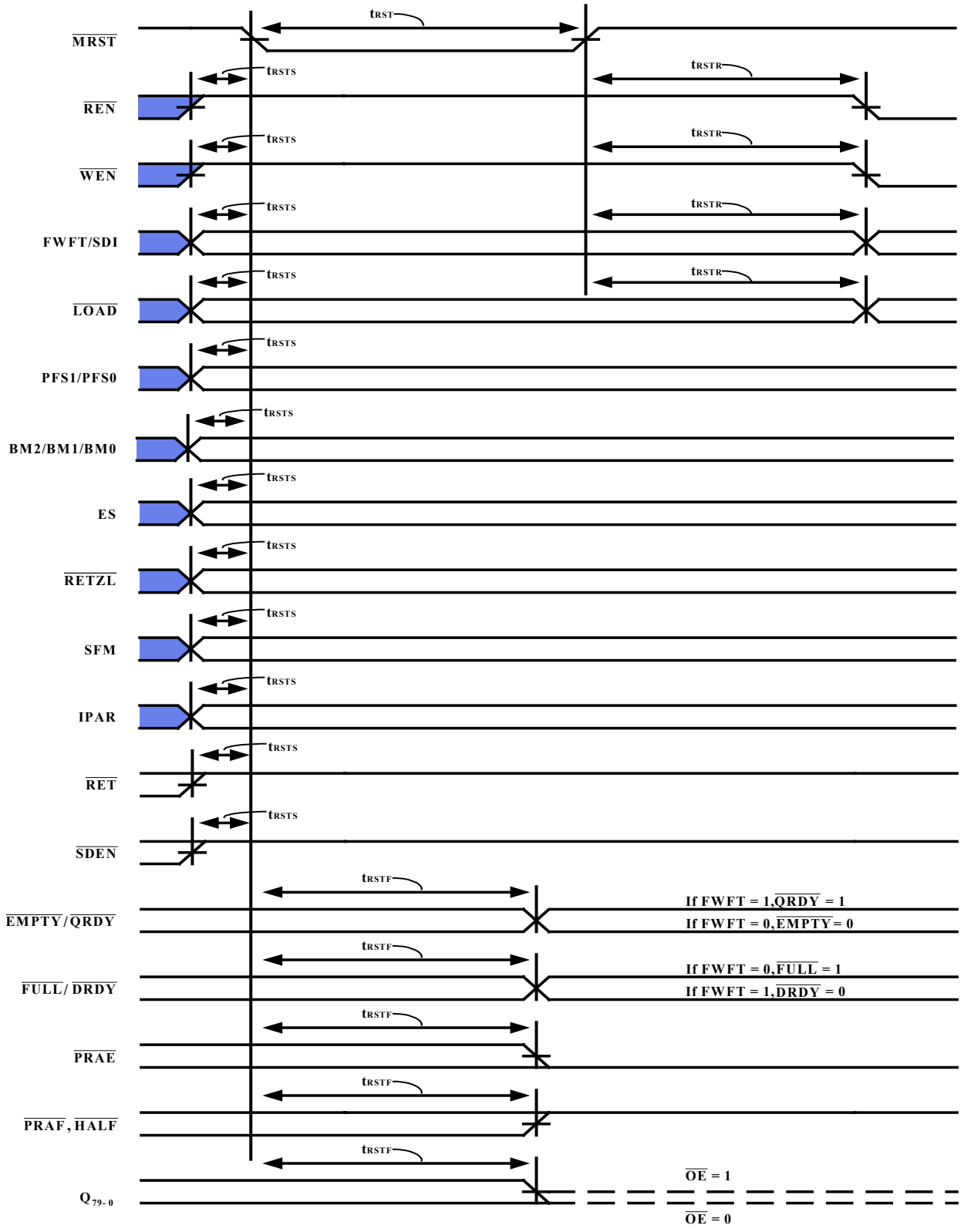


Diagram 1. Master Reset Timing

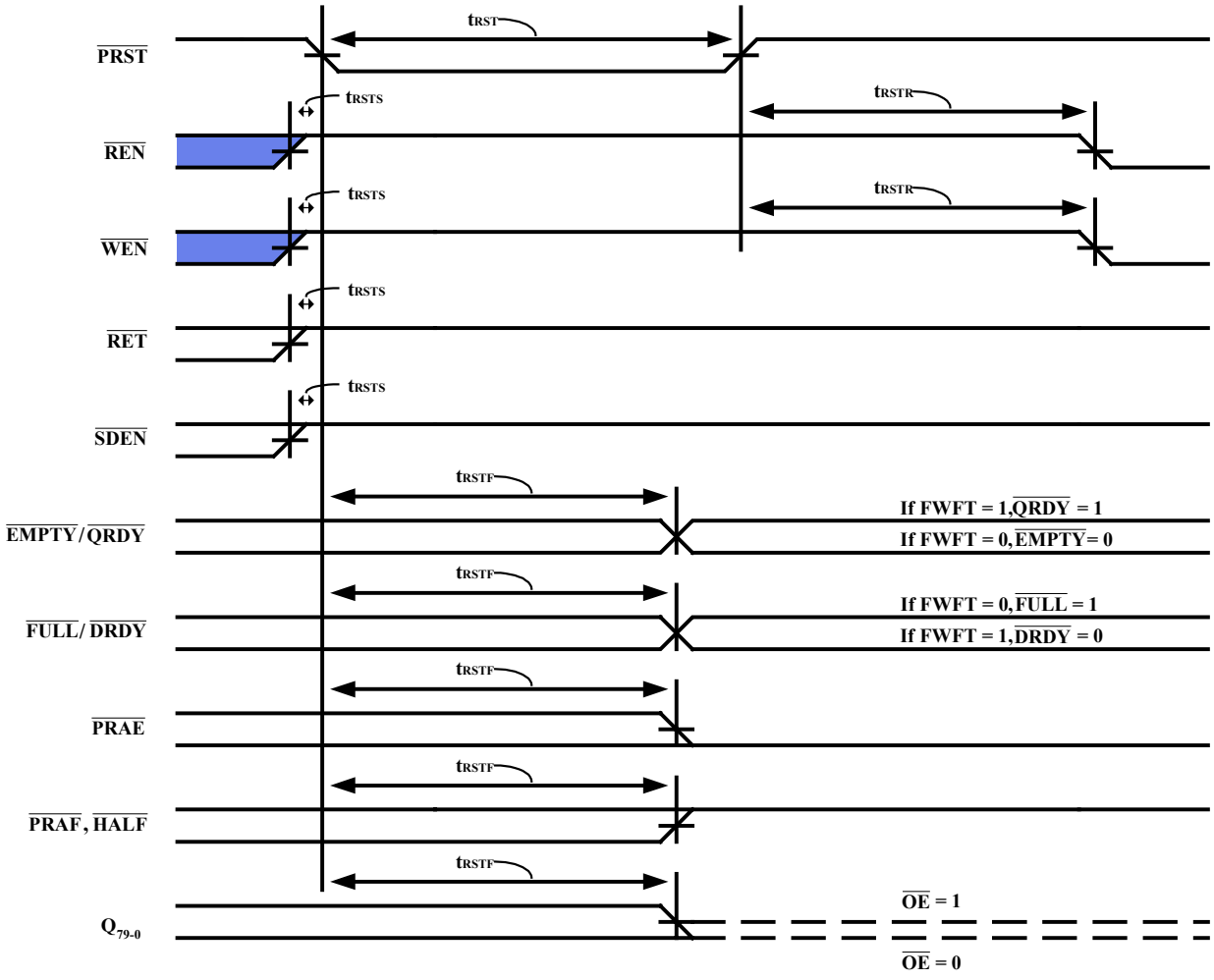
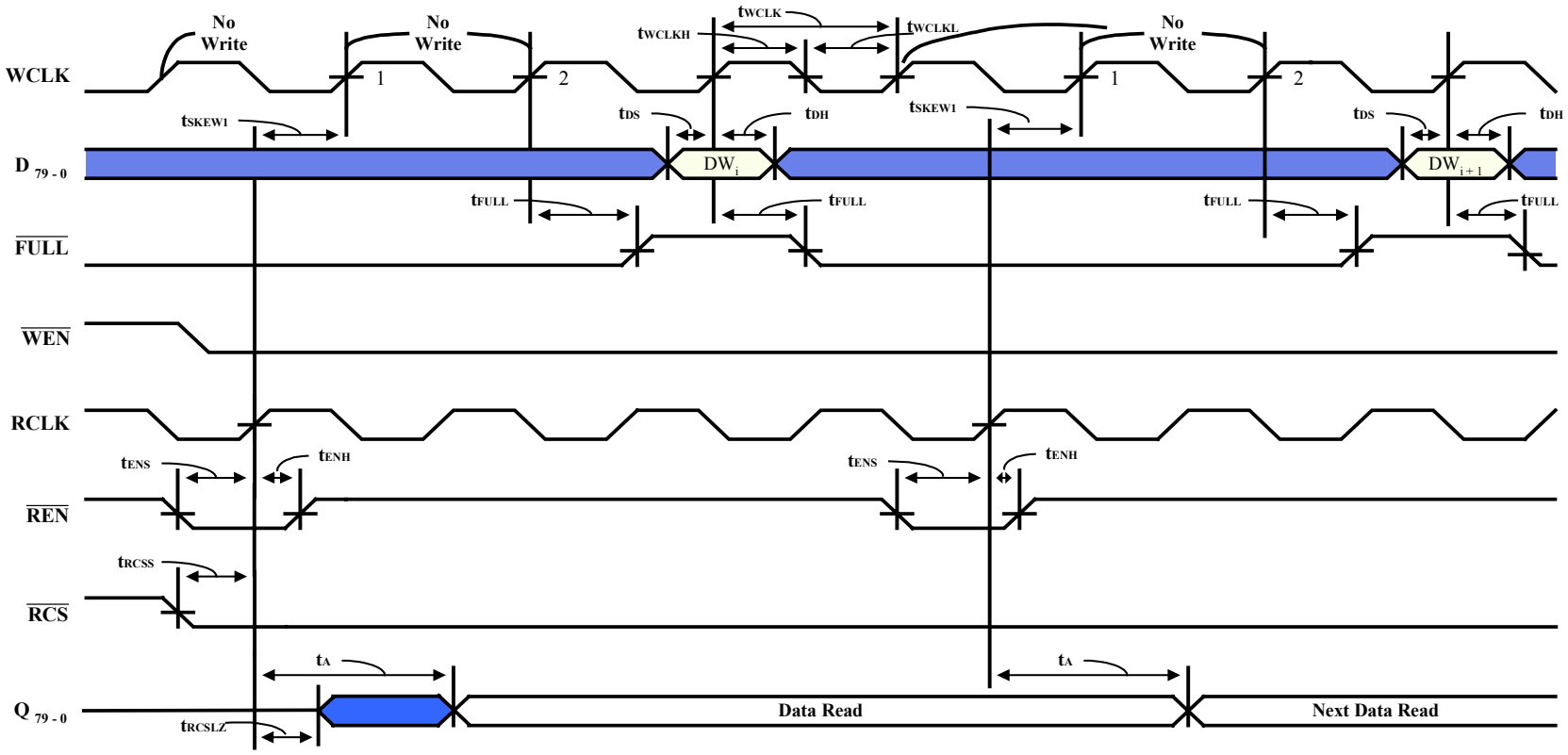


Diagram 2. Partial Reset Timing



NOTES:

1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW1}, $\overline{FULL}$ will go high (after one WCLK cycle plus t_{FULL}). If t_{SKEW1} is not met, then $\overline{FULL}$ will assert 1 or more WCLK cycles.
2. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.

Diagram 3. Write Cycle and Full Flag Timing (Standard Mode)

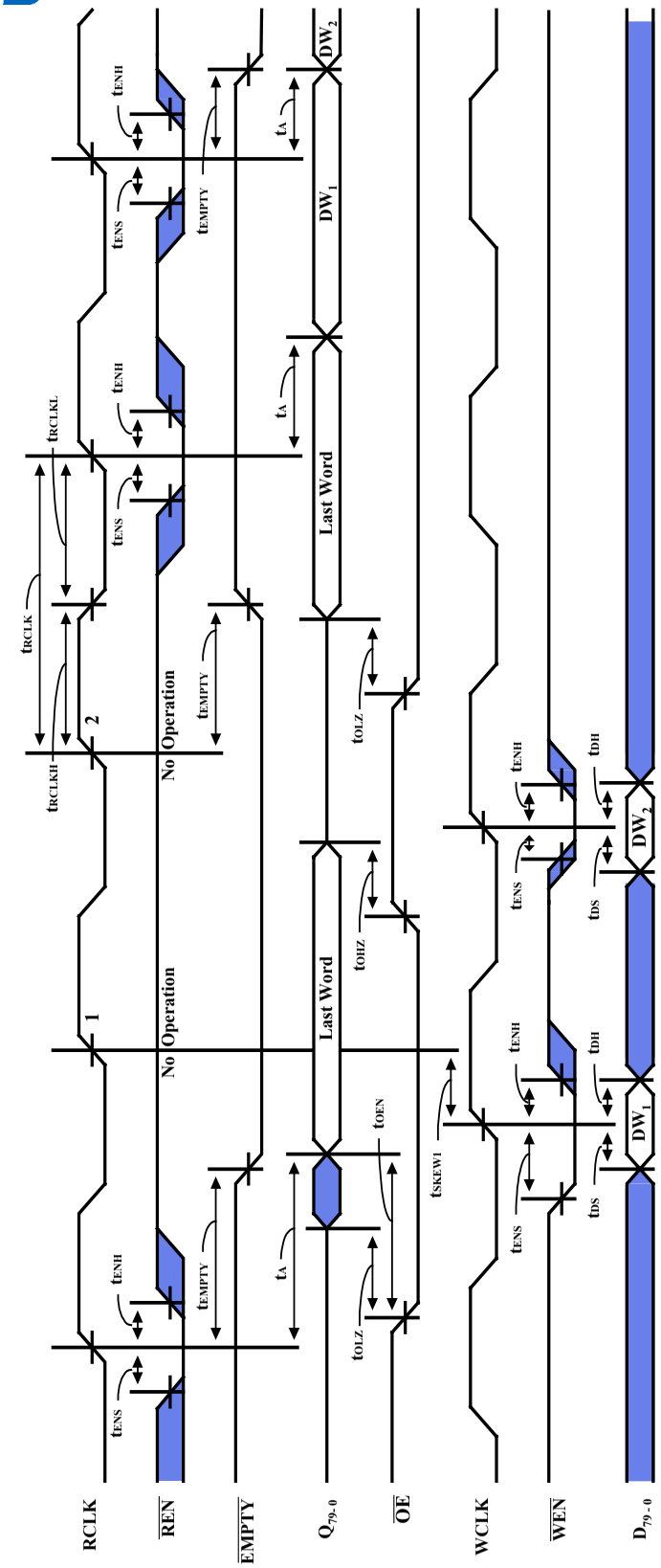


Diagram 4. Read Cycle, Empty Flag and First Data Word Latency Timing (Standard Mode)

NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW1}, $\overline{EMPTY}$ will go high (after RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.
2. $\overline{LOAD}$ = High.
3. First word latency: $t_{SKEW1} + t_{EMPTY} + 1 * t_{RCLK}$.

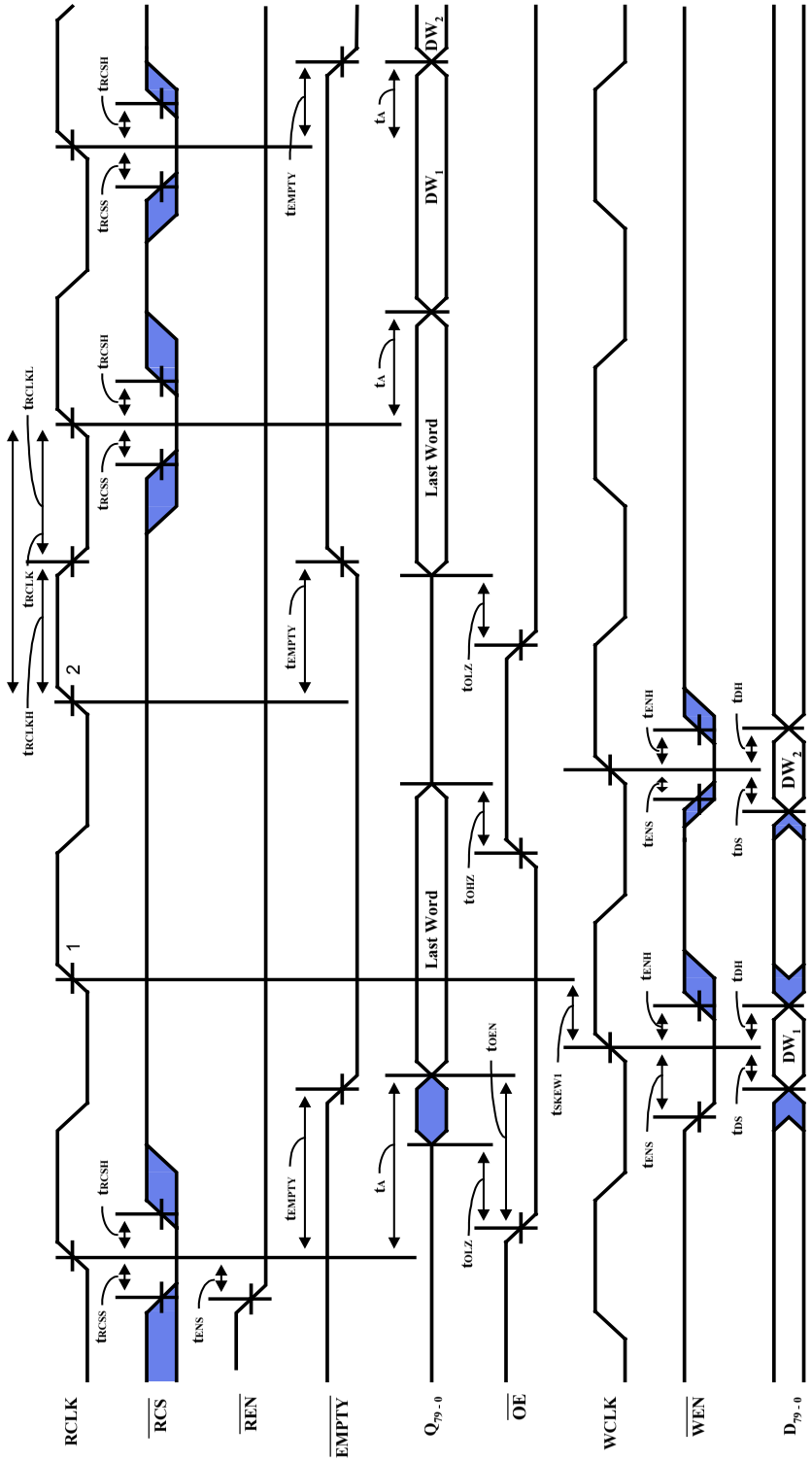
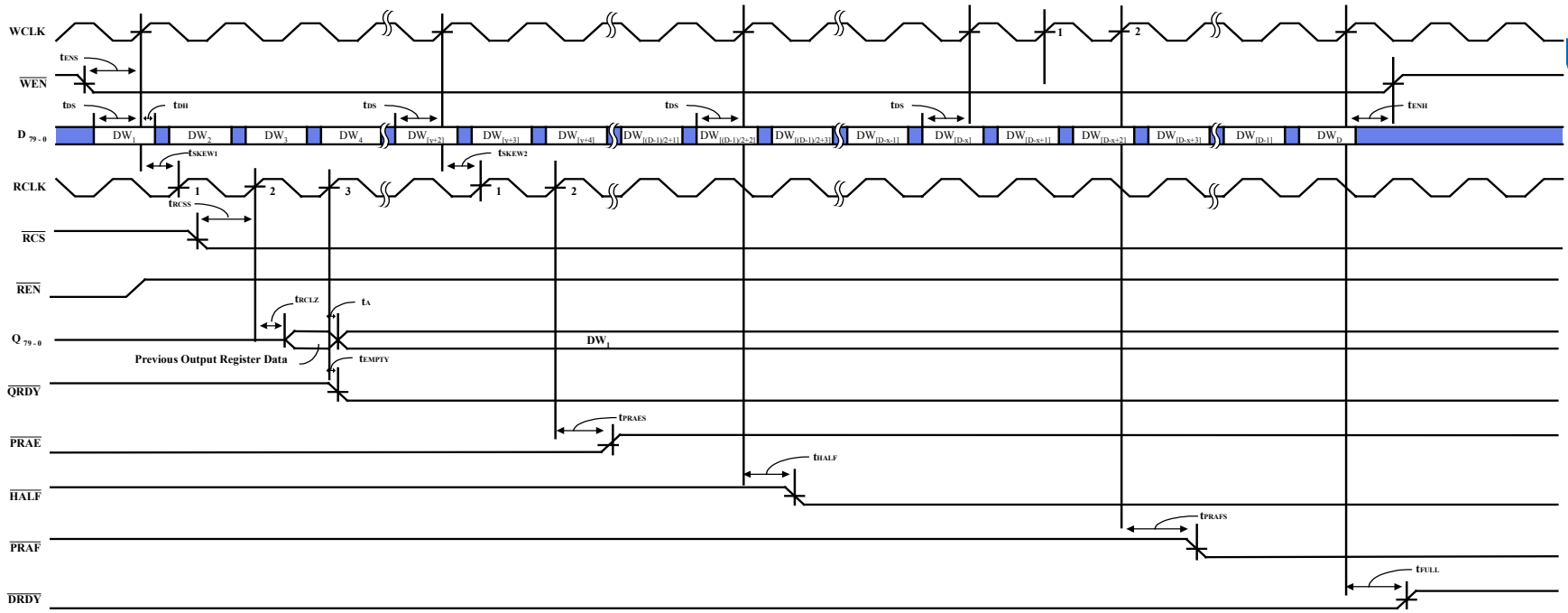


Diagram 5. Read Cycle and Read Chip Select Timing (Standard Mode)

NOTES:

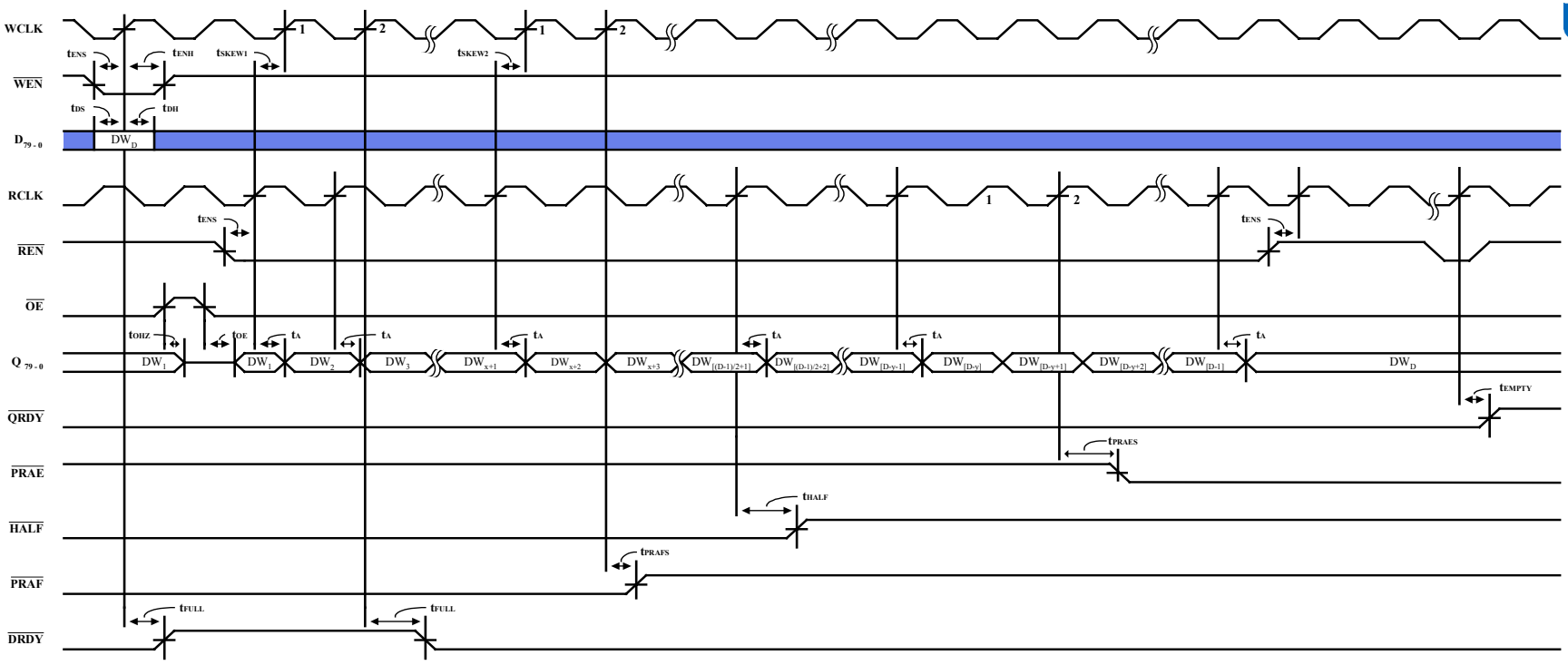
1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW1}, $\overline{EMPTY}$ will go high (after RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.
2. LOAD = High.
3. First word latency: $t_{SKEW1} + t_{EMPTY} + 1 * t_{RCLK}$.



NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to tSKEW1, $\overline{\text{QRDY}}$ will go low (after two RCLK cycle plus tEMPTY). If tSKEW1 is not met, then $\overline{\text{QRDY}}$ will assert 1 or more RCLK cycles.
2. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to tSKEW2, $\overline{\text{PRAE}}$ will go high (after one RCLK cycle plus tPRAES). If tSKEW2 is not met, then $\overline{\text{PRAE}}$ will assert 1 or more RCLK cycles.
3. $\overline{\text{LOAD}}$ = High, $\overline{\text{OE}}$ = Low.
4. y = $\overline{\text{PRAE}}$ offset, x = $\overline{\text{PRAF}}$ offset.
5. D = maximum queue depth. Please refer to Table 7 for Depth.
6. First word latency: tSKEW1 + tEMPTY + 2 * tRCLK

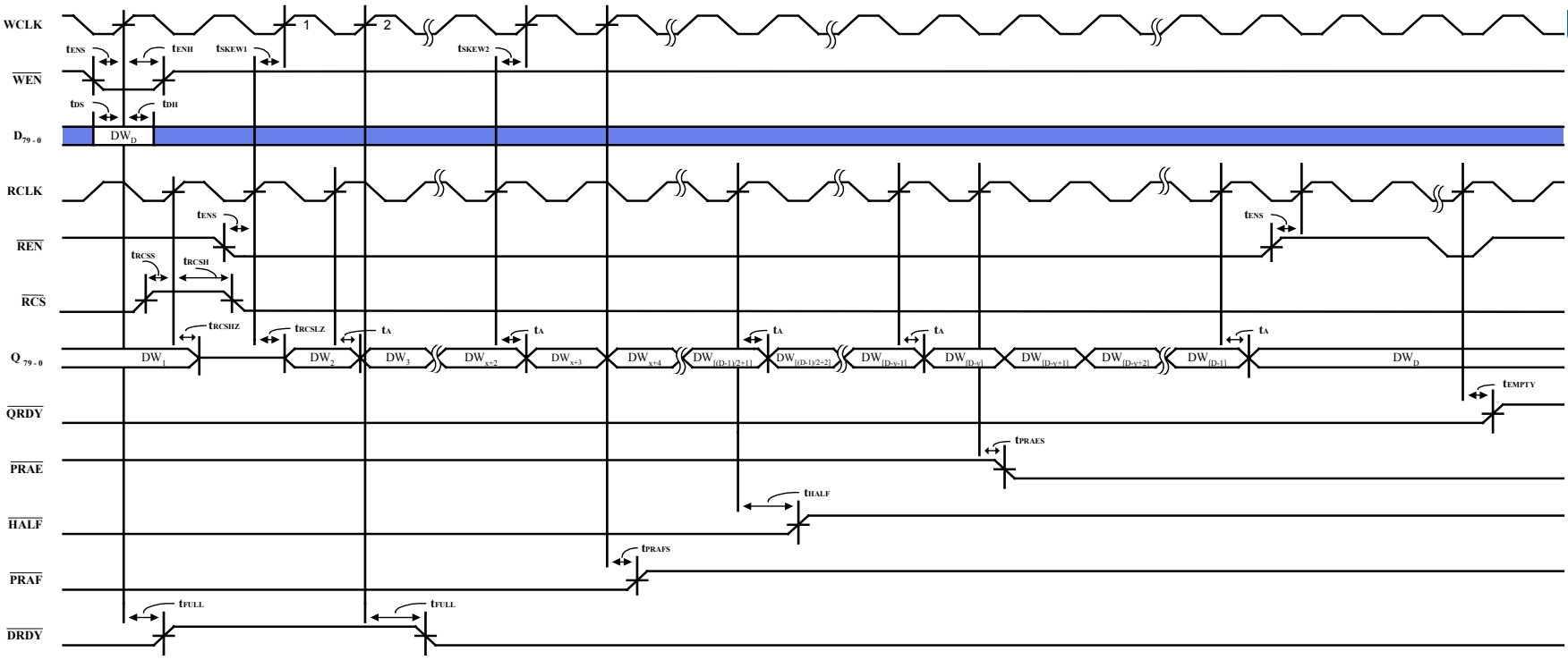
Diagram 6. Write Timing (FWFT Mode)



NOTES:

1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW1}, $\overline{DRDY}$ will go low (after one WCLK cycle plus t_{FULL}) . If t_{SKEW1} is not met, then $\overline{DRDY}$ will assert 1 or more WCLK cycles.
2. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW2}, $\overline{PRAF}$ will go high (after one WCLK cycle plus t_{PRAFS}) If t_{SKEW2} is not met, then $\overline{PRAF}$ will assert 1 or more WCLK cycles.
3. $\overline{LOAD}$ = High, $\overline{RCS}$= Low
4. y = $\overline{PRAE}$ Offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 7 for Depth.

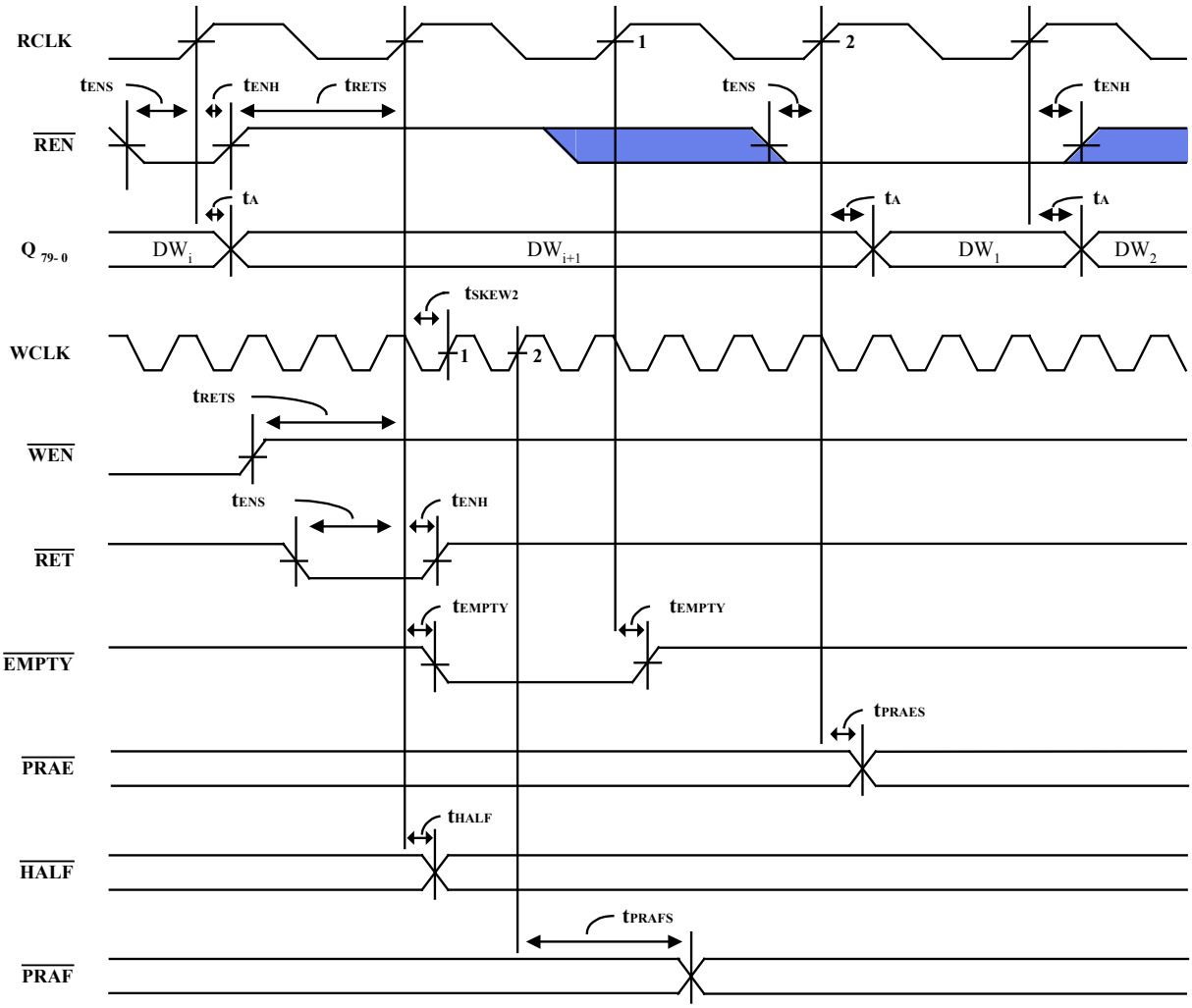
Diagram 7. Read Timing (FWFT Mode)



NOTES:

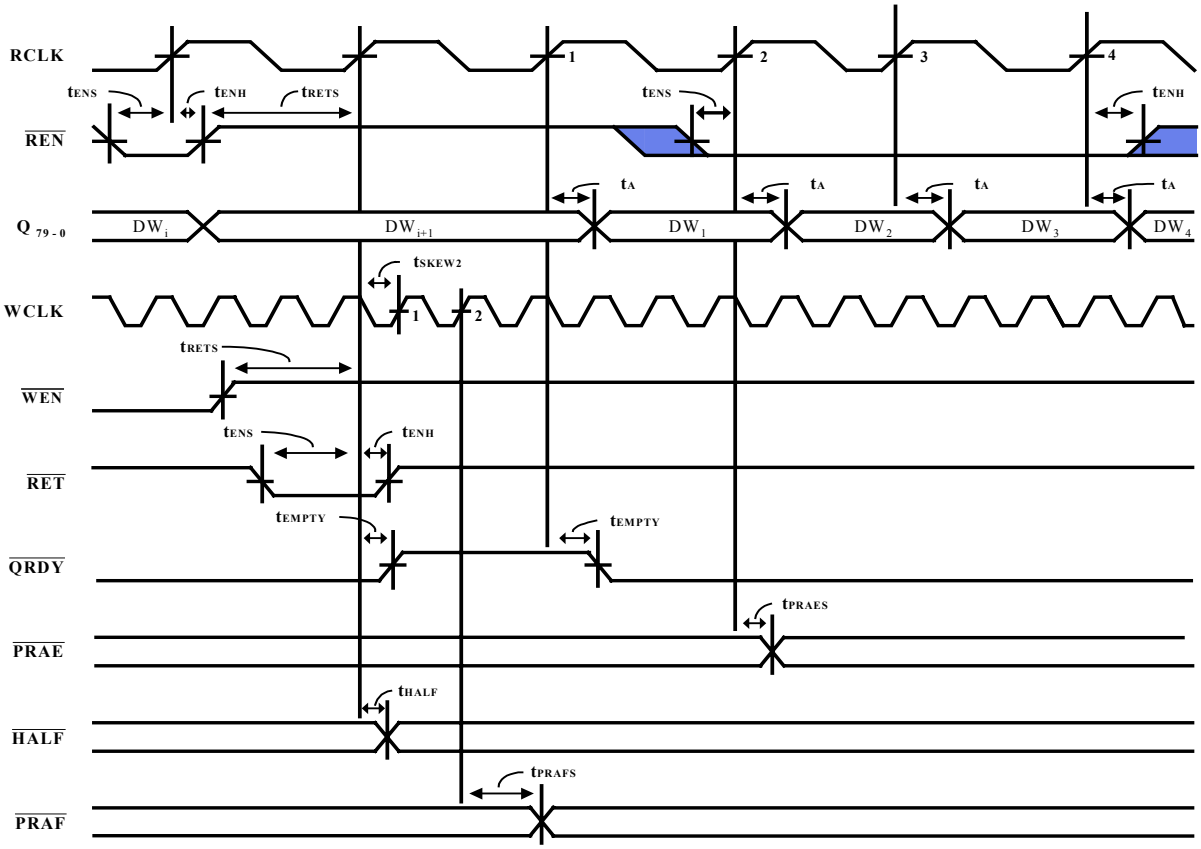
1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW1}, $\overline{DRDY}$ will go low (after one WCLK cycle plus t_{FULL}) . If t_{SKEW1} is not met, then $\overline{DRDY}$ will assert 1 or more WCLK cycles.
2. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW2}, $\overline{PRAF}$ will go high (after one WCLK cycle plus t_{PRAFS}) If t_{SKEW2} is not met, then $\overline{PRAF}$ will assert 1 or more WCLK cycles.
3. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.
4. y = $\overline{PRAE}$ Offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 7 for Depth.

Diagram 8. Read Cycle and Read Chip Select Timing (FWFT Mode)



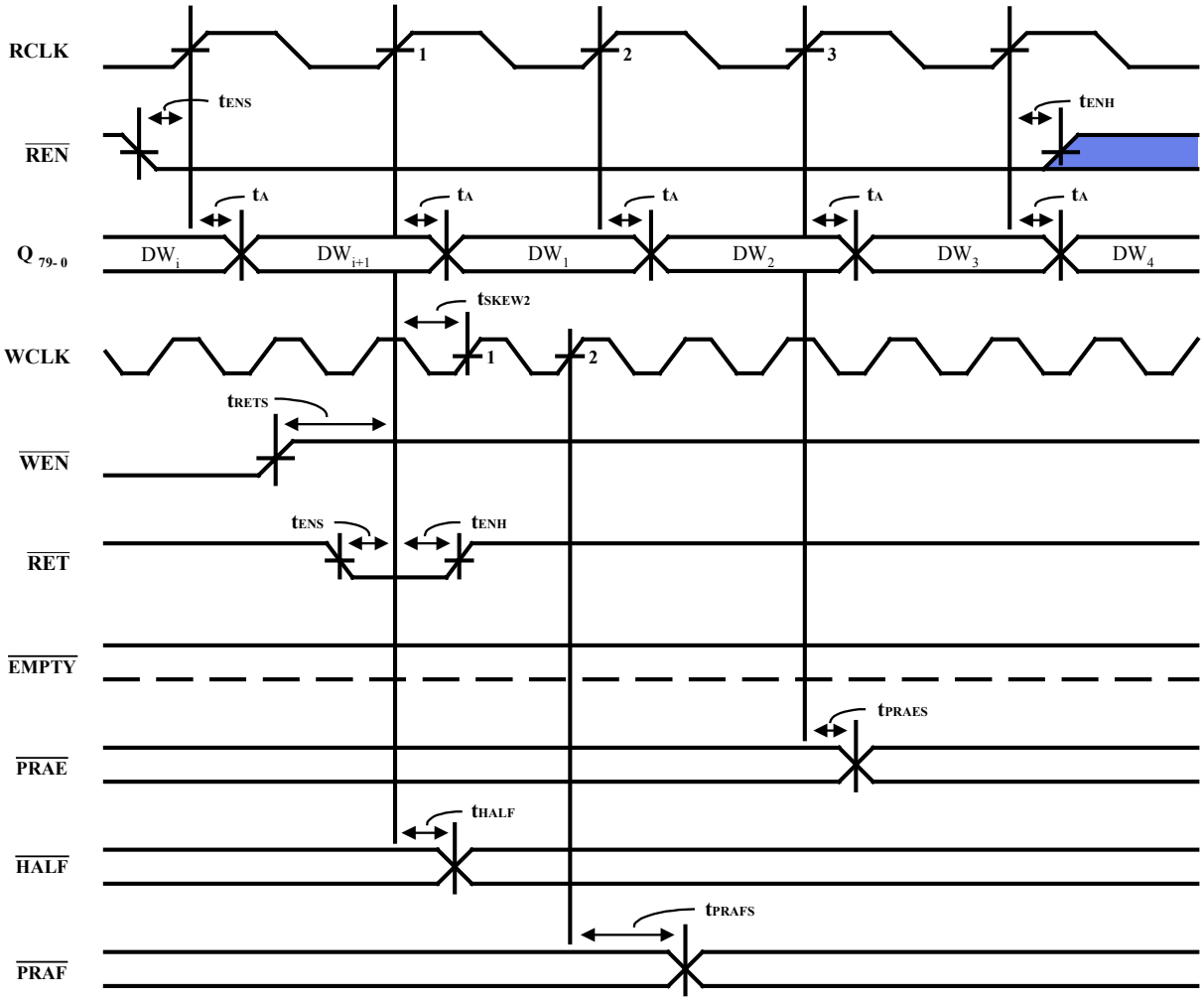
NOTES:
1. Upon completion of retransmit setup, a read operation can begin only after $\overline{\text{EMPTY}}$ returns high.
2. $\overline{\text{OE}}$ = Low.
3. DW_i = Words written to the queue after $\overline{\text{MRST}}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than 2 words written to the queue for a retransmit setup to be valid.

Diagram 9. Retransmit Timing (Standard Mode)



NOTES:
1. Upon completion of retransmit setup, a read operation can begin only after $\overline{QRDY}$ returns low.
2. $\overline{OE}$ = Low.
3. DW_i = Words written to the queue after $\overline{MRST}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than 2 words written to the queue for a retransmit setup to be valid.
5. Please refer to Table 7 for Depth.

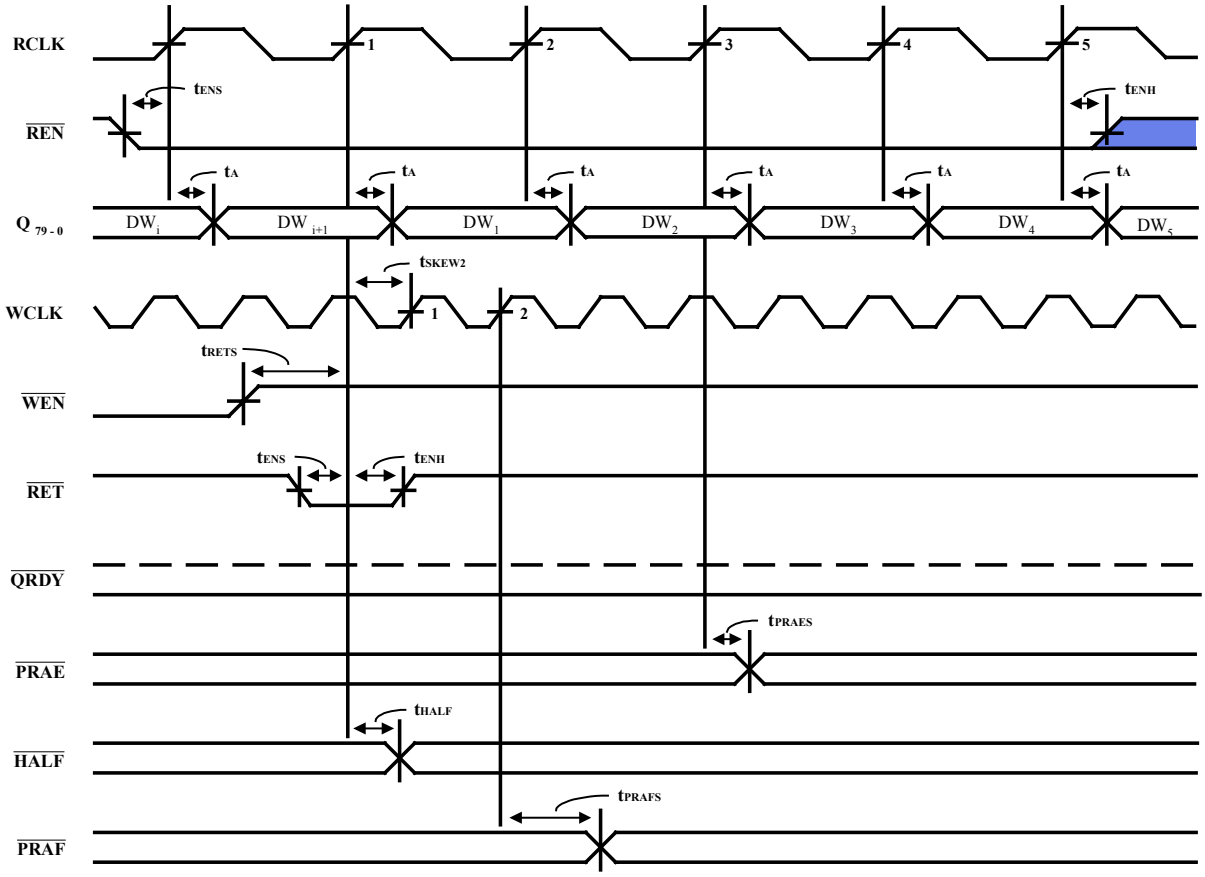
Diagram 10. Retransmit Timing (FWFT Mode)



NOTES:

1. If the part is empty at the point of retransmit, the Empty Flag ($\overline{\text{EMPTY}}$) will be updated based on RCLK (Retransmit Clock cycle). Valid data will appear on the output.
2. $\overline{\text{OE}}$ = Low; enables data to be read on outputs Q_{79-0}.
3. DW_1= first word written to the queue after Master Reset; DW_2= second word written to the queue after Master Reset.
4. No more than D-2 may be written to the queue between reset (Master or Partial) and retransmit setup. Therefore, $\overline{\text{FULL}}$ will be high throughout the retransmit setup procedure. Please refer to Table 7 for Depth.
5. There must be at least two words written to zero latency retransmit from the queue before a retransmit operation can be invoked.
6. $\overline{\text{RETZL}}$ is set Low during $\overline{\text{MRST}}$.

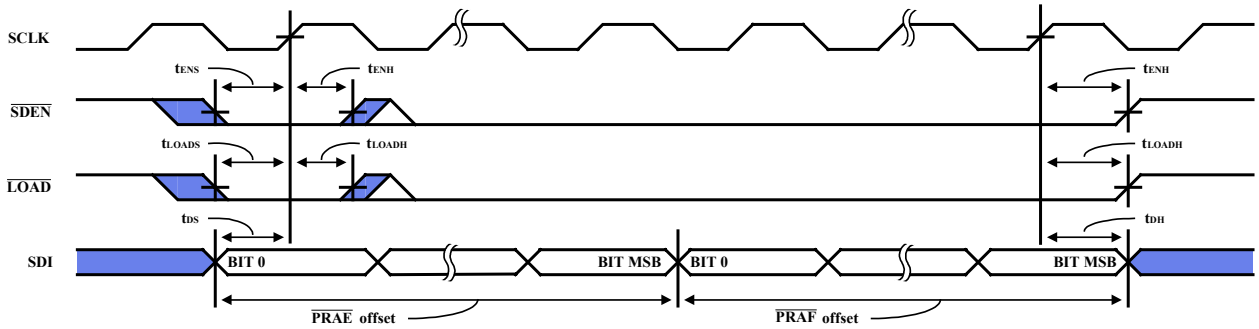
Diagram 11. Zero Latency Retransmit Timing (Standard Mode)



NOTES:

1. If the part is empty at the point of retransmit, the output ready flag ($\overline{QRDY}$) will be updated based on RCLK (Retransmit Clock cycle). Valid data will appear on the output.
2. No more than D-2 words maybe written to the queue between reset (Master or Partial) and retransmit setup. Therefore, $\overline{DRDY}$ will be low throughout the retransmit setup procedure. Please refer to Table 7 for Depth.
3. $\overline{OE}$ = Low.
4. DW_1, DW_2, DW_3 = first, second and third words written to the queue after Master Reset.
5. There must be at least two words written to the queue before a retransmit operation can be invoked.
6. $\overline{RETZL}$ is set low during $\overline{MRST}$.

Diagram 12. Zero Latency Retransmit Timing (FWFT Mode)



*Refer to Table 13

Diagram 13. Serial Loading of Programmable Flag Registers (Standard and FWFT Mode)

	FQV80100	FQV8090	FQV8080	FQV8070	FQV8060	FQV8050	FQV8040	FQV8030
MSB	15	14	13	12	11	10	9	8

Table 13. Reference Table for Diagram 13

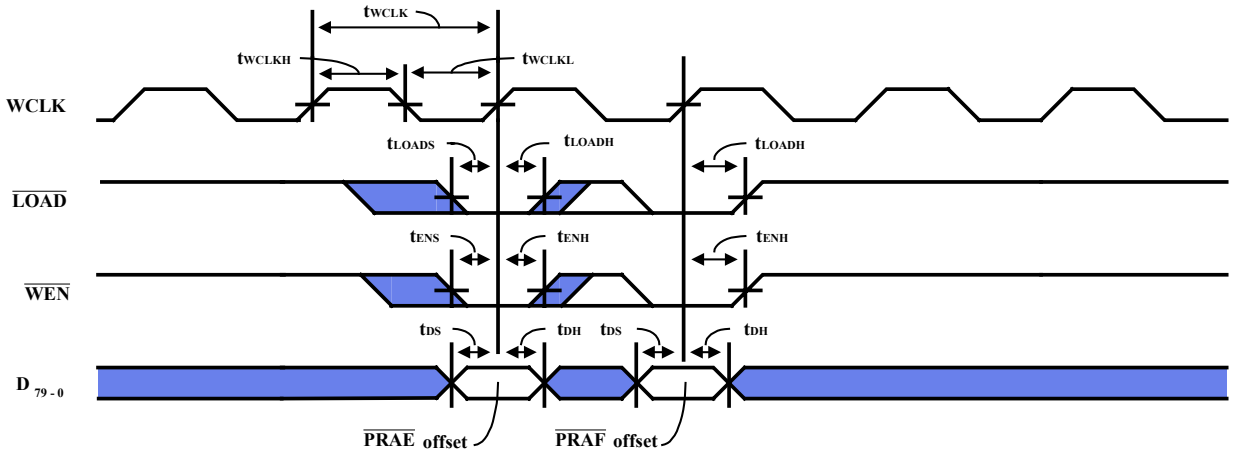
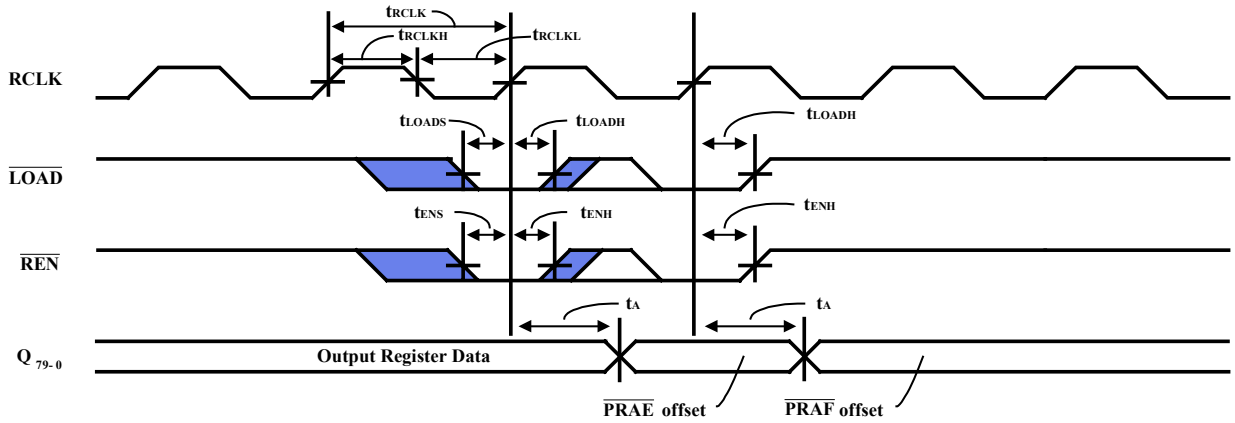


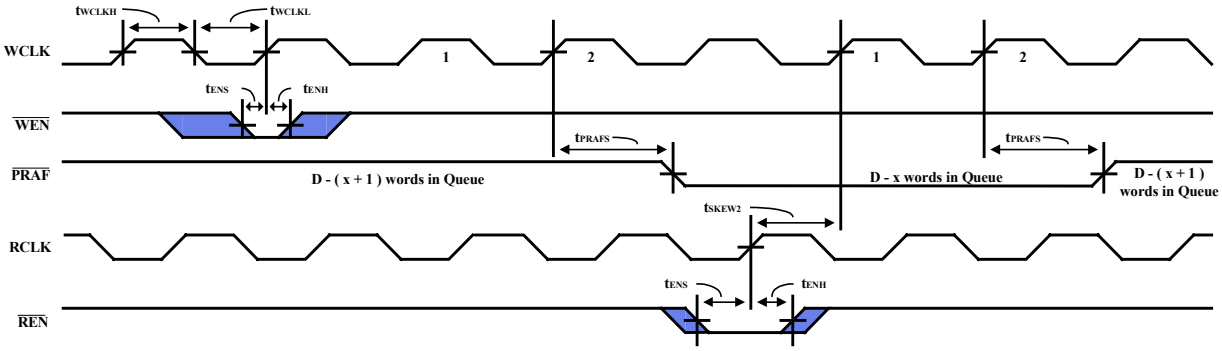
Diagram 14. Parallel Loading of Programmable Flag Registers for (Standard and FWFT Mode)



NOTES:

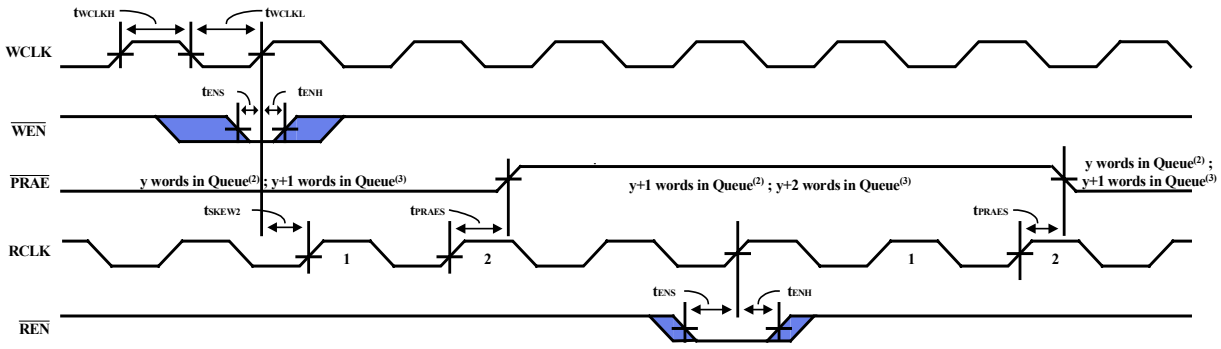
1. $\overline{OE}$ = Low, $\overline{RCS}$ = Low.

Diagram 15. Parallel Read of Programmable Flag Registers for (Standard and FWFT Mode)



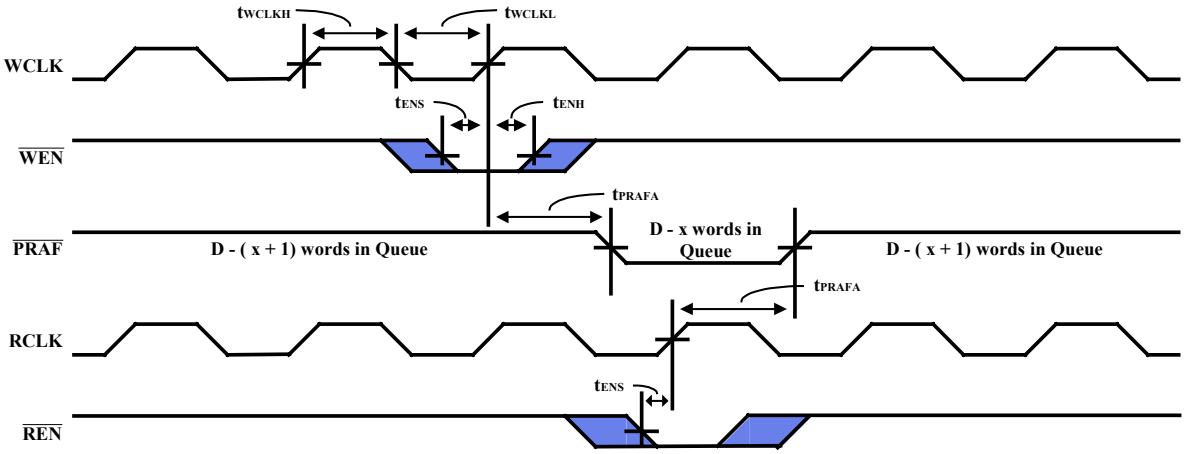
NOTES:
1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth. Please refer to Table 7 for Depth.
3. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW2}, $\overline{\text{PRAF}}$ will go high (after on WCLK cycle plus t_{PRAFS}). If t_{SKEW2} is not met, then $\overline{\text{PRAF}}$ will assert 1 or more WCLK cycles.
4. $\overline{\text{PRAF}}$ synchronizes to the rising edge of WCLK only.

Diagram 16. Synchronous Programmable Almost-Full Flag Timing (Standard and FWFT Mode)



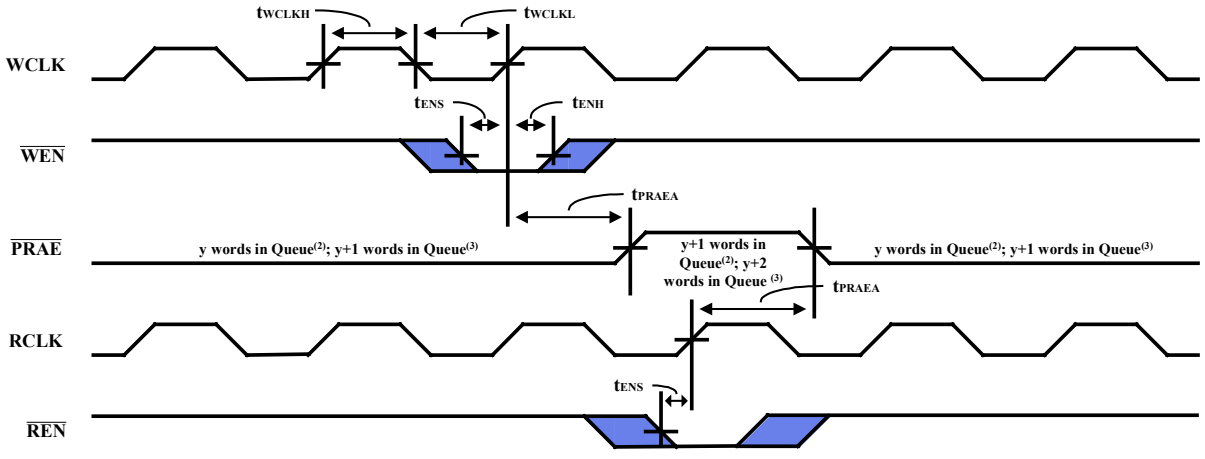
NOTES:
1. y = $\overline{\text{PRAE}}$ offset.
2. For Standard Mode.
3. For FWFT Mode.
4. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW2}, $\overline{\text{PRAE}}$ will go high (after one RCLK cycle plus t_{PRAES}). If t_{SKEW2} is not met, then $\overline{\text{PRAE}}$ will assert 1 or more RCLK cycles.
5. $\overline{\text{PRAE}}$ synchronizes to the rising edge of RCLK only.

Diagram 17. Synchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Mode)



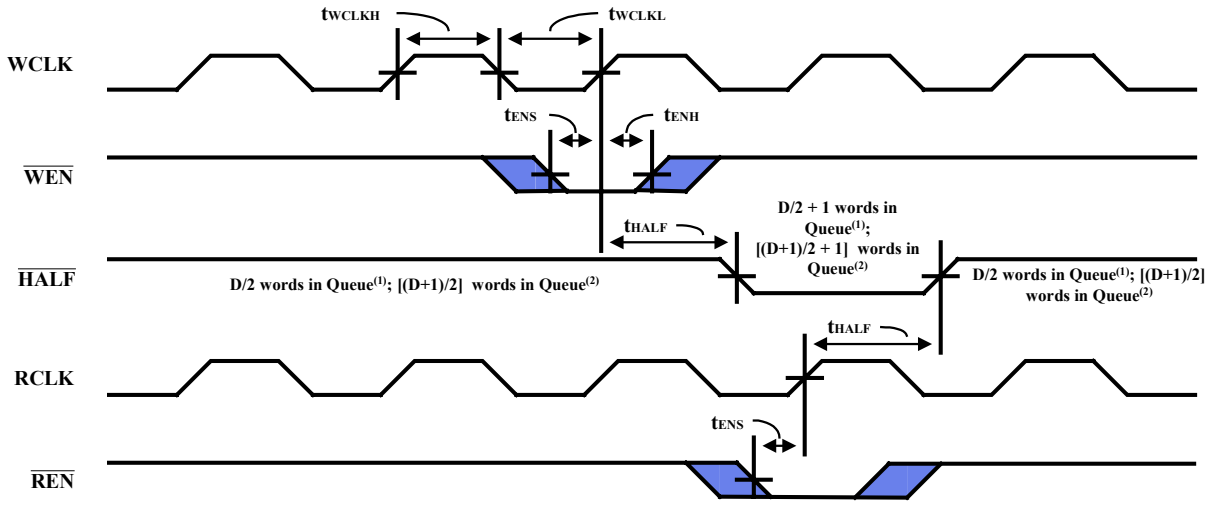
NOTES:
1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth. Please refer to Table 7 for Depth.
3. $\overline{\text{PRAF}}$ is asserted to low on WCLK transition and reset to high on RCLK transition.
4. Select this mode by setting SFM low during Master Reset.

Diagram 18. Asynchronous Programmable Almost-Full Flag Timing (Standard and FWFT Mode)



NOTES:
1. y = $\overline{\text{PRAE}}$ offset.
2. For Standard Mode.
3. For FWFT Mode.
4. $\overline{\text{PRAE}}$ is asserted to low on RCLK transition and reset to high on WCLK transition.
5. Select this mode by setting SFM low during Master Reset.

Diagram 19. Asynchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Mode)



NOTES:
1. For Standard Mode.
2. For FWFT Mode.
3. Please refer to Table 7 for Depth.

Diagram 20. Half-Full Flag Timing (Standard and FWFT Mode)

Order Information:

HBA Device Family	Device Type	Power	Speed (ns) *	Package**	Temperature Range
XX	XXXXX	X	XX	XX	X
FQ	**V80100** (65,536 x 80)	Low	**6** – 166 MHz	**BB**	Blank – Commercial (0°C to 70°C)
	V8090 (32,768 x 80)		**7-5** – 133 MHz		**I** – Industrial (-40° to 85°C)
	V8080 (16,384 x 80)		**10** – 100 MHz		
	V8070 (8,192 x 80)				
	V8060 (4,096 x 80)				
	V8050 (2,048 x 80)				
	V8040 (1,024 x 80)				
	V8030 (512 x 80)				

***Speed –** 6ns available only in Commercial temp (0°C to 70°C)
****Package** – 256 pin Fine Pitch Ball Grid Array (BGA)

Example:

FQV8070L6BB (8k x 80, 6ns, Commercial temp)
FQV8060L10BBI (4k x 80, 10ns, Industrial temp)

Document Revision History:

11/04/02 pg. 1, 3, 4, 5, 6, 15, 18, 31
11/15/02 pg. 9, 11, 12, 14, 15, 16, 22, 23, 31, 34, 35, 36, 37, 38, 39, 45, 47, 48, 50

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