



## 2.8 Volt x16 Very Low Power Dual-Port Static RAM

Memory	Device
4K x 16	HDV24VL

### Key Features:

- Very low power true Dual-Port Static RAM with high speed access
- Simultaneous memory access through two ports
- LVTTTL compatible; 2.8V power supply
- Bus Width can easily expand to over 16 bits by using both MASTER and SLAVE select function
- Interrupt, Semaphore, and Busy Logic
- Supports Interrupt and Semaphore arbitration schemes
- Available packages: 108 ball 8mmx8mm 0.5mm pitch BGA and 84 ball 7mmx7mm 0.5mm pitch BGA
- (-40°C to 85°C) Industrial operating temperature available for access time of 55ns

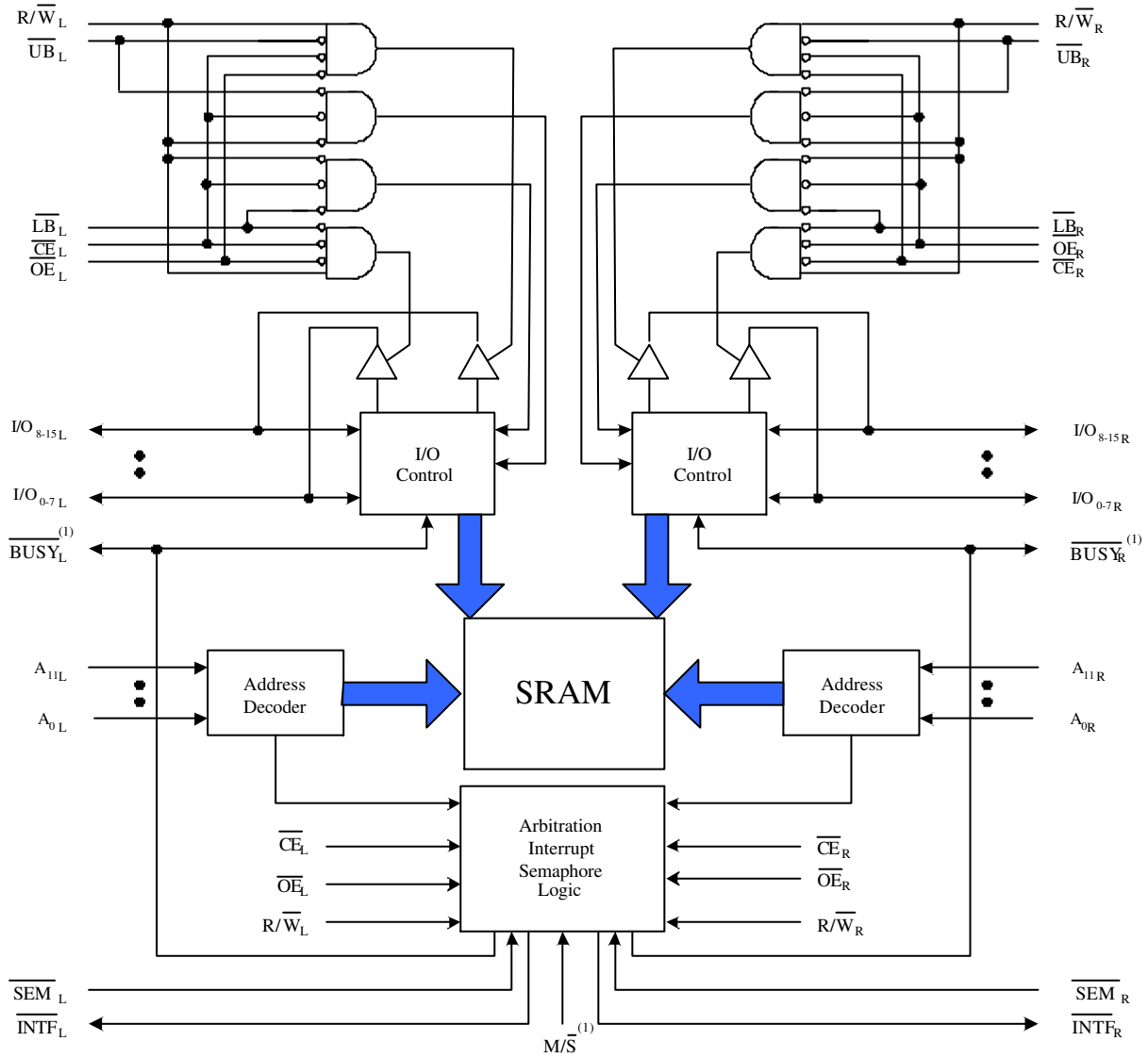
### Product Description:

The HDV24VL Dual-Port Static RAM offers industry leading CMOS process technology and 4K x 16 memory configuration. The device supports two memory ports with independent control, address, and I/O pins that enable simultaneous, asynchronous access to any location in memory. System designer has full flexibility of implementing deeper and wider memory using the depth and width expansion features.

The HDV24VL is a stand alone 4K x 16 Asynchronous Dual-Port SRAM. For 32 bits or more bus width, the MASTER/SLAVE pin offers bus width expansion without additional discrete logic. Bus width expansion can easily be done without external logic.

The device has low power consumption, hence minimizing system power requirements. It is ideal for applications such as data communication, telecommunication, multiprocessing, test equipment, network switching, etc.

**Block Diagram of Dual Port Static RAM  
 4K x 16**



**Figure 2. Device Architecture**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
A	I/O <sub>8R</sub>	I/O <sub>7R</sub>	NC	I/O <sub>6R</sub>	I/O <sub>4R</sub>	I/O <sub>2R</sub>	I/O <sub>1R</sub>	VCC	I/O <sub>13L</sub>	GND	I/O <sub>10L</sub>	NC	I/O <sub>9L</sub>	GND				
B	I/O <sub>9R</sub>													I/O <sub>7L</sub>				
C	I/O <sub>11R</sub>	GND	VCC	I/O <sub>5R</sub>	I/O <sub>3R</sub>	I/O <sub>0R</sub>	I/O <sub>15L</sub>	I/O <sub>12L</sub>	NC	VCC	I/O <sub>8L</sub>			I/O <sub>6L</sub>				
D	VCC	I/O <sub>10R</sub>									I/O <sub>5L</sub>			I/O <sub>4L</sub>				
E	I/O <sub>13R</sub>	VCC	<table border="1" style="margin: auto;"> <tr> <td>NC</td> <td>GND</td> <td>GND</td> <td>I/O<sub>14L</sub></td> <td>I/O<sub>11L</sub></td> <td>VCC</td> </tr> </table>				NC	GND	GND	I/O <sub>14L</sub>	I/O <sub>11L</sub>	VCC			GND			VCC
NC	GND	GND	I/O <sub>14L</sub>	I/O <sub>11L</sub>	VCC													
F	I/O <sub>15R</sub>	I/O <sub>14R</sub>	<table border="1" style="margin: auto;"> <tr> <td>I/O<sub>12R</sub></td> <td colspan="3"></td> <td>I/O<sub>3L</sub></td> </tr> </table>				I/O <sub>12R</sub>				I/O <sub>3L</sub>			I/O <sub>2L</sub>			I/O <sub>1L</sub>	
I/O <sub>12R</sub>				I/O <sub>3L</sub>														
G	R/W <sub>R</sub>	OE <sub>R</sub>	<table border="1" style="margin: auto;"> <tr> <td>GND</td> <td colspan="3"></td> <td>OE<sub>L</sub></td> </tr> </table>				GND				OE <sub>L</sub>			GND			I/O <sub>0L</sub>	
GND				OE <sub>L</sub>														
H	GND	GND	<table border="1" style="margin: auto;"> <tr> <td>SEM<sub>R</sub></td> <td colspan="3"></td> <td>VCC</td> </tr> </table>				SEM <sub>R</sub>				VCC			SEM <sub>L</sub>			R/W <sub>L</sub>	
SEM <sub>R</sub>				VCC														
J	CE <sub>R</sub>	UB <sub>R</sub>	<table border="1" style="margin: auto;"> <tr> <td>LB<sub>R</sub></td> <td colspan="3"></td> <td>LB<sub>L</sub></td> </tr> </table>				LB <sub>R</sub>				LB <sub>L</sub>			CE <sub>L</sub>			VCC	
LB <sub>R</sub>				LB <sub>L</sub>														
K	NC	A <sub>11R</sub>	<table border="1" style="margin: auto;"> <tr> <td>A<sub>7R</sub></td> <td>A<sub>0R</sub></td> <td>M/S</td> <td>GND</td> <td>A<sub>0L</sub></td> <td>NC</td> </tr> </table>				A <sub>7R</sub>	A <sub>0R</sub>	M/S	GND	A <sub>0L</sub>	NC			A <sub>11L</sub>			UB <sub>L</sub>
A <sub>7R</sub>	A <sub>0R</sub>	M/S	GND	A <sub>0L</sub>	NC													
L	A <sub>10R</sub>	A <sub>9R</sub>									A <sub>9L</sub>			NC				
M	A <sub>8R</sub>	NC	A <sub>4R</sub>	A <sub>2R</sub>	BUSY <sub>R</sub>	GND	VCC	INTF <sub>L</sub>	A <sub>2L</sub>	A <sub>4L</sub>	A <sub>7L</sub>			A <sub>10L</sub>				
N	A <sub>6R</sub>													A <sub>8L</sub>				
P	A <sub>5R</sub>	NC	A <sub>3R</sub>	A <sub>1R</sub>	INTF <sub>R</sub>	NC	GND	NC	BUSY <sub>L</sub>	A <sub>1L</sub>	A <sub>3L</sub>	NC	A <sub>5L</sub>	A <sub>6L</sub>				

**Top View**

**Figure 3.108-Ball 0.5mm Pitch BGA (Order code: BZ)**

	1	2	3	4	5	6	7	8	9	10	11	12
A	I/O8L	I/O7L	I/O5L	I/O2L	$\overline{OE}L$	VCC	$\overline{R\#}WL$	A8L	A11L	A10L	A6L	A7L
B	I/O9L											A5L
C	I/O10L	I/O6L	I/O4L	I/O0L	GND	$\overline{SE}ML$	$\overline{CE}L$	$\overline{UB}L$	A9L			A2L
D	I/O11L	I/O13L							A4L			A3L
E	I/O15L	GND	I/O3L	I/O1L	$\overline{LB}L$	GND			A1L			$\overline{BUSY}L$
F	GND	I/O0R	GND	HDV24VL 0.5mm Pitch 84 pin BGA Top view			$\overline{INT}L$	M/S			$\overline{BUSY}R$	
G	I/O2R	GND	I/O14L				I/O12L			A3R	$\overline{INTR}$	
H	I/O3R	VCC	VCC	GND	GND	I/O1R			A0L			A0R
J	I/O4R	I/O12R							A2R			A1R
K	I/O5R	I/O11R	I/O13R	I/O14R	I/O6R	$\overline{UB}R$	$\overline{LB}R$	A10R	A8R			A3R
L	I/O7R											A4R
M	I/O8R	I/O9R	I/O10R	I/O15R	$\overline{OE}R$	$\overline{R\#}WR$	$\overline{SE}MR$	$\overline{CE}R$	A11R	A7R	A6R	A5R

**NOTES:**

All VCC connect to power supply and all GND connect to ground supply.

**84-Ball 0.5mm Pitch BGA (Order code: BY)**

**Figure 4. Device Pin-Out**

Left Port	Right Port	Name
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L-11L}$	$A_{0R-11R}$	Address
$I/O_{0-15L}$	$I/O_{0-15R}$	Data Inputs/ Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INTF}_L$	$\overline{INTF}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
VCC		Power
GND		Ground

Table 1. Pin Descriptions

Symbol	Rating	Com & Ind	Unit
$V_{TERM}$	Terminal Voltage with respect to GND	-0.5 to +4.6	V
$T_{BIAS}$	Temperature Under Bias	-55 to +125	°C
$T_{STG}$	Storage Temperature	-65 to +150	°C
$I_{OUT}$	DC Output Current	-50 to +50	mA

**NOTES:**

1. Absolute Max Ratings are for reference only. Permanent damage to the device may occur if extended period of operation is outside this range. Standard operation should fall within the Recommended Operating Conditions.
2.  $V_{TERM}$  must not exceed  $V_{CC}+0.3V$  for more than 25% of the cycle time or 10ns maximum, and is limited to  $<+ 20Ma$  for the period over  $V_{TERM}=V_{DD}+0.3V$ .

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
<b>Recommended Operating Conditions</b>					
VCC	Supply Voltage	2.6	2.8	3.0	V
GND	Ground Voltage	0	0	0	V
$V_{IH}$	Input High Voltage	2.0	-	$V_{CC}+0.3$	V
$V_{IL}$	Input Low Voltage	-0.3	-	0.8	V
$T_A^{(1)}$	Operating Temperature Industrial	-40	-	85	°C
<b>DC Electrical Characteristics</b>					
$I_{LI}^{(1)}$	Input Leakage Current ( $V_{CC}=2.8V, V_{IN}=0V$ to $V_{CC}$ )	-	-	10	$\mu A$
$I_{LO}$	Output Leakage Current ( $\overline{CE}=V_{IH}, V_{OUT}=0V$ to $V_{CC}$ )	-	-	10	$\mu A$
$V_{OH}$	Output Logic "1" Voltage, $I_{OH}=-4mA$	2.0	-	-	V
$V_{OL}$	Output Logic "0" Voltage, $I_{OL}=4mA$	-	-	0.4	V
<b>Capacitance at 1.0MHz Ambient Temperature (25° C)</b>					
Symbol	Parameter	Conditions	Max.	Unit	
$C_{IN}^{(2)}$	Input Capacitance	$V_{IN}=3dV$	9	pF	
$C_{OUT}^{(2)}$	Output Capacitance	$V_{OUT}=3dV$	10	pF	

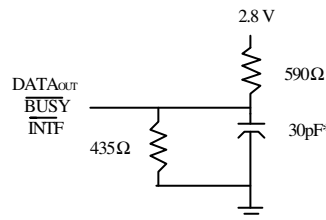
**NOTES:**

1.  $T_A$  is the "instant on" case temperature.
2.  $C_{IN}$  and  $C_{OUT}$  are determined by device characterization, not production tested.

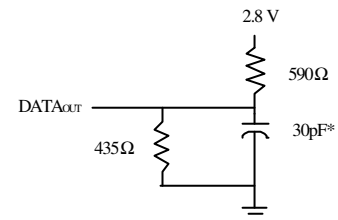
Table 3. Operating conditions

Power Consumption (Continued)						
Symbol	Parameter	Conditions	Version	HDV24VL55		Unit
				Typ.	Max.	
I <sub>CC</sub>	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ , Outputs Disabled, $\overline{SEM} = V_{IH}$ , $f=f_{MAX}$	Industrial VL	20	25	mA
I <sub>SB1</sub>	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CEL} = \overline{CER} = V_{IH}$ , $\overline{SEMR} = \overline{SEML} = V_{IH}$ , $f=f_{MAX}$	Industrial VL	5	10	mA
I <sub>SB2</sub>	Standby Current (One Port – TTL Level Inputs)	$\overline{CEA} = V_{IL}$ and $\overline{CEB} = V_{IH}$ Active Port Outputs Disabled, $f=f_{MAX}$ , $\overline{SEMR} = \overline{SEML} = V_{IH}$	Industrial VL	15	20	mA
I <sub>SB3</sub>	Full Standby Current (Both Ports – All CMOS Level Inputs)	Both Ports $\overline{CEL}$ and $\overline{CER} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $\overline{SEMR} = \overline{SEML} \geq V_{CC} - 0.2V$	Industrial VL	0.2	0.3	mA
I <sub>SB4</sub>	Standby Current (One Port – All CMOS Level Inputs)	$\overline{CEA} \leq 0.2V$ and $\overline{CEB} > V_{CC} - 0.2V$ , $\overline{SEMR} = \overline{SEML} \geq V_{CC} - 0.2V$ , Active Port Outputs Disabled, $f=f_{MAX}$	Industrial VL	12	15	mA

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load, clock = 15 ns	Refer to Figure 4
Output Load <sup>(1)</sup> , clock = 15ns, 20ns, 25ns, 30ns	Refer to Figure 5



**Figure 4. AC Test Load**  
(for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{VZ}$ ,  $t_{OW}$ )



**Figure 5. Output Load**  
(for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{VZ}$ ,  $t_{OW}$ )  
\*Includes jig and scope capacitances.

**NOTES:**

1. Include jig and scope capacitances

**Table 4. AC Test Conditions**

70V24VL55I				
Symbol	Parameter	Min.	Max.	Unit
<b>Read Cycle</b>				
t <sub>RC</sub>	Read Cycle Time	55	-	MHz
t <sub>AA</sub>	Address Access Time	-	55	ns
t <sub>ACE</sub>	Chip Enable Access Time	-	55	ns
t <sub>ABE</sub>	Byte Enable Access Time	-	55	ns
t <sub>AOE</sub>	Output Enable Access Time	-	30	ns
t <sub>OH</sub>	Output Hold from Address Change	3	-	ns
t <sub>LZ</sub>	Output Low-Z Time	3	-	ns
t <sub>HZ</sub>	Output High-Z Time	-	25	ns
t <sub>PU</sub>	Chip Enable to Power Up Time	0	-	ns
t <sub>PD</sub>	Chip Disable to Power Down Time	-	50	ns
t <sub>SOP</sub>	Semaphore Flag Update Pulse	15	-	ns
t <sub>SAA</sub>	Semaphore Address Access Time	-	55	ns
<b>Write Cycle</b>				
t <sub>WC</sub>	Write Cycle Time	55	-	ns
t <sub>EW</sub>	Chip Enable to End-of-Write	45	-	ns
t <sub>AW</sub>	Address Valid to End-of-Write	45	-	ns
t <sub>AS</sub>	Address Set-up Time	0	-	ns
t <sub>WP</sub>	Write Pulse Width	40	-	ns
t <sub>WR</sub>	Write Recovery Time	0	-	ns
t <sub>DW</sub>	Data Valid to End-of-Write	30	-	ns
t <sub>HZ</sub>	Output High-Z Time	-	25	ns
t <sub>DH</sub>	Data Hold Time	0	-	ns
t <sub>WZ</sub>	Write Enable to Output in High-Z	-	25	ns
t <sub>OW</sub>	Output Active from End-of-Write	0	-	ns
t <sub>SWRD</sub>	$\overline{\text{SEM}}$ Flag Write to Read Time	5	-	ns
t <sub>SPS</sub>	SEM Flag Contention Window	5	-	ns
<b>Interrupt Timing</b>				
t <sub>AS</sub>	Address Set-up Time	0	-	ns
t <sub>WR</sub>	Write Recover Time	0	-	
t <sub>INS</sub>	Interrupt Set Time	-	40	ns
t <sub>INR</sub>	Interrupt Reset Time	-	40	ns

Table 5. AC Electrical Characteristics

Symbol	Parameter	Min	Max.	Unit
<b>BUSY Timing (MASTER)</b>				
t <sub>BAA</sub>	$\overline{\text{BUSY}}$ Access Time form Address Match	-	45	MHz
t <sub>BDA</sub>	$\overline{\text{BUSY}}$ Disable Time from Address Not Matched	-	40	ns
t <sub>BAC</sub>	$\overline{\text{BUSY}}$ Access Time from Chip Enable Low	-	40	ns
t <sub>BDC</sub>	$\overline{\text{BUSY}}$ Access Time from Chip Enable High	-	35	ns
t <sub>APS</sub>	Arbitration Priority Set-up Time	5	-	ns
t <sub>BDD</sub>	$\overline{\text{BUSY}}$ Disable to Valid Data	-	40	ns
t <sub>WH</sub>	Write Hold after $\overline{\text{BUSY}}$	25	-	ns
<b>BUSY Timing (SLAVE)</b>				
t <sub>WB</sub>	$\overline{\text{BUSY}}$ Input to Write	0	-	ns
t <sub>WH</sub>	Write Hold after $\overline{\text{BUSY}}$	25	-	ns
<b>Port-to-Port Delay Timing</b>				
t <sub>WDD</sub>	Write Cycle Time	-	80	ns
t <sub>DOD</sub>	Chip Enable to End-of-Write	-	65	ns

Table 4. AC Electrical Characteristics (Continued)