

### 3.3 Volt Synchronous x9 First-In/First-Out Queue

Memory Configuration	Device	Memory Configuration	Device
8,192 x 9	FQV251	512 x 9	FQV211
4,096 x 9	FQV241	256 x 9	FQV201
2,048 x 9	FQV231	128 x 9	FQV621
1,024 x 9	FQV221	64 x 9	FQV421

#### Key Features:

- Industry leading First-In/First-Out Queues (up to 100MHz)
- Independent Write and Read cycle time
- 3.3V power supply
- 5V input tolerant on all control and data input pins
- 5V output tolerant on all flags and data output pins
- Full, Empty, Almost Full, and Almost Empty flag indicators
- Preset for Almost Full ( PRAF ) and Almost Empty ( PRAE ) offset values
- Programmable PRAF and PRAE offset values
- Asynchronous output enable tri-state data output drivers
- Available packages: 32 - pin Plastic Lead Chip Carrier (PLCC), 32 - pin Plastic Thin Quad Flat Package (TQFP)
- (0°C to 70°C) Commercial operating temperature available for cycle time of 10ns and above
- (-40°C to 85°C) Industrial operating temperature available for cycle time of 10ns and above

#### Product Description:

HBA's FlexQ™ I offers industry leading FIFO queuing bandwidth (up to 1 Gbps) with a wide range of memory configurations (from 64 x 9 to 8,192 x 9). System designer has full flexibility of implementing deeper and wider queues using the depth and width expansion features. Full and Empty indicators allow easy handshaking between transmitters and receivers. User programmable Almost Full and Almost Empty (Parallel) indicators allow implementation of virtual queue depths.

5V tolerant on all input and output pins allow easy interfacing with devices operating at higher voltage levels. Asynchronous Output Enable pin configures the tri-state data output drivers. Independent Write and Read controls provide rate-matching capability.

These FlexQ™ I devices have low power consumption, hence minimizing system power requirements. In addition, industry standard 32 - pin PLCC and 32 - pin TQFP are offered to save system board space.

These queues are ideal for applications such as data communication, telecommunication, graphics, multiprocessing, test equipment, network switching, etc.

**Block Diagram of Single Synchronous Queue**  
8,192 x 9 / 4,096 x 9 / 2,048 x 9 / 1,024 x 9 / 512 x 9 / 256 x 9 / 128 x 9 / 64 x 9

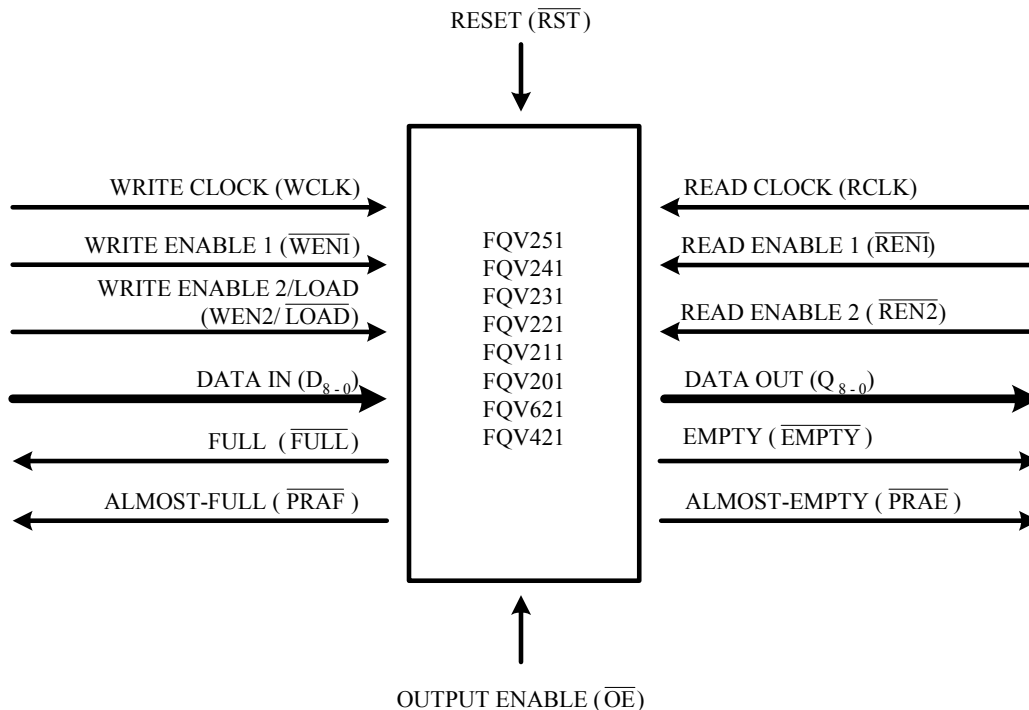


Figure 1. Single Device Configuration Signal Flow Diagram

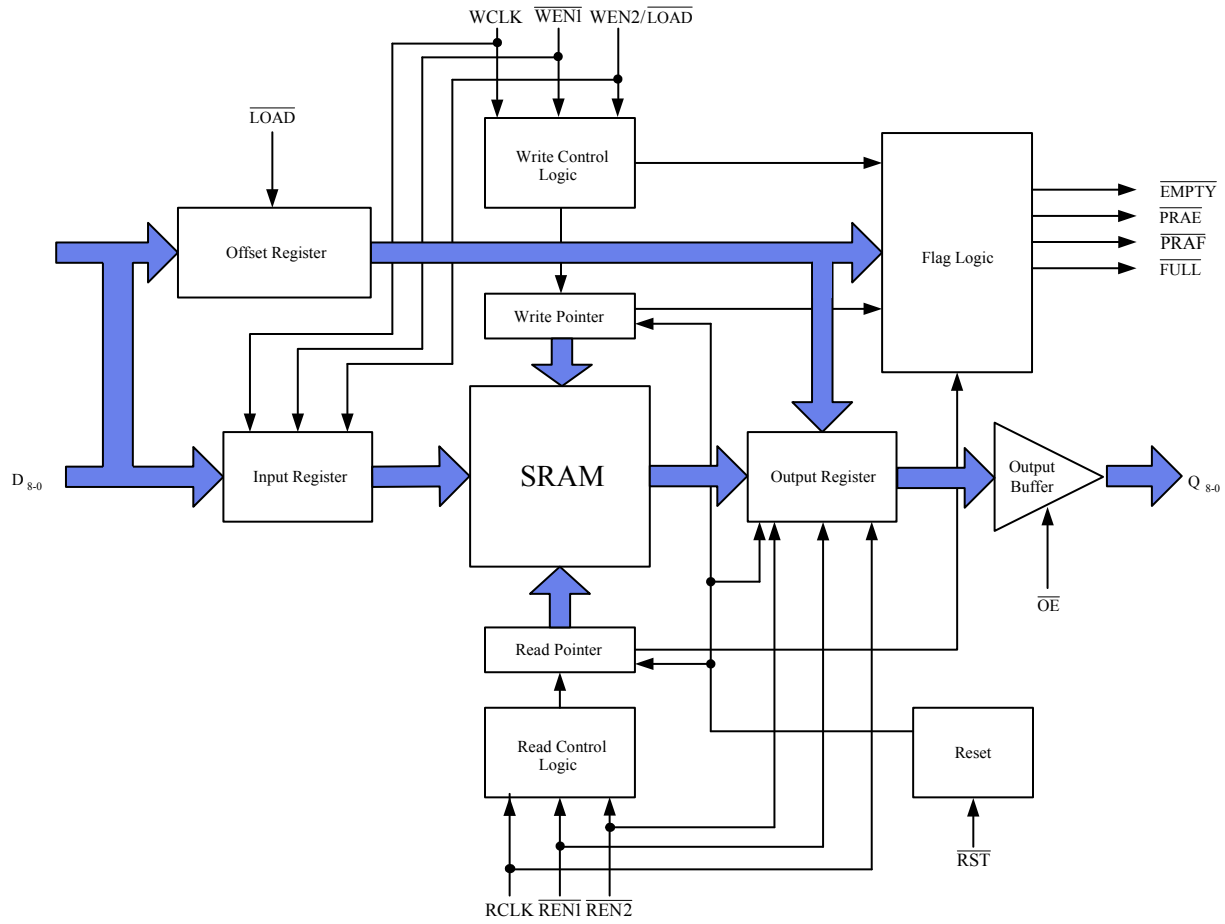
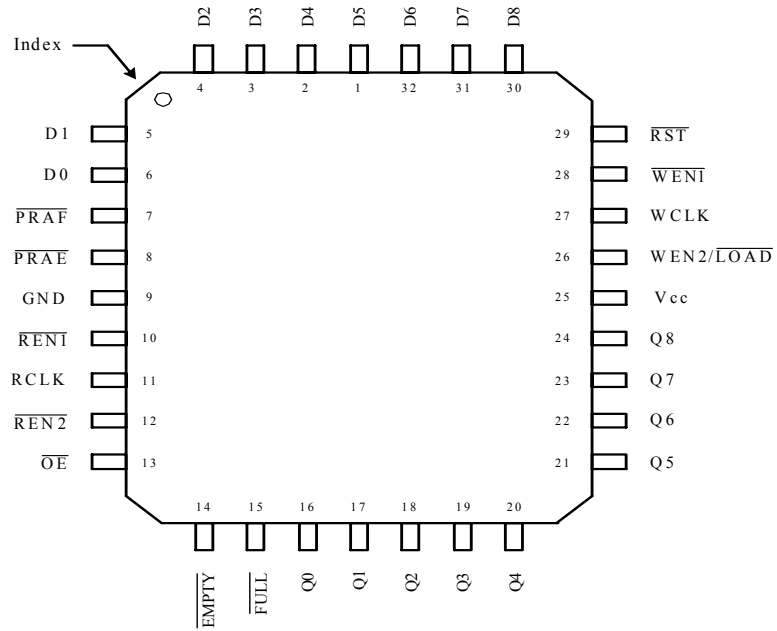
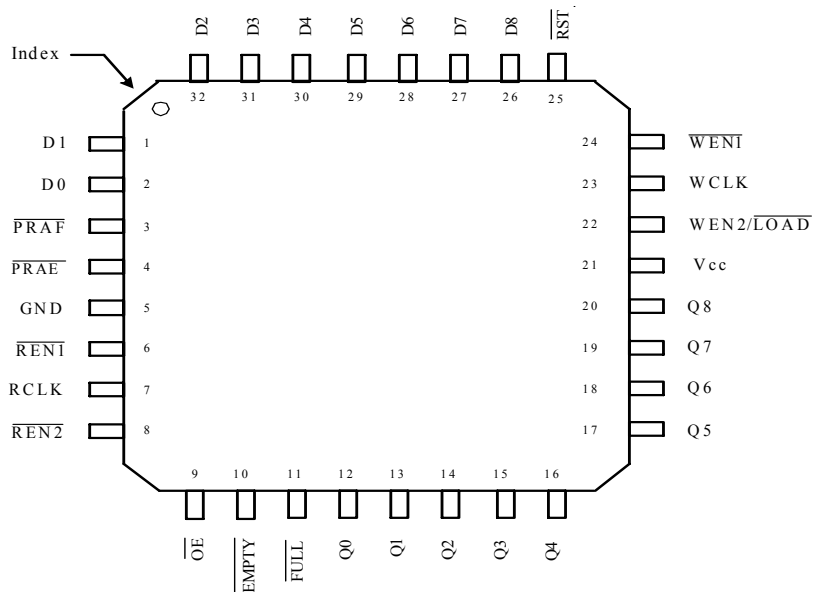


Figure 2. Device Architecture



PLCC - 32 (Drw No: J-01A;  
Order code: J)  
Top View



TQFP - 32 (Drw No: PF-04A;  
Order code: PF)  
Top View

Figure 3. Device Pin-Out



Pin # TQFP	Pin # PLCC	Symbol	Name	Input/Output	Description
25	29	$\overline{\text{RST}}$	Reset	Input	Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{RST}}$ low. $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low.
23	27	WCLK	Write Clock	Input	Writes data into queue during low to high transitions of WCLK if $\overline{\text{WEN1}}$ is activated.
24	28	$\overline{\text{WEN1}}$	Write Enable	Input	Use as first or as only write enable control for the queue depending on the state of $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ during reset.
22	26	$\overline{\text{WEN2}}/\overline{\text{LOAD}}$	Write Enable 2 / Load	Input	During reset, setting $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ high places the queue into the dual write enable mode. $\overline{\text{WEN1}}$ must be set low and $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ must be set high to perform a valid write in this mode. During reset, setting $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ low places the queue into the single write enable/programmable flag mode. $\overline{\text{WEN1}}$ must be set low and $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ must be set high to perform a valid write in this mode. In this mode, $\overline{\text{WEN1}}$ and $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ must be set low to program the offset values for $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ .
26,27,28, 29,30,31 32,01,02	30,31,32, 01,02,03, 04,05,06	D <sub>8-0</sub>	Data Inputs	Input	9 - bit wide input data bus.
7	11	RCLK	Read Clock	Input	Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are set to low.
6	10	$\overline{\text{REN1}}$	Read Enable 1	Input	Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are both set to low.
8	12	$\overline{\text{REN2}}$	Read Enable 2	Input	Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are both set to low.
9	13	$\overline{\text{OE}}$	Output Enable	Input	Setting $\overline{\text{OE}}$ low activates the data output drivers. Setting $\overline{\text{OE}}$ high deactivates the data output drivers (High-Z).
20,19,18 17,16,15, 14,13,12	24,23,22, 21,20,19, 18,17,16	Q <sub>8-0</sub>	Data Output	Output	9 - bit wide output data bus.
11	15	$\overline{\text{FULL}}$	Full Flag	Output	Queue is full when $\overline{\text{FULL}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue.
10	14	$\overline{\text{EMPTY}}$	Empty Flag	Output	Queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue.
3	7	$\overline{\text{PRAF}}$	Programmable Almost-Full Flag	Output	Queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-7) or programmed offset values determine the status of $\overline{\text{PRAF}}$ .
4	8	$\overline{\text{PRAE}}$	Programmable Almost-Empty Flag	Output	Queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty+7) or programmed offset values determine the status of $\overline{\text{PRAE}}$ .
21	25	Vcc	Power	N/A	5V power supply.
5	9	GND	Ground	N/A	0V Ground.

Table 1. Pin Descriptions



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Symbol	Rating	Com'l & Ind'l	Unit
V <sub>TERM</sub>	Terminal Voltage with respect to GND	-0.5 to +5.0	V
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA

**NOTES:**

Absolute Max Ratings are for reference only. Permanent damage to the device may occur if extended period of operation is outside this range. Standard operation should fall within the Recommended Operating Conditions.

Table 2. Absolute Maximum Ratings

		FQV251, FQV241 FQV231, FQV221 FQV211, FQV201 FQV621, FQV421						Unit
		Commercial Clock = 10ns, 15ns, 20ns			Industrial Clock = 10ns, 15ns, 20ns			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
<b>Recommended Operating Conditions</b>								
V <sub>CC</sub>	Supply Voltage Com'l/Ind'l	3.0	3.3	3.6	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	0	0	0	V
V <sub>IH</sub>	Input High Voltage Com'l/Ind'l	2.0	-	5.5	2.0	-	5.5	V
V <sub>IL</sub>	Input Low Voltage Com'l/Ind'l	-	-	0.8	-	-	0.8	V
T <sub>A</sub>	Operating Temperature Commercial	0	-	70	0	-	70	°C
T <sub>A</sub>	Operating Temperature Industrial	-40	-	85	-40	-	85	°C
<b>DC Electrical Characteristics</b>								
I <sub>LI</sub> <sup>(1)</sup>	Input Leakage Current (any input)	-10	-	10	-10	-	10	μA
I <sub>LO</sub>	Output Leakage Current	-10	-	10	-10	-	10	μA
V <sub>OH</sub>	Output Logic "1" Voltage, IOH=-2mA	2.4	-	-	2.4	-	-	V
V <sub>OL</sub>	Output Logic "0" Voltage, IOL = 8mA	-	-	0.4	-	-	0.4	V
<b>Power Consumption</b>								
I <sub>CC1</sub> <sup>(2,3)</sup>	Active Power Supply Current	-	-	20	-	-	20	mA
I <sub>CC2</sub> <sup>(2,3)</sup>	Standby Current	-	-	5	-	-	5	mA

Table 3. DC Specifications



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Capacitance at 1.0 MHz Ambient Temperature (25°C)				
Symbol	Parameter	Conditions	Max.	Unit
$C_{IN}^{(4)}$	Input Capacitance	$V_{IN} = 0V$	10	pF
$C_{OUT}^{(2,4)}$	Output Capacitance	$V_{OUT} = 0V$	10	pF

**NOTES:**

1. Measurement with  $0.4 \leq V_{IN} \leq V_{cc}$
2. With output tri-stated ( $\overline{OE} = \text{High}$ )
3.  $I_{cc(1,2)}$  is measured with WCLK and RCLK at 20 MHz
4. Design simulated, not tested.

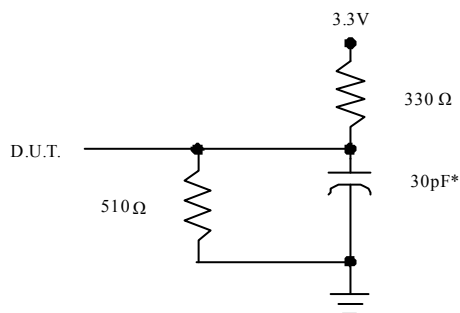
**Table 3. DC Specifications (Continued)**



Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load*, clock = 10ns, 15ns, 20ns	Refer to Figure 4

\* Include jig and scope capacitances

**Table 5. AC Test Condition**



**Figure 4. Output Load**  
for clock = 10ns, 15ns, 20ns  
\*Includes jig and scope capacitances.

## Pin Functions

<b><math>\overline{\text{RST}}</math></b>	Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{RST}}$ low. $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. All data outputs will be set low. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ offset will be set to their default values (Full-7 and Empty+7 respectively).
<b>WCLK</b>	Writes data into queue during low to high transitions of WCLK if $\overline{\text{WEN1}}$ is activated. Synchronizes $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ flags. WCLK and RCLK are independent of each other.
<b><math>\overline{\text{WEN1}}</math></b>	Use as single or as dual write enable control for the queue depending on the state of $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ during reset.  To perform a write operation in single write enable mode: Set $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ low during reset. Set $\overline{\text{WEN1}}$ low, and $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ high during low to high transition of WCLK.  To perform an offset programming operation in single write enable mode: Set $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ low during reset. Set $\overline{\text{WEN1}}$ low, and $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ low during low to high transition of WCLK.  To perform a write operation in dual write enable mode: Set $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ high during reset. Set $\overline{\text{WEN1}}$ low, and $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ high during low to high transition of WCLK.
<b><math>\overline{\text{WEN2}}/\overline{\text{LOAD}}</math></b>	During reset, setting $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ low puts the queue into single write enable/offset programming mode. Setting $\overline{\text{WEN2}}/\overline{\text{LOAD}}$ high places the queue into dual write enable mode.
<b>D<sub>8-0</sub></b>	9 - bit wide input data bus
<b>RCLK</b>	Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are activated. Synchronizes $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ flags. RCLK and WCLK are independent of each other.
<b><math>\overline{\text{REN1}}</math></b>	Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are both set to low. This also advances the Read pointer of the queue.
<b><math>\overline{\text{REN2}}</math></b>	Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are both set to low. This also advances the Read pointer of the queue.
<b><math>\overline{\text{OE}}</math></b>	Setting $\overline{\text{OE}}$ low activates the data output drivers. Setting $\overline{\text{OE}}$ high deactivates the data output drivers (High-Z). $\overline{\text{OE}}$ does not control advancement of Read pointer.
<b>Q<sub>8-0</sub></b>	9 - bit wide output data bus.
<b><math>\overline{\text{FULL}}</math></b>	Queue is full when $\overline{\text{FULL}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. Refer to Table 9 for behavior of $\overline{\text{FULL}}$ .
<b><math>\overline{\text{EMPTY}}</math></b>	Queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. Refer to Table 9 for behavior of $\overline{\text{EMPTY}}$ .



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**Pin Functions (Continued)**

$\overline{\text{PRAF}}$	Queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-7) or programmed offset values determine the status of $\overline{\text{PRAF}}$ . Refer to Table 9 for behavior of $\overline{\text{PRAF}}$ .
$\overline{\text{PRAE}}$	Queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty+7) or programmed offset values determine the status of $\overline{\text{PRAE}}$ . Refer to Table 9 for behavior of $\overline{\text{PRAE}}$ .

WEN2/ $\overline{\text{LOAD}}$	$\overline{\text{WEN1}}$	WCLK	FQV251 FQV241 FQV231 FQV221 FQV211 FQV201 FQV621 FQV421 Selection / Sequence
0	0		Write to offset registers: Empty offset (Low Byte)      1. $\overline{\text{PRAE}}$ Low Byte Empty offset (High Byte)     2. $\overline{\text{PRAE}}$ High Byte Full offset (Low Byte)         3. $\overline{\text{PRAF}}$ Low Byte Full offset (High Byte)         4. $\overline{\text{PRAF}}$ High Byte
0	1		No Operation
1	0		Write Memory
1	1		No Operation

Figure 5. Write Offset Register







<b>WEN2/LOAD</b>	<b>REN1 &amp; REN2</b>	<b>RCLK</b>	<b>FQV251</b> <b>FQV241</b> <b>FQV231</b> <b>FQV221</b> <b>FQV211</b> <b>FQV201</b> <b>FQV621</b> <b>FQV421</b> <b>Selection / Sequence</b>
0	0		Read from offset registers: Empty offset (Low Byte)  1. $\overline{\text{PRAE}}$ Low Byte Empty offset (High Byte)      2. $\overline{\text{PRAE}}$ High Byte Full offset (Low Byte)      3. $\overline{\text{PRAF}}$ Low Byte Full offset (High Byte)      4. $\overline{\text{PRAF}}$ High Byte 
0	1		No Operation
1	0		Read Memory
1	1		No Operation

Figure 6. Read Offset Register

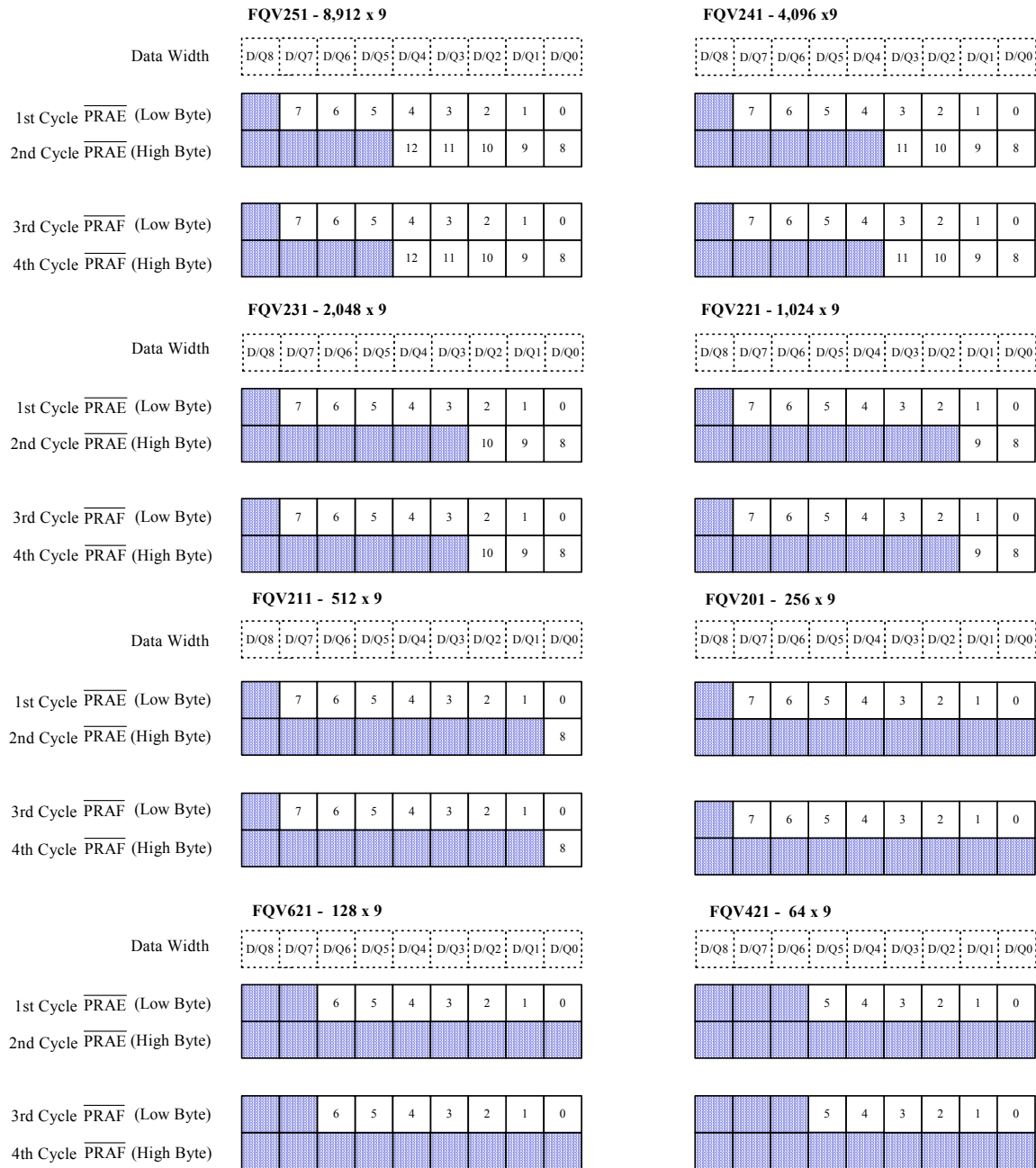


Device	PRAE Programming (bits)		PRAF Programming (bits)	
FQV251	D/Q <sub>7-0</sub> D/Q <sub>4-0</sub>	Low Byte High Byte	D/Q <sub>7-0</sub> D/Q <sub>4-0</sub>	Low Byte High Byte
FQV241	D/Q <sub>7-0</sub> D/Q <sub>3-0</sub>	Low Byte High Byte	D/Q <sub>7-0</sub> D/Q <sub>3-0</sub>	Low Byte High Byte
FQV231	D/Q <sub>7-0</sub> D/Q <sub>2-0</sub>	Low Byte High Byte	D/Q <sub>7-0</sub> D/Q <sub>2-0</sub>	Low Byte High Byte
FQV221	D/Q <sub>7-0</sub> D/Q <sub>1-0</sub>	Low Byte High Byte	D/Q <sub>7-0</sub> D/Q <sub>1-0</sub>	Low Byte High Byte
FQV211	D/Q <sub>7-0</sub> D/Q <sub>0</sub>	Low Byte High Byte	D/Q <sub>7-0</sub> D/Q <sub>0</sub>	Low Byte High Byte
FQV201	D/Q <sub>7-0</sub> Don't Care	Low Byte High Byte	D/Q <sub>7-0</sub> Don't Care	Low Byte High Byte
FQV621	D/Q <sub>6-0</sub> Don't Care	Low Byte High Byte	D/Q <sub>6-0</sub> Don't Care	Low Byte High Byte
FQV421	D/Q <sub>5-0</sub> Don't Care	Low Byte High Byte	D/Q <sub>5-0</sub> Don't Care	Low Byte High Byte
ALL	Default Value 007H		Default Value 007H	

Table 7. Parallel Offset Register Data Mapping Table and Default Values

Device	Standard Mode
FQV251	8,192 x 9
FQV241	4,096 x 9
FQV231	2,048 x 9
FQV221	1,024 x 9
FQV211	512 x 9
FQV201	256 x 9
FQV621	128 x 9
FQV421	64 x 9

Table 8. Maximum Depth of Queue



# of Bits for Offset Registers
13 bits for FQV251
12 bits for FQV241
11 bits for FQV231
10 bits for FQV221
9 bits for FQV211
8 bits for FQV201
7 bits for FQV621
6 bits for FQV421

**Note: Don't Care applies to all unused bits for both High Byte and Low Byte**

Figure 7. Parallel Offset Write/Read Cycles Diagram



FQV251	FULL	PRAF	PRAE	EMPTY
0	H	H	L	L
1 to $y^{(1)}$	H	H	L	H
$(y+1)$ to $[8,192-(x+1)]$	H	H	H	H
$(8,192-x^{(2)})$ to 8,191	H	L	H	H
8,192	L	L	H	H

FQV241	FULL	PRAF	PRAE	EMPTY
0	H	H	L	L
1 to $y^{(1)}$	H	H	L	H
$(y+1)$ to $[4,096-(x+1)]$	H	H	H	H
$(4,096-x^{(2)})$ to 4,095	H	L	H	H
4,096	L	L	H	H

FQV231	FULL	PRAF	PRAE	EMPTY
0	H	H	L	L
1 to $y^{(1)}$	H	H	L	H
$(y+1)$ to $[2,048-(x+1)]$	H	H	H	H
$(2,048-x^{(2)})$ to 2,047	H	L	H	H
2,048	L	L	H	H

FQV221	FULL	PRAF	PRAE	EMPTY
0	H	H	L	L
1 to $y^{(1)}$	H	H	L	H
$(y+1)$ to $[1,024-(x+1)]$	H	H	H	H
$(1,024-x^{(2)})$ to 1,023	H	L	H	H
1,024	L	L	H	H

FQV211	FULL	PRAF	PRAE	EMPTY
0	H	H	L	L
1 to $y^{(1)}$	H	H	L	H
$(y+1)$ to $[512-(x+1)]$	H	H	H	H
$(512-x^{(2)})$ to 511	H	L	H	H
512	L	L	H	H

Table 9. Status Flags

FQV201	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	L	L
1 to $y^{(1)}$	H	H	L	H
$(y+1)$ to $[256-(x+1)]$	H	H	H	H
$(256-x^{(2)})$ to 255	H	L	H	H
256	L	L	H	H

FQV621	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	L	L
1 to $y^{(1)}$	H	H	L	H
$(y+1)$ to $[128-(x+1)]$	H	H	H	H
$(128-x^{(2)})$ to 127	H	L	H	H
128	L	L	H	H

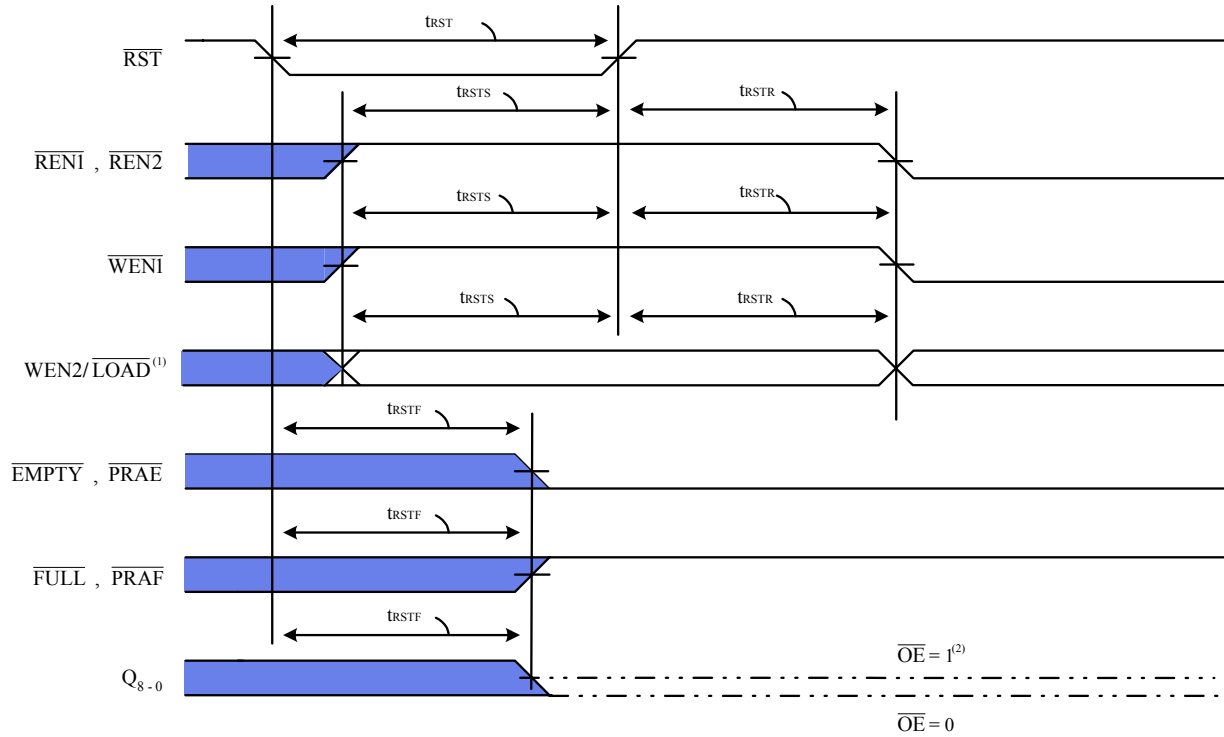
FQV421	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	L	L
1 to $y^{(1)}$	H	H	L	H
$(y+1)$ to $[64-(x+1)]$	H	H	H	H
$(64-x^{(2)})$ to 63	H	L	H	H
64	L	L	H	H

**NOTES:**

1.  $y = \overline{\text{PRAE}}$  offset ( $y = 7$  default value).
2.  $x = \overline{\text{PRAF}}$  offset ( $x = 7$  default value).

**Table 9. Status Flags (Continued)**

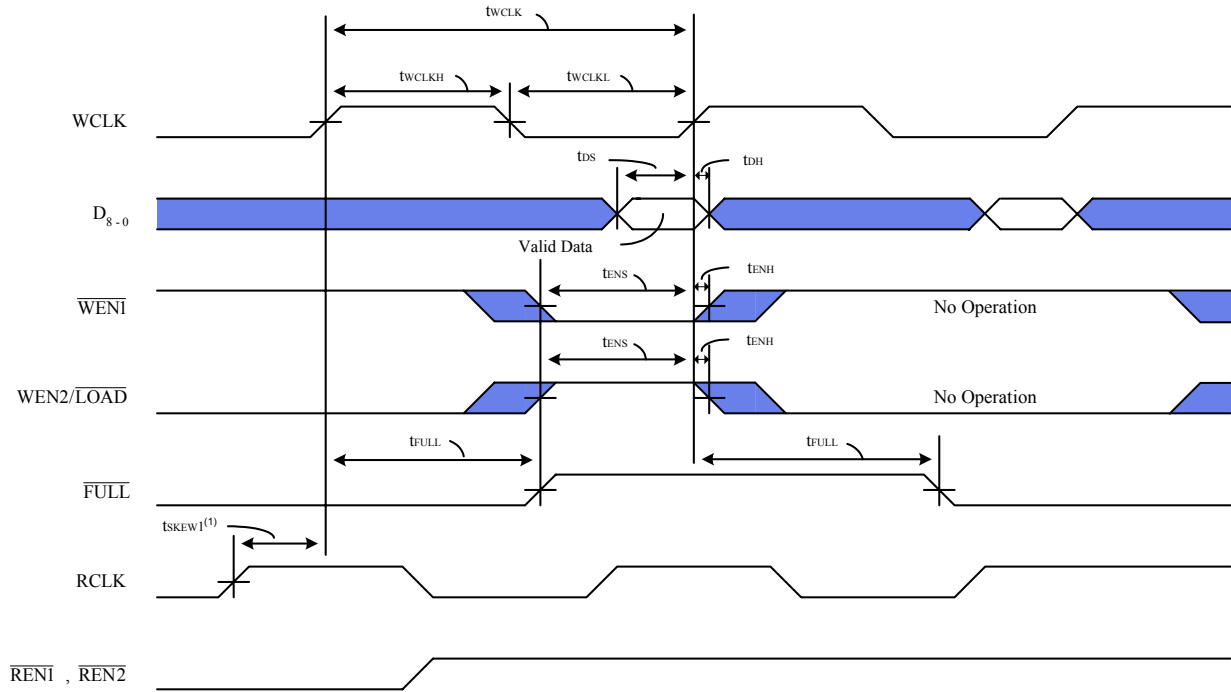
## Timing Diagrams



### NOTES:

1. Holding  $\overline{WEN2/LOAD}$  high during reset will make the pin act as a second Write Enable pin. Holding  $\overline{WEN2/LOAD}$  low during reset will make the pin act as a Load Enable for the programmable flag offset registers.
2. After reset, the outputs will be low if  $\overline{OE} = 0$  and high-impedance if  $\overline{OE} = 1$ .
3. The clocks (RCLK, WCLK) can be free-running during reset.

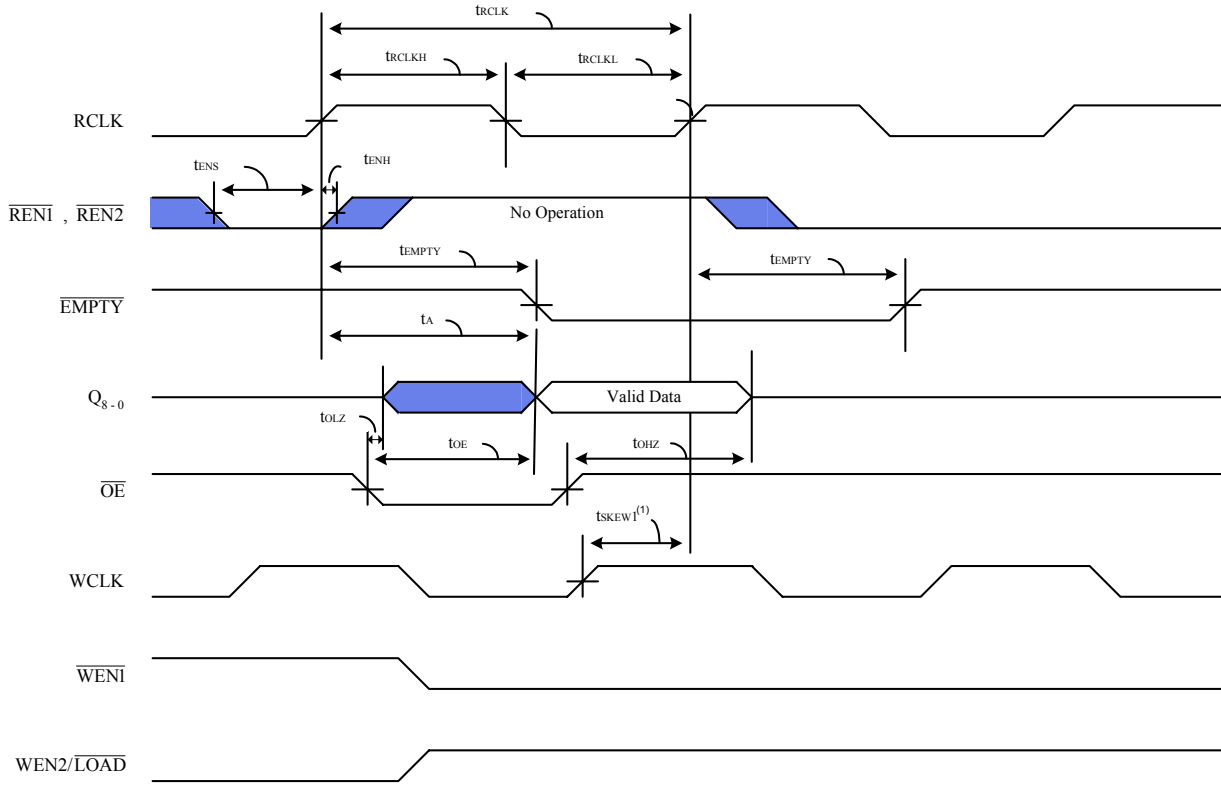
Diagram 1. Reset Timing



**NOTES:**

1.  $t_{sKEW1}$  is the minimum time between a rising RCLK edge and a rising WCLK edge for  $\overline{FULL}$  to change during the current clock cycle. If the time between the rising edge of RCLK and the rising WCLK is less than  $t_{sKEW1}$ , the  $\overline{FULL}$  may not change state until the next WCLK edge.

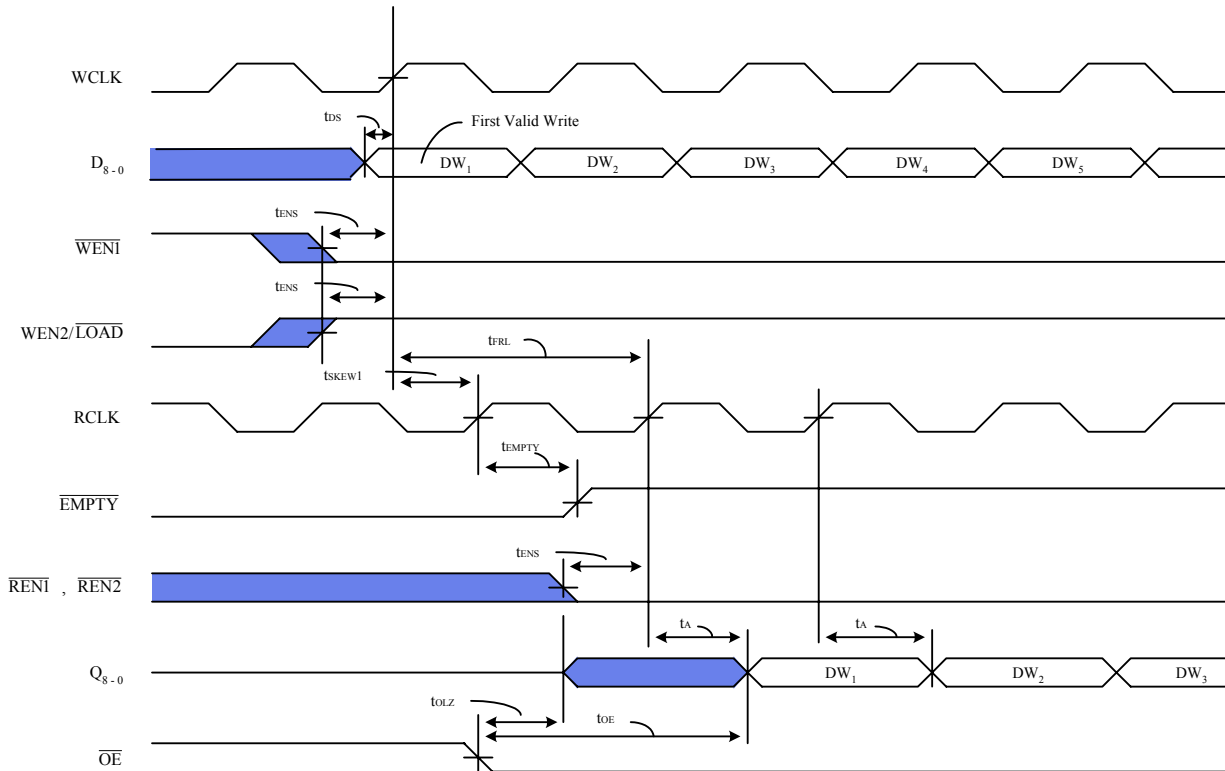
**Diagram 2. Write Cycle Timing**



**NOTES:**

1.  $t_{SKEW1}$  is the minimum time between a rising WCLK edge and a rising RCLK edge for  $\overline{EMPTY}$  to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than  $t_{SKEW1}$ , then  $\overline{EMPTY}$  may not change state until the next RCLK edge.

**Diagram 3. Read Cycle Timing**



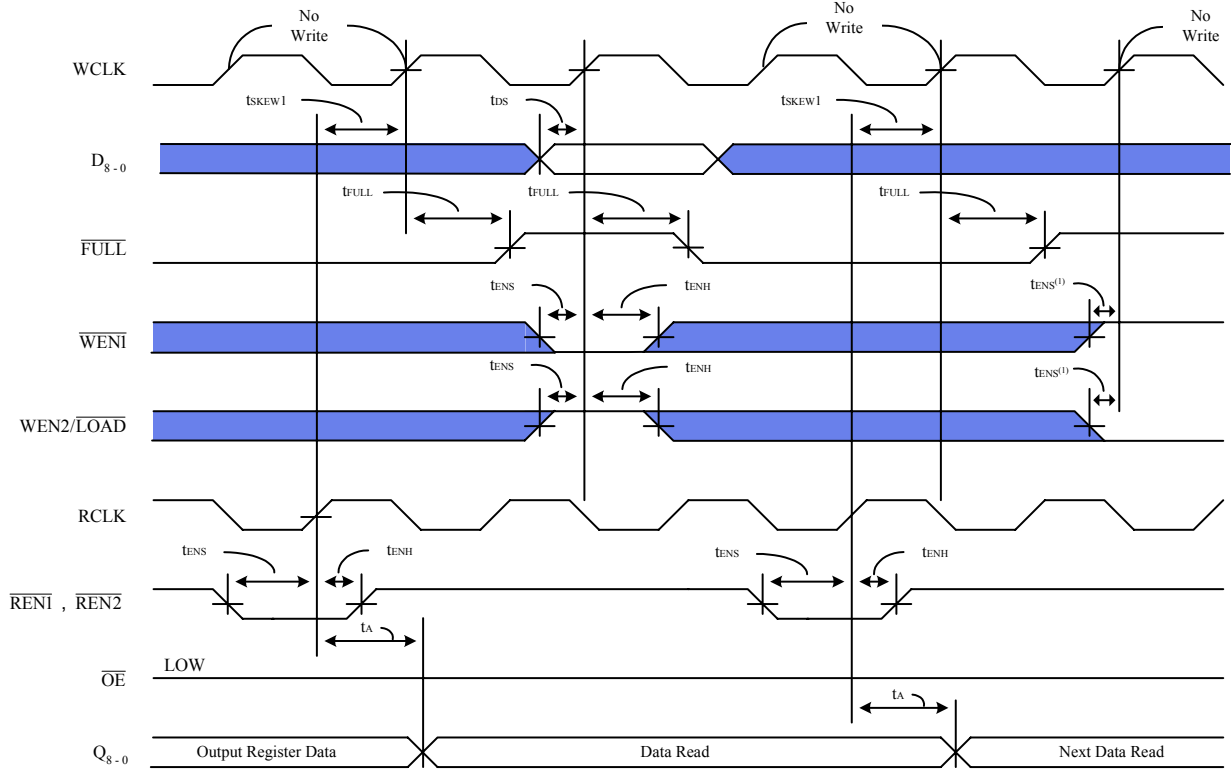
**NOTES:**

1.  $t_{FRL} = \text{First Read Latency}$ . When  $t_{SKEW1}$  is greater than or equal to the minimum specification,  $t_{FRL} = t_{RCLK} + t_{SKEW1}$ . When  $t_{SKEW1}$  is less than minimum specification,  $t_{FRL} = 2 * t_{RCLK} + t_{SKEW1}$  or  $t_{RCLK} + t_{SKEW1}$
2. The Latency Timings apply only at the Empty Boundary (EMPTY = Low).

**Diagram 4. First Data Word Latency Timing**

Speed Grade		First Word Latency
100 MHz	66MHz	tFRL
$t_{SKEW1} \geq 5$	$t_{SKEW1} \geq 6$	$t_{RCLK} + t_{SKEW1}$
$t_{SKEW1} < 5$	$t_{SKEW1} < 6$	$2 * t_{RCLK} + t_{SKEW1}$ OR $t_{RCLK} + t_{SKEW1}$

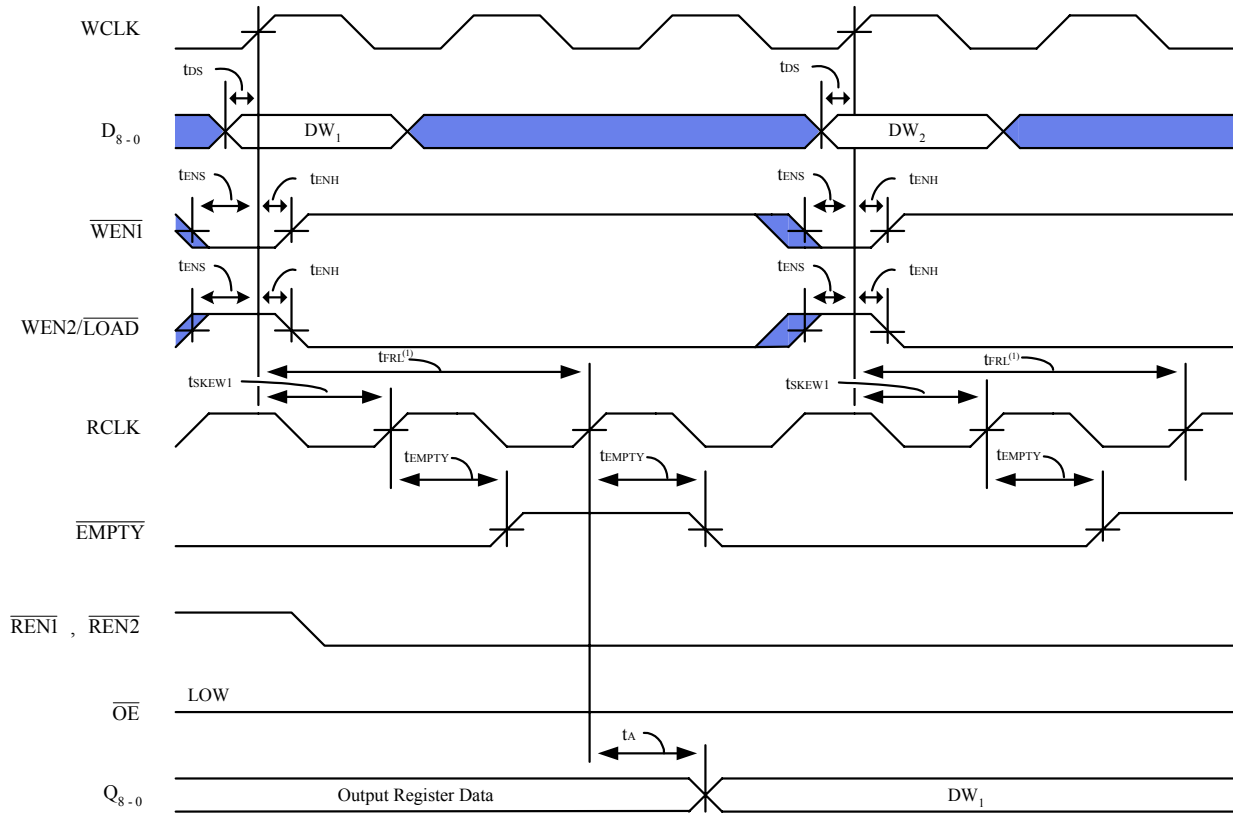
**Table 10. Empty Boundary Latency Timing**



**NOTES:**

1. Only one of the two Write Enable inputs,  $\overline{WEN1}$  or  $\overline{WEN2}$ , needs to go inactive to inhibit writes to the Queue.

**Diagram 5. Full Flag Timing**

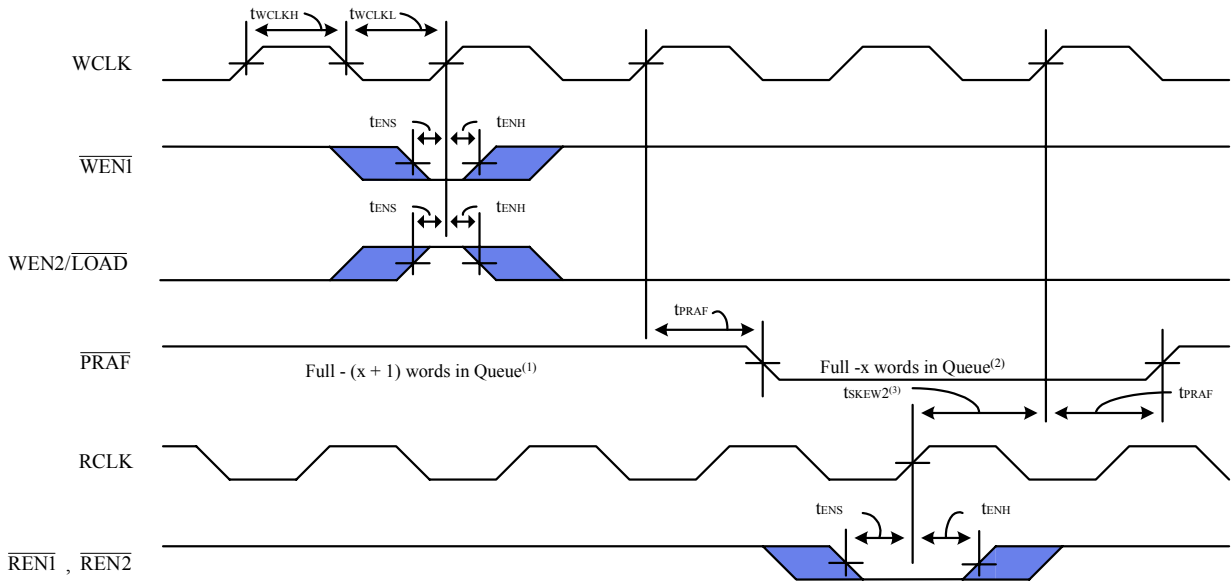


**NOTES:**

1. When  $t_{SKEW1}$  is greater than or equal to minimum specification,  $t_{FRL} = t_{RCLK} + t_{SKEW1}$ . When  $t_{SKEW1}$  is less than minimum specification,  $t_{FRL}$  maximum =  $2 * t_{RCLK} + t_{SKEW1}$  or  $t_{RCLK} + t_{SKEW1}$
2. The Latency Timings apply only at Empty Boundary (  $EMPTY = Low$  )

\* Refer to Table 10.

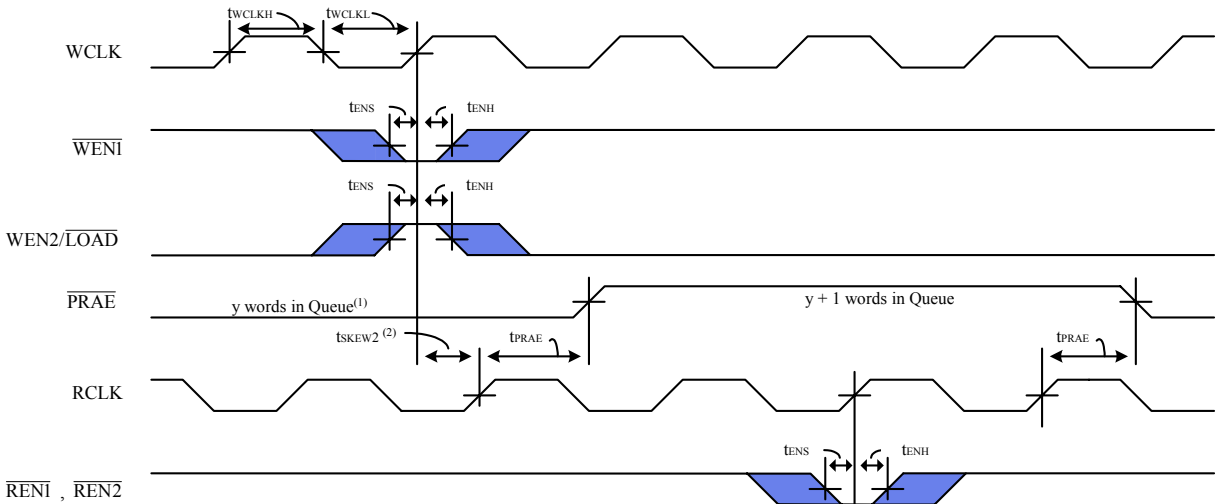
**Diagram 6. Empty Flag Timing**



**NOTES:**

1.  $x = \text{PRAF offset}$ .
2.  $64 - x$  words in queue for FQV421;  $128 - x$  words for queue for FQV621;  $256 - x$  words in queue for FQV201;  $512 - x$  words for FQV211;  $1,024 - x$  words for FQV221;  $2,048 - x$  words for FQV231;  $4,096 - x$  words for FQV241;  $8,192 - x$  words for FQV251.
3.  $\text{tsKEW2}$  is the minimum time between a rising RCLK edge and a rising WCLK edge for PRAF to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than  $\text{tsKEW2}$ , then PRAF may not change state until the next WCLK rising edge.

**Diagram 7. Programmable Full Flag Timing**



**NOTES:**

1.  $y = \text{PRAE offset}$
2.  $\text{tsKEW2}$  is the minimum time between a rising WCLK edge and a rising RCLK edge for PRAE to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than  $\text{tsKEW2}$ , then PRAE may not change state until the next RCLK rising edge.

**Diagram 8. Programmable Empty Flag Timing**

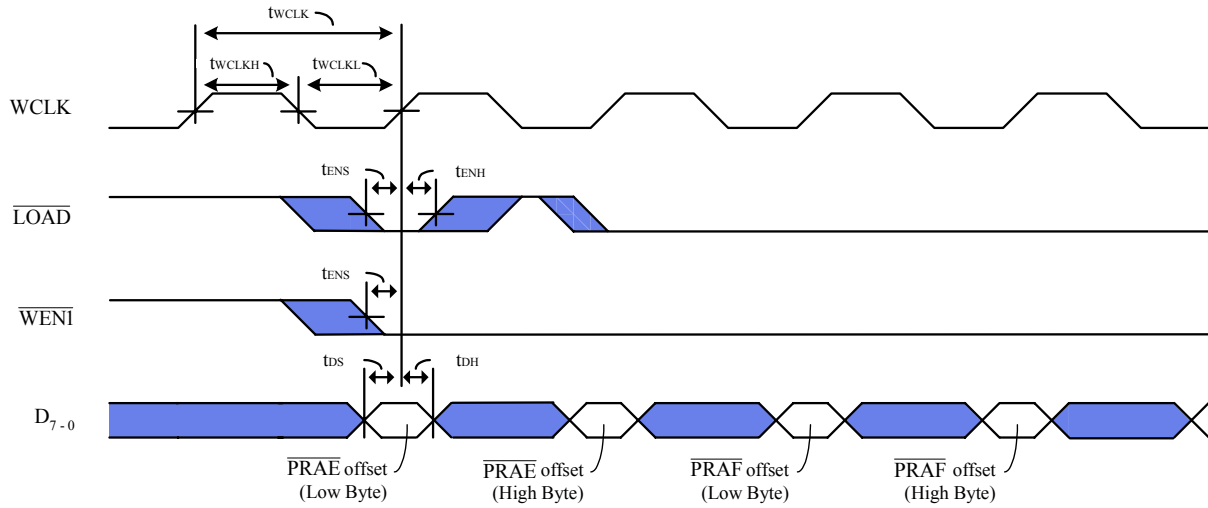


Diagram 9. Write Offset Registers Timing

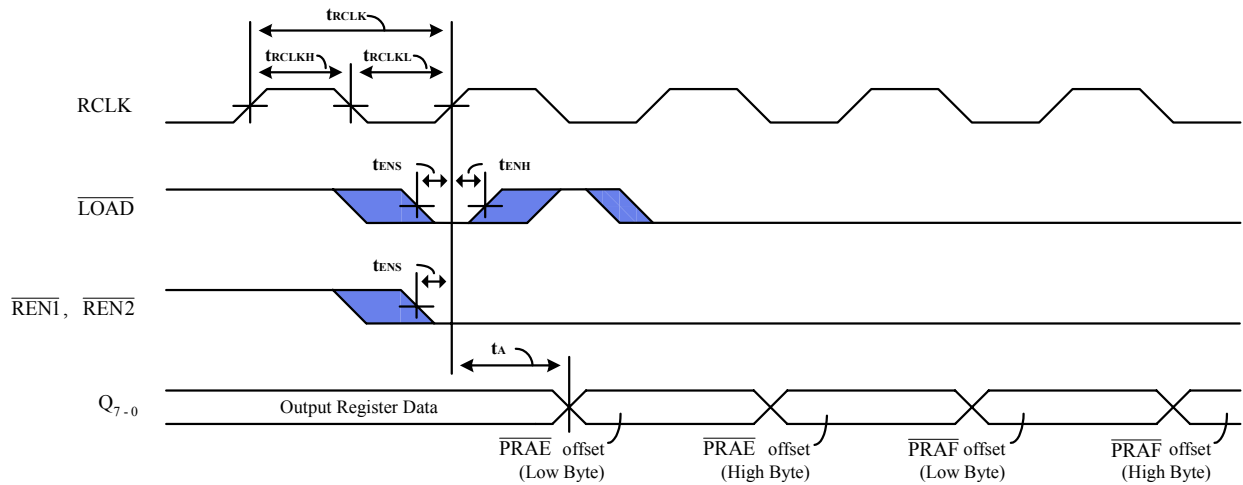


Diagram 10. Read Offset Registers Timing



Make Memory Smarter™

**Order Information:**

HBA Device Family	Device Type	Power	Speed (ns)*	Package**	Temperature Range
<u>XX</u>	<u>XXXX</u>	<u>X</u>	<u>XX</u>	<u>X</u>	<u>X</u>
FQ	V251 (8,192 x 9)	Low	10 – 100 MHz	J	Blank – Commercial (0°C to 70°C)
	V241 (4,096 x 9)		15 – 66 MHz	PF	I – Industrial (-40° to 85°C)
	V231 (2,048 x 9)		20 – 50 MHz		
	V221 (1,024 x 9)				
	V211 (512 x 9)				
	V201 (256 x 9)				
	V621 (128 x 9)				
	V421 (64 x 9)				

\*Speed – Slower speeds available upon request.

\*\*Package – 32 pin Plastic Lead Chip Carrier (PLCC), 32 pin Plastic Thin Quad Flat Pack (TQFP)

**Example:**

FQV241L10J (4k x 9, 10ns, Commercial temp)  
 FQV231L15JI (2k x 9, 15ns, Industrial temp)

**Document Revision History:**

02/07/03 pg. 1, 5, 6, 7, 8, 13, 14, 18, 19, 20, 21, 22, 23, 24, 25, 26

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