Document Title

3.3 Volt Synchronous x36 First-In / First-Out Queue

Revision History

Rev. No.	History	Issue Date	Remark
C	pg. 1,2, 6, 9, 10, 11, 12, 13, 14, 16, 27, 28, 30, 31, 39	January 10, 2002	
D	Add Pb-Free package type	December 20, 2006	

3.3 Volt Synchronous x36 First-In/First-Out Queue

Memory Organization	Device	Memory Organization	Device
131,072 x 36	FQV36110	8,192 x 36	FQV3670
65,536 x 36	FQV36100	4,096 x 36	FQV3660
32,768 x 36	FQV3690	2,048 x 36	FQV3650
16,384 x 36	FQV3680	1,024 x 36	FQV3640

Key Features

- **Industry leading First-In/First-Out Queues (up to 166MHz)**
- **Write cycle time of 6.0ns independent of Read cycle time (Data Setup time = 2.0ns)**
- **Read cycle time of 6.0ns independent of Write cycle time (Data Access time = 4.0ns)**
- **User selectable input and output ports bus-sizing**
- **Big Endian/Little Endian user selectable byte representation**
- **3.3V power supply**
- **5V input tolerant on all control and data input pins**
- **5V output tolerant on all flags and data output pins**
- **Master Reset clears all previously programmed configurations including Write and Read pointers**
- **Partial Reset clears Write and Read pointers but maintains all previously programmed configurations**
- **First Word Fall Through (FWFT) and Standard Timing modes**
- **Presets for eight different Almost Full and Almost Empty offset values**
- **Parallel/Serial programming of $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ offset values**
- **Programmable 8-bit or 9-bit parallel programming mode for offset values**
- **Full, Empty, Almost Full, Almost Empty, and Half Full indicators**
- **$\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ operate in either synchronous or asynchronous mode**
- **Asynchronous output enable tri-state data output drivers**
- **Data retransmission with programmable zero or normal latency mode**
- **Available package: 128 - pin Plastic Thin Quad Flat Pack (TQFP)**
- **(0°C to 70°C) Commercial operating temperature available for cycle time of 6.0ns and above**
- **(-40°C to 85°C) Industrial operating temperature available for cycle time of 7.5ns and above**

Product Description

AMIC's FlexQ™ III offers industry leading FIFO queuing bandwidth (up to 6.0 Gbps), with a wide range of memory configurations (from 1,024 x 36 to 131,072 x 36). System designer has full flexibility of implementing deeper and wider queues using FWFT mode and width expansion features. Full, Empty, and Half-Full indicators allow easy handshaking between transmitters and receivers. User programmable Almost Full and Almost Empty (Parallel/Serial) indicators allow implementation of virtual queue depths.

5V tolerant on all input and output pins allow easy interfacing with devices operating at higher voltage levels. Asynchronous Output Enable pin configures the tri-state data output drivers. Independent Write and Read controls provide rate-matching capability.

Master Reset clears all previously programmed configurations by providing a low pulse on $\overline{\text{MRST}}$ pin. In addition, Write and Read pointers to the queue are initialized to zero. Partial Reset will not alter previously programmed configurations but will initialize Write and Read pointers to zero.

In FWFT mode, first data written into the queue appears on output data bus after the specified latency period at the low to high transition of RCLK. Subsequent reads from the queue will require asserting $\overline{\text{REN}}$. This feature is useful when implementing depth expansion functions. In this mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ are used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ respectively.

In Standard mode, always assert $\overline{\text{REN}}$ for read operation. $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ are used instead of $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ respectively.

Product Description (Continued)

Bus matching feature is available with the following memory configurations:

Input Bus Width	Output Bus Width
x9	x36
x18	x36
x36	x36
x36	x18
x36	x9

In addition, Endian Select is available for implementing byte re-ordering on data outputs.

Eight different default offset values are available for Almost Full ($\overline{\text{PRAF}}$) and Almost Empty ($\overline{\text{PRAE}}$) flags. Parallel and Serial programming of these offset values provide total flexibility other than the pre-defined default values. Both 8-bit and 9-bit parallel programming modes for offset values can be selected for convenience.

$\overline{\text{PRAF}}$, $\overline{\text{PRAE}}$, and $\overline{\text{HALF}}$ are available in either FWFT or Standard mode. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ can operate in either synchronous or asynchronous mode.

At any time, data previously read from the queue can be retransmitted by asserting $\overline{\text{RET}}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue. Both zero and normal latency timing modes are available for retransmit operation.

These FlexQ™ III devices have low power consumption, hence minimizing system power requirements. In addition, industry standard 128 - pin Plastic TQFP is offered to save system board space.

These queues are ideal for applications such as data communication, telecommunication, graphics, multiprocessing, test equipment, network switching, etc.

Block Diagram of Single Synchronous Queue
131,072 x 36 / 65,536 x 36 / 32,768 x 36 / 16,384 x 36 / 8,192 x 36 / 4,096 x 36 / 2,048 x 36 / 1,024 x 36

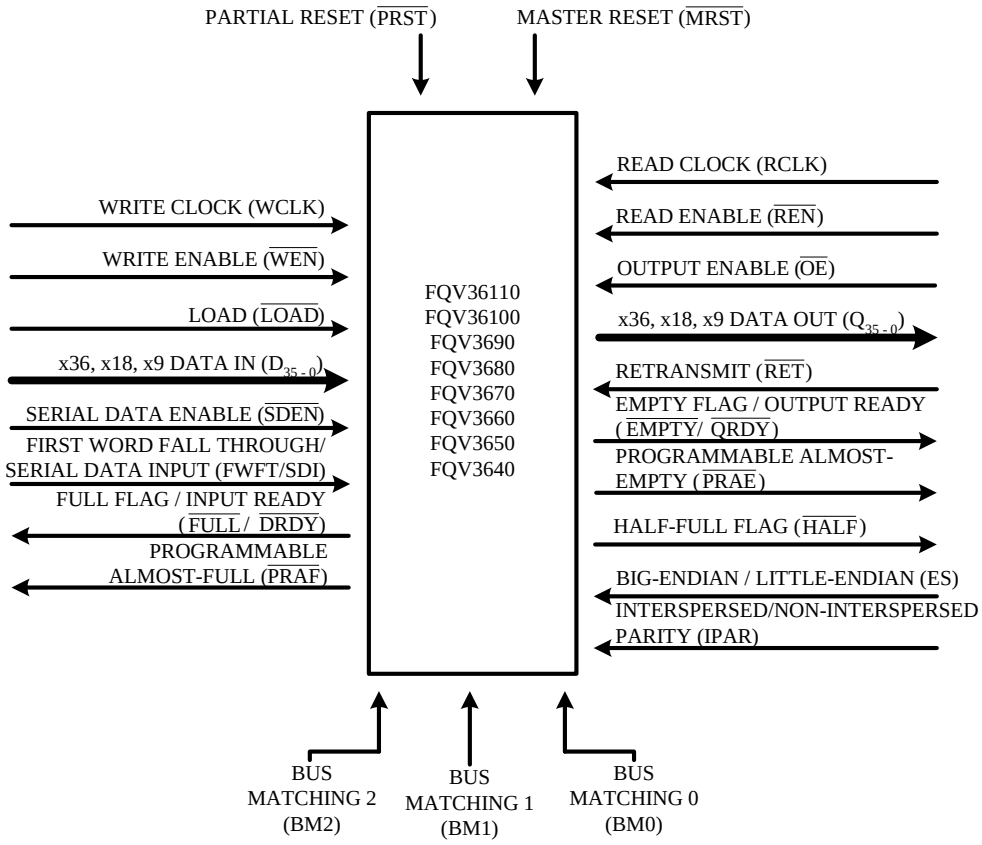


Figure 1. Single Device Configuration Signal Flow Diagram

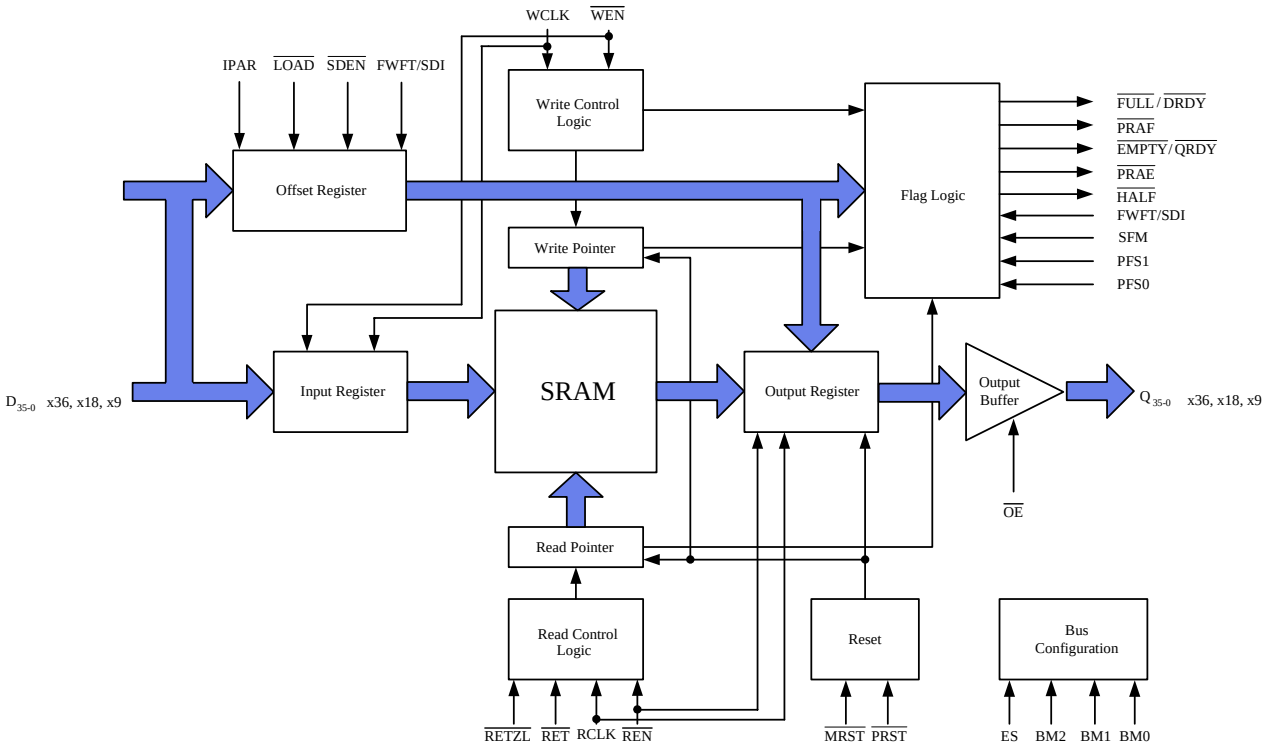
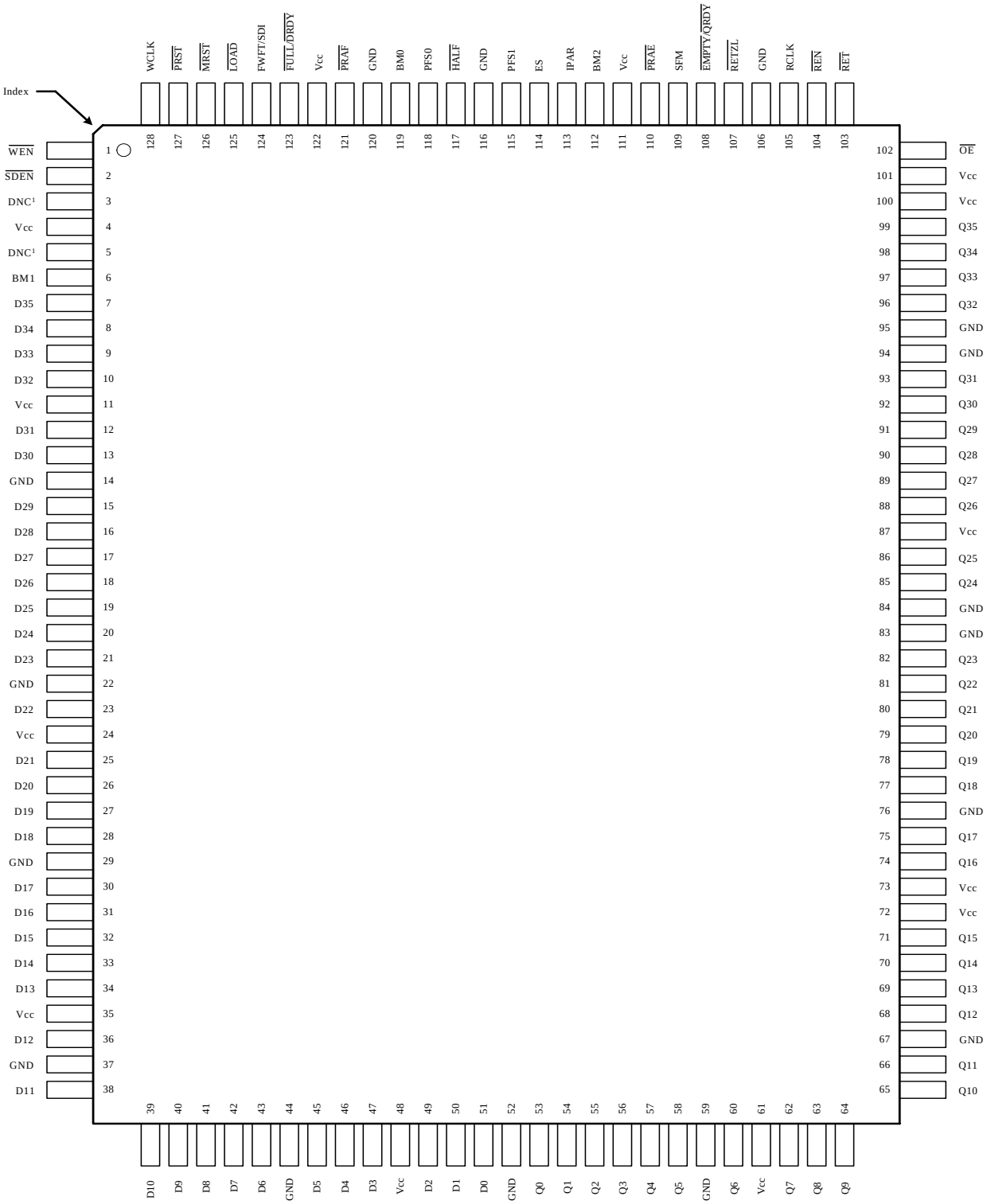


Figure 2. Device Architecture



TQFP - 128 (Drw No: PF-02A; Order code: PF)
Top View

NOTES:
1. DNC = Do Not Connect.

Figure 3. Device Pin Out

Pin #	Pin Name	Pin Symbol	Input/Output	Description
126	Master Reset	$\overline{MRST}$	Input	Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{MRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will not be maintained.
127	Partial Reset	$\overline{PRST}$	Input	Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{PRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will be maintained.
128	Write Clock	WCLK	Input	Writes data into queue during low to high transitions of WCLK if $\overline{WEN}$ is set to low.
1	Write Enable	$\overline{WEN}$	Input	Controls write operation into queue or offset registers during low to high transition of WCLK.
125	Load Enable	$\overline{LOAD}$	Input	During Master Reset, set $\overline{LOAD}$ low to select parallel programming and one of eight default offset values. Set $\overline{LOAD}$ high to select serial programming and one of eight default offset values. After Master Reset, $\overline{LOAD}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively. Use in conjunction with $\overline{WEN}$ / $\overline{REN}$.
115	Default Programming 1	PFS1	Input	During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{LOAD}$ and PFS0.
118	Default Programming 0	PFS0	Input	During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{LOAD}$ and PFS1.
07,08,09, 10,12,13, 15,16,17, 18,19,20, 21,23,25, 26,27,28, 30,31,32, 33,34,36, 38,39,40, 41,42,43, 45,46,47, 49,50,51.	Data Inputs	D_{35-0}	Input	36 - bit wide input data bus.
105	Read Clock	RCLK	Input	Reads data from queue during low to high transitions of RCLK if $\overline{REN}$ is set to low.
104	Read Enable	$\overline{REN}$	Input	Controls read operation from queue or offset registers during low to high transition of RCLK.

Table 1. Pin Descriptions

Pin #	Pin Name	Pin Symbol	Input/Output	Description
102	Output Enable	$\overline{OE}$	Input	Setting $\overline{OE}$ low activates the data output drivers. Setting $\overline{OE}$ high deactivates the data output drivers (High-Z).
99,98,97, 96,93,92, 91,90,89, 88,86,85, 82,81,80, 79,78,77, 75,74,71, 70,69,68, 66,65,64, 63,62,60, 58,57,56, 55,54,53	Data Outputs	Q_{35-0}	Output	36 - bit wide output data bus.
124	First Word Fall Through/Serial Data Input	FWFT/SDI	Input	Selects FWFT timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{LOAD}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{SDEN}$.
2	Serial Data Input Enable	$\overline{SDEN}$	Input	If serial programming is selected, setting $\overline{SDEN}$ low and $\overline{LOAD}$ low enables serial data input to be written into offset registers during the low to high transition of WCLK.
112	Bus Matching 2	BM2	Input	During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM1 and BM0.
6	Bus Matching 1	BM1	Input	During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM2 and BM0.
119	Bus Matching 0	BM0	Input	During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM2 and BM1.
114	Endian Select	ES	Input	During Master Reset, set ES high to select byte re-ordering on data outputs or ES low to select no byte re-ordering on data outputs.
103	Retransmit	$\overline{RET}$	Input	Data previously read from the queue can be retransmitted by asserting $\overline{RET}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue.
107	Zero Latency Retransmit	$\overline{RETZL}$	Input	During Master Reset, set $\overline{RETZL}$ low to select zero latency retransmit or $\overline{RETZL}$ high to select normal latency retransmit.
123	Full/Data Input Ready Flag	$\overline{FULL}$ / $\overline{DRDY}$	Output	Queue is full when $\overline{FULL}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue. In FWFT mode, queue is full when $\overline{DRDY}$ goes high during low to high transition of WCLK. This prohibits further writes into the queue.

Table 1. Pin Descriptions (Continued)

Pin #	Pin Name	Pin Symbol	Input/Output	Description
108	Empty/Data Output Ready Flag	$\overline{EMPTY}$ / $\overline{QRDY}$	Output	Queue is empty when $\overline{EMPTY}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue. In FWFT mode, queue is empty when $\overline{QRDY}$ goes high during the low to high transition of RCLK. This prohibits further reads from the queue.
113	Interspersed Parity	IPAR	Input	During Master Reset, set IPAR low to select 9-bit parallel programming mode or IPAR high to select 8-bit parallel programming mode.
109	Synchronous Partial Flag Mode	SFM	Input	During Master Reset, set SFM high to select Synchronous Partial Flag mode or SFM low to select Asynchronous Partial Flag mode.
121	Almost Full	$\overline{PRAF}$	Output	Queue is almost full when $\overline{PRAF}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{PRAF}$.
110	Almost Empty	$\overline{PRAE}$	Output	Queue is almost empty when $\overline{PRAE}$ goes low during the low to high transition of RCLK. Default (Empty +offset) or programmed offset values determine the status of $\overline{PRAE}$.
117	Half Full	$\overline{HALF}$	Output	Queue is more than half full when $\overline{HALF}$ goes low. Triggered by both WCLK and RCLK.
03, 05	Do Not Connect	DNC	N/A	Do not connect.
04,11,24, 35,48,61, 72,73,87, 100,101, 111,122.	Power	Vcc	N/A	3.3V power supply.
14,22,29, 37,44,52, 59,67,76, 83,84,94, 95,106, 116,120	Ground	GND	N/A	0V Ground.

Table 1. Pin Descriptions (Continued)

Symbol	Rating	Com'l & Ind'l	Unit
VTERM	Terminal Voltage with respect to GND	-0.5 to + 4.5	V
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	-50 to +50	mA

NOTES:
Absolute Max Ratings are for reference only. Permanent damage to the device may occur if extended period of operation is outside this range. Standard operation should fall within the Recommended Operating Conditions.

Table 2. Absolute Maximum Ratings

		FQV36110, FQV36100, FQV3690, FQV3680, FQV3670, FQV3660, FQV3650, FQV3640						
		Commercial Clock = 6ns, 7.5ns, 10ns, 15ns			Industrial Clock = 7.5ns, 10ns, 15ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Recommended Operating Conditions								
Vcc	Supply Voltage Com'l / Ind'l	3.15	3.3	3.45	3.15	3.3	3.45	V
GND	Supply Voltage	0	0	0	0	0	0	V
VIH	Input High Voltage Com'l / Ind'l	2.0	-	5.5	2.0	-	5.5	V
VIL	Input Low Voltage Com'l / Ind'l	-	-	0.8	-	-	0.8	V
TA	Operating Temperature Commercial	0	-	70	0	-	70	°C
TA	Operating Temperature Industrial	-40	-	85	-40	-	85	°C
DC Electrical Characteristics								
ILI(1)	Input Leakage Current (any input)	-10	-	10	-10	-	10	µA
ILO	Output Leakage Current	-10	-	10	-10	-	10	µA
VOH	Output Logic "1" Voltage, IOH=-2mA	2.4	-	-	2.4	-	-	V
VOL	Output Logic "0" Voltage, IOL = 8mA	-	-	0.4	-	-	0.4	V
Power Consumption								
Icc1(2,3)	Active Power Supply Current	-	-	40	-	-	40	mA
Icc2(4)	Standby Current	-	-	15	-	-	15	mA

Capacitance at 1.0MHz Ambient Temperature (25°C)				
Symbol	**Parameter**	**Conditions**	**Max.**	**Unit**
CIN(2)	Input Capacitance	VIN= 0V	10	pF
COUT(2,4)	Output Capacitance	VOUT= 0V	10	pF

NOTES:
1. Measurement with 0.4<=VIN<=Vcc
2. With output tri-stated ($\overline{OE}$ = High)
3. Icc(1,2) is measured with WCLK and RCLK at 20 MHz
4. Design simulated, not tested.

Table 3. DC Specifications

Symbol	Parameter	Commercial		Commercial & Industrial						Unit
		FQV36110-6 FQV36100-6 FQV3690-6 FQV3680-6 FQV3670-6 FQV3660-6 FQV3650-6 FQV3640-6		FQV36110-7.5 FQV36100-7.5 FQV3690-7.5 FQV3680-7.5 FQV3670-7.5 FQV3660-7.5 FQV3650-7.5 FQV3640-7.5		FQV36110-10 FQV36100-10 FQV3690-10 FQV3680-10 FQV3670-10 FQV3660-10 FQV3650-10 FQV3640-10		FQV36110-15 FQV36100-15 FQV3690-15 FQV3680-15 FQV3670-15 FQV3660-15 FQV3650-15 FQV3640-15		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Cycle Frequency	-	166	-	133	-	100	-	66	MHz
t_A	Data Access Time	1	4.2	2	5	2	6.5	2	10	ns
t_{WCLK}	Write Clock Cycle Time	6	-	7.5	-	10	-	15	-	ns
t_{WCLKH}	Write Clock High Time	2.5	-	3.5	-	4.5	-	6	-	ns
t_{WCLKL}	Write Clock Low Time	2.5	-	3.5	-	4.5	-	6	-	ns
t_{RCLK}	Read Clock Cycle Time	6	-	7.5	-	10	-	15	-	ns
t_{RCLKH}	Read Clock High Time	2.5	-	3.5	-	4.5	-	6	-	ns
t_{RCLKL}	Read Clock Low Time	2.5	-	3.5	-	4.5	-	6	-	ns
t_{DS}	Data Set-up Time	1.8	-	2.5	-	3.5	-	4	-	ns
t_{DH}	Data Hold Time	0.5	-	0.5	-	0.5	-	1	-	ns
t_{ENS}	Enable Set-up Time	1.8	-	2.5	-	3.5	-	4	-	ns
t_{ENH}	Enable Hold Time	0.5	-	0.5	-	0.5	-	1	-	ns
t_{RST}	Reset Pulse Width[1]	8	-	10	-	10	-	15	-	ns
t_{RSTS}	Reset Set-up Time	10	-	15		15	-	15	-	ns
t_{RSTR}	Reset Recovery Time	10	-	10	-	10	-	15	-	ns
t_{RSTF}	Reset to Flag and Output Time	-	10	-	15	-	15	-	15	ns
t_{OLZ}	Output Enable to Output in Low-Z[1]	0	-	0	-	0	-	0	-	ns
t_{OE}	Output Enable to Output Valid	1	4	2	6	2	6	2	8	ns
t_{OHZ}	Output Enable to Output in High-Z[1]	1	4	2	6	2	6	2	8	ns
t_{FULL}	Write Clock to Full Flag	-	4	-	5	-	6.5	-	10	ns
t_{EMPTY}	Read Clock to Empty Flag	-	4	-	5	-	6.5	-	10	ns
t_{PRAFS}	Write Clock to Synchronous Almost-Full Flag	-	4	-	5	-	6.5	-	10	ns
t_{PRAES}	Read Clock to Synchronous Almost-Empty Flag	-	4	-	5	-	6.5	-	10	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Full Flag / Empty Flag	4	-	5	-	7	-	9	-	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for $\overline{PRAE}$ & $\overline{PRAF}$	5	-	7	-	10	-	14	-	ns
t_{LOADS}	Load Setup Time	2.0	-	2.5	-	3.5	-	4	-	ns
t_{LOADH}	Load Hold Time	0.5	-	0.5	-	0.5	-	1	-	ns

Table 4. AC Electrical Characteristics

Symbol	Parameter	Commercial		Commercial & Industrial						Unit
		FQV36110-6 FQV36100-6 FQV3690-6 FQV3680-6 FQV3670-6 FQV3660-6 FQV3650-6 FQV3640-6		FQV36110-7.5 FQV36100-7.5 FQV3690-7.5 FQV3680-7.5 FQV3670-7.5 FQV3660-7.5 FQV3650-7.5 FQV3640-7.5		FQV36110-10 FQV36100-10 FQV3690-10 FQV3680-10 FQV3670-10 FQV3660-10 FQV3650-10 FQV3640-10		FQV36110-15 FQV36100-15 FQV3690-15 FQV3680-15 FQV3670-15 FQV3660-15 FQV3650-15 FQV3640-15		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RETS}	Retransmit Setup Time	2.5	-	3.5	-	3.5	-	4	-	ns
t_{HALF}	Clock to $\overline{HALF}$	-	10	-	12.5	-	16	-	20	ns
t_{PRAFA}	Write Clock to Asynchronous Programmable Almost-Full Flag	-	10	-	12.5	-	16	-	20	ns
t_{PRAEA}	Read Clock to Asynchronous Programmable Almost-Empty Flag	-	10	-	12.5	-	16	-	20	ns

NOTES:

1. Design simulated, not tested.

Table 4. AC Electrical Characteristics (Continued)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns(1)
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load, clock = 6ns, 7.5 ns	Refer to Figure 4 & 6
Output Load*, clock = 10ns, 15ns	Refer to Figure 5

* Include jig and scope capacitances

NOTES:
1. For 166 MHz and 133 MHz, operation input rise/fall times are 1.5ns.

Table 5. AC Test Condition

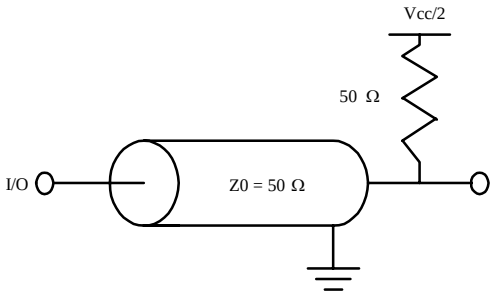


Figure 4. AC Test Load
for clock = 6ns, 7.5ns

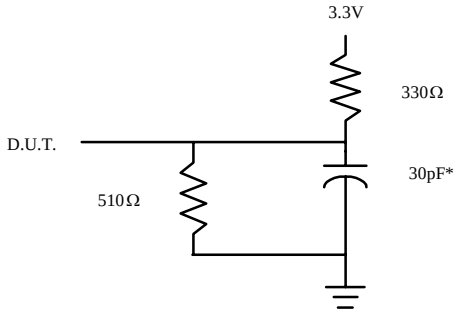


Figure 5. Output Load
for clock = 10ns, 15ns
*Includes jig and scope capacitances.

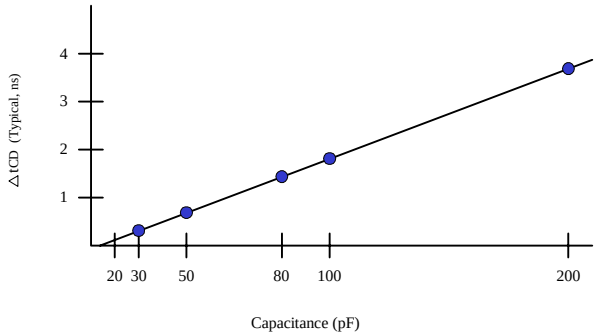


Figure 6. Lumped Capacitive Load

Pin Functions

$\overline{\text{MRST}}$ Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{MRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will not be maintained.

$\overline{\text{PRST}}$ Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{PRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will be maintained.

WCLK Writes data into queue during low to high transitions of WCLK if $\overline{\text{WEN}}$ is activated. Synchronizes $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ and $\overline{\text{PRAF}}$ flags. WCLK and RCLK are independent of each other.

$\overline{\text{WEN}}$ Controls write operation into queue or offset registers during low to high transition of WCLK.

$\overline{\text{LOAD}}$ During Master Reset, set $\overline{\text{LOAD}}$ low to select parallel programming or one of eight default offset values. Set $\overline{\text{LOAD}}$ high to select serial programming or one of eight default offset values. After Master Reset, $\overline{\text{LOAD}}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively for parallel programming. Use in conjunction with $\overline{\text{WEN}}$ / $\overline{\text{REN}}$. During programming of offset registers, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flag status is invalid. For Serial programming, $\overline{\text{LOAD}}$ is used to enable serial loading of offset registers together with $\overline{\text{SDEN}}$. Refer to Figure 7 & Table 13 for details.

PFS1 During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{\text{LOAD}}$ and PFS0. Refer to Table 13 for details.

PFS0 During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{\text{LOAD}}$ and PFS1. Refer to Table 13 for details.

D_{35-0} 36 - bit wide input data bus.

RCLK Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN}}$ is set low. Synchronizes the $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ and $\overline{\text{PRAE}}$ flags. RCLK and WCLK are independent of each other.

$\overline{\text{REN}}$ Reads data from queue or offset registers during low to high transitions of RCLK if $\overline{\text{REN}}$ is set to low. This also advances the Read pointer of the queue.

$\overline{\text{OE}}$ Setting $\overline{\text{OE}}$ low activates the data output drivers. Setting $\overline{\text{OE}}$ high deactivates the data output drivers (High-Z). $\overline{\text{OE}}$ does not control advancement of Read pointer.

Q_{35-0} 36 - bit wide output data bus.

FWFT/SDI Selects FWFT timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{\text{LOAD}}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{\text{SDEN}}$. In FWFT mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ are used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$. Refer to Table 11 for all flags status. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ are used instead of $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$. Refer to Table 10 for all flags status.

$\overline{\text{SDEN}}$ If serial programming is selected, setting $\overline{\text{SDEN}}$ and $\overline{\text{LOAD}}$ low enables serial data to be written into offset registers during the low to high transition of WCLK. During serial programming, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flags status is invalid. Refer to Figure 7 for details.

Pin Functions (Continued)

BM2 During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM1 and BM0. Refer to Table 12 for details.

BM1 During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM2 and BM0. Refer to Table 12 for details.

BM0 During Master Reset, select one of five input and output bus width configurations. Use in conjunction with BM2 and BM1. Refer to Table 12 for details.

ES During Master Reset, set ES high to select byte re-ordering on data outputs or set ES low to select no byte re-ordering on data outputs. ES must be static throughout device operation. Refer to Table 12 for details.

$\overline{\text{RET}}$ Data previously read from the queue can be retransmitted by asserting $\overline{\text{RET}}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue. Refer to Diagram 7 & 8 for details.

$\overline{\text{RETZL}}$ During Master Reset, set $\overline{\text{RETZL}}$ low to select zero latency retransmit or set $\overline{\text{RETZL}}$ high to select normal latency retransmit.

$\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ In Standard mode, queue is full when $\overline{\text{FULL}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. In FWFT mode, queue is full when $\overline{\text{DRDY}}$ goes high during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. Refer to Table 10 & 11 for behavior of $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$.

$\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ In Standard mode, queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. In FWFT mode, queue is empty when $\overline{\text{QRDY}}$ goes high during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. Refer to Table 10 & 11 for behavior of $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$.

IPAR During Master Reset, set IPAR low to select 9-bit parallel programming mode or set IPAR high to select 8-bit parallel programming mode. In 9-bit mode, 9-bit wide data input/output bus width is used for storing/fetching offset values. In 8-bit mode, 8-bit wide data input/output bus is used for storing/fetching offset values.

SFM During Master Reset, set SFM high to select Synchronous Partial Flag mode or set SFM low to select Asynchronous Partial Flag mode. In Synchronous mode, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ are synchronous to WCLK and RCLK respectively. In Asynchronous mode, WCLK synchronizes the assertion of $\overline{\text{PRAF}}$ and de-assertion of $\overline{\text{PRAE}}$. RCLK synchronizes the assertion of $\overline{\text{PRAE}}$ and de-assertion of $\overline{\text{PRAF}}$.

$\overline{\text{PRAF}}$ In Synchronous mode, queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{\text{PRAF}}$. In Asynchronous mode, $\overline{\text{PRAF}}$ is triggered by both WCLK and RCLK. Refer to Table 10 & 11 for behavior of $\overline{\text{PRAF}}$.

$\overline{\text{PRAE}}$ In Synchronous mode, queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty+offset) or programmed offset values determine the status of $\overline{\text{PRAE}}$. In Asynchronous mode, $\overline{\text{PRAE}}$ is triggered by both WCLK and RCLK. Refer to Table 10 & 11 for behavior of $\overline{\text{PRAE}}$.

$\overline{\text{HALF}}$ Queue is more than half full when $\overline{\text{HALF}}$ goes low during the low to high transition of WCLK. $\overline{\text{HALF}}$ goes high during low to high transition of RCLK when queue is less than half full. Refer to Table 10 & 11 for details.

$\overline{\text{LOAD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	$\overline{\text{SDEN}}$	WCLK	RCLK	FQV36110 FQV36100 FQV3690 FQV3680 FQV3670 FQV3660 FQV3650 FQV3640 Selection / Sequence
0	0	1	1	↑	X	Parallel write to offset registers: Empty Offset Full Offset Parallel write to registers: 1. $\overline{\text{PRAE}}$ 2. $\overline{\text{PRAF}}$
0	1	0	1	X	↑	Parallel read from offset registers: Empty Offset Full Offset Parallel read from registers: 1. $\overline{\text{PRAE}}$ 2. $\overline{\text{PRAF}}$
0	1	1	0	↑	X	Serial shift into registers: 34 bits for the FQV36110 32 bits for the FQV36100 30 bits for the FQV3690 28 bits for the FQV3680 26 bits for the FQV3670 24 bits for the FQV3660 22 bits for the FQV3650 20 bits for the FQV3640 1 bit for each rising WCLK edge Starting with Empty Offset (Low Byte) Ending with Full Offset (High Byte)
X	1	1	1	X	X	No Operation
1	0	X	X	↑	X	Write Memory
1	X	0	X	X	↑	Read Memory
1	1	1	X	X	X	No Operation

Figure 7. Programmable Flag Offset Programming Sequence
(FQV36110, FQV36100, FQV3690, FQV3680, FQV3670, FQV3660, FQV3650 and FQV3640)

Device	$\overline{\text{PRAF}}$ Programming (bits)		$\overline{\text{PRAE}}$ Programming (bits)	
FQV36110	D/Q_{16-0}	Non-IPAR	D/Q_{16-0}	Non-IPAR
	D/Q_{18} & D/Q_{16-9} & D/Q_{7-0}	IPAR	D/Q_{18} & D/Q_{16-9} & D/Q_{7-0}	IPAR
FQV36100	D/Q_{15-0}	Non-IPAR	D/Q_{15-0}	Non-IPAR
	D/Q_{16-9} & D/Q_{7-0}	IPAR	D/Q_{16-9} & D/Q_{7-0}	IPAR
FQV3690	D/Q_{14-0}	Non-IPAR	D/Q_{14-0}	Non-IPAR
	D/Q_{15-9} & D/Q_{7-0}	IPAR	D/Q_{15-9} & D/Q_{7-0}	IPAR
FQV3680	D/Q_{13-0}	Non-IPAR	D/Q_{13-0}	Non-IPAR
	D/Q_{14-9} & D/Q_{7-0}	IPAR	D/Q_{14-9} & D/Q_{7-0}	IPAR
FQV3670	D/Q_{12-0}	Non-IPAR	D/Q_{12-0}	Non-IPAR
	D/Q_{13-9} & D/Q_{7-0}	IPAR	D/Q_{13-9} & D/Q_{7-0}	IPAR
FQV3660	D/Q_{11-0}	Non-IPAR	D/Q_{11-0}	Non-IPAR
	D/Q_{12-9} & D/Q_{7-0}	IPAR	D/Q_{12-9} & D/Q_{7-0}	IPAR
FQV3650	D/Q_{10-0}	Non-IPAR	D/Q_{10-0}	Non-IPAR
	D/Q_{11-9} & D/Q_{7-0}	IPAR	D/Q_{11-9} & D/Q_{7-0}	IPAR
FQV3640	D/Q_{9-0}	Non-IPAR	D/Q_{9-0}	Non-IPAR
	D/Q_{10-9} & D/Q_{7-0}	IPAR	D/Q_{10-9} & D/Q_{7-0}	IPAR

Table 6. Parallel Offset Register Data Mapping Table for x36 Bus Width

Device	$\overline{\text{PRAF}}$ Programming (bits)			$\overline{\text{PRAE}}$ Programming (bits)		
FQV36110	D/Q_{15-0}	Low Byte	Non-IPAR	D/Q_{15-0}	Low Byte	Non-IPAR
	D/Q_0	High Byte	Non-IPAR	D/Q_0	High Byte	Non-IPAR
	D/Q_{16-9} & D/Q_{7-0}	Low Byte	IPAR	D/Q_{16-9} & D/Q_{7-0}	Low Byte	IPAR
	D/Q_0	High Byte	IPAR	D/Q_0	High Byte	IPAR
FQV36100	D/Q_{15-0}		Non-IPAR	D/Q_{15-0}		Non-IPAR
	D/Q_{16-9} & D/Q_{7-0}		IPAR	D/Q_{16-9} & D/Q_{7-0}		IPAR
FQV3690	D/Q_{14-0}		Non-IPAR	D/Q_{14-0}		Non-IPAR
	D/Q_{15-9} & D/Q_{7-0}		IPAR	D/Q_{15-9} & D/Q_{7-0}		IPAR
FQV3680	D/Q_{13-0}		Non-IPAR	D/Q_{13-0}		Non-IPAR
	D/Q_{14-9} & D/Q_{7-0}		IPAR	D/Q_{14-9} & D/Q_{7-0}		IPAR
FQV3670	D/Q_{12-0}		Non-IPAR	D/Q_{12-0}		Non-IPAR
	D/Q_{13-9} & D/Q_{7-0}		IPAR	D/Q_{13-9} & D/Q_{7-0}		IPAR
FQV3660	D/Q_{11-0}		Non-IPAR	D/Q_{11-0}		Non-IPAR
	D/Q_{12-9} & D/Q_{7-0}		IPAR	D/Q_{12-9} & D/Q_{7-0}		IPAR
FQV3650	D/Q_{10-0}		Non-IPAR	D/Q_{10-0}		Non-IPAR
	D/Q_{11-9} & D/Q_{7-0}		IPAR	D/Q_{11-9} & D/Q_{7-0}		IPAR
FQV3640	D/Q_{9-0}		Non-IPAR	D/Q_{9-0}		Non-IPAR
	D/Q_{10-9} & D/Q_{7-0}		IPAR	D/Q_{10-9} & D/Q_{7-0}		IPAR

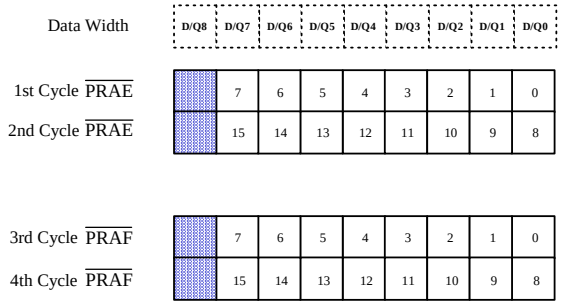
Table 7. Parallel Offset Register Data Mapping Table for x18 Bus Width

Device	$\overline{PRAF}$ Programming (bits)		$\overline{PRAE}$ Programming (bits)	
FQV36110	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{7-0}	Mid Byte	D/Q_{7-0}	Mid Byte
	D/Q_0	High Byte	D/Q_0	High Byte
FQV36100	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{7-0}	High Byte	D/Q_{7-0}	High Byte
FQV3690	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{6-0}	High Byte	D/Q_{6-0}	High Byte
FQV3680	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{5-0}	High Byte	D/Q_{5-0}	High Byte
FQV3670	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{4-0}	High Byte	D/Q_{4-0}	High Byte
FQV3660	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{3-0}	High Byte	D/Q_{3-0}	High Byte
FQV3650	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{2-0}	High Byte	D/Q_{2-0}	High Byte
FQV3640	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{1-0}	High Byte	D/Q_{1-0}	High Byte

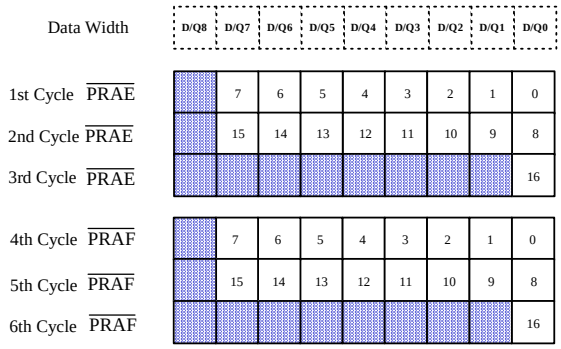
Table 8. Parallel Offset Register Data Mapping for Table x9 Bus Width

Device	Standard Mode	FWFT Mode
FQV36110	131,072 x 36	131,073 x 36
FQV36100	65,536 x 36	65,537 x 36
FQV3690	32,768 x 36	32,769 x 36
FQV3680	16,384 x 36	16,385 x 36
FQV3670	8,192 x 36	8,193 x 36
FQV3660	4,096 x 36	4,097 x 36
FQV3650	2,048 x 36	2,049 x 36
FQV3640	1,024 x 36	1,025 x 36

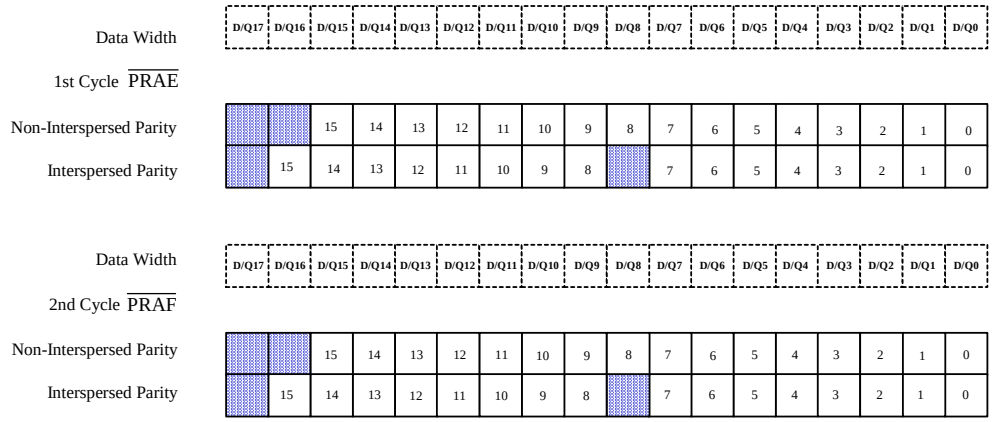
Table 9. Maximum Depth of Queue for Standard and FWFT Mode



FQV36100, FQV3690, FQV3680, FQV3670, FQV3660, FQV3650, FQV3640
Parallel Offset Write/Read Cycles for x9 Bus Width

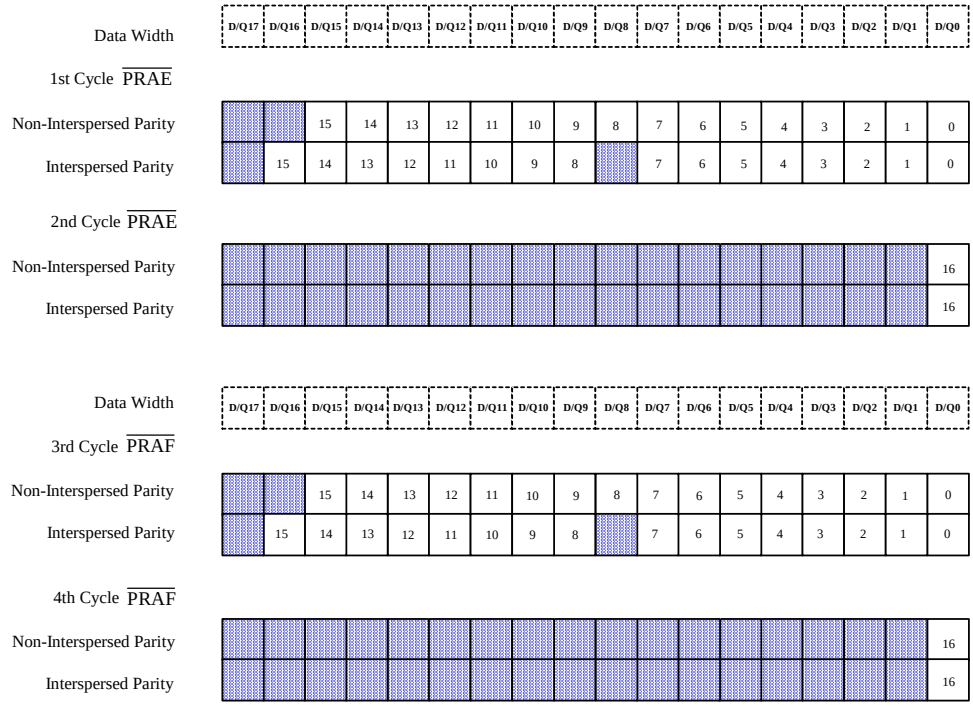


FQV36110
Parallel Offset Write/Read Cycles for x9 Bus Width

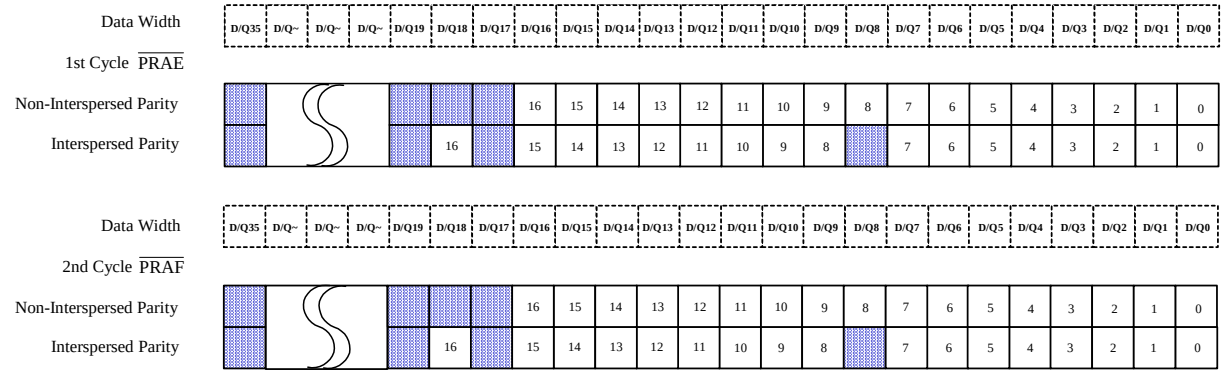


FQV36100, FQV3690, FQV3680, FQV3670, FQV3660, FQV3650, FQV3640
Parallel Offset Write/Read Cycles for x18 Bus Width

Figure 8. Parallel Offset Write/Read Cycle Diagram



FQV36110
Parallel Offset Write/Read Cycles for x18 Bus Width



FQV36110, FQV36100, FQV3690, FQV3680, FQV3670, FQV3660, FQV3650, FQV3640
Parallel Offset Write/Read Cycles for x36 Bus Width

# of Bits for Offset Registers
17 bits for FQV36110 16 bits for FQV36100 15 bits for FQV3690 14 bits for FQV3680 13 bits for FQV3670 12 bits for FQV3660 11 bits for FQV3650 10 bits for FQV3640
Note: Don't Care applies to all unused bits

Figure 8. Parallel Offset Write/Read Cycle Diagram (Continued)

FQV36110	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 65,536	H	H	H	H	H
65,537 to [131,072-(x+1)]	H	H	L	H	H
(131,072-x) to 131,071	H	L	L	H	H
131,072	L	L	L	H	H

FQV36100	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 32,768	H	H	H	H	H
32,769 to [65,536-(x+1)]	H	H	L	H	H
(65,536-x) to 65,535	H	L	L	H	H
65,536	L	L	L	H	H

FQV3690	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 16,384	H	H	H	H	H
16,385 to [32,768-(x+1)]	H	H	L	H	H
(32,768-x) to 32,767	H	L	L	H	H
32,768	L	L	L	H	H

FQV3680	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 8,192	H	H	H	H	H
8,193 to [16,384-(x+1)]	H	H	L	H	H
(16,384 -x) to 16,383	H	L	L	H	H
16,384	L	L	L	H	H

FQV3670	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 4,096	H	H	H	H	H
4,097 to [8,192-(x+1)]	H	H	L	H	H
(8,192 -x) to 8,191	H	L	L	H	H
8,192	L	L	L	H	H

FQV3660	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 2,048	H	H	H	H	H
2,049 to [4,096-(x+1)]	H	H	L	H	H
(4,096 –x) to 4,095	H	L	L	H	H
4,096	L	L	L	H	H

Table 10. Status Flags (Standard Mode)

FQV3650	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 1,024	H	H	H	H	H
1,025 to [2,048-(x+1)]	H	H	L	H	H
(2,048 -x) to 2,047	H	L	L	H	H
2,048	L	L	L	H	H

FQV3640	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 512	H	H	H	H	H
513 to [1,024-(x+1)]	H	H	L	H	H
(1,024 –x) to 1,023	H	L	L	H	H
1,024	L	L	L	H	H

NOTES:
1. See Table 13 for values x, y.

Table 10. Status Flags (Standard Mode) (Continued)

FQV36110	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[(1)]	L	H	H	L	L
(y+2) to 65,537	L	H	H	H	L
65,538 to [131,073-(x+1)]	L	H	L	H	L
(131,073-x) to 131,072	L	L	L	H	L
131,073	H	L	L	H	L

FQV36100	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[(1)]	L	H	H	L	L
(y+2) to 32,769	L	H	H	H	L
32,770 to [65,537-(x+1)]	L	H	L	H	L
(65,537-x) to 65,536	L	L	L	H	L
65,537	H	L	L	H	L

FQV3690	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[(1)]	L	H	H	L	L
(y+2) to 16,385	L	H	H	H	L
16,386 to [32,769-(x+1)]	L	H	L	H	L
(32,769-x) to 32,768	L	L	L	H	L
32,769	H	L	L	H	L

FQV3680	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[(1)]	L	H	H	L	L
(y+2) to 8,193	L	H	H	H	L
8,194 to [16,385-(x+1)]	L	H	L	H	L
(16,385 -x) to 16,384	L	L	L	H	L
16,385	H	L	L	H	L

FQV3670	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[(1)]	L	H	H	L	L
(y+2) to 4,097	L	H	H	H	L
4,098 to [8,193-(x+1)]	L	H	L	H	L
(8,193-x) to 8,192	L	L	L	H	L
8,193	H	L	L	H	L

FQV3660	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[(1)]	L	H	H	L	L
(y+2) to 2,049	L	H	H	H	L
2,050 to [4,097-(x+1)]	L	H	L	H	L
(4,097 -x) to 4,096	L	L	L	H	L
4,097	H	L	L	H	L

Table 11. Status Flags (FWFT Mode)

FQV3650	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 1,025	L	H	H	H	L
1,026 to [2,049-(x+1)]	L	H	L	H	L
(2,049 -x) to 2,048	L	L	L	H	L
2,049	H	L	L	H	L

FQV3640	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 513	L	H	H	H	L
514 to [1,025-(x+1)]	L	H	L	H	L
(1,025 -x) to 1,024	L	L	L	H	L
1,025	H	L	L	H	L

NOTES:
1. See Table 13 for values x, y.

Table 11. Status Flags (FWFT Mode) (Continued)

ES	BM2	BM1	BM0	I/O	Width	D/Q_{35-27}	D/Q_{26-18}	D/Q_{17-9}	D/Q_{8-0}	Sequence
X	0	X	X	I	36	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	36	Byte 4	Byte 3	Byte 2	Byte 1	1st Read
0	1	0	0	I	36	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	18	X	X	Byte 4	Byte 3	1st Read
						X	X	Byte 2	Byte 1	2nd Read
0	1	0	1	I	36	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	9	X	X	X	Byte 4	1st Read
						X	X	X	Byte 3	2nd Read
						X	X	X	Byte 2	3rd Read
						X	X	X	Byte1	4th Read
0	1	1	0	I	18	X	X	Byte 4	Byte 3	1st Write
						X	X	Byte 2	Byte 1	2nd Write
				O	36	Byte 4	Byte 3	Byte 2	Byte 1	1st Read
0	1	1	1	I	9	X	X	X	Byte 4	1st Write
						X	X	X	Byte 3	2nd Write
						X	X	X	Byte 2	3rd Write
						X	X	X	Byte1	4th Write
				O	36	Byte 4	Byte 3	Byte 2	Byte 1	1st Read
1	1	0	0	I	36	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	18	X	X	Byte 2	Byte 1	1st Read
						X	X	Byte 4	Byte 3	2nd Read
1	1	0	1	I	36	Byte 4	Byte 3	Byte 2	Byte 1	1st Write
				O	9	X	X	X	Byte 1	1st Read
						X	X	X	Byte 2	2nd Read
						X	X	X	Byte 3	3rd Read
						X	X	X	Byte4	4th Read
1	1	1	0	I	18	X	X	Byte 4	Byte 3	1st Write
						X	X	Byte 2	Byte 1	2nd Write
				O	36	Byte 2	Byte 1	Byte 4	Byte 3	1st Read
1	1	1	1	I	9	X	X	X	Byte 4	1st Write
						X	X	X	Byte 3	2nd Write
						X	X	X	Byte 2	3rd Write
						X	X	X	Byte1	4th Write
				O	36	Byte 1	Byte 2	Byte 3	Byte 4	1st Read

Table 12. Bus-Matching Table

$\overline{LOAD}$	PFS1	PFS0	FQV3650 FQV3640 Default Offsets x, y(1)
0	0	0	127
0	0	1	255
0	1	0	511
0	1	1	63
1	0	0	31
1	0	1	7
1	1	0	15
1	1	1	3

$\overline{LOAD}$	PFS1	PFS0	FQV3650 FQV3640 Program Mode
1	X	X	Serial
0	X	X	Parallel

$\overline{LOAD}$	PFS1	PFS0	FQV3690 FQV3680 FQV3670 FQV3660 Default Offsets x, y(1)
0	0	0	127
0	0	1	255
0	1	0	511
0	1	1	63
1	0	0	1,023
1	0	1	15
1	1	0	31
1	1	1	7

$\overline{LOAD}$	PFS1	PFS0	FQV3690 FQV3680 FQV3670 FQV3660 Program Mode
1	X	X	Serial
0	X	X	Parallel

NOTES:

1. x = $\overline{PRAF}$ offset, y = $\overline{PRAE}$ offset.

Table 13. Default Programmable Flag Offsets

$\overline{\text{LOAD}}$	PFS1	PFS0	FQV36110 FQV36100
			Default Offsets x, y(1)
0	0	0	127
0	0	1	8,191
0	1	0	16,383
0	1	1	4,095
1	0	0	1,023
1	0	1	511
1	1	0	2,047
1	1	1	255

$\overline{\text{LOAD}}$	PFS1	PFS0	FQV36110 FQV36100
			Program Mode
1	X	X	Serial
0	X	X	Parallel

NOTES:

1. x = $\overline{\text{PRAF}}$ offset, y = $\overline{\text{PRAE}}$ offset.

Table 13. Default Programmable Flag Offsets (Continued)

Timing Diagrams

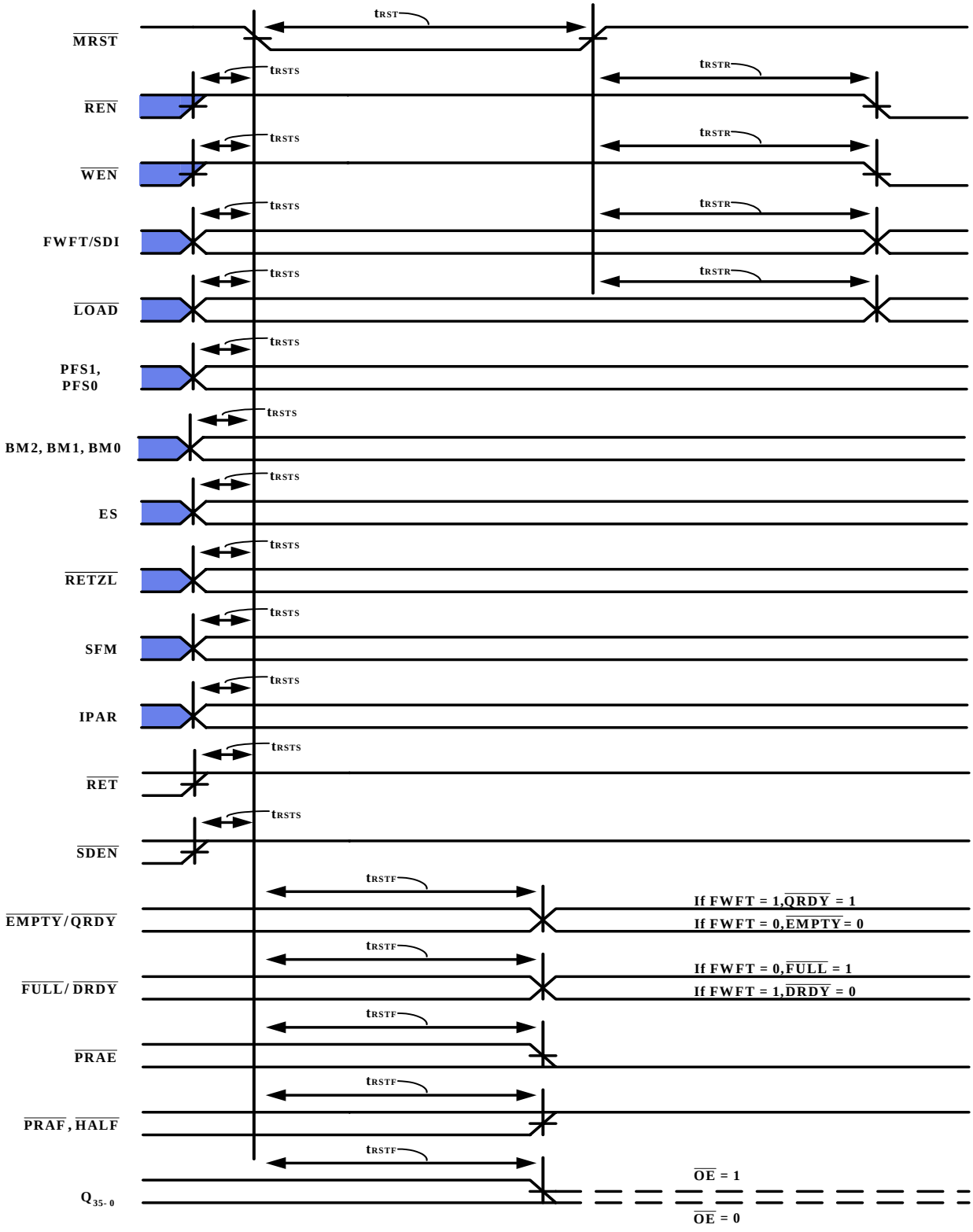


Diagram 1. Master Reset Timing

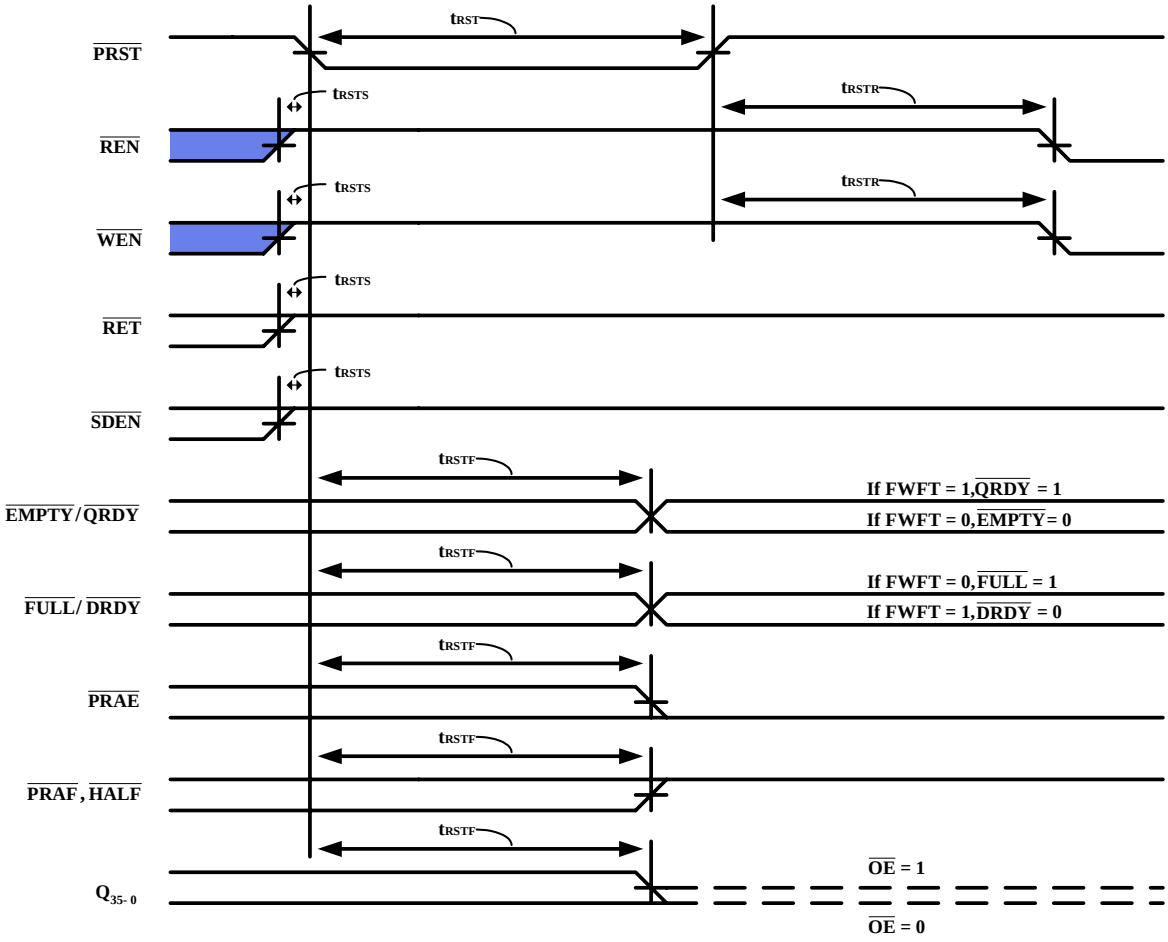


Diagram 2. Partial Reset Timing

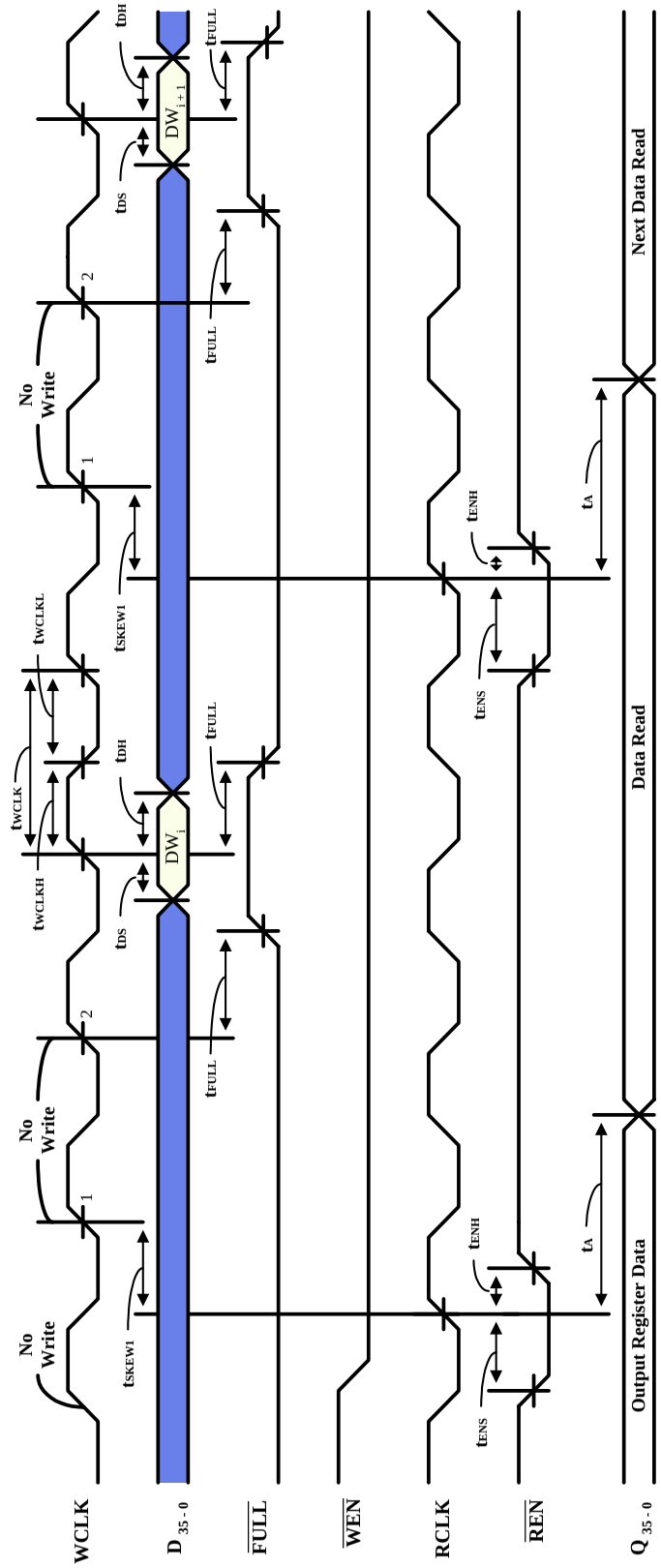


Diagram 3. Write Cycle and Full Flag Timing (Standard Mode)

NOTES:

1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW1}, $\overline{FULL}$ will go high (after one WCLK cycle plus t_{FULL}). If t_{SKEW1} is not met, then $\overline{FULL}$ will assert 1 or more WCLK cycles.
2. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.

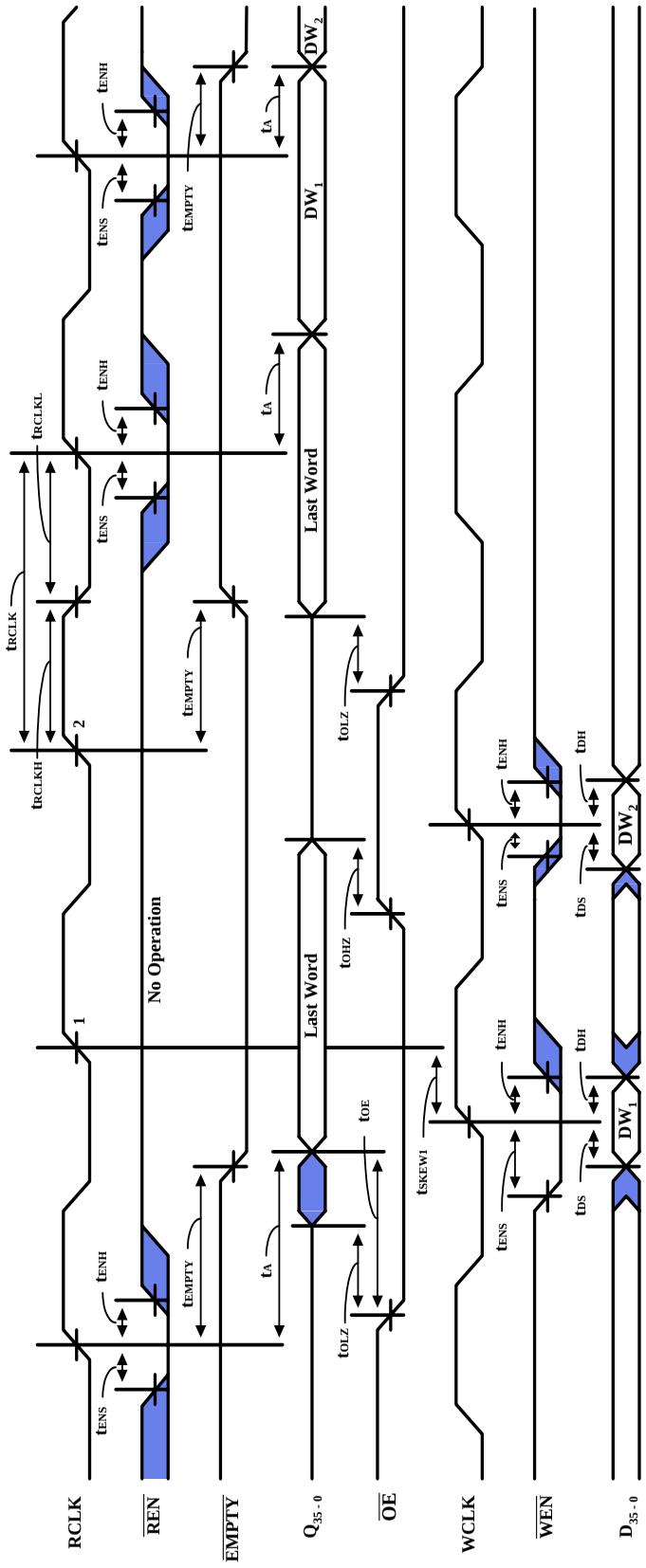


Diagram 4. Read Cycle, Empty Flag and First Data Word Latency Timing (Standard Mode)

NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW1}, $\overline{EMPTY}$ will go high (after one RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.
2. $\overline{LOAD}$ = High.
3. First word latency: $t_{SKEW1} + t_{EMPTY} + 1 * t_{RCLK}$.

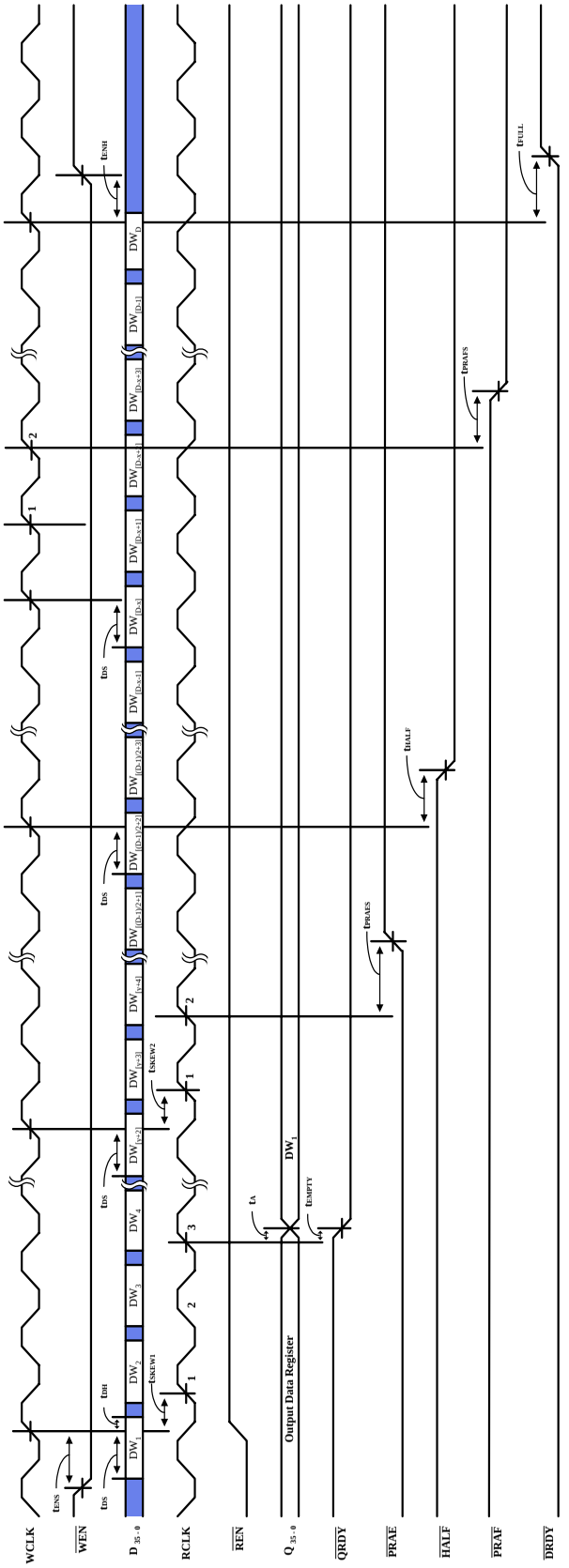
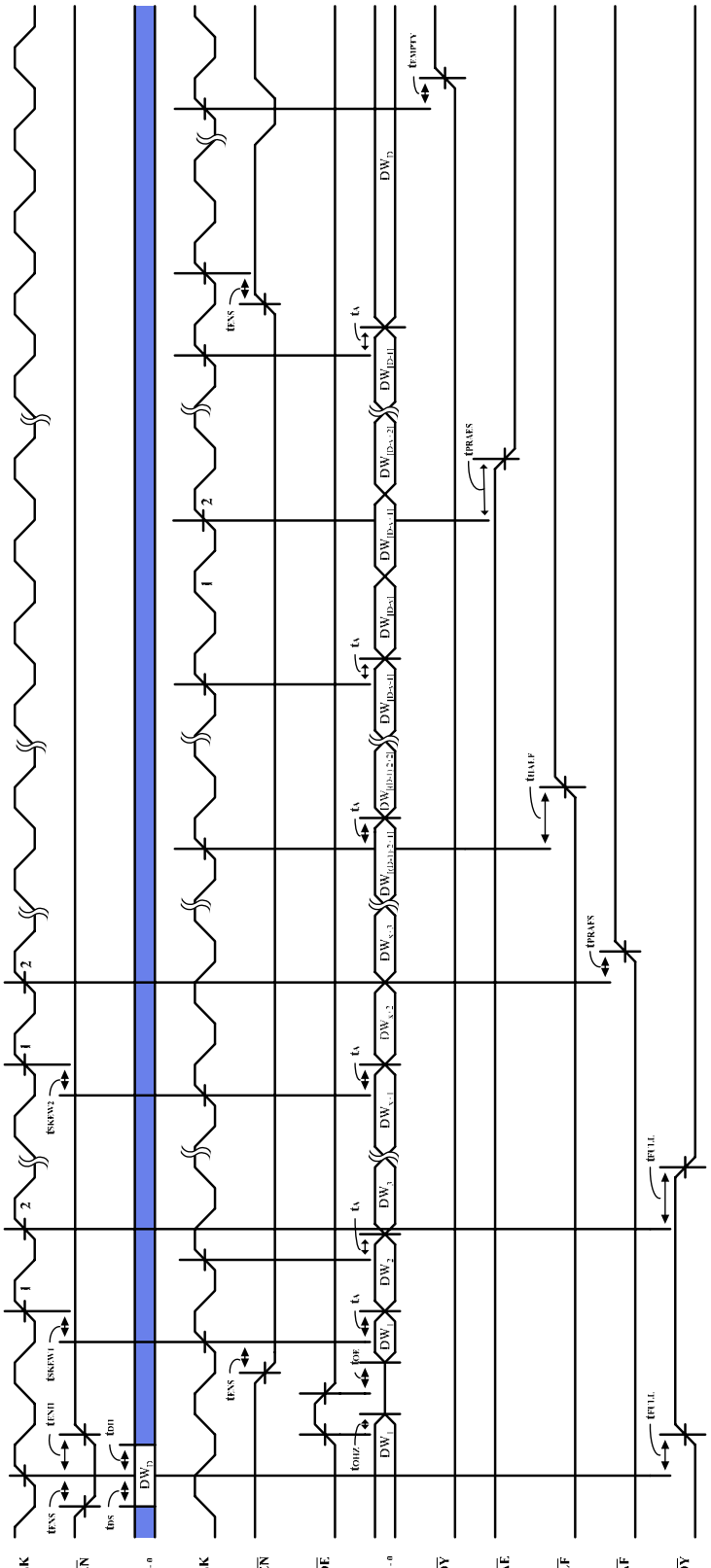


Diagram 5. Write Timing (FWFT Mode)

NOTES:

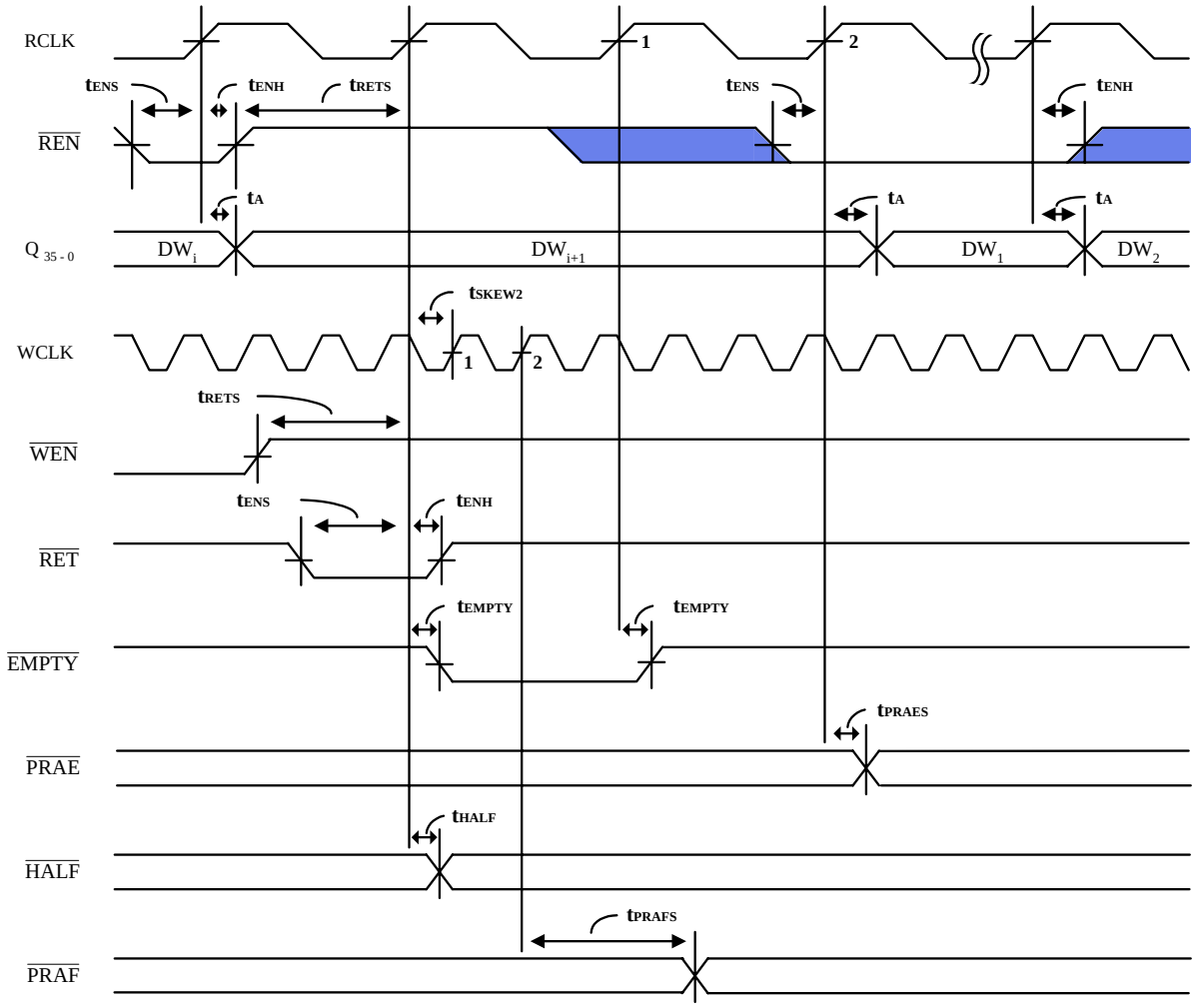
1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW1}, $\overline{QRDY}$ will go low (after two RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{QRDY}$ will assert 1 or more RCLK cycles.
2. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW2}, $\overline{PRAE}$ will go high (after one RCLK cycle plus t_{PRAES}). If t_{SKEW2} is not met, then $\overline{PRAE}$ will assert 1 or more RCLK cycles.
3. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.
4. y = $\overline{PRAE}$ offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 9 for Depth.
6. First word latency: $t_{SKEW1} + t_{EMPTY} + 2 * t_{RCLK}$



NOTES:

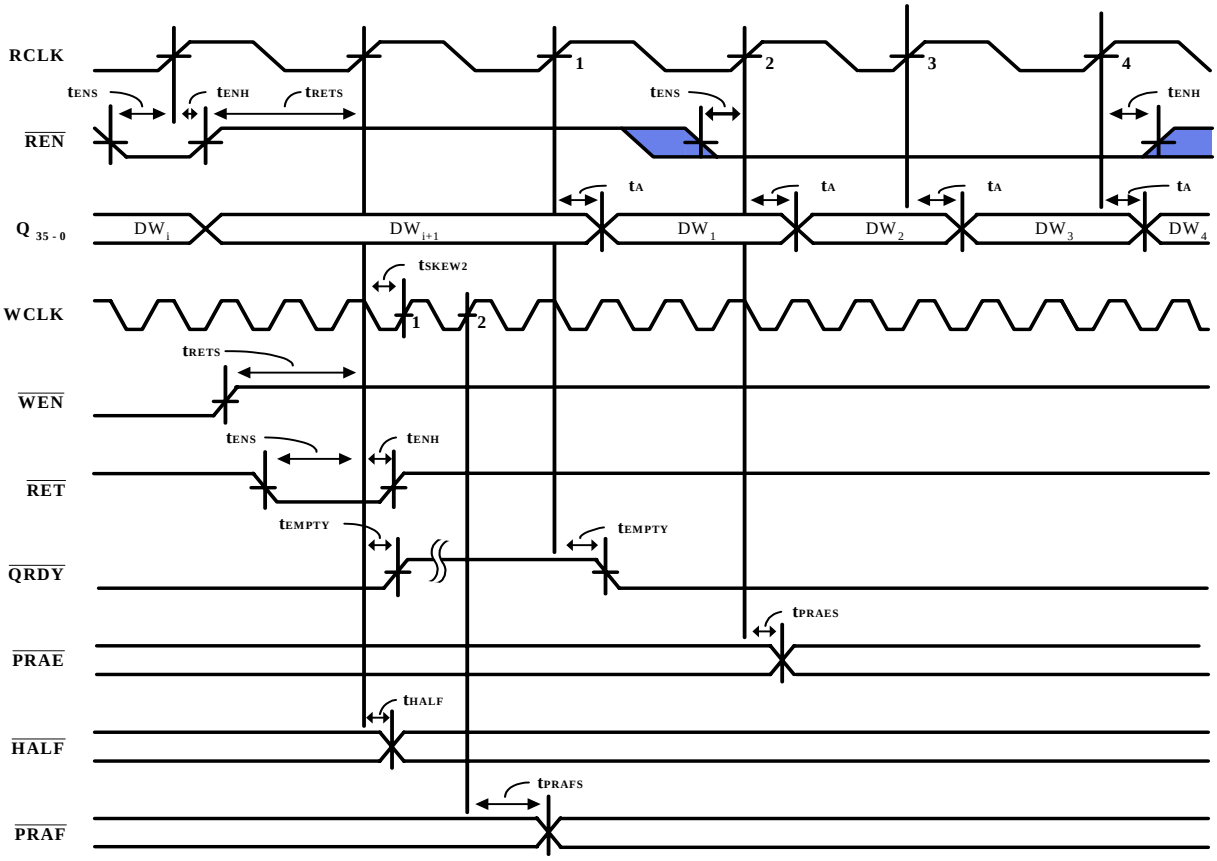
1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW1}, $\overline{DRDY}$ will go low (after one WCLK cycle plus t_{FULL}) . If t_{SKEW1} is not met, then $\overline{DRDY}$ will assert 1 or more WCLK cycles.
2. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW2}, $\overline{PRAF}$ will go high (after one WCLK cycle plus t_{PRAFS}) If t_{SKEW2} is not met, then $\overline{PRAF}$ will assert 1 or more WCLK cycles.
3. $\overline{LOAD}$ = High
4. y = $\overline{PRAE}$ Offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 9 for Depth.

Diagram 6. Read Timing (FWFT Mode)



NOTES:
1. Upon completion of retransmit setup, a read operation can begin only after $\overline{EMPTY}$ returns high.
2. $\overline{OE}$ = Low.
3. DW_i = Words written to the queue after $\overline{MRST}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than two words written to the queue for a retransmit setup to be valid.

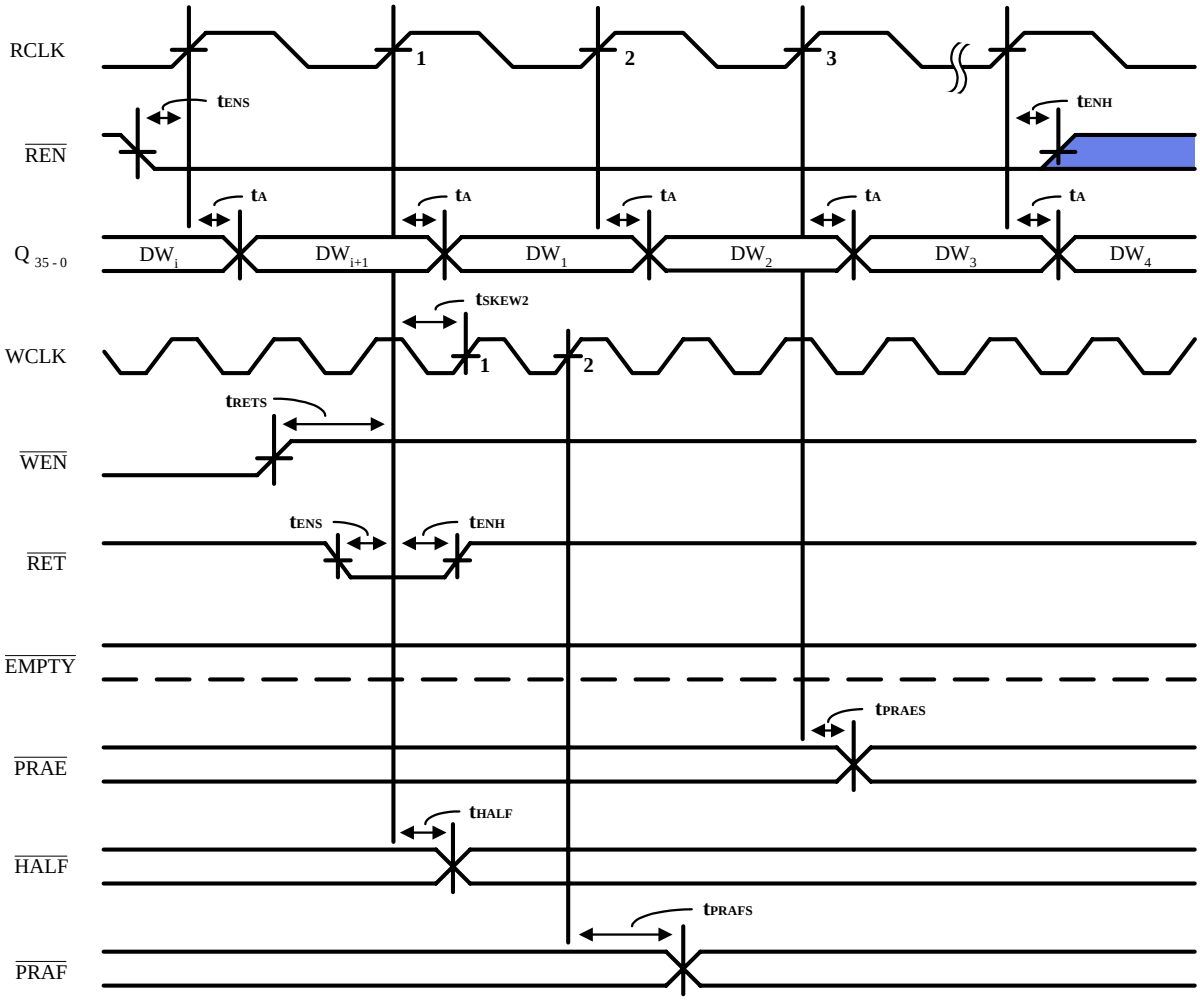
Diagram 7. Retransmit Timing (Standard Mode)



NOTES:

1. Upon completion of retransmit setup, a read operation can begin only after $\overline{QRDY}$ returns low.
2. $\overline{OE}$ = Low.
3. DW_i = Words written to the queue after $\overline{MRST}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than two words written to the queue for a retransmit setup to be valid.
5. Please refer to Table 9 for Depth.

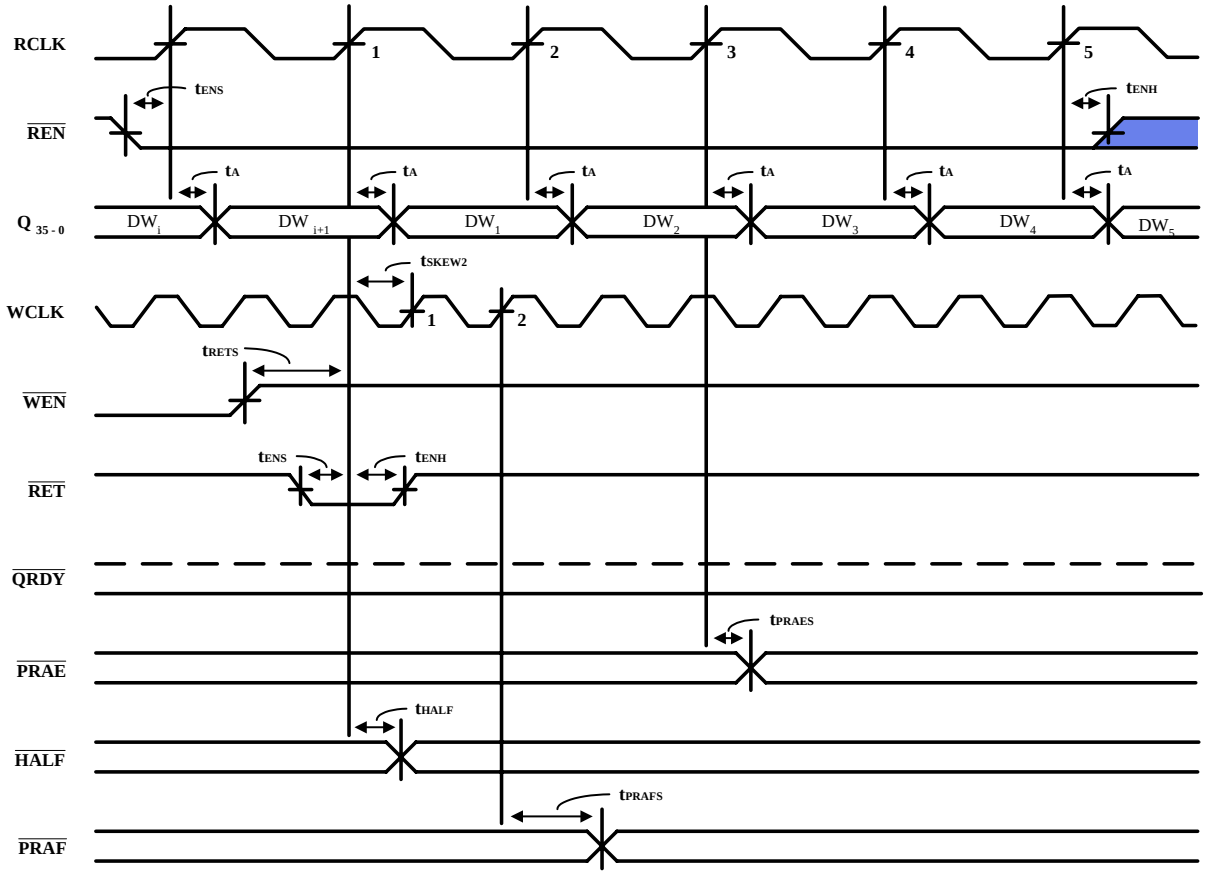
Diagram 8. Retransmit Timing (FWFT Mode)



NOTES:

1. If the part is empty at the point of retransmit, the Empty Flag ($\overline{\text{EMPTY}}$) will be updated based on RCLK (Retransmit Clock cycle). Valid data will appear on the output.
2. $\overline{\text{OE}}$ = Low; enables data to be read on outputs Q_{35-0}.
3. DW_1= first word written to the queue after Master Reset; DW_2= second word written to the queue after Master Reset.
4. No more than D-2 may be written to the queue between reset (Master or Partial) and retransmit setup. Therefore, $\overline{\text{FULL}}$ will be high throughout the retransmit setup procedure. Please refer to Table 9 for Depth.
5. There must be at least two words written to zero latency retransmit from the queue before a retransmit operation can be invoked.
6. $\overline{\text{RETZL}}$ is set Low during $\overline{\text{MRST}}$.

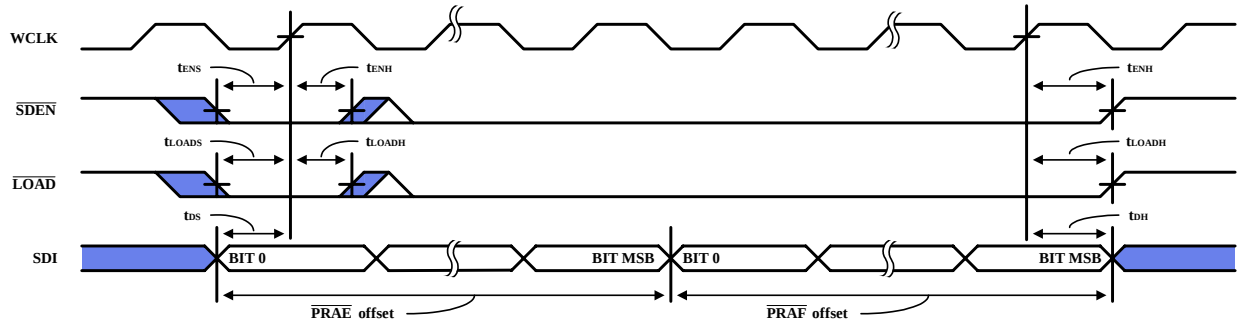
Diagram 9. Zero Latency Retransmit Timing (Standard Mode)



NOTES:

1. If the part is empty at the point of retransmit, the output ready flag ($\overline{\text{QRDY}}$) will be updated based on RCLK (Retransmit Clock cycle). Valid data will appear on the output.
2. No more than D-2 words may be written to the queue between reset (Master or Partial) and retransmit setup. Therefore, $\overline{\text{DRDY}}$ will be low throughout the retransmit setup procedure. Please refer to Table 9 for Depth.
3. $\overline{\text{OE}}$ = Low.
4. DW_1, DW_2, DW_3 = first, second and third words written to the queue after Master Reset.
5. There must be at least two words written to the queue before a retransmit operation can be invoked.
6. $\overline{\text{RETZL}}$ is set low during $\overline{\text{MRST}}$.

Diagram 10. Zero Latency Retransmit Timing (FWFT Mode)



*Refer to Table 14

Diagram 11. Serial Loading of Programmable Flag Registers (Standard and FWFT Mode)

	FQV36110	FQV36100	FQV3690	FQV3680	FQV3670	FQV3660	FQV3650	FQV3640
MSB	16	15	14	13	12	11	10	9

Table 14. Reference Table for Diagram 11

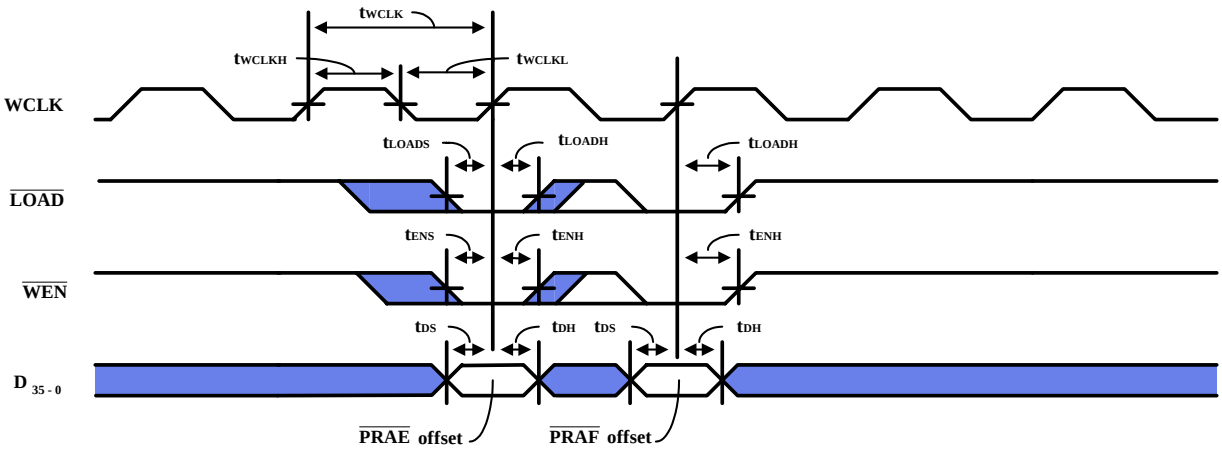


Diagram 12. Parallel Loading of Programmable Flag Registers (Standard and FWFT Mode)

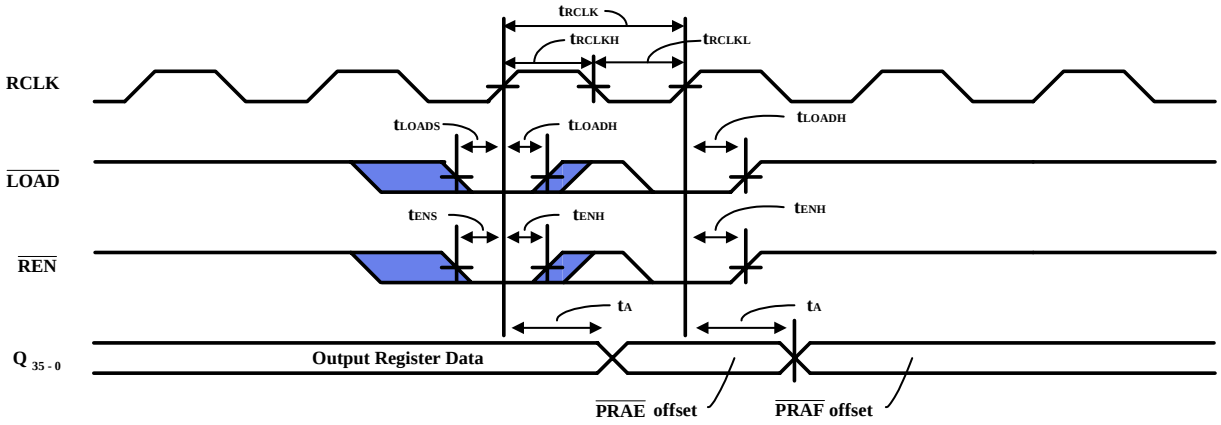
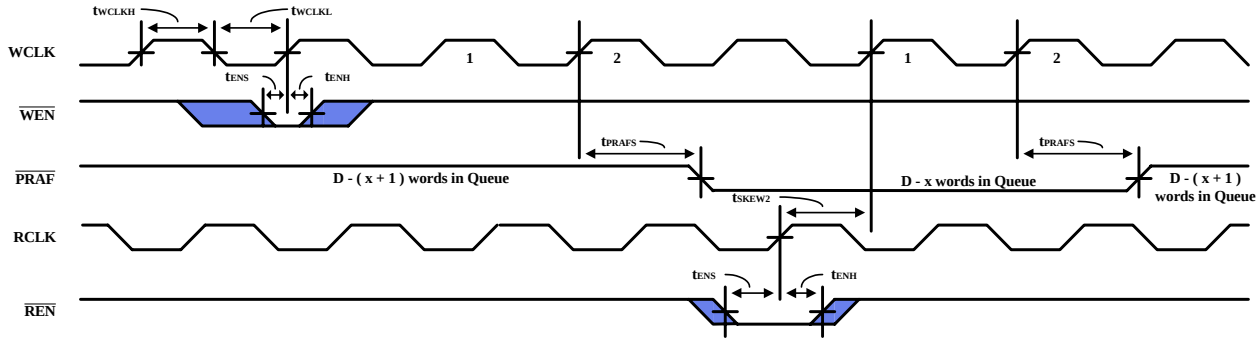
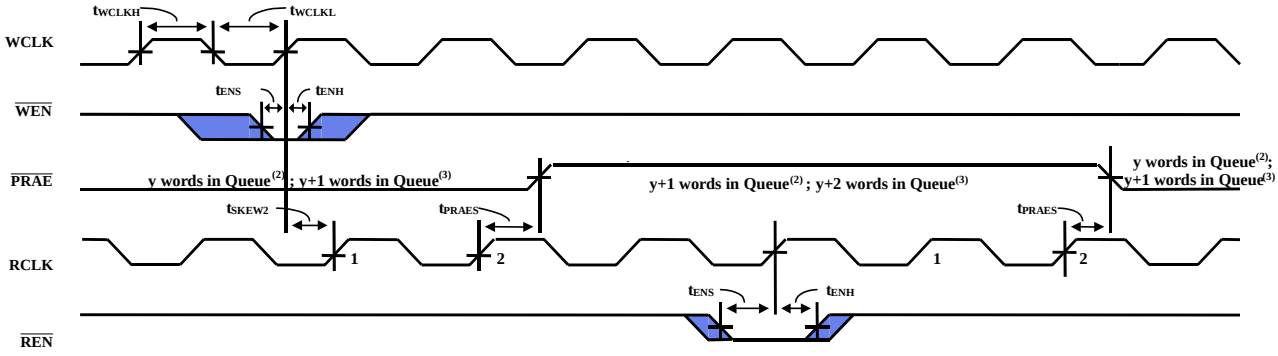


Diagram 13. Parallel Read of Programmable Flag Registers (Standard and FWFT Mode)



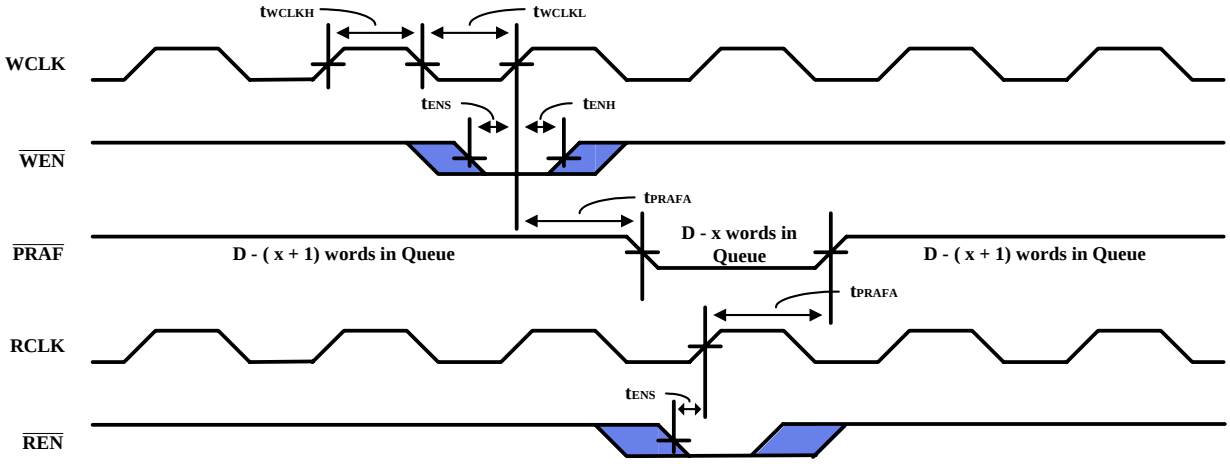
NOTES:
1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth. Please refer to Table 9 for Depth.
3. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW2}, $\overline{\text{PRAF}}$ will go high (after one WCLK cycle plus t_{PRAFS}). If t_{SKEW2} is not met, then $\overline{\text{PRAF}}$ will assert 1 or more WCLK cycles.
4. $\overline{\text{PRAF}}$ synchronizes to the rising edge of WCLK only.

Diagram 14. Synchronous Programmable Almost-Full Flag Timing (Standard and FWFT Mode)



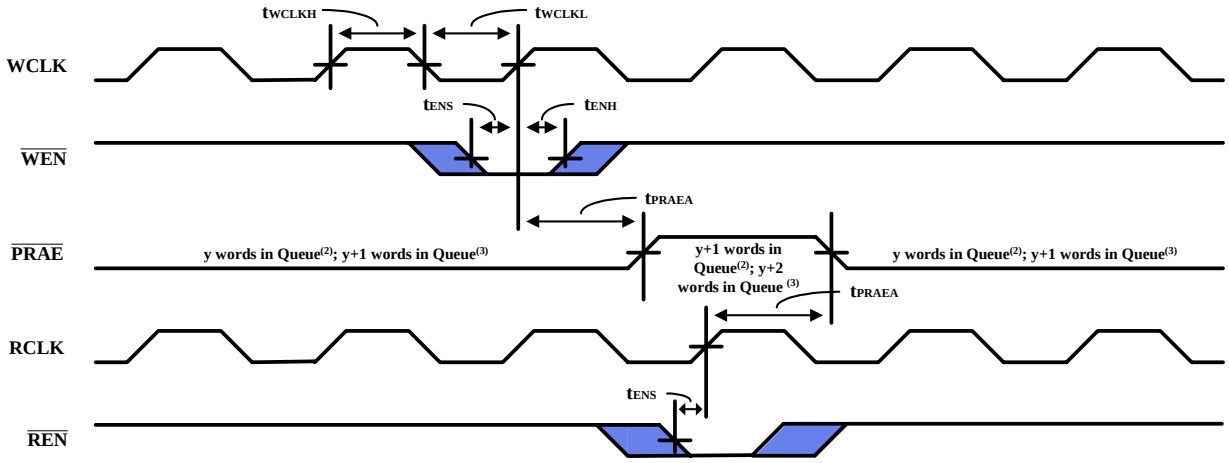
NOTES:
1. y = $\overline{\text{PRAE}}$ offset.
2. For Standard Mode.
3. For FWFT Mode.
4. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW2}, $\overline{\text{PRAE}}$ will go high (after one RCLK cycle plus t_{PRAES}). If t_{SKEW2} is not met, then $\overline{\text{PRAE}}$ will assert 1 or more RCLK cycles.
5. $\overline{\text{PRAE}}$ synchronizes to the rising edge of RCLK only.

Diagram 15. Synchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Mode)



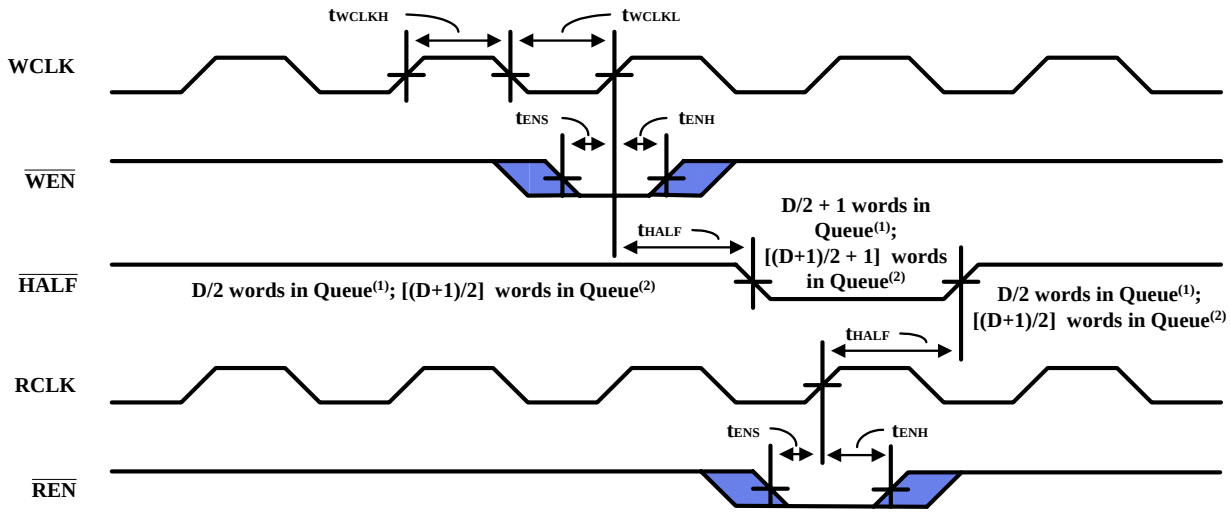
NOTES:
1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth. Please refer to Table 9 for Depth.
3. $\overline{\text{PRAF}}$ is asserted to low on WCLK transition and reset to high on RCLK transition.
4. Select this mode by setting SFM low during Master Reset.

Diagram 16. Asynchronous Programmable Almost-Full Flag Timing (Standard and FWFT Mode)



NOTES:
1. y = $\overline{\text{PRAE}}$ offset.
2. For Standard Mode.
3. For FWFT Mode.
4. $\overline{\text{PRAE}}$ is asserted to low on RCLK transition and reset to high on WCLK transition.
5. Select this mode by setting SFM low during Master Reset.

Diagram 17. Asynchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Mode)



NOTES:
1. For Standard Mode.
2. For FWFT Mode.
3. Please refer to Table 9 for Depth.

Diagram 18. Half-Full Flag Timing (Standard and FWFT Mode)

Order Information:

AMIC Device Family	Device Type	Power	Speed (ns) *	Package**	Temperature Range	Material
XX	XXXXX	X	XX	XX	X	X
FQ	**V36110** (131,072 x 36)	Low	**6** – 166 MHz	PF	Blank – Commercial (0°C to 70°C)	Blank – Normal material
	V36100 (65,536 x 36)		**7-5** – 133 MHz		**I** – Industrial (-40° to 85°C)	-F – Pb-Free material
	V3690 (32,768 x 36)		**10** – 100 MHz			
	V3680 (16,384 x 36)		**15** – 66 MHz			
	V3670 (8,192 x 36)					
	V3660 (4,096 x 36)					
	V3650 (2,048 x 36)					
	V3640 (1,024 x 36)					

***Speed –** 6ns available only in Commercial temp (0°C to 70°C). Slower speeds available upon request.
****Package** – 128 pin Plastic Thin Quad Flat Pack (TQFP)

Example:

FQV3680L6PF (16k x 36, 6ns, Commercial temp, Normal material)
FQV3670L10PFI (8k x 36, 10ns, Industrial temp, Normal material)
FQV3670L10PFI-F (8K x 36, 10ns, Industrial temp, Pb-Free material)