Make Memory Smarter ™

3.3 Volt Synchronous x9/x18 First-In/First-Out Queue

Memory Organization	Device	Memory Organization	Device
262,144 x 18 / 524,288 x 9	FQV2113	16,384 x 18 / 32,768 x 9	FQV273
131,072 x 18 / 262,144 x 9	FQV2103	8,192 x 18 / 16,384 x 9	FQV263
65,536 x 18 / 131,072 x 9	FQV293	4,096 x 18 / 8,192 x 9	FQV253
32,768 x 18 / 65,536 x 9	FQV283	2,048 x 18 / 4,096 x 9	FQV243

Key Features

- **Industry leading First-In/First-Out Queues (up to 166MHz)**
- **Write cycle time of 6.0ns independent of Read cycle time (Data Setup time = 2.0ns)**
- **Read cycle time of 6.0ns independent of Write cycle time (Data Access time = 4.0ns)**
- **User selectable input and output port bus-sizing**
- **Big Endian/Little Endian user selectable byte representation**
- **3.3V power supply**
- **5V input tolerant on all control and data input pins**
- **5V output tolerant on all flags and data output pins**
- **Master Reset clears all previously programmed configurations including Write and Read pointers**
- **Partial Reset clears Write and Read pointers but maintains all previously programmed configurations**
- **First Word Fall Through (FWFT) and Standard Timing modes**
- **Presets for eight different Almost Full and Almost Empty offset values**
- **Parallel/Serial programming of $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ offset values**
- **Programmable 8-bit or 9-bit parallel programming modes for offset values**
- **Full, Empty, Almost Full, Almost Empty, and Half Full indicators**
- **$\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ operates in either synchronous or asynchronous modes**
- **Asynchronous output enable tri-state data output drivers**
- **Data retransmission with programmable zero or normal latency modes**
- **Available package: 80 - pin Plastic Thin Quad Flat Pack (TQFP)**
- **(0°C to 70°C) Commercial operating temperature available for cycle time of 6.0ns and above**
- **(-40°C to 85°C) Industrial operating temperature available for cycle time of 7.5ns and above**

Product Description

HBA's FlexQ™ III offers industry leading FIFO queuing bandwidth (up to 3.0 Gbps), with a wide range of memory configurations (from 2,048 x 18 to 262,144 x 18 or 4,096 x 9 to 524,286 x 9). System designer has full flexibility of implementing deeper and wider queues using FWFT mode and width expansion features. Full, Empty, and Half-Full indicators allow easy handshaking between transmitters and receivers. User programmable Almost Full and Almost Empty (Parallel/Serial) indicators allow implementation of virtual queue depths.

5V tolerant on all input and output pins allows easy interfacing with devices operating at higher voltage levels. Asynchronous Output Enable pin configures the tri-state data output drivers. Independent Write and Read controls provide rate-matching capability.

Master Reset clears all previously programmed configurations by providing a low pulse on $\overline{\text{MRST}}$ pin. In addition, Write and Read pointers to the queue are initialized to zero. Partial Reset will not alter previously programmed configurations but will initialize Write and Read pointers to zero.

In FWFT mode, the first data written into the queue appears on output data bus after the specified latency period at the low to high transition of RCLK. Subsequent reads from the queue will require asserting $\overline{\text{REN}}$. This feature is useful when implementing depth expansion functions. In this mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ are used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ respectively.

Product Description (Continued)

In Standard mode, always assert $\overline{REN}$ whenever a read operation. $\overline{FULL}$ and $\overline{EMPTY}$ are used instead of $\overline{DRDY}$ and $\overline{QRDY}$ respectively.

Bus matching feature is available with the following configurations:

Input Bus Width	Output Bus Width
x9	x9
x9	x18
x18	x9
x18	x18

In addition, Endian Select is available for implementing byte re-ordering on data outputs.

Eight different default offset values are available for Almost Full ($\overline{PRAF}$) and Almost Empty ($\overline{PRAE}$) flags. Parallel and Serial programming of these offset values provide total flexibility other than the pre-defined default values. Both 8-bit and 9-bit parallel programming modes for offset values can be selected for convenience.

$\overline{PRAF}$, $\overline{PRAE}$, and $\overline{HALF}$ are available in either FWFT or Standard mode. $\overline{PRAF}$ and $\overline{PRAE}$ can operate in either synchronous or asynchronous modes.

At any time, data previously read from the queue can be retransmitted by asserting $\overline{RET}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue. Both zero and normal latency timing modes are available for retransmit operation.

These FlexQ™ III devices have low power consumption, hence minimizing system power requirements. In addition, industry standard 80 - pin Plastic TQFP is offered to save system board space.

These queues are ideal for applications such as data communication, telecommunication, graphics, multiprocessing, test equipment, network switching, etc.

Block Diagram of Single Synchronous Queue
262,144 x 18 / 131,072 x 18 / 65,536 x 18 / 32,768 x 18 / 16,384 x 18 / 8,192 x 18 / 4,096 x 18 / 2,048 x 18 / 524,288 x 9 / 262,144 x 9 / 131,072 X 9 / 65,536 X 9 / 32,768 X 9 / 16,384 X 9 / 8,192 x 9 / 4,096 x 9

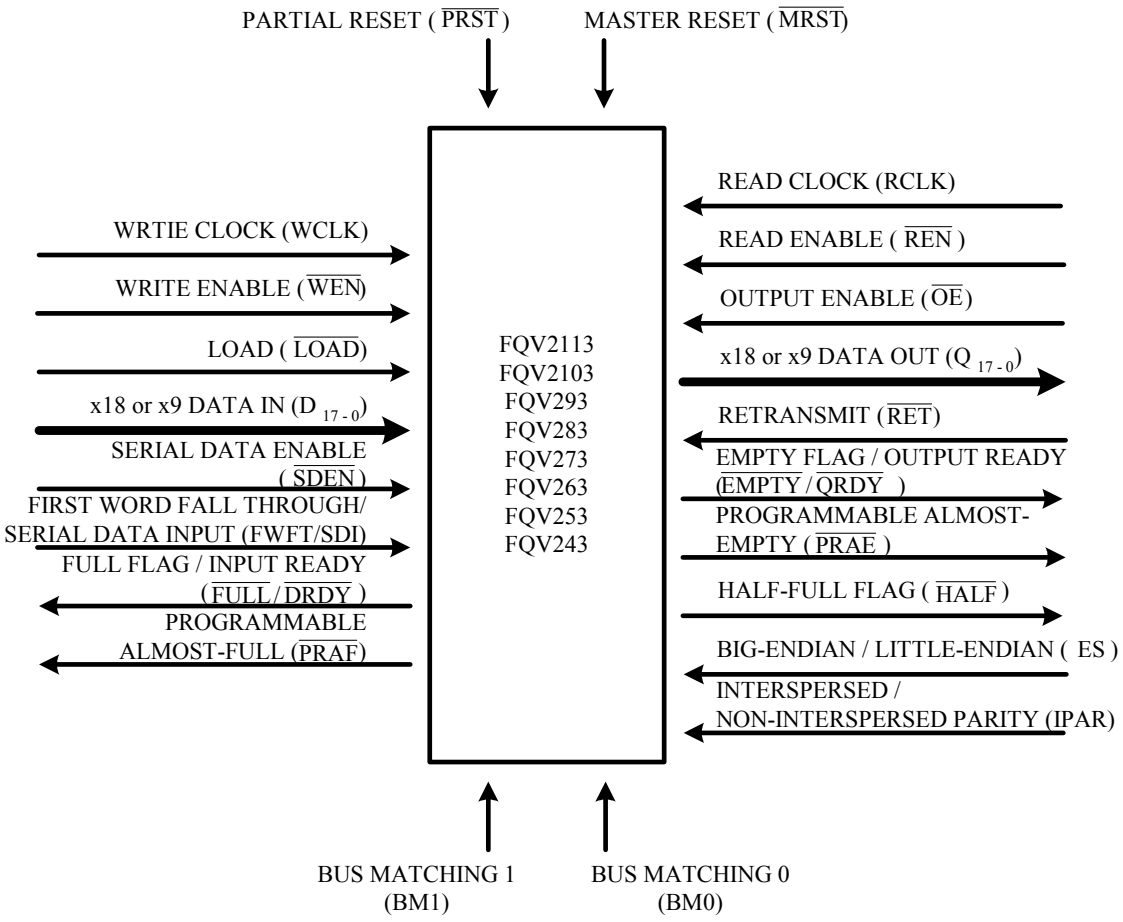


Figure 1. Single Device Configuration Signal Flow Diagram

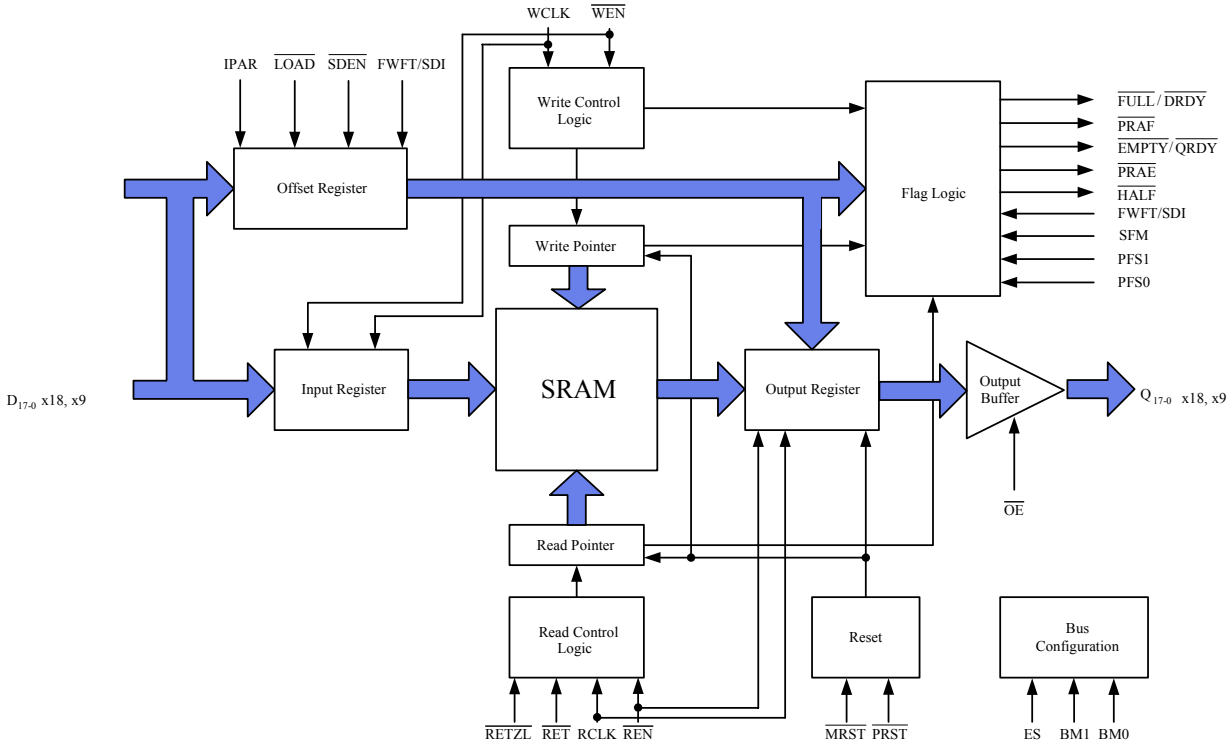
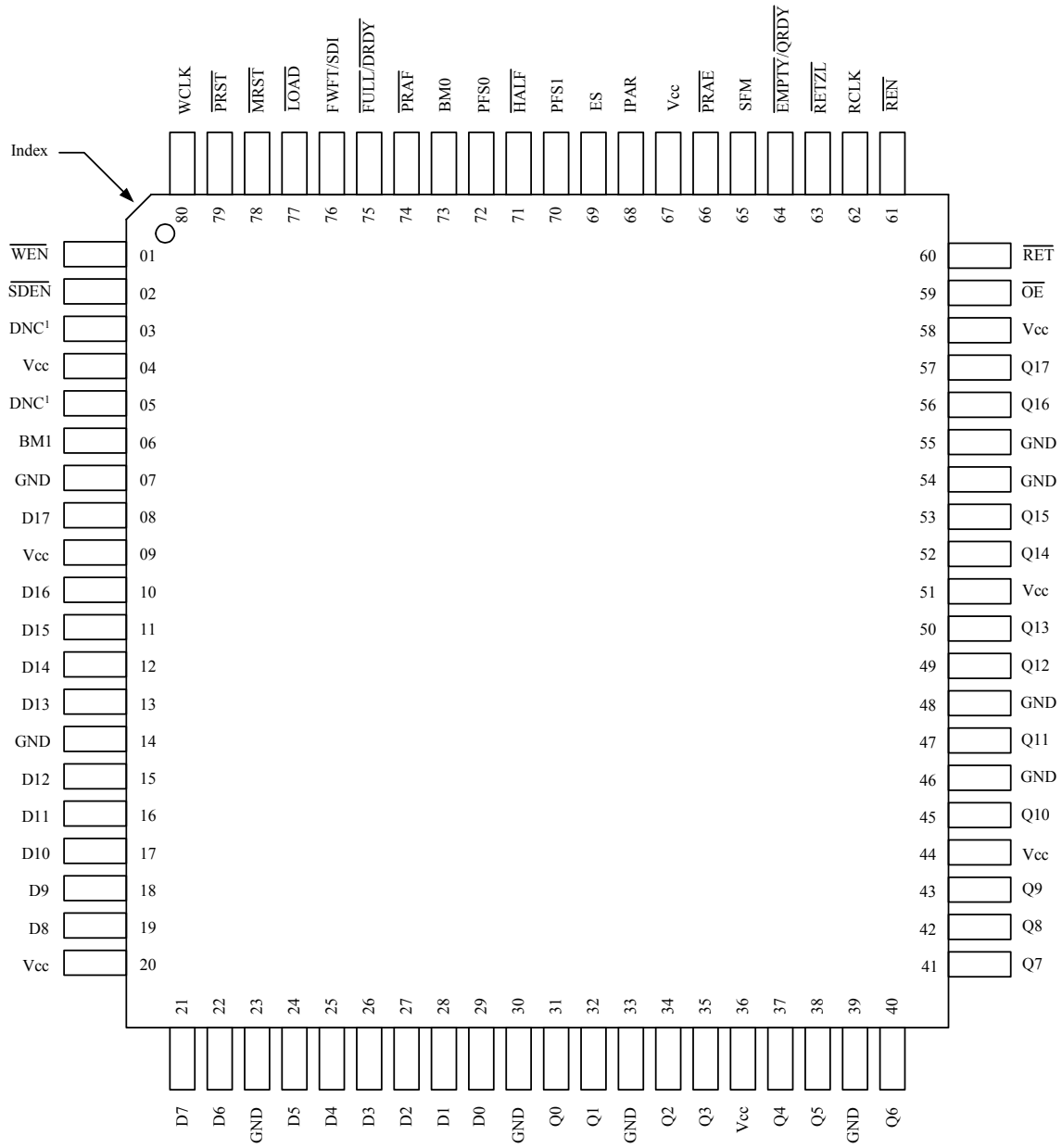


Figure 2. Device Architecture



TQFP - 80 (Drw No: PF-01A; Order code: PF)
Top View

NOTES:
1. DNC = Do Not Connect.

Figure 3. Device Pin Out

Pin #	Pin Name	Pin Symbol	Input/Output	Description
78	Master Reset	$\overline{MRST}$	Input	Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{MRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will not be maintained.
79	Partial Reset	$\overline{PRST}$	Input	Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{PRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will be maintained.
80	Write Clock	WCLK	Input	Writes data into queue during low to high transitions of WCLK if $\overline{WEN}$ is set to low.
01	Write Enable	$\overline{WEN}$	Input	Controls write operation into queue or offset registers during low to high transition of WCLK.
77	Load Enable	$\overline{LOAD}$	Input	During Master Reset, set $\overline{LOAD}$ low to select parallel programming and one of eight default-offset values. Set $\overline{LOAD}$ high to select serial programming and one of eight default offset values. After Master Reset, $\overline{LOAD}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively. Use in conjunction with $\overline{WEN}$ / $\overline{REN}$.
70	Default Programming 1	PFS1	Input	During Master Reset, select one of eight default-offset values. Use in conjunction with $\overline{LOAD}$ and PFS0.
72	Default Programming 0	PFS0	Input	During Master Reset, select one of eight default-offset values. Use in conjunction with $\overline{LOAD}$ and PFS1.
08,10,11, 12,13,15, 16,17,18 19,21,22, 24,25,26, 27,28,29	Data Inputs	D_{17-0}	Input	18 - bit wide input data bus.
62	Read Clock	RCLK	Input	Reads data from queue during low to high transitions of RCLK if $\overline{REN}$ is set to low.
61	Read Enable	$\overline{REN}$	Input	Controls read operation from queue or offset registers during low to high transition of RCLK.
59	Output Enable	$\overline{OE}$	Input	Setting $\overline{OE}$ low activates the data output drivers. Setting $\overline{OE}$ high deactivates the data output drivers (High-Z).

Table 1. Pin Descriptions

Pin #	Pin Name	Pin Symbol	Input/Output	Description
57,56,53, 52,50,49, 47,45,43, 42,41,40, 38,37,35, 34,32,31	Data Outputs	Q_{17-0}	Output	18 - bit wide output data bus.
76	First Word Fall Through/Serial Data Input	FWFT/SDI	Input	Selects FWFT timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{\text{LOAD}}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{\text{SDEN}}$.
02	Serial Data Input Enable	$\overline{\text{SDEN}}$	Input	If serial programming is selected, setting $\overline{\text{SDEN}}$ low and $\overline{\text{LOAD}}$ low enables serial data input to be written into offset registers during the low to high transition of WCLK.
06	Bus Matching 1	BM1	Input	During Master Reset, set BM1 low to select x18 input bus width or BM1 high to select x9 input bus width.
73	Bus Matching 0	BM0	Input	During Master Reset, set BM0 low to select x18 output bus width or BM0 high to select x9 output bus width.
69	Endian Select	ES	Input	During Master Reset, set ES high to select byte re-ordering on data outputs or ES low to select no byte re-ordering on data outputs.
60	Retransmit	$\overline{\text{RET}}$	Input	Data previously read from the queue can be retransmitted by asserting $\overline{\text{RET}}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue.
63	Zero Latency Retransmit	$\overline{\text{RETZL}}$	Input	During Master Reset, set $\overline{\text{RETZL}}$ low to select zero latency retransmit or $\overline{\text{RETZL}}$ high to select normal latency retransmit.
75	Full/Data Input Ready Flag	$\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$	Output	Queue is full when $\overline{\text{FULL}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue. In FWFT mode, queue is full when $\overline{\text{DRDY}}$ goes high during low to high transition of WCLK. This prohibits further writes into the queue.
64	Empty/Data Output Ready Flag	$\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$	Output	Queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue. In FWFT mode, queue is empty when $\overline{\text{QRDY}}$ goes high during the low to high transition of RCLK. This prohibits further reads from the queue.
68	Interspersed Parity	IPAR	Input	During Master Reset, set IPAR low to select 9-bit parallel programming mode or IPAR high to select 8-bit parallel programming mode.

Table 1. Pin Descriptions (Continued)

Pin #	Pin Name	Pin Symbol	Input/Output	Description
65	Synchronous Partial Flag Mode	SFM	Input	During Master Reset, set SFM high to select Synchronous Partial Flag mode or SFM low to select Asynchronous Partial Flag mode.
74	Almost Full	$\overline{\text{PRAF}}$	Output	Queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{\text{PRAF}}$.
66	Almost Empty	$\overline{\text{PRAE}}$	Output	Queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty +offset) or programmed offset values determine the status of $\overline{\text{PRAE}}$.
71	Half Full	$\overline{\text{HALF}}$	Output	Queue is more than half full when $\overline{\text{HALF}}$ goes low. Triggered by both WCLK and RCLK.
03, 05	Do Not Connect	DNC	N/A	Do not connect.
04,09,20 36,44,51, 58,67	Power	V_{CC}	N/A	3.3V power supply.
07,14,23, 30,33,39, 46,48,54,55,	Ground	GND	N/A	0V Ground.

Table 1. Pin Descriptions (Continued)

Symbol	Rating	Com'l & Ind'l	Unit
VTERM	Terminal Voltage with respect to GND	-0.5 to + 4.5	V
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	-50 to +50	mA

NOTES:
Absolute Max Ratings are for reference only. Permanent damage to the device may occur if extended period of operation is outside this range. Standard operation should fall within the Recommended Operating Conditions.

Table 2. Absolute Maximum Ratings

		FQV2113, FQV2103FQV293, FQV283 FQV273, FQV263, FQV253, FQV243						
		Commercial Clock = 6ns, 7.5ns, 10ns, 15ns			Industrial Clock = 7.5ns, 10ns, 15ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Recommended Operating Conditions								
Vcc	Supply Voltage Com'l / Ind'l	3.15	3.3	3.45	3.15	3.3	3.45	V
GND	Supply Voltage	0	0	0	0	0	0	V
VIH	Input High Voltage Com'l / Ind'l	2.0	-	5.5	2.0	-	5.5	V
VIL	Input Low Voltage Com'l / Ind'l	-	-	0.8	-	-	0.8	V
TA	Operating Temperature Commercial	0	-	70	0	-	70	°C
TA	Operating Temperature Industrial	-40	-	85	-40	-	85	°C
DC Electrical Characteristics								
ILI(1)	Input Leakage Current (any input)	-1	-	1	-1	-	1	µA
ILO	Output Leakage Current	-10	-	10	-10	-	10	µA
VOH	Output Logic "1" Voltage, IOH=-2mA	2.4	-	-	2.4	-	-	V
VOL	Output Logic "0" Voltage, IOL = 8mA	-	-	0.4	-	-	0.4	V
Power Consumption								
ICC1(2,3)	Active Power Supply Current (x9 Input to x9 Output)	-	-	30	-	-	30	mA
ICC1(2,3)	Active Power Supply Current (x18 Input to x18 Output)	-	-	35	-	-	35	mA
ICC2(4)	Standby Current	-	-	15	-	-	15	mA

Table 3. DC Specifications

Capacitance at 1.0MHz Ambient Temperature (25°C)				
Symbol	**Parameter**	**Conditions**	**Max.**	**Unit**
C_{IN}[2]	Input Capacitance	V_{IN}= 0V	10	pF
C_{OUT}[2,4]	Output Capacitance	V_{OUT}= 0V	10	pF

NOTES:
1. Measurement with 0.4<=V_{IN}<=Vcc.
2. With output tri-stated ($\overline{OE}$ = High).
3. Icc(1,2) is measured with WCLK and RCLK at 20 MHz.
4. Design simulated, not tested.

Table 3. DC Specifications (Continued)

Symbol	Parameter	Commercial		Commercial & Industrial						Unit
		FQV2113-6 FQV2103-6 FQV293-6 FQV283-6 FQV273-6 FQV263-6 FQV253-6 FQV243-6		FQV2113-7.5 FQV2103-7.5 FQV293-7.5 FQV283-7.5 FQV273-7.5 FQV263-7.5 FQV253-7.5 FQV243-7.5		FQV2113-10 FQV2103-10 FQV293-10 FQV283-10 FQV273-10 FQV263-10 FQV253-10 FQV243-10		FQV2113-15 FQV2103-15 FQV293-15 FQV283-15 FQV273-15 FQV263-15 FQV253-15 FQV243-15		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Cycle Frequency	-	166	-	133	-	100	-	66	MHz
t_A	Data Access Time	1	4	2	5	2	6.5	2	10	ns
t_{WCLK}	Write Clock Cycle Time	6	-	7.5	-	10	-	15	-	ns
t_{WCLKH}	Write Clock High Time	2.5	-	3.5	-	4.5	-	6	-	ns
t_{WCLKL}	Write Clock Low Time	2.5	-	3.5	-	4.5	-	6	-	ns
t_{RCLK}	Read Clock Cycle Time	6	-	7.5	-	10	-	15	-	ns
t_{RCLKH}	Read Clock High Time	2.5	-	3.5	-	4.5	-	6	-	ns
t_{RCLKL}	Read Clock Low Time	2.5	-	3.5	-	4.5	-	6	-	ns
t_{DS}	Data Set-up Time	2.0	-	2.5	-	3.5	-	4	-	ns
t_{DH}	Data Hold Time	0.5	-	0.5	-	0.5	-	1	-	ns
t_{ENS}	Enable Set-up Time	2.0	-	2.5	-	3.5	-	4	-	ns
t_{ENH}	Enable Hold Time	0.5	-	0.5	-	0.5	-	1	-	ns
t_{RST}	Reset Pulse Width[1]	8	-	10	-	10	-	15	-	ns
t_{RSTS}	Reset Set-up Time	10	-	15		15	-	15	-	ns
t_{RSTR}	Reset Recovery Time	10	-	10	-	10	-	15	-	ns
t_{RSTF}	Reset to Flag and Output Time	-	10	-	15	-	15	-	15	ns
t_{OLZ}	Output Enable to Output in Low-Z[1]	0	-	0	-	0	-	0	-	ns
t_{OE}	Output Enable to Output Valid	2	4	2	6	2	6	2	8	ns
t_{OHZ}	Output Enable to Output in High-Z[1]	2	4	2	6	2	6	2	8	ns
t_{FULL}	Write Clock to Full Flag	-	4	-	5	-	6.5	-	10	ns
t_{EMPTY}	Read Clock to Empty Flag	-	4	-	5	-	6.5	-	10	ns
t_{PRAFS}	Write Clock to Synchronous Almost-Full Flag	-	4	-	5	-	6.5	-	10	ns
t_{PRAES}	Read Clock to Synchronous Almost-Empty Flag	-	4	-	5	-	6.5	-	10	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Full Flag / Empty Flag	4	-	5	-	7	-	9	-	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for $\overline{PRAE}$ & $\overline{PRAF}$	6	-	7	-	10	-	14	-	ns
t_{LOADS}	Load Setup Time	2	-	2.5	-	3.5	-	4	-	ns
t_{LOADH}	Load Hold Time	0.5	-	0.5	-	0.5	-	1	-	ns

Table 4. AC Electrical Characteristics

Symbol	Parameter	Commercial		Commercial & Industrial						Unit
		FQV2113-6 FQV2103-6 FQV293-6 FQV283-6 FQV273-6 FQV263-6 FQV253-6 FQV243-6		FQV2113-7.5 FQV2103-7.5 FQV293-7.5 FQV283-7.5 FQV273-7.5 FQV263-7.5 FQV253-7.5 FQV243-7.5		FQV2113-10 FQV2103-10 FQV293-10 FQV283-10 FQV273-10 FQV263-10 FQV253-10 FQV243-10		FQV2113-15 FQV2103-15 FQV293-15 FQV283-15 FQV273-15 FQV263-15 FQV253-15 FQV243-15		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RETS}	Retransmit Setup Time	3	-	3.5	-	3.5	-	4	-	ns
t_{HALF}	Clock to $\overline{HALF}$	-	12	-	12.5	-	16	-	20	ns
t_{PRAFA}	Write Clock to Asynchronous Programmable Almost-Full Flag	-	12	-	12.5	-	16	-	20	ns
t_{PRAEA}	Read Clock to Asynchronous Programmable Almost-Empty Flag	-	12	-	12.5	-	16	-	20	ns

NOTES:
1. Design simulated, not tested.

Table 4. AC Electrical Characteristics (Continued)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load, clock = 6ns, 7.5ns	Refer to Figure 4 & 6
Output Load*, clock = 10ns, 15 ns	Refer to Figure 5

* Include jig and scope capacitances

Table 5. AC Test Condition

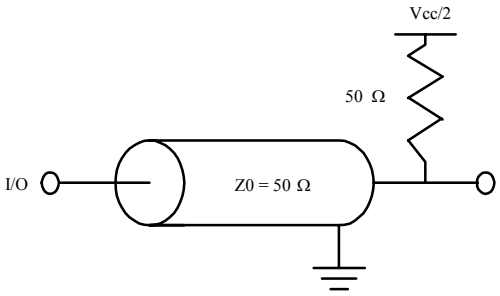


Figure 4. AC Test Load
for clock = 6ns, 7.5ns

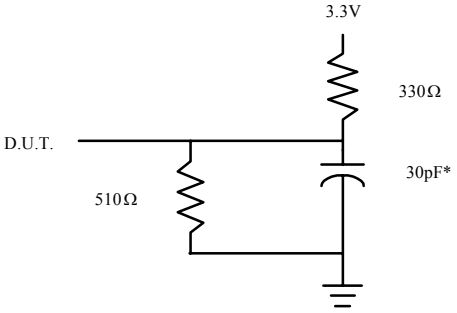


Figure 5. Output Load
for clock = 10ns, 15ns
*Includes jig and scope capacitances.

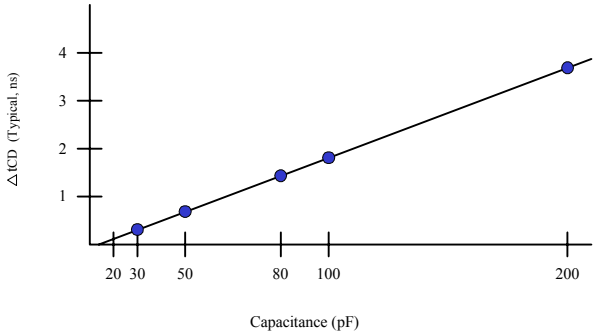


Figure 6. Lumped Capacitive Load

Pin Functions

$\overline{\text{MRST}}$ Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{MRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will not be maintained.

$\overline{\text{PRST}}$ Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{PRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will be maintained.

WCLK Writes data into queue during low to high transitions of WCLK if $\overline{\text{WEN}}$ is activated. Synchronizes $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ and $\overline{\text{PRAF}}$ flags. WCLK and RCLK are independent of each other.

$\overline{\text{WEN}}$ Controls write operation into queue or offset registers during low to high transition of WCLK.

$\overline{\text{LOAD}}$ During Master Reset, set $\overline{\text{LOAD}}$ low to select parallel programming and one of eight default offset values. Set $\overline{\text{LOAD}}$ high to select serial programming and one of eight default offset values. After Master Reset, $\overline{\text{LOAD}}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively for parallel programming. Use in conjunction with $\overline{\text{WEN}}$ / $\overline{\text{REN}}$. During programming of offset registers, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flag status are invalid. For Serial programming, $\overline{\text{LOAD}}$ is used to enable serial loading of offset registers together with $\overline{\text{SDEN}}$. Refer to Figure 7 & Table 11 for details.

PFS1 During Master Reset, select one of eight default-offset values. Use in conjunction with $\overline{\text{LOAD}}$ and PFS0. Refer to Table 11 for details.

PFS0 During Master Reset, select one of eight default-offset values. Use in conjunction with $\overline{\text{LOAD}}$ and PFS1. Refer to Table 11 for details.

D_{17-0} 18 - bit wide input data bus.

RCLK Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN}}$ is set low. Synchronizes the $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ and $\overline{\text{PRAE}}$ flags. RCLK and WCLK are independent of each other.

$\overline{\text{REN}}$ Reads data from queue or offset registers during low to high transitions of RCLK if $\overline{\text{REN}}$ is set low. This also advances the Read pointer of the queue.

$\overline{\text{OE}}$ Setting $\overline{\text{OE}}$ low activates the data output drivers. Setting $\overline{\text{OE}}$ high deactivates the data output drivers (High-Z). $\overline{\text{OE}}$ does not control advancement of Read pointer.

Q_{17-0} 18 - bit wide output data bus.

FWFT/SDI Selects FWFT timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{\text{LOAD}}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{\text{SDEN}}$. In FWFT mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ is used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$. Refer to Table 9 for all flags status. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ are used instead of $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$. Refer to Table 8 for all flags status.

$\overline{\text{SDEN}}$ If serial programming is selected, setting $\overline{\text{SDEN}}$ low and $\overline{\text{LOAD}}$ low enables serial data to be written into offset registers during the low to high transition of WCLK. During serial programming, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flags status are invalid. Refer to Figure 7 for details.

Pin Functions (Continued)

BM1 — During Master Reset, setting BM1 low selects x18 input bus width. Set BM1 high selects x9 input bus width. Refer to Table 10 for details.

BM0 — During Master Reset, set BM0 low to select x18 output bus width. Set BM0 high to select x9 output bus width. Refer to Table 10 for details.

ES — During Master Reset, Set ES high to select byte re-ordering on data outputs or set ES low to select no byte re-ordering on data outputs. ES must be static throughout device operation. Refer to Table 10 for details.

$\overline{\text{RET}}$ — Data previously read from the queue can be retransmitted by asserting $\overline{\text{RET}}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero), location of the queue. Refer to Diagram 7 & 8 for details.

$\overline{\text{RETZL}}$ — During Master Reset, set $\overline{\text{RETZL}}$ low to select zero latency retransmit or set $\overline{\text{RETZL}}$ high to select normal latency retransmit.

$\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ — In Standard mode, queue is full when $\overline{\text{FULL}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. In FWFT mode, queue is full when $\overline{\text{DRDY}}$ goes high during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. Refer to Table 8 & 9 for behavior of $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$.

$\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ — In Standard mode, queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. In FWFT mode, queue is empty when $\overline{\text{QRDY}}$ goes high during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. Refer to Table 8 & 9 for behavior of $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$.

IPAR — During Master Reset, set IPAR low to select 9-bit parallel programming mode or set IPAR high to select 8-bit parallel programming mode. In 9-bit mode, 9-bit wide data input/output bus width is used for storing/fetching offset values. In 8-bit mode, 8-bit wide data input/output bus is used for storing/fetching offset values.

SFM — During Master Reset, set SFM high to select Synchronous Partial Flag mode or set SFM low to select Asynchronous Partial Flag mode. In Synchronous mode, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ are synchronous to WCLK and RCLK respectively. In Asynchronous mode, WCLK synchronizes the assertion of $\overline{\text{PRAF}}$ and de-assertion of $\overline{\text{PRAE}}$. RCLK synchronizes the assertion of $\overline{\text{PRAE}}$ and de-assertion of $\overline{\text{PRAF}}$.

$\overline{\text{PRAF}}$ — In Synchronous mode, queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{\text{PRAF}}$. In Asynchronous mode, $\overline{\text{PRAF}}$ is triggered by both WCLK and RCLK. Refer to Table 8 & 9 for behavior of $\overline{\text{PRAF}}$.

$\overline{\text{PRAE}}$ — In Synchronous mode, queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty+offset) or programmed offset values determine the status of $\overline{\text{PRAE}}$. In Asynchronous timing mode, $\overline{\text{PRAE}}$ is triggered by both WCLK and RCLK. Refer to Table 8 & 9 for behavior of $\overline{\text{PRAE}}$.

$\overline{\text{HALF}}$ — Queue is more than half full when $\overline{\text{HALF}}$ goes low during the low to high transition of WCLK. $\overline{\text{HALF}}$ goes high during low to high transition of RCLK when queue is less than half full. Refer to Table 8 & 9 for details.

$\overline{\text{LOAD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	$\overline{\text{SDEN}}$	WCLK	RCLK	FQV283 FQV273 FQV263 FQV253 FQV243 Selection / Sequence
0	0	1	1	↑	X	Parallel write to offset registers: Empty Offset (Low Byte) Empty Offset (High Byte) Full Offset (Low Byte) Full Offset (High Byte) Parallel write to registers: 1. $\overline{\text{PRAE}}$ Low Byte 2. $\overline{\text{PRAE}}$ High Byte 3. $\overline{\text{PRAF}}$ Low Byte 4. $\overline{\text{PRAF}}$ High Byte
0	1	0	1	X	↑	Parallel read from offset registers: Empty Offset (Low Byte) Empty Offset (High Byte) Full Offset (Low Byte) Full Offset (High Byte) Parallel read from registers: 1. $\overline{\text{PRAE}}$ Low Byte 2. $\overline{\text{PRAE}}$ High Byte 3. $\overline{\text{PRAF}}$ Low Byte 4. $\overline{\text{PRAF}}$ High Byte
0	1	1	0	↑	X	**x9 to x9 Mode** Serial shift into registers: 32 bits for the FQV283 30 bits for the FQV273 28 bits for the FQV263 26 bits for the FQV253 24 bits for the FQV243 1 bit for each rising WCLK edge Starting with Empty Offset (Low Byte) Ending with Full Offset (High Byte) **All Other Modes** Serial shift into registers: 30 bits for the FQV283 28 bits for the FQV273 26 bits for the FQV263 24 bits for the FQV253 22 bits for the FQV243 1 bit for each rising WCLK edge Starting with Empty Offset (Low Byte) Ending with Full Offset (High Byte)
X	1	1	1	X	X	No Operation
1	0	X	X	↑	X	Write Memory
1	X	0	X	X	↑	Read Memory
1	1	1	X	X	X	No Operation

Figure 7. Programmable Flag Offset Programming Sequence (FQV283, FQV273, FQV263, FQV253 and FQV243)

$\overline{\text{LOAD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	$\overline{\text{SDEN}}$	WCLK	RCLK	FQV2113 FQV2103 FQV293 Selection / Sequence
0	0	1	1	↑	X	Parallel write to offset registers: Empty Offset (Low Byte) Empty Offset (Mid Byte) Empty Offset (High Byte) Full Offset (Low Byte) Full Offset (Mid Byte) Full Offset (High Byte) Parallel write to registers: 1. $\overline{\text{PRAE}}$ Low Byte 2. $\overline{\text{PRAE}}$ Mid Byte 3. $\overline{\text{PRAE}}$ High Byte 4. $\overline{\text{PRAF}}$ Low Byte 5. $\overline{\text{PRAF}}$ Mid Byte 6. $\overline{\text{PRAF}}$ High Byte
0	1	0	1	X	↑	Parallel read from offset registers: Empty Offset (Low Byte) Empty Offset (Mid Byte) Empty Offset (High Byte) Full Offset (Low Byte) Full Offset (Mid Byte) Full Offset (High Byte) Parallel read from registers: 1. $\overline{\text{PRAE}}$ Low Byte 2. $\overline{\text{PRAE}}$ Mid Byte 3. $\overline{\text{PRAE}}$ High Byte 4. $\overline{\text{PRAF}}$ Low Byte 5. $\overline{\text{PRAF}}$ Mid Byte 6. $\overline{\text{PRAF}}$ High Byte
0	1	1	0	↑	X	**x9 to x9 Mode** Serial shift into registers: 38 bits for the FQV2113 36 bits for the FQV2103 34 bits for the FQV293 1 bit for each rising WCLK edge Starting with Empty Offset (Low Byte) Ending with Full Offset (High Byte) **All Other Modes** Serial shift into registers: 36 bits for the FQV2113 34 bits for the FQV2103 32 bits for the FQV293 1 bit for each rising WCLK edge Starting with Empty Offset (Low Byte) Ending with Full Offset (High Byte)
X	1	1	1	X	X	No Operation
1	0	X	X	↑	X	Write Memory
1	X	0	X	X	↑	Read Memory
1	1	1	X	X	X	No Operation

Figure 8. Programmable Flag Offset Programming Sequence (FQV2113, FQV2103, FQV293)

Device	$\overline{\text{PRAF}}$ Programming (bits)		$\overline{\text{PRAE}}$ Programming (bits)	
FQV2113	D/Q_{15-0}	Non-IPAR	D/Q_{15-0}	Non-IPAR
	D/Q_{16-9} & D/Q_{7-0}	IPAR	D/Q_{16-9} & D/Q_{7-0}	IPAR
FQV2103	D/Q_{15-0}	Non-IPAR	D/Q_{15-0}	Non-IPAR
	D/Q_{16-9} & D/Q_{7-0}	IPAR	D/Q_{16-9} & D/Q_{7-0}	IPAR
FQV293	D/Q_{15-0}	Non-IPAR	D/Q_{15-0}	Non-IPAR
	D/Q_{16-9} & D/Q_{7-0}	IPAR	D/Q_{16-9} & D/Q_{7-0}	IPAR
FQV283	D/Q_{14-0}	Non-IPAR	D/Q_{14-0}	Non-IPAR
	D/Q_{15-9} & D/Q_{7-0}	IPAR	D/Q_{15-9} & D/Q_{7-0}	IPAR
FQV273	D/Q_{13-0}	Non-IPAR	D/Q_{13-0}	Non-IPAR
	D/Q_{14-9} & D/Q_{7-0}	IPAR	D/Q_{14-9} & D/Q_{7-0}	IPAR
FQV263	D/Q_{12-0}	Non-IPAR	D/Q_{12-0}	Non-IPAR
	D/Q_{13-9} & D/Q_{7-0}	IPAR	D/Q_{13-9} & D/Q_{7-0}	IPAR
FQV253	D/Q_{11-0}	Non-IPAR	D/Q_{11-0}	Non-IPAR
	D/Q_{12-9} & D/Q_{7-0}	IPAR	D/Q_{12-9} & D/Q_{7-0}	IPAR
FQV243	D/Q_{10-0}	Non-IPAR	D/Q_{10-0}	Non-IPAR
	D/Q_{11-9} & D/Q_{7-0}	IPAR	D/Q_{11-9} & D/Q_{7-0}	IPAR

Condition Applies to: Write Cycle with x18 input Bus Width and/or Read Cycle with x18 output Bus Width

Device	$\overline{\text{PRAF}}$ Programming (bits)		$\overline{\text{PRAE}}$ Programming (bits)	
FQV2113	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{7-0}	Mid Byte	D/Q_{7-0}	Mid Byte
	D/Q_{1-0}	High Byte	D/Q_{1-0}	High Byte
FQV2103	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{7-0}	Mid Byte	D/Q_{7-0}	Mid Byte
	D/Q_{0}	High Byte	D/Q_{0}	High Byte
FQV293	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{7-0}	High Byte	D/Q_{7-0}	High Byte
FQV283	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{6-0}	High Byte	D/Q_{6-0}	High Byte
FQV273	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{5-0}	High Byte	D/Q_{5-0}	High Byte
FQV263	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{4-0}	High Byte	D/Q_{4-0}	High Byte
FQV253	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{3-0}	High Byte	D/Q_{3-0}	High Byte
FQV243	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{2-0}	High Byte	D/Q_{2-0}	High Byte

Condition Applies to: Write Cycle with x9 input Bus Width or Read Cycle with x9 output Bus Width (except x9 to x9 mode)

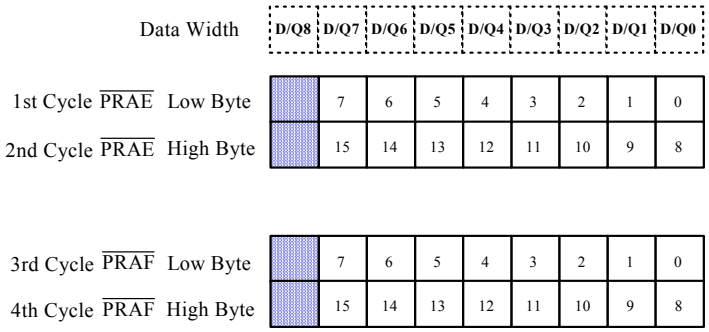
Device	$\overline{PRAF}$ Programming (bits)		$\overline{PRAE}$ Programming (bits)	
FQV2113	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{7-0}	Mid Byte	D/Q_{7-0}	Mid Byte
	D/Q_{2-0}	High Byte	D/Q_{2-0}	High Byte
FQV2103	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{7-0}	Mid Byte	D/Q_{7-0}	Mid Byte
	D/Q_{1-0}	High Byte	D/Q_{1-0}	High Byte
FQV293	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{7-0}	Mid Byte	D/Q_{7-0}	Mid Byte
	D/Q_{0}	High Byte	D/Q_{0}	High Byte
FQV283	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{7-0}	High Byte	D/Q_{7-0}	High Byte
FQV273	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{6-0}	High Byte	D/Q_{6-0}	High Byte
FQV263	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{5-0}	High Byte	D/Q_{5-0}	High Byte
FQV253	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{4-0}	High Byte	D/Q_{4-0}	High Byte
FQV243	D/Q_{7-0}	Low Byte	D/Q_{7-0}	Low Byte
	D/Q_{3-0}	High Byte	D/Q_{3-0}	High Byte

Condition Applies to: Write Cycle with x9 input Bus Width and
Read Cycle with x9 output Bus Width (only x9 to x9 mode)

Table 6. Parallel Offset Write/Read Cycle Register Location

Device	Standard Mode	FWFT Mode
FQV2113	262,144 x 18 / 524,288 x9	262,145 x 18 / 524,289 x9
FQV2103	131,072 x 18 / 262,144 x9	131,073 x 18 / 262,145 x 9
FQV293	65,536 x 18 / 131,072 x 9	65,537,x 18 / 131,073 x 9
FQV283	32,768 x 18 / 65,536 x 9	32,769 x 18 / 65,537 x 9
FQV273	16,384 x 18 / 32,768 x 9	16,385 x 18 / 32,769 x 9
FQV263	8,192 x 18 / 16,384 x 9	8,193 x 18 / 16,385 x 9
FQV253	4,096 x 18 / 8,192 x 9	4,097 x 18 / 8,193 x 9
FQV243	2,048 x 18 / 4,096 x 9	2,049 x 18 / 4,097 x 9

Table 7. Maximum Depth of Queue for Standard and FWFT Mode

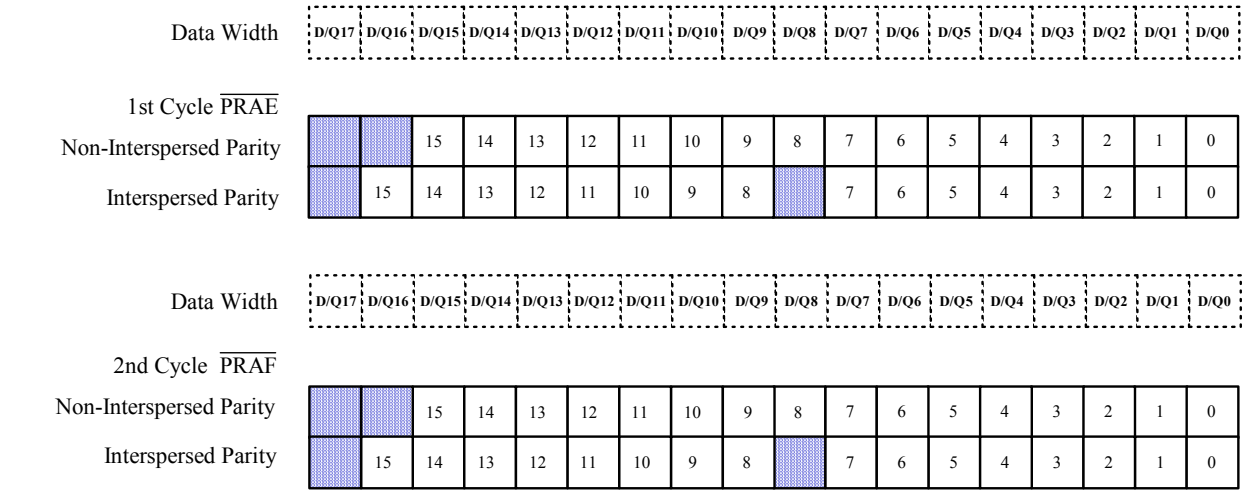


FQV293, FQV283, FQV273, FQV263, FQV253, FQV243
Parallel Offset Write/Read Cycles for x9 Bus Width
Condtion Applies to: Write Cycle with x9 input Bus Width and/or Read Cycle output with x9 Bus Width (except FQV293 x9 to x9 mode)

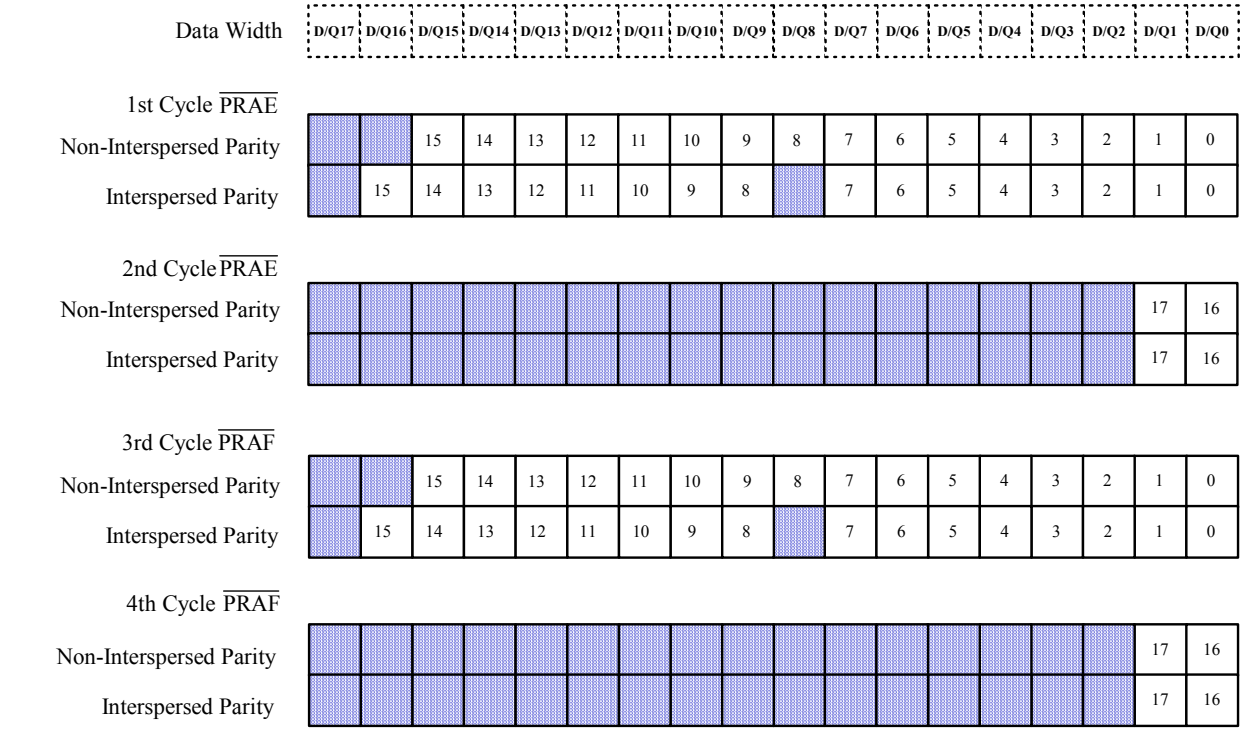
FQV2113, FQV2103, FQV293
Parallel Offset Write/Read Cycles for x9 Bus Width
Condtion Applies to: FQV293 x9 to x9 mode or FQV2113, FQV2103 for all modes

x9 to x9 Mode	All Other Modes
# of Bits for Offset Registers	**# of Bits for Offset Registers**
19 bits for FQV2113 18 bits for FQV2103 17 bits for FQV293 16 bits for FQV283 15 bits for FQV273 14 bits for FQV263 13 bits for FQV253 12 bits for FQV243	18 bits for FQV2113 17 bits for FQV2103 16 bits for FQV293 15 bits for FQV283 14 bits for FQV273 13 bits for FQV263 12 bits for FQV253 11 bits for FQV243
Note: Don't Care applies to all unused bits	**Note: Don't Care applies to all unused bits**

Figure 9. Parallel Offset Write/Read Cycle Diagram



FQV293, FQV283, FQV273, FQV263, FQV253, FQV243
Parallel Offset Write/Read Cycles for x18 Bus Width
Condtion Applies to: Write Cycle with x18 input Bus Width
and/or Read Cycle for x18 output Bus Width



FQV2113, FQV2103
Parallel Offset Write/Read Cycles for x18 Bus Width
Condtion Applies to: Write Cycle with x18 input Bus Width
and/or Read Cycle for x18 output Bus Width

Figure 9. Parallel Offset Write/Read Cycles Diagram (Continued)

FQV2113					
BM1 = BM0 = x9	**$\overline{FULL}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{EMPTY}$**
0	H	H	H	L	L
1 to y[1]	H	H	H	L	H
(y+1) to 262,144	H	H	H	H	H
262,145 to [524,288-(x+1)]	H	H	L	H	H
(524,288 -x[1]) to 524,287	H	L	L	H	H
524,288	L	L	L	H	H

FQV2103	FQV2113					
BM1 = BM0 = x9	**BM1 ≠ BM0 or BM1 = BM0 = x18**	**$\overline{FULL}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{EMPTY}$**
0		H	H	H	L	L
1 to y		H	H	H	L	H
(y+1) to 131,072		H	H	H	H	H
131,073 to [262,144-(x+1)]		H	H	L	H	H
(262,144 -x) to 262,143		H	L	L	H	H
262,144		L	L	L	H	H

FQV293	FQV2103					
BM1 = BM0 = x9	**BM1 ≠ BM0 or BM1 = BM0 = x18**	**$\overline{FULL}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{EMPTY}$**
0		H	H	H	L	L
1 to y		H	H	H	L	H
(y+1) to 65,536		H	H	H	H	H
65,537 to [131,072-(x+1)]		H	H	L	H	H
(131,072 -x) to 131,071		H	L	L	H	H
131,072		L	L	L	H	H

FQV283	FQV293					
BM1 = BM0 = x9	**BM1 ≠ BM0 or BM1 = BM0 = x18**	**$\overline{FULL}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{EMPTY}$**
0		H	H	H	L	L
1 to y		H	H	H	L	H
(y+1) to 32,768		H	H	H	H	H
32,769 to [65,536-(x+1)]		H	H	L	H	H
(65,536 -x) to 65,535		H	L	L	H	H
65,536		L	L	L	H	H

FQV273	FQV283					
BM1 = BM0 = x9	**BM1 ≠ BM0 or BM1 = BM0 = x18**	**$\overline{FULL}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{EMPTY}$**
0		H	H	H	L	L
1 to y		H	H	H	L	H
(y+1) to 16,384		H	H	H	H	H
16,385 to [32,768-(x+1)]		H	H	L	H	H
(32,768 -x) to 32,767		H	L	L	H	H
32,768		L	L	L	H	H

NOTES:
1. See Table 11 for values x, y.

Table 8. Status Flags (Standard Mode)

FQV263	FQV273					
BM1 = BM0 = x9	BM1 ≠ BM0 or BM1 = BM0 = x18	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0		H	H	H	L	L
1 to y		H	H	H	L	H
(y+1) to 8,192		H	H	H	H	H
8,193 to [16,384-(x+1)]		H	H	L	H	H
(16,384 –x) to 16,383		H	L	L	H	H
16,384		L	L	L	H	H

FQV253	FQV263					
BM1 = BM0 = x9	BM1 ≠ BM0 or BM1 = BM0 = x18	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0		H	H	H	L	L
1 to y		H	H	H	L	H
(y+1) to 4,096		H	H	H	H	H
4,097 to [8,192-(x+1)]		H	H	L	H	H
(8,192 –x) to 8,191		H	L	L	H	H
8,192		L	L	L	H	H

FQV243	FQV253					
BM1 = BM0 = x9	BM1 ≠ BM0 or BM1 = BM0 = x18	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0		H	H	H	L	L
1 to y		H	H	H	L	H
(y+1) to 2,048		H	H	H	H	H
2,049 to [4,096-(x+1)]		H	H	L	H	H
(4,096 –x) to 4,095		H	L	L	H	H
4,096		L	L	L	H	H

FQV243					
BM1 ≠ BM0 or BM1 = BM0 = x18	$\overline{FULL}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{EMPTY}$
0	H	H	H	L	L
1 to y	H	H	H	L	H
(y+1) to 1,024	H	H	H	H	H
1,025 to [2,048-(x+1)]	H	H	L	H	H
(2,048–x) to 2,047	H	L	L	H	H
2,048	L	L	L	H	H

NOTES:
1. See Table 11 for values x, y.

Table 8. Status Flags (Standard Mode) (Continued)

FQV2113					
BM1 = BM0 = x9	**$\overline{DRDY}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{QRDY}$**
0	L	H	H	L	H
1 to y+1[(1)]	L	H	H	L	L
(y+2) to 262,145	L	H	H	H	L
262,146 to [524,289-(x+1)]	L	H	L	H	L
(524,289-x[(1)]) to 524,288	L	L	L	H	L
524,289	H	L	L	H	L

FQV2103	FQV2113					
BM1 = BM0 = x9	**BM1 ≠ BM0 or BM1 = BM0 = x18**	**$\overline{DRDY}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{QRDY}$**
0		L	H	H	L	H
1 to y+1		L	H	H	L	L
(y+2) to 131,073		L	H	H	H	L
131,074 to [262,145-(x+1)]		L	H	L	H	L
(262,145-x) to 262,144		L	L	L	H	L
262,145		H	L	L	H	L

FQV293	FQV2103					
BM1 = BM0 = x9	**BM1 ≠ BM0 or BM1 = BM0 = x18**	**$\overline{DRDY}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{QRDY}$**
0		L	H	H	L	H
1 to y+1		L	H	H	L	L
(y+2) to 65,537		L	H	H	H	L
65,538 to [131,073-(x+1)]		L	H	L	H	L
(131,073-x) to 131,072		L	L	L	H	L
131,073		H	L	L	H	L

FQV283	FQV293					
BM1 = BM0 = x9	**BM1 ≠ BM0 or BM1 = BM0 = x18**	**$\overline{DRDY}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{QRDY}$**
0		L	H	H	L	H
1 to y+1		L	H	H	L	L
(y+2) to 32,769		L	H	H	H	L
32,770 to [65,537-(x+1)]		L	H	L	H	L
(65,537 -x) to 65,536		L	L	L	H	L
65,537		H	L	L	H	L

FQV273	FQV283					
BM1 = BM0 = x9	**BM1 ≠ BM0 or BM1 = BM0 = x18**	**$\overline{DRDY}$**	**$\overline{PRAF}$**	**$\overline{HALF}$**	**$\overline{PRAE}$**	**$\overline{QRDY}$**
0		L	H	H	L	H
1 to y+1		L	H	H	L	L
(y+2) to 16,385		L	H	H	H	L
16,386 to [32,769-(x+1)]		L	H	L	H	L
(32,769-x) to 32,768		L	L	L	H	L
32,769		H	L	L	H	L

NOTES:
1. See Table 11 for values x, y.

Table 9. Status Flags (FWFT Mode)

FQV263	FQV273					
BM1 = BM0 = x9	BM1 ≠ BM0 or BM1 = BM0 = x18	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0		L	H	H	L	H
1 to y+1		L	H	H	L	L
(y+2) to 8,193		L	H	H	H	L
8,194 to [16,385-(x+1)]		L	H	L	H	L
(16,385 -x) to 16,384		L	L	L	H	L
16,385		H	L	L	H	L

FQV253	FQV263					
BM1 = BM0 = x9	BM1 ≠ BM0 or BM1 = BM0 = x18	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0		L	H	H	L	H
1 to y+1		L	H	H	L	L
(y+2) to 4,097		L	H	H	H	L
4,098 to [8,193-(x+1)]		L	H	L	H	L
(8,193 -x) to 8,192		L	L	L	H	L
8,193		H	L	L	H	L

FQV243	FQV253					
BM1 = BM0 = x9	BM1 ≠ BM0 or BM1 = BM0 = x18	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0		L	H	H	L	H
1 to y+1		L	H	H	L	L
(y+2) to 2,049		L	H	H	H	L
2,050 to [4,097-(x+1)]		L	H	L	H	L
(4,097-x) to 4,096		L	L	L	H	L
4,097		H	L	L	H	L

FQV243						
BM1 ≠ BM0 or BM1 = BM0 = x18		$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0		L	H	H	L	H
1 to y+1		L	H	H	L	L
(y+2) to 1,025		L	H	H	H	L
1,026 to [2,049 -(x+1)]		L	H	L	H	L
(2,049 -x) to 2,048		L	L	L	H	L
2,049		H	L	L	H	L

NOTES:
1. See Table 11 for values x, y.

Table 9. Status Flags (FWFT Mode) (Continued)

ES	BM1	BM0	I/O	Width	D/Q_{17-9}	D/Q_{8-0}	Sequence
0	0	0	I	18	Byte 2	Byte 1	1st Write
			O	18	Byte 2	Byte 1	1st Read
0	0	1	I	18	Byte 2	Byte 1	1st Write
			O	9	X	Byte 2	1st Read
					X	Byte 1	2nd Read
0	1	0	I	9	X	Byte 2	1st Write
					X	Byte 1	2nd Write
			O	18	Byte 2	Byte 1	1st Read
X	1	1	I	9	X	Byte 2	1st Write
					X	Byte 1	2nd Write
			O	9	X	Byte 2	1st Read
					X	Byte 1	2nd Read
1	0	0	I	18	Byte 2	Byte 1	1st Write
			O	18	Byte 1	Byte 2	1st Read
1	0	1	I	18	Byte 2	Byte 1	1st Write
			O	9	X	Byte 1	1st Read
					X	Byte 2	2nd Read
1	1	0	I	9	X	Byte 2	1st Write
					X	Byte 1	2nd Read
			O	18	Byte 1	Byte 2	1st Read

Table 10. Bus-Matching Table

$\overline{\text{LOAD}}$	PFS0	PFS1	FQV243 Offsets x, y		FQV273 FQV263 FQV253
			All Other Modes	x9 to x9 Mode	Offsets x, y
0	0	0	127	127	127
0	0	1	511	511	511
0	1	0	255	255	255
0	1	1	63	63	63
1	0	0	31	1,023	1,023
1	0	1	15	31	31
1	1	0	7	15	15
1	1	1	3	7	7
1	X	X	Serial		
0	X	X	Parallel		

$\overline{\text{LOAD}}$	PFS0	PFS1	FQV283 Offsets x, y		FQV2113 FQV2103 FQV293
			All Other Modes	x9 to x9 Mode	Offsets x, y
0	0	0	127	127	127
0	0	1	511	16,383	16,383
0	1	0	255	8,191	8,191
0	1	1	63	4,095	4,095
1	0	0	1,023	1,023	1,023
1	0	1	31	2,047	2,047
1	1	0	15	511	511
1	1	1	7	255	255
1	X	X	Serial		
0	X	X	Parallel		

NOTES:
1. x = $\overline{\text{PRAF}}$ offset, y = $\overline{\text{PRAE}}$ offset.

Table 11. Default Programmable Flag Offsets

Timing Diagrams

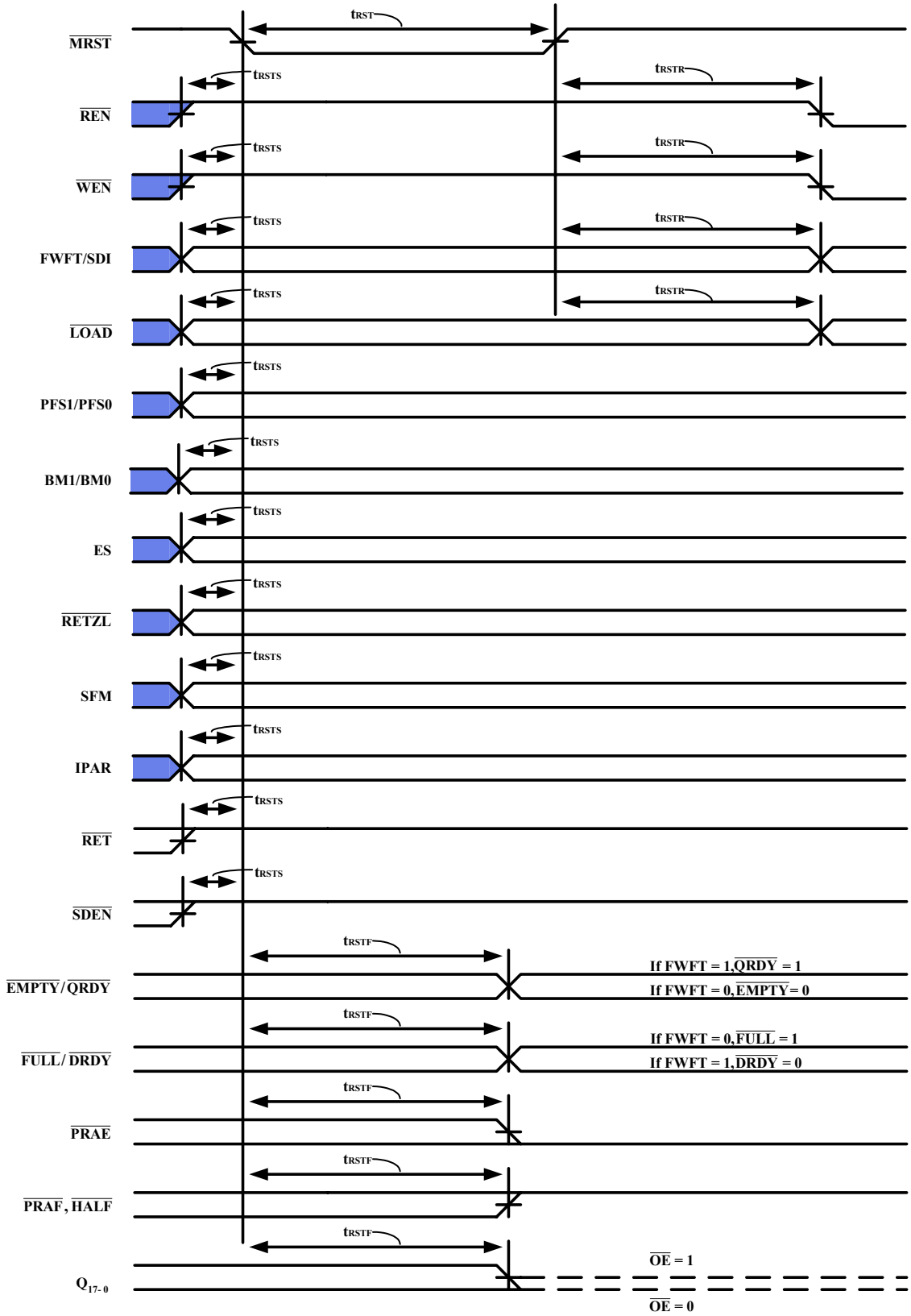


Diagram 1. Master Reset Timing

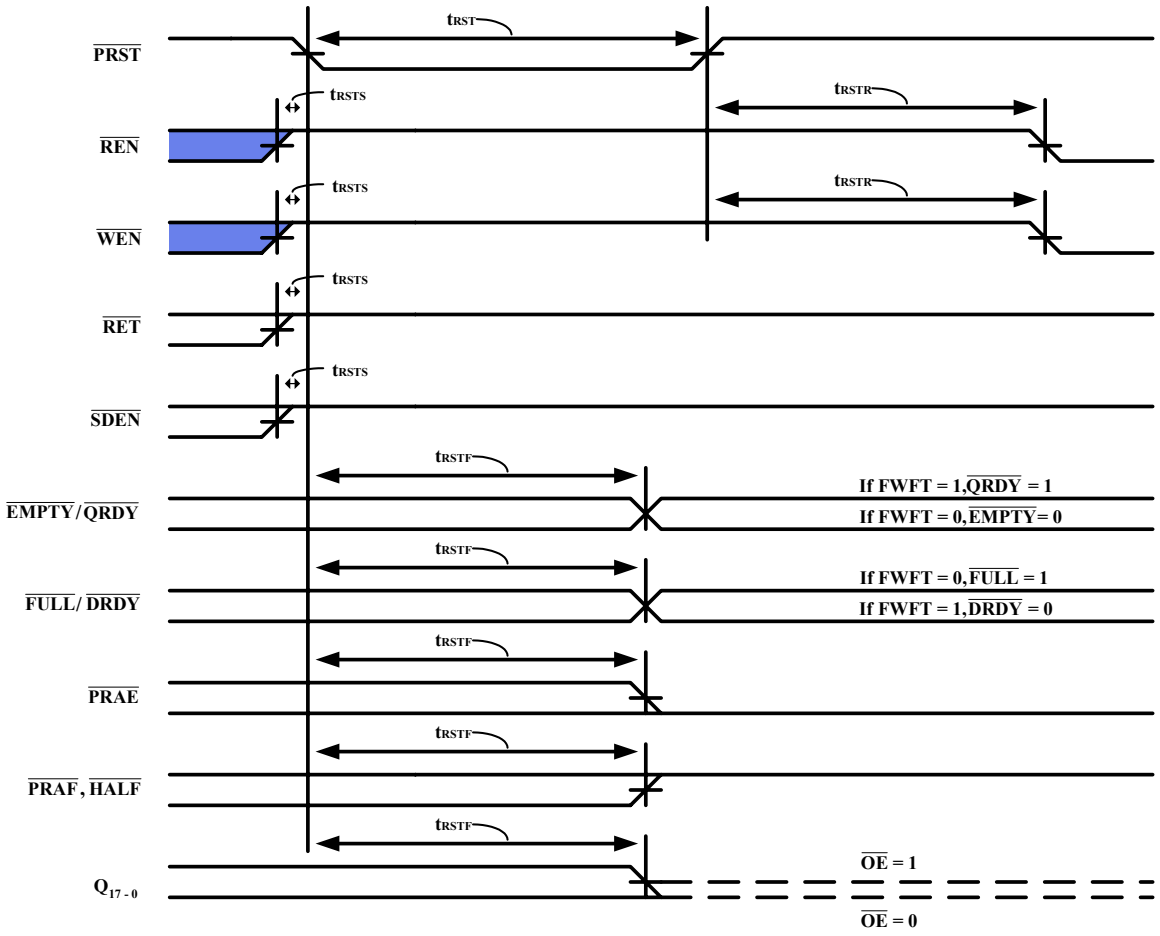
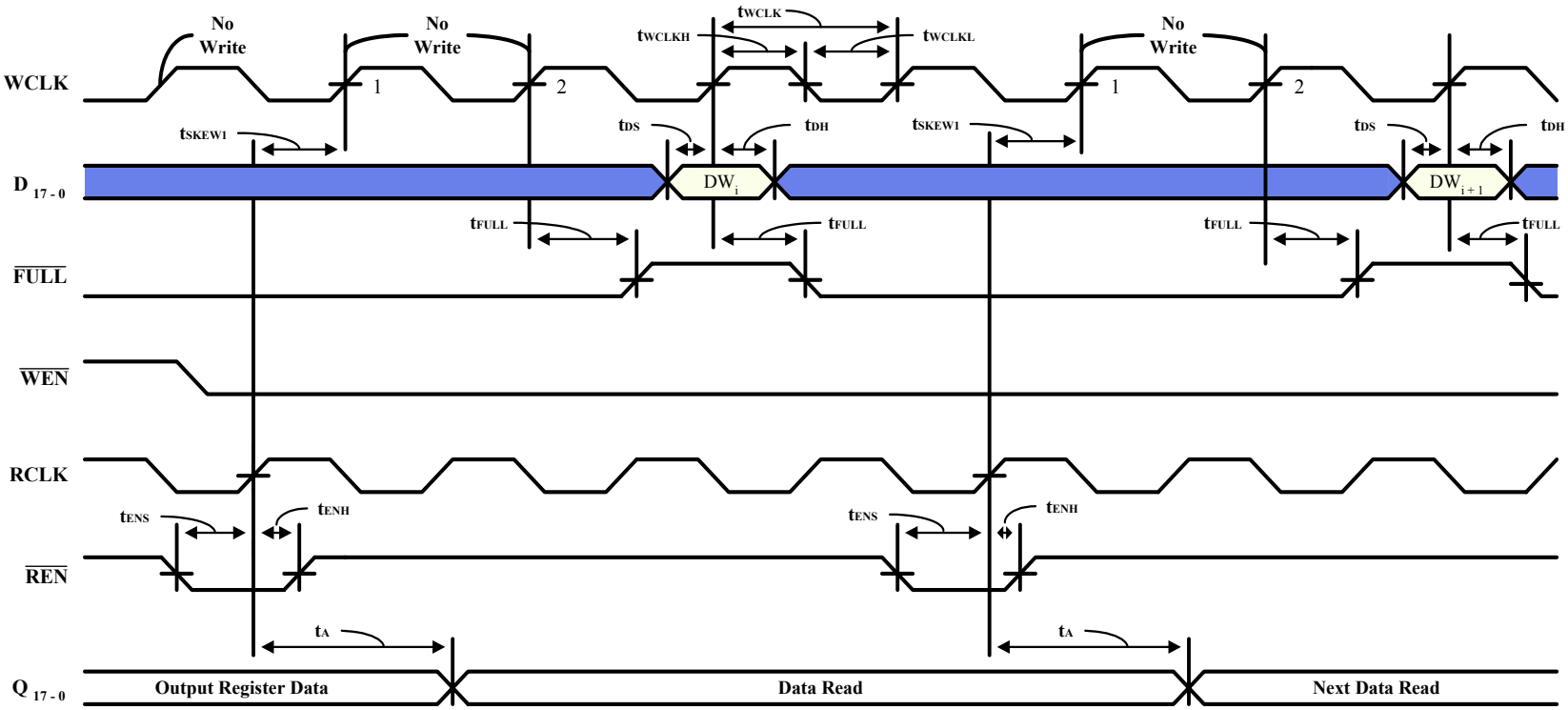


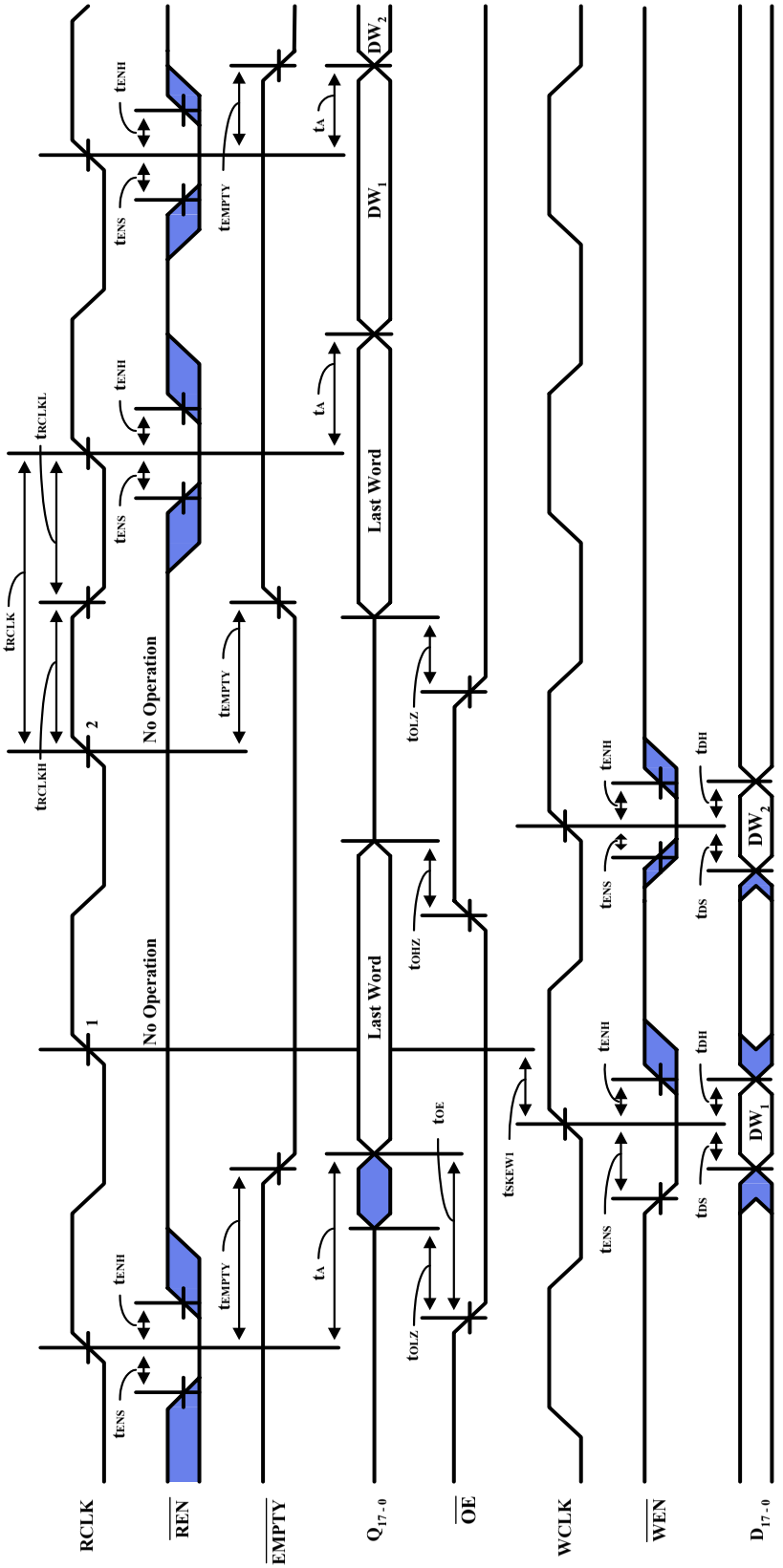
Diagram 2. Partial Reset Timing



NOTES:

1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater or equal than t_{SKEW1}, $\overline{FULL}$ will go high (after one WCLK cycle plus t_{FULL}). If t_{SKEW1} is not met, then $\overline{FULL}$ will assert 1 or more WCLK cycles.
2. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.

Diagram 3. Write Cycle and Full Flag Timing (Standard Mode)



NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater or equal than t_{SKEW1}, $\overline{EMPTY}$ will go high (after one RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.
2. $\overline{LOAD}$ = High.
3. First word latency: $t_{SKEW1} + t_{EMPTY} + 1 * t_{RCLK}$.

Diagram 4. Read Cycle, Empty Flag and First Data Word Latency Timing (Standard Mode)

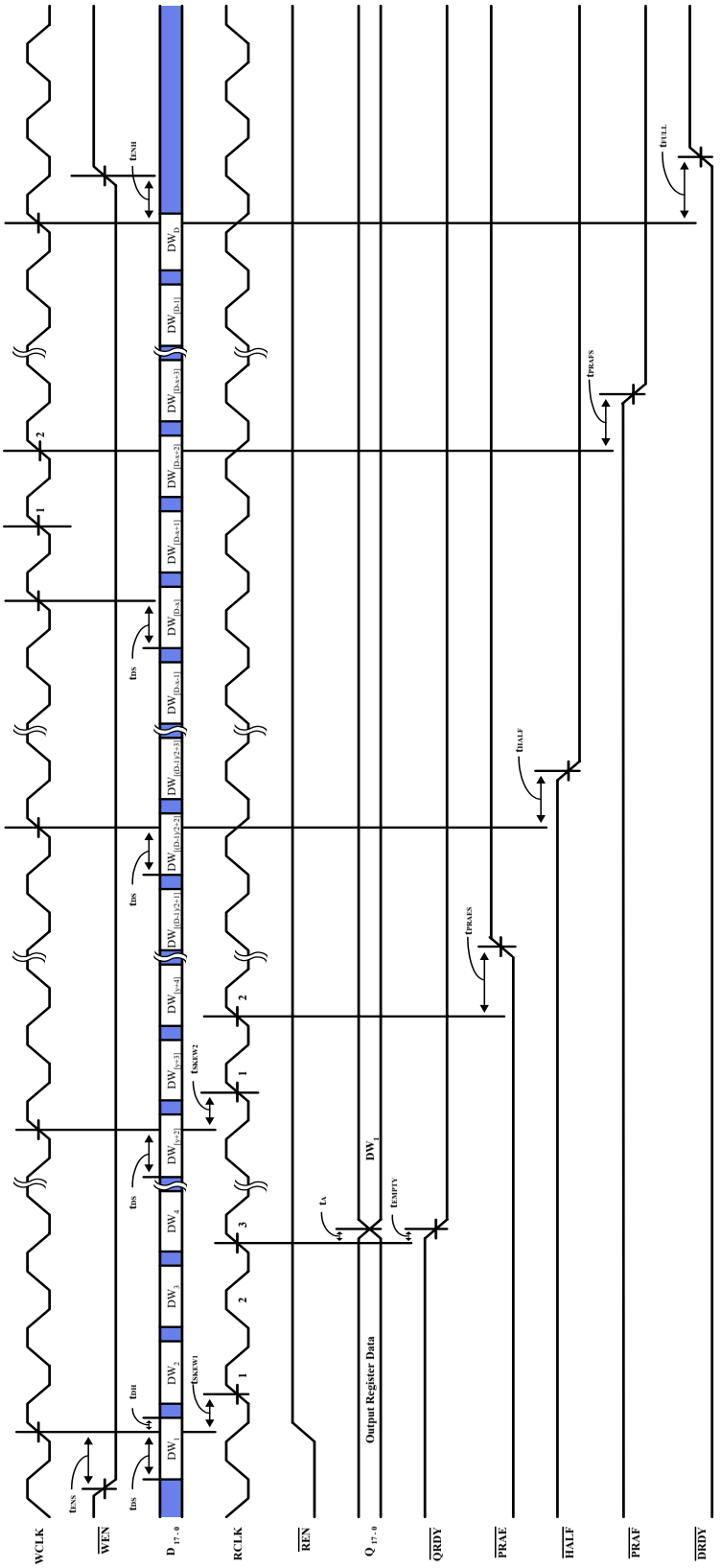
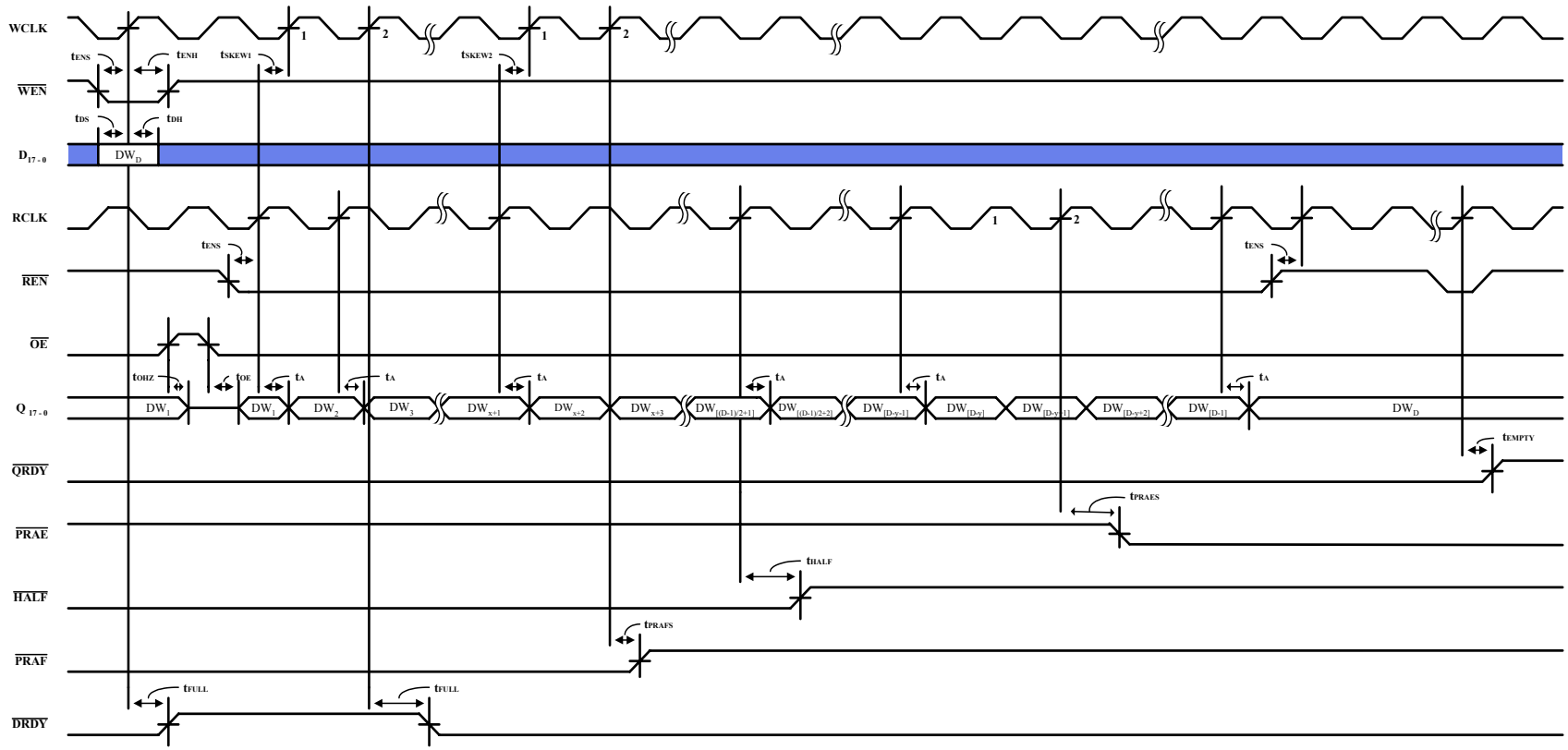


Diagram 5. Write Timing (FWFT Mode)

NOTES:

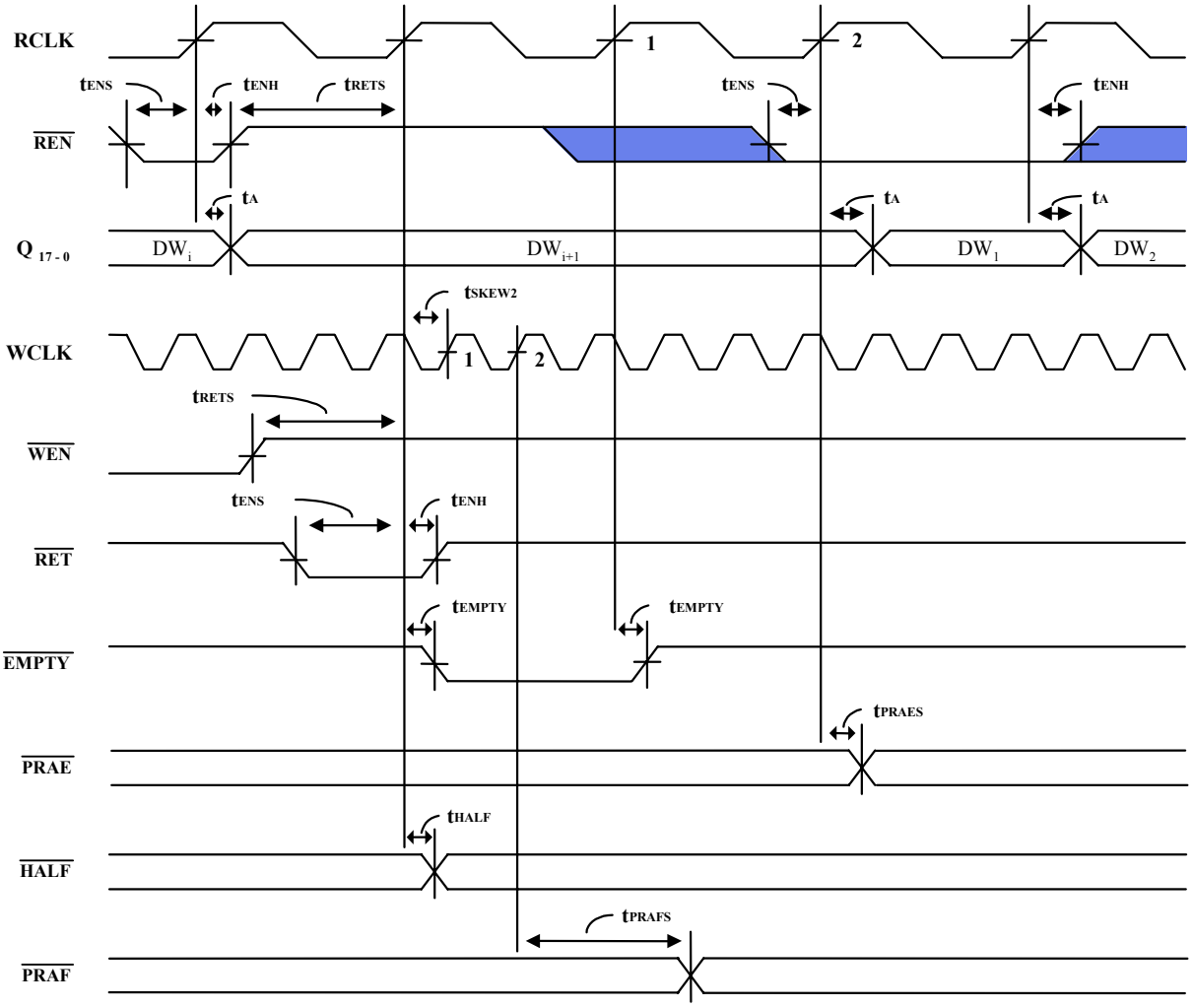
1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater or equal than t_{SKEW1}, $\overline{QRDY}$ will go low (after two RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{QRDY}$ will assert 1 or more RCLK cycles.
2. If the time between a rising edge of WCLK to the rising edge of RCLK is greater or equal than t_{SKEW2}, $\overline{PRAE}$ will go high (after one RCLK cycle plus t_{PRAES}). If t_{SKEW2} is not met, then $\overline{PRAE}$ will assert 1 or more RCLK cycles.
3. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.
4. y = $\overline{PRAE}$ offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 7 for Depth.
6. First word latency: $t_{SKEW1} + t_{EMPTY} + 2 * t_{RCLK}$



NOTES:

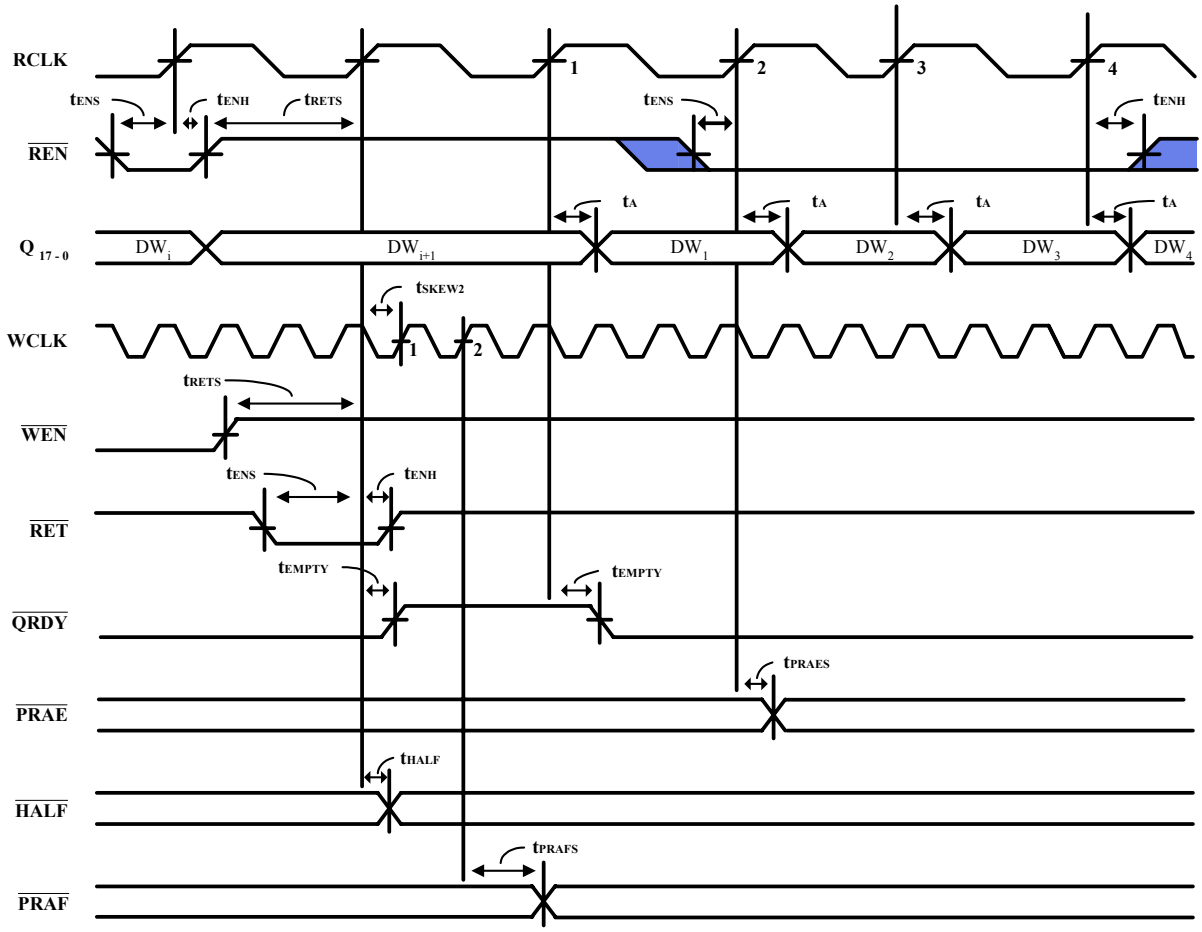
1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater or equal than t_{SKEW1}, $\overline{DRDY}$ will go low (after one WCLK cycle plus t_{FULL}) . If t_{SKEW1} is not met, then $\overline{DRDY}$ will assert 1 or more WCLK cycles.
2. If the time between a rising edge of RCLK to the rising edge of WCLK is greater or equal than t_{SKEW2}, $\overline{PRAF}$ will go high (after one WCLK cycle plus t_{PRAFS}) If t_{SKEW2} is not met, then $\overline{PRAF}$ will assert 1 or more WCLK cycles.
3. $\overline{LOAD}$ = High
4. y = $\overline{PRAE}$ Offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 7 for Depth.

Diagram 6. Read Timing (FWFT Mode)



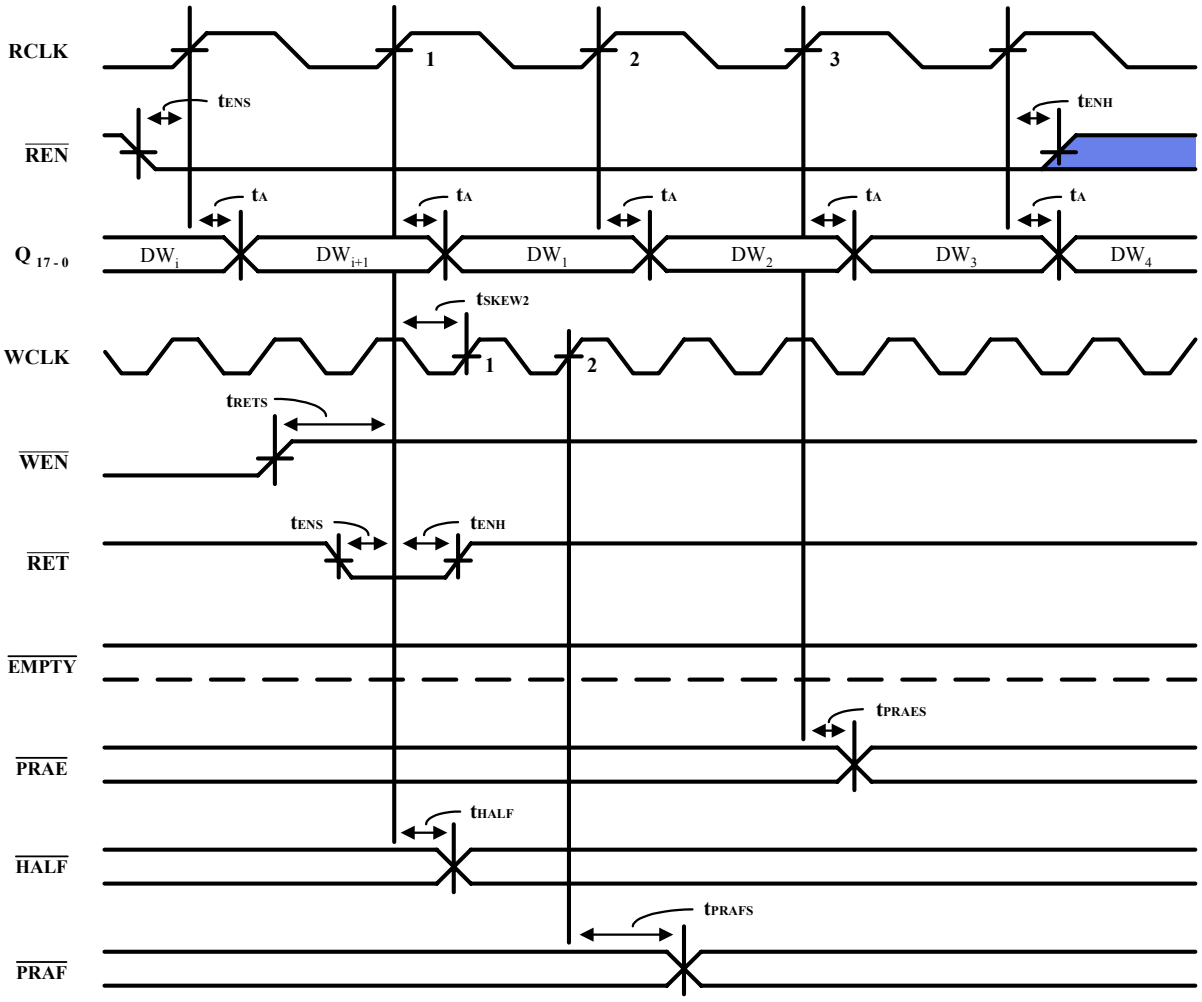
NOTES:
1. Upon completion of retransmit setup, a read operation can begin only after $\overline{\text{EMPTY}}$ returns high.
2. $\overline{\text{OE}}$ = Low.
3. DW_i = Words written to the queue after $\overline{\text{MRST}}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than two words written to the queue for a retransmit setup to be valid.

Diagram 7. Retransmit Timing (Standard Mode)



NOTES:
1. Upon completion of retransmit setup, a read operation can begin only after $\overline{QRDY}$ returns low.
2. $\overline{OE}$ = Low.
3. DW_i = Words written to the queue after $\overline{MRST}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than two words written to the queue for a retransmit setup to be valid.
5. Please refer to Table 7 for Depth.

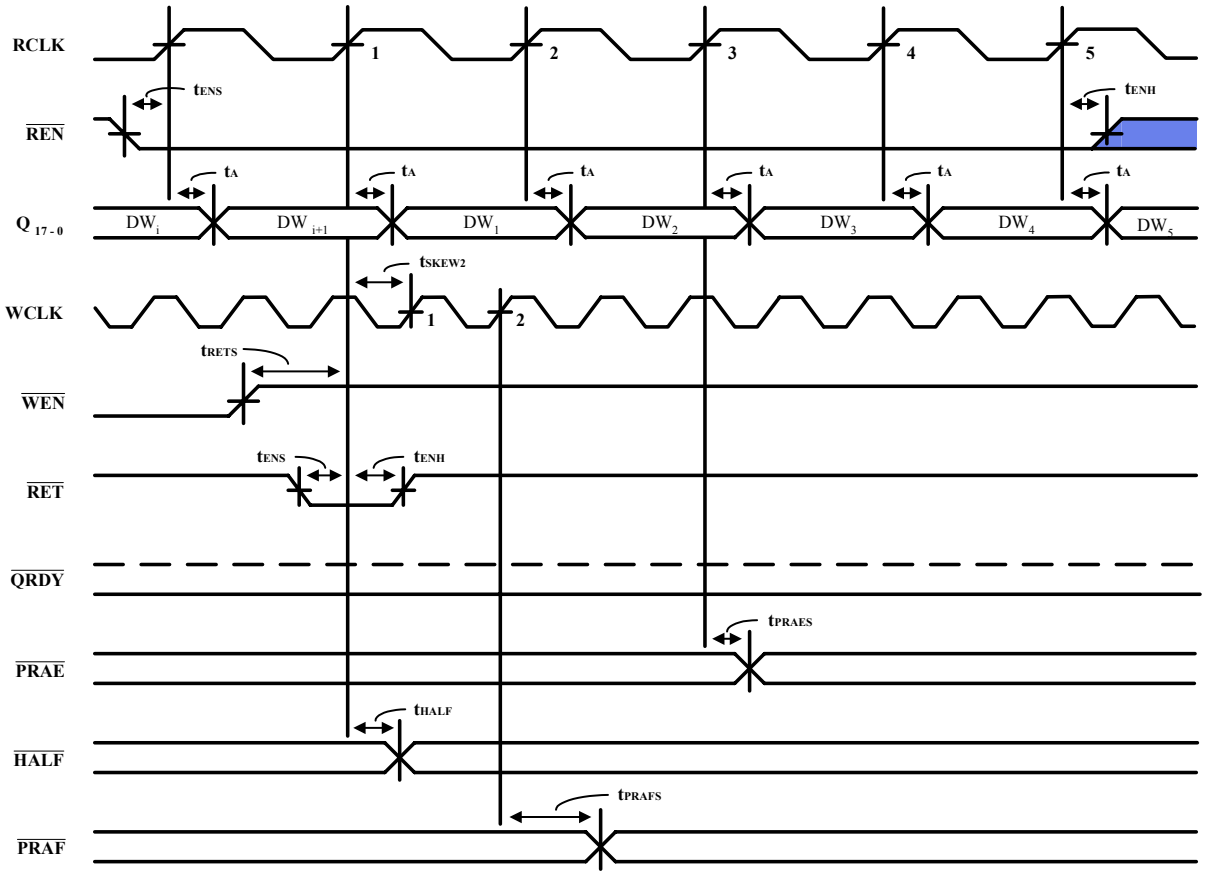
Diagram 8. Retransmit Timing (FWFT Mode)



NOTES:

1. If the part is empty at the point of retransmit, the Empty Flag ($\overline{\text{EMPTY}}$) will be updated based on RCLK (Retransmit Clock cycle). Valid data will appear on the output.
2. $\overline{\text{OE}}$ = Low; enables data to be read on outputs Q_{17-0}.
3. DW_1= first word written to the queue after Master Reset; DW_2= second word written to the queue after Master Reset.
4. No more than D-2 may be written to the queue between reset (Master or Partial) and retransmit setup. Therefore, $\overline{\text{FULL}}$ will be high throughout the retransmit setup procedure. Please refer to Table 7 for Depth.
5. There must be at least two words written to zero latency retransmit from the queue before a retransmit operation can be invoked.
6. $\overline{\text{RETZL}}$ is set Low during $\overline{\text{MRST}}$.

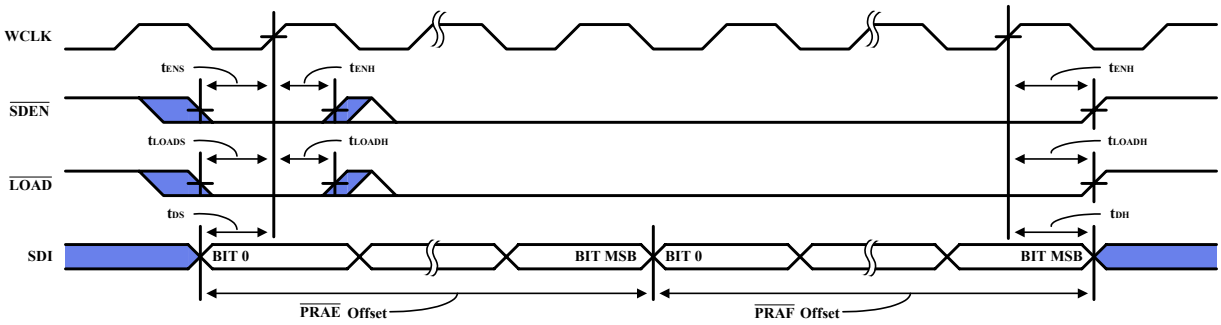
Diagram 9. Zero Latency Retransmit Timing (Standard Mode)



NOTES:

1. If the part is empty at the point of retransmit, the output ready flag ($\overline{QRDY}$) will be updated based on RCLK (Retransmit Clock cycle). Valid data will appear on the output.
2. No more than D-2 words may be written to the queue between reset (Master or Partial) and retransmit setup. Therefore, $\overline{DRDY}$ will be low throughout the retransmit setup procedure. Please refer to Table 7 for Depth.
3. $\overline{OE}$ = Low.
4. DW_1, DW_2, DW_3 = first, second and third words written to the queue after Master Reset.
5. There must be at least two words written to the queue before a retransmit operation can be invoked.
6. $\overline{RETZL}$ is set low during $\overline{MRST}$.

Diagram 10. Zero Latency Retransmit Timing (FWFT Mode)

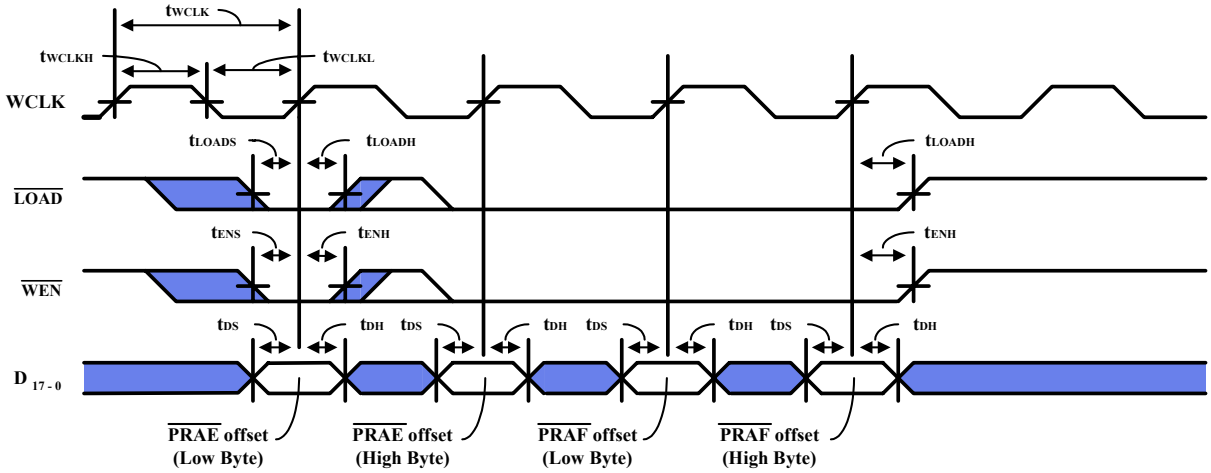


*Refer to Table 12

Diagram 11. Serial Loading of Programmable Flag Registers (Standard and FWFT Mode)

	FQV21113	FQV2103	FQV293	FQV283	FQV273	FQV263	FQV253	FQV243
MSB for x9 to x9	18	17	16	15	14	13	12	11
MSB for All Other Modes	17	16	15	14	13	12	11	10

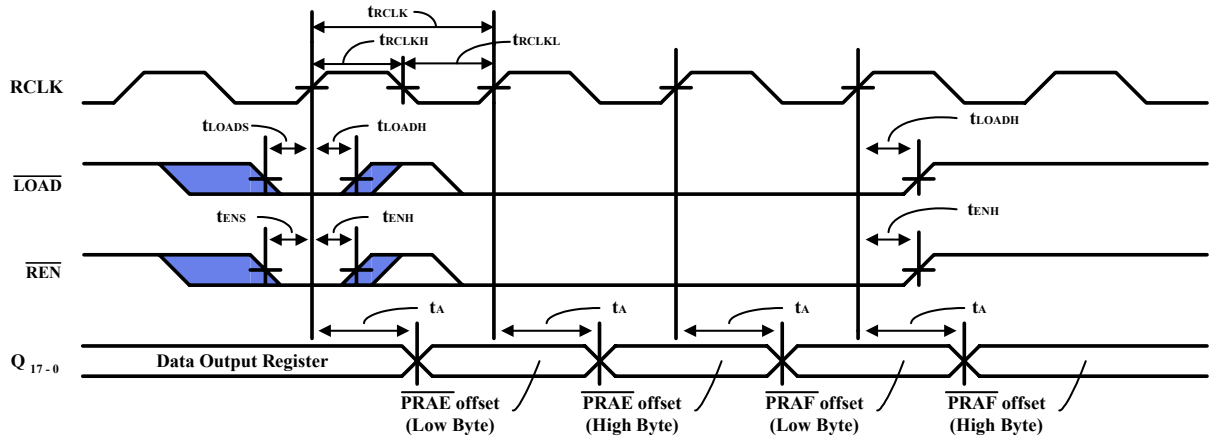
Table 12. Reference Table for Diagram 11



NOTES:

1. Based on programming the x18 bus width. For the x9 bus width, add one extra cycle to both $\overline{\text{PRAE}}$ and $\overline{\text{PRAF}}$ offsets.

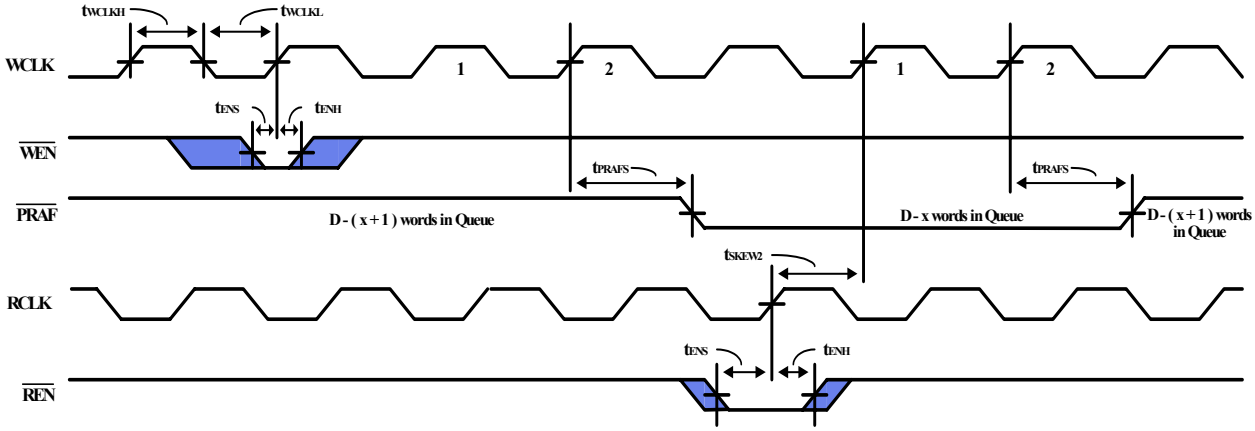
Diagram 12. Parallel Loading of Programmable Flag Registers (Standard and FWFT Mode)



NOTES:

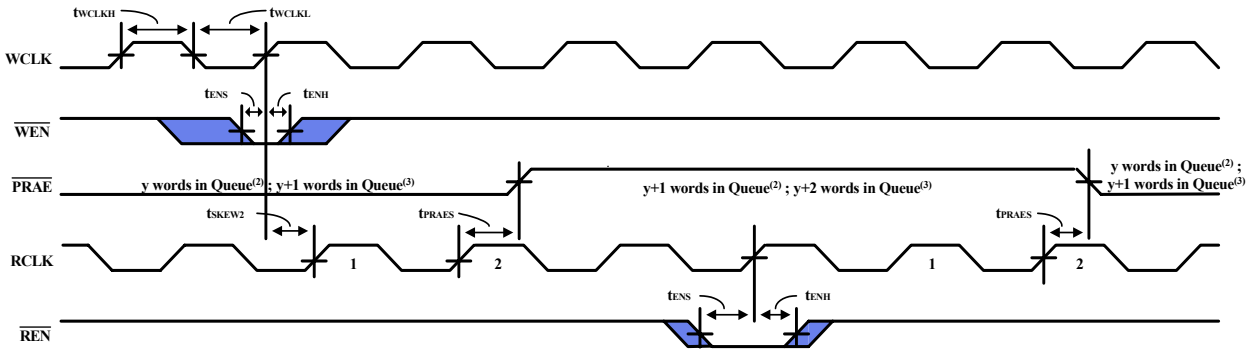
1. Based on programming the x18 bus width. For the x9 bus width, add one extra cycle to both $\overline{\text{PRAE}}$ and $\overline{\text{PRAF}}$ offsets.

Diagram 13. Parallel Read of Programmable Flag Registers (Standard and FWFT Mode)



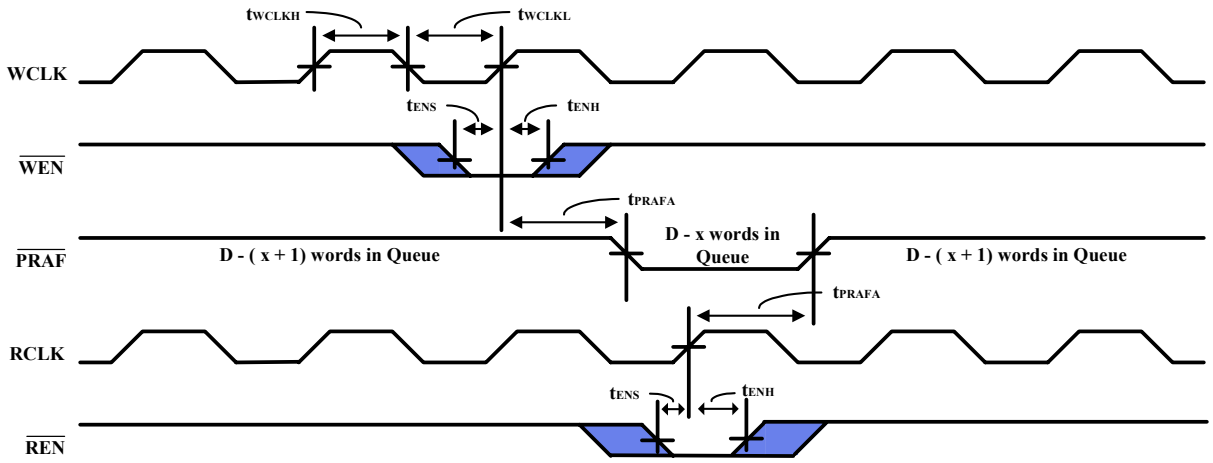
NOTES:
1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth. Please refer to Table 7 for Depth.
3. If the time between a rising edge of RCLK to the rising edge of WCLK is greater or equal than t_{SKEW2}, $\overline{\text{PRAF}}$ will go high (after one WCLK cycle plus t_{PRAFS}). If t_{SKEW2} is not met, then $\overline{\text{PRAF}}$ will assert 1 or more WCLK cycles.
4. $\overline{\text{PRAF}}$ synchronizes to the rising edge of WCLK only.

Diagram 14. Synchronous Programmable Almost-Full Flag Timing (Standard and FWFT Mode)



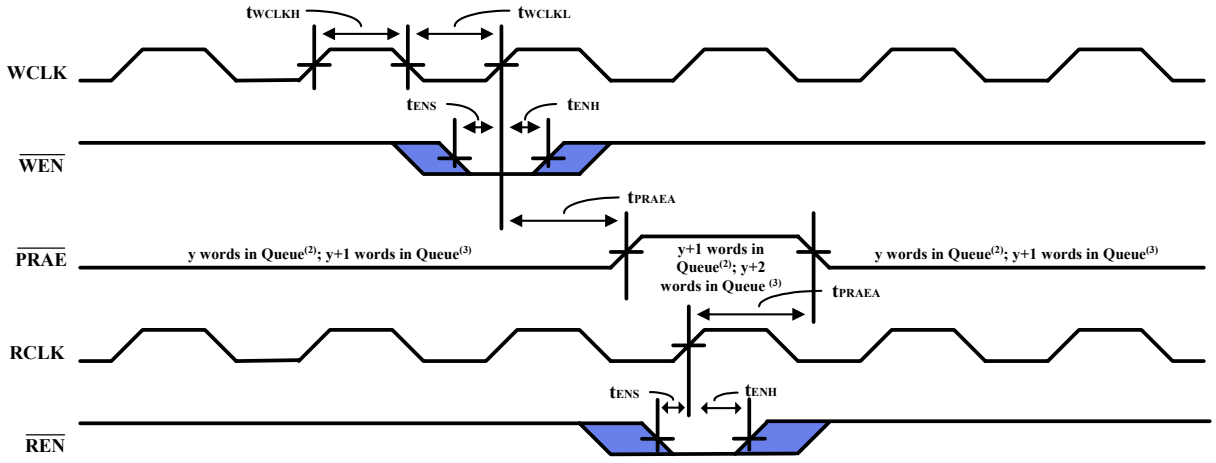
NOTES:
1. y = $\overline{\text{PRAE}}$ offset.
2. For Standard Mode.
3. For FWFT Mode.
4. If the time between a rising edge of WCLK to the rising edge of RCLK is greater or equal than t_{SKEW2}, $\overline{\text{PRAE}}$ will go high (after one RCLK cycle plus t_{PRAES}). If t_{SKEW2} is not met, then $\overline{\text{PRAE}}$ will assert 1 or more RCLK cycles.
5. $\overline{\text{PRAE}}$ synchronizes to the rising edge of RCLK only.

Diagram 15. Synchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Mode)



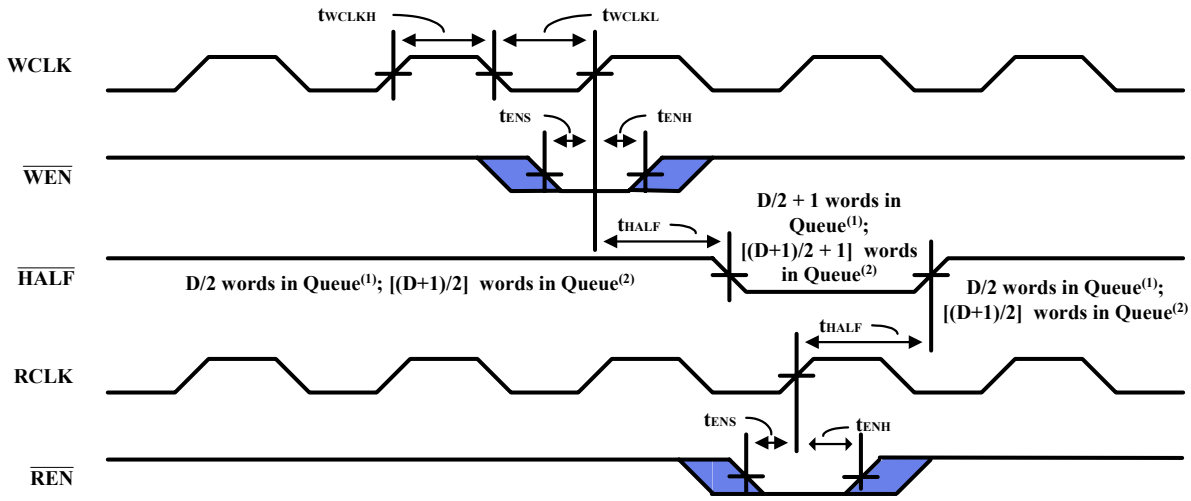
NOTES:
1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth. Please refer to Table 7 for Depth.
3. $\overline{\text{PRAF}}$ is asserted to low on WCLK transition and reset to high on RCLK transition.
4. Select this mode by setting SFM low during Master Reset.

Diagram 16. Asynchronous Programmable Almost-Full Flag Timing (Standard and FWFT Mode)



NOTES:
1. y = $\overline{\text{PRAE}}$ offset.
2. For Standard Mode.
3. For FWFT Mode.
4. $\overline{\text{PRAE}}$ is asserted to low on RCLK transition and reset to high on WCLK transition.
5. Select this mode by setting SFM low during Master Reset.

Diagram 17. Asynchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Mode)



NOTES:
1. For Standard Mode.
2. For FWFT Mode.
3. Please refer to Table 7 for Depth.

Diagram 18. Half-Full Flag Timing (Standard and FWFT Mode)

Order Information:

HBA Device Family	Device Type	Power	Speed (ns) *	Package**	Temperature Range
XX	XXXXX	X	XX	XX	X
FQ	**V2113** (524,288 x 9) (262,144 x 18)	Low	**6** – 166 MHz	PF	Blank – Commercial (0°C to 70°C)
	V2103 (262,144 x 9) (131,072 x 18)		**7-5** – 133 MHz		**I** – Industrial (-40° to 85°C)
	V293 (131,072 x 9) (65,536 x 18)		**10** – 100 MHz		
	V283 (65,536 x 9) (32,768 x 18)		**15** – 66 MHz		
	V273 (32,768 x 9) (16,384 x 18)				
	V263 (16,384 x 9) (8,192 x 18)				
	V253 (8,192 x 9) (4,096 x 18)				
	V243 (4,096 x 9) (2,048 x 18)				

***Speed –** 6ns available only in Commercial temp (0°C to 70°C). Slower speeds available upon request.
****Package** – 80 pin Plastic Thin Quad Flat Pack (TQFP)

Example:

FQV283L6PF (64k x 9, 6ns, Commercial temp)
FQV273L10PFI (32k x 9, 10ns, Industrial temp)

Document Revision History:

02/26/03 pg. 1, 2, 3, 5, 6, 7, 8, 9, 10, 13, 14, 15, 20, 21, 24, 25, 27, 28, 29, 30, 31, 32, 34, 38, 39, 40, 41, 42

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