5 Volt Synchronous x9 First-In/First-Out Queue

Memory Configuration	Device
131,072 x 9	FQ291
65,536 x 9	FQ281
32,768 x 9	FQ271
16,384 x 9	FQ261

Key Features

- **Industry leading First-In/First-Out Queues (up to 100MHz)**
- **Write cycle time of 10ns independent of Read cycle time**
- **Read cycle time of 10ns independent of Write cycle time**
- **User selectable input and output port bus-sizing**
- **Big Endian/Little Endian user selectable byte representation**
- **5V power supply**
- **Master Reset clears all previously programmed configurations including Write and Read pointers.**
- **Partial Reset clears Write and Read pointers but maintain all previously programmed configurations.**
- **First Word Fall Through (FWFT) and Standard Timing modes**
- **Preset for Almost Full ($\overline{\text{PRAF}}$) and Almost Empty ($\overline{\text{PRAE}}$) offsets values**
- **Parallel/Serial programming of $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ offset values**
- **Full, Empty, Almost Full, Almost Empty and Half Full indicators**
- **Asynchronous output enable tri-state data output drivers**
- **Data retransmission**
- **Available package: 64 - pin Plastic Thin Quad Flat Pack (TQFP), 64 – pin Slim Thin Quad Flat Pack (STQFP)**
- **(0°C to 70°C) Commercial operating temperature available for cycle time of 10ns and above**
- **(-40°C to 85°C) Industrial operating temperature available for cycle time of 10ns and above**

Product Description

HBA's FlexQ™ II offers industry leading FIFO queuing bandwidth (up to 1 Gbps) with a wide range of memory configurations (from 16,384 x 9 to 131,072 x 9). System designer has full flexibility of implementing deeper and wider queues using FWFT mode and width expansion features. Full, Empty, and Half-Full indicators allow easy handshaking between transmitters and receivers. User programmable Almost Full and Almost Empty (Parallel/Serial) indicators allow implementation of virtual queue depths.

Asynchronous Output Enable pin configures the tri-state data output drivers. Independent Write and Read controls provide rate-matching capability.

Master Reset clears all previously programmed configurations by providing a low pulse on $\overline{\text{MRST}}$ pin. In addition, Write and Read pointers to the queue are initialized to zero. Partial Reset will not alter previously programmed configurations but will initialize Write and Read pointers to zero.

In FWFT mode, first data written into the queue appears on output data bus after the specified latency period at the low to high transition of RCLK. Subsequent reads from the queue will require asserting $\overline{\text{REN}}$. This feature is useful when implementing depth expansion functions. In this mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ are used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ respectively.

In Standard mode, always assert $\overline{\text{REN}}$ for read operation. $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ are used instead of $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ respectively.

$\overline{\text{PRAF}}$, $\overline{\text{PRAE}}$, and $\overline{\text{HALF}}$ are available in either FWFT or Standard mode. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ can operate in either synchronous or asynchronous modes.

Product Description (Continued)

At any time, data previously read from the queue can be retransmitted by asserting $\overline{RET}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero), location of the queue.

These FlexQ™ II devices have low power consumption, hence minimizing system power requirements. In addition, industry standard 64 - pin Plastic TQFP and 64 - pin STQFP are offered to save system board space.

These queues are ideal for applications such as data communication, telecommunication, graphics, multiprocessing, test equipment, network switching, etc.

Block Diagram of Single Synchronous Queue
131,072 x 9 / 65,536 x 9 / 32,768 x 9 / 16,384 x 9

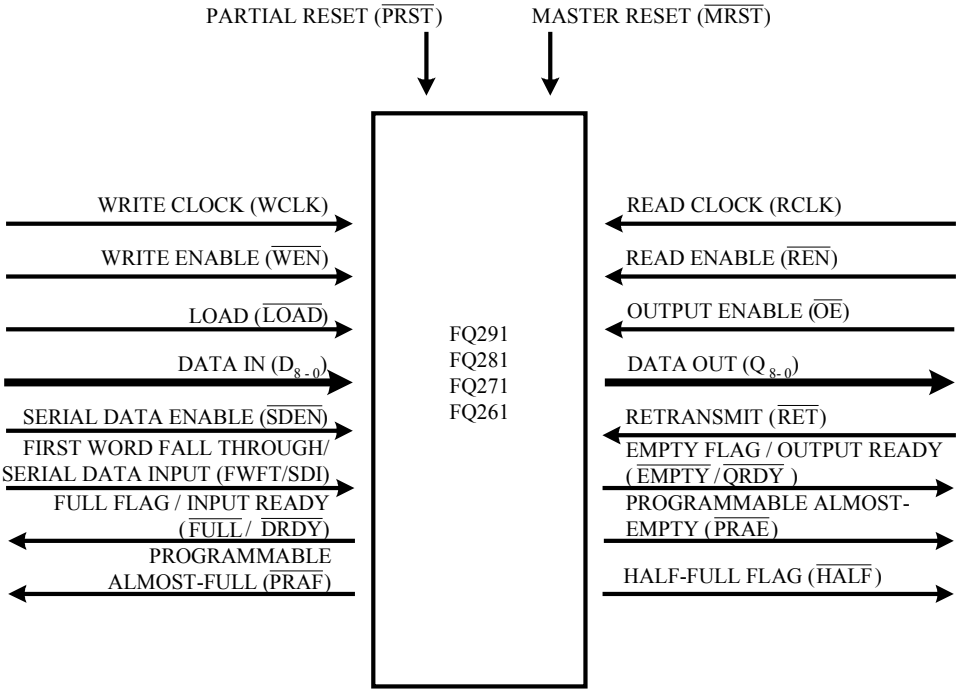


Figure 1. Single Device Configuration Signal Flow Diagram

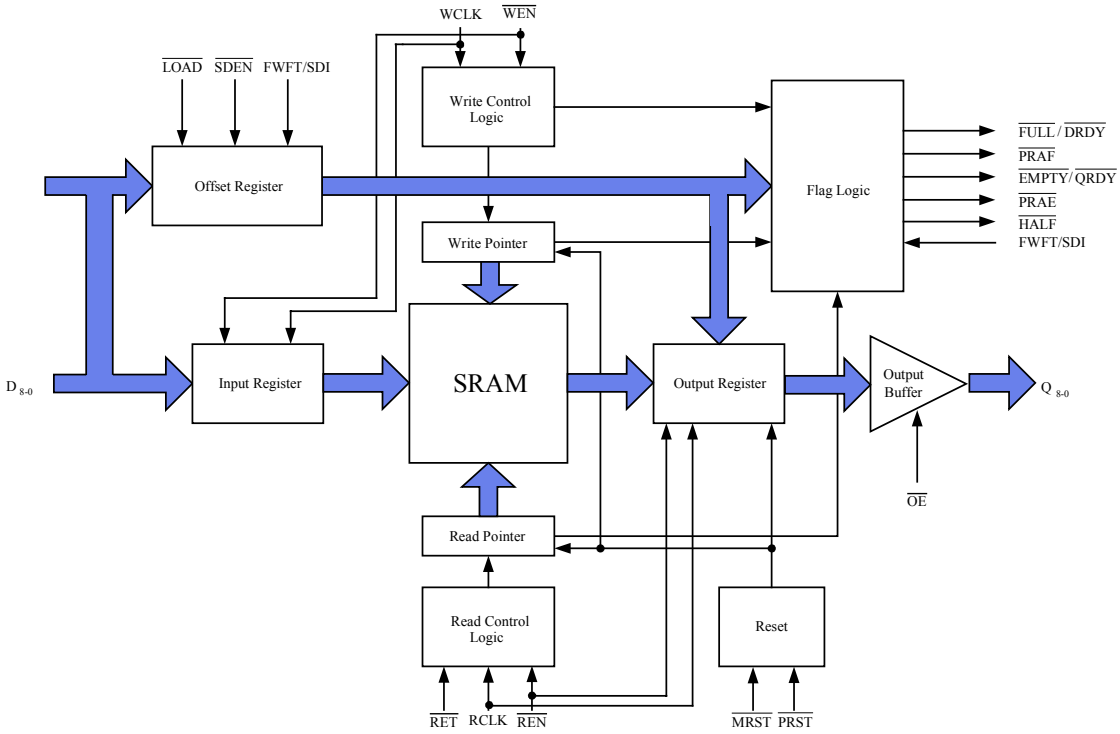
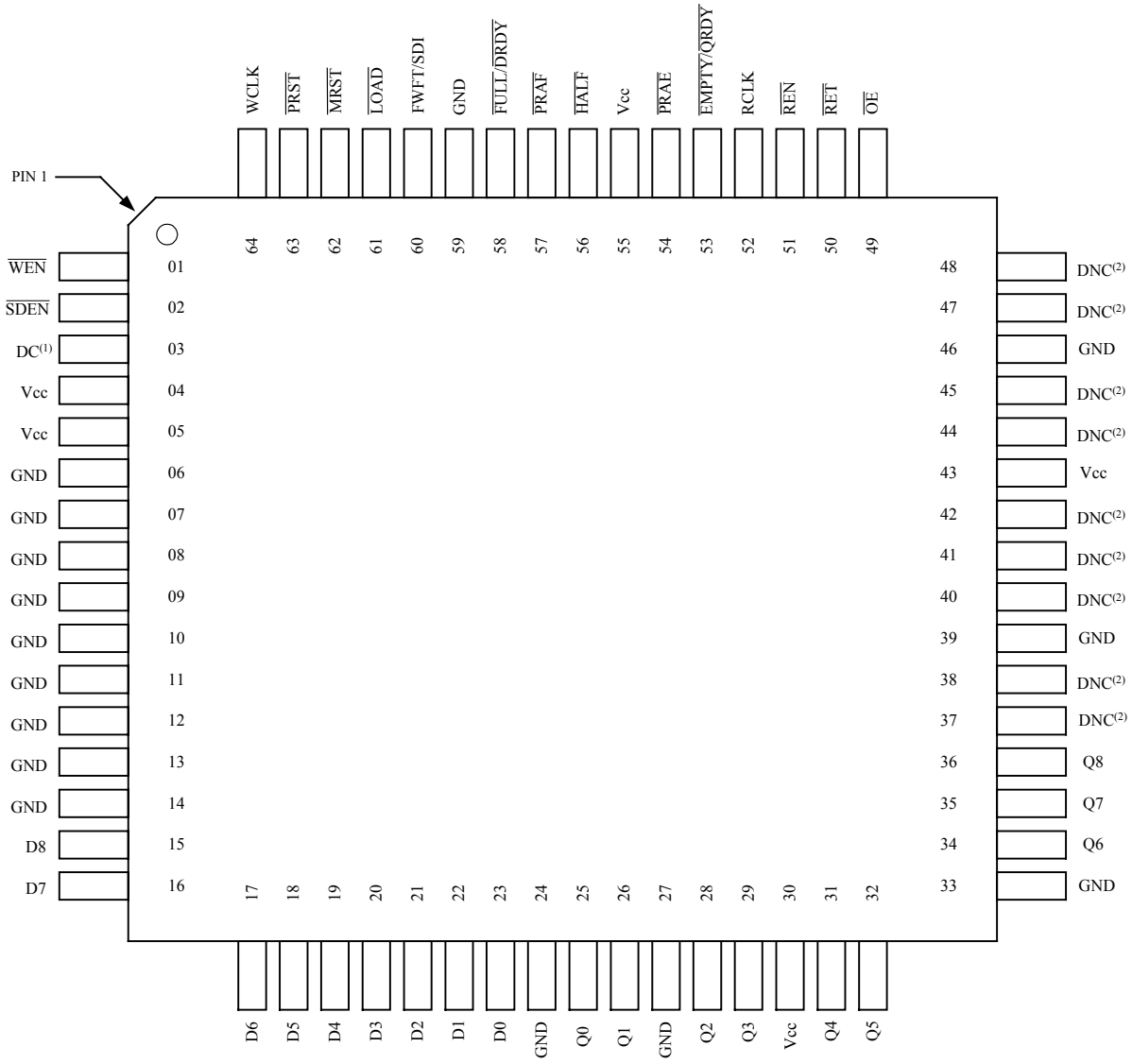


Figure 2. Device Architecture



TQFP - 64 (Drw No: PF-01A; Order code: PF)
STQFP – 64 (Drw No: TF-01A; Order code: TF)
Top View

NOTES:
1. DC = Don't Care. Must be tied to GND or Vcc, cannot be left open.
2. DNC = Do Not Connect.

Figure 3. Device Pin Out

Pin #	Pin Name	Pin Symbol	Input/Output	Description
62	Master Reset	$\overline{MRST}$	Input	Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{MRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will not be maintained.
63	Partial Reset	$\overline{PRST}$	Input	Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{PRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will be maintained.
64	Write Clock	WCLK	Input	Writes data into queue during low to high transitions of WCLK if $\overline{WEN}$ is set to low.
01	Write Enable	$\overline{WEN}$	Input	Controls write operation into queue or offset registers during low to high transition of WCLK.
61	Load Enable	$\overline{LOAD}$	Input	During Master Reset, set $\overline{LOAD}$ low to select parallel programming or default offset value of 127. Set $\overline{LOAD}$ high to select serial programming or default offset value of 1023. After Master Reset, $\overline{LOAD}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively. Use in conjunction with $\overline{WEN}$ / $\overline{REN}$.
15,16,17, 18,19,20, 21,22,23	Data Inputs	D_{8-0}	Input	9 - bit wide input data bus.
52	Read Clock	RCLK	Input	Reads data from queue during low to high transitions of RCLK if $\overline{REN}$ is set to low.
51	Read Enable	$\overline{REN}$	Input	Controls read operation from queue or offset registers during low to high transition of RCLK.
49	Output Enable	$\overline{OE}$	Input	Setting $\overline{OE}$ low activates the data output drivers. Setting $\overline{OE}$ high deactivates the data output drivers (High-Z).
36,35,34, 32,31,29, 28,26,25	Data Outputs	Q_{8-0}	Output	9 - bit wide output data bus.
60	First Word Fall Through/Serial Data Input	FWFT/SDI	Input	Selects FWFT timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{LOAD}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{SDEN}$.

Table 1. Pin Descriptions

Pin #	Pin Name	Pin Symbol	Input/Output	Description
02	Serial Data Input Enable	$\overline{SDEN}$	Input	If serial programming is selected, setting $\overline{SDEN}$ and $\overline{LOAD}$ low enables serial data input to be written into offset registers during the low to high transition of WCLK.
50	Retransmit	$\overline{RET}$	Input	Data previously read from the queue can be retransmitted by asserting $\overline{RET}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue.
58	Full / Data Input Ready Flag	$\overline{FULL}$ / $\overline{DRDY}$	Output	Queue is full when $\overline{FULL}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue. In FWFT mode, queue is full when $\overline{DRDY}$ goes high during the low to high transition of WCLK. This prohibits further writes into the queue.
53	Empty / Data Output Ready Flag	$\overline{EMPTY}$ / $\overline{QRDY}$	Output	Queue is empty when $\overline{EMPTY}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue. In FWFT mode, queue is empty when $\overline{QRDY}$ goes high during the low to high transition of RCLK. This prohibits further reads form the queue.
57	Almost Full	$\overline{PRAF}$	Output	Queue is almost full when $\overline{PRAF}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{PRAF}$.
54	Almost Empty	$\overline{PRAE}$	Output	Queue is almost empty when $\overline{PRAE}$ goes low during the low to high transition of RCLK. Default (Empty+offset) or programmed offset values determine the status of $\overline{PRAE}$.
56	Half Full	$\overline{HALF}$	Output	Queue is more than half full when $\overline{HALF}$ goes low. Triggered by both WCLK and RCLK.
03	Don't Care	DC	N/A	This pin can be tied high or low, cannot be left open.
4, 5, 30, 43, 55	Power	Vcc	N/A	5V power supply.
6, 7, 8, 9, 10, 11, 12, 13, 14, 24, 27, 33, 39, 46, 59	Ground	GND	N/A	0V Ground.
37, 37, 40, 41, 42, 44, 45, 47, 48	Do Not Connect	DNC	N/A	Do not connect.

Table 1. Pin Descriptions (Continued)

Symbol	Rating	Com'l & Ind'l	Unit
VTERM	Terminal Voltage with respect to GND	-0.5 to + 7	V
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	-50 to +50	MA

NOTES:
Absolute Max Ratings are for reference only. Permanent damage to the device may occur if extended period of operation is outside this range. Standard operation should fall within the Recommended Operating Conditions.

Table 2. Absolute Maximum Ratings

		FQ291, FQ281 FQ271, FQ261						
		Commercial Clock = 10ns, 15ns, 20ns			Industrial Clock = 10ns, 15ns, 20ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Recommended Operating Conditions								
VCC	Supply Voltage Com'l / Ind'l	4.5	5.0	5.5	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	0	0	0	V
VIH	Input High Voltage Com'l / Ind'l	2.0	-	5.0	2.0	-	5.0	V
VIL	Input Low Voltage Com'l / Ind'l	-	-	0.8	-	-	0.8	V
TA	Operating Temperature Commercial	0	-	70	0	-	70	°C
TA	Operating Temperature Industrial	-40	-	85	-40	-	85	°C
DC Electrical Characteristics								
ILI(1)	Input Leakage Current (any input)	-10	-	10	-10	-	10	µA
ILO	Output Leakage Current	-10	-	10	-10	-	10	µA
VOH	Output Logic "1" Voltage, IOH=-2mA	2.4	-	-	2.4	-	-	V
VOL	Output Logic "0" Voltage, IOL = 8mA	-	-	0.4	-	-	0.4	V
Power Consumption								
Icc1(2,3)	Active Power Supply Current	-	-	55	-	-	55	mA
Icc2(4)	Standby Current	-	-	20	-	-	20	mA

Table 3. DC Specifications

Capacitance at 100MHz Ambient Temperature (25°C)				
Symbol	**Parameter**	**Conditions**	**Max.**	**Unit**
CIN(2)	Input Capacitance	VIN= 0V	10	pF
COUT(2,4)	Output Capacitance	VOUT= 0V	10	pF

NOTES:
1. Measurement with 0.4<=VIN<=Vcc
2. With output tri-stated ($\overline{OE}$ = High)
3. Icc(1,2) is measured with WCLK and RCLK at 20 MHz
4. Design simulated, not tested.

Table 3. DC Specifications (Continued)

Symbol	Parameter	Commercial & Industrial						Unit
		FQ291-10 FQ281-10 FQ271-10 FQ261-10		FQ291-15 FQ281-15 FQ271-15 FQ261-15		FQ291-20 FQ281-20 FQ271-20 FQ261-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Cycle Frequency	-	100	-	66	-	50	MHz
t_A	Data Access Time	2	6.5	2	10	2	12	ns
t_{WCLK}	Write Clock Cycle Time	10	-	15	-	20	-	ns
t_{WCLKH}	Write Clock High Time	4.5	-	6	-	8	-	ns
t_{WCLKL}	Write Clock Low Time	4.5	-	6	-	8	-	ns
t_{RCLK}	Read Clock Cycle Time	10	-	15	-	20	-	ns
t_{RCLKH}	Read Clock High Time	4.5	-	6	-	8	-	ns
t_{RCLKL}	Read Clock Low Time	4.5	-	6	-	8	-	ns
t_{DS}	Data Set-up Time	3	-	4	-	5	-	ns
t_{DH}	Data Hold Time	0.5	-	1	-	1	-	ns
t_{ENS}	Enable Set-up Time	3	-	4	-	5	-	ns
t_{ENH}	Enable Hold Time	0.5	-	1	-	1	-	ns
t_{RST}	Reset Pulse Width[1]	10	-	15	-	20	-	ns
t_{RSTS}	Reset Set-up Time	10	-	15	-	20	-	ns
t_{RSTR}	Reset Recovery Time	10	-	15	-	20	-	ns
t_{RSTF}	Reset to Flag and Output Time	-	10	-	15	-	20	ns
t_{OLZ}	Output Enable to Output in Low-Z[1]	0	-	0	-	0	-	ns
t_{OE}	Output Enable to Output Valid	2	6	3	8	3	10	ns
t_{OHZ}	Output Enable to Output in High-Z[1]	2	6	3	8	3	10	ns
t_{FULL}	Write Clock to Full Flag	-	6.5	-	10	-	12	ns
t_{EMPTY}	Read Clock to Empty Flag	-	6.5	-	10	-	12	ns
t_{PRAFS}	Write Clock to Almost-Full Flag	-	6.5	-	10	-	12	ns
t_{PRAES}	Read Clock to Almost-Empty Flag	-	6.5	-	10	-	12	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Full Flag / Empty Flag	5	-	6	-	10	-	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for $\overline{PRAF}$ & $\overline{PRAE}$	12	-	15	-	20	-	ns
t_{SKEW3}	Skew time between Read Clock & Write Clock for $\overline{EMPTY}$ / $\overline{QRDY}$	60	-	60	-	60	-	ns

Table 4. AC Electrical Characteristics

Symbol	Parameter	Commercial & Industrial						Unit
		FQ291-10 FQ281-10 FQ271-10 FQ261-10		FQ291-15 FQ281-15 FQ271-15 FQ261-15		FQ291-20 FQ281-20 FQ271-20 FQ261-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{LOADS}	Load Setup Time	3	-	4	-	5	-	ns
t_{LOADH}	Load Hold Time	0.5	-	1	-	1	-	ns
t_{RTS}	Retransmit Setup Time	3	-	4	-	5	-	ns
t_{HF}	Clock to $\overline{HALF}$	-	16	-	20	-	22	ns

NOTES:
1. Design simulated, not tested.

Table 4. AC Electrical Characteristics (Continued)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load, clock = 10ns	Refer to Figure 4
Output Load*, clock = 10ns, 15ns, 20ns	Refer to Figure 5

* Include jig and scope capacitances

Table 5. AC Test Condition

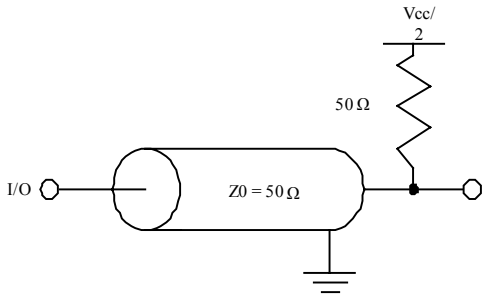


Figure 4. AC Test Load
for clock = 10ns

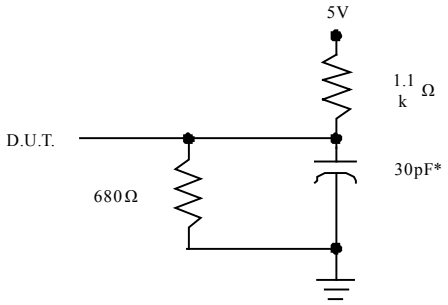


Figure 5. Output Load
for clock = 10ns, 15ns, 20ns
*Includes jig and scope capacitances.

Pin Functions

$\overline{\text{MRST}}$ — Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{MRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will not be maintained.

$\overline{\text{PRST}}$ — Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{PRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will be maintained.

WCLK — Writes data into queue during low to high transitions of WCLK if $\overline{\text{WEN}}$ is activated. Synchronizes $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ and $\overline{\text{PRAF}}$ flags. WCLK and RCLK are independent of each other.

$\overline{\text{WEN}}$ — Controls write operation into queue or offset registers during low to high transition of WCLK.

$\overline{\text{LOAD}}$ — During Master Reset, set $\overline{\text{LOAD}}$ low to select parallel programming or default offset value of 127. Set $\overline{\text{LOAD}}$ high to select serial programming or default offset value of 1023. After Master Reset, $\overline{\text{LOAD}}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively for parallel programming. Use in conjunction with $\overline{\text{WEN}}$ / $\overline{\text{REN}}$. During programming of offset registers, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flag status is invalid. For Serial programming, $\overline{\text{LOAD}}$ is used to enable serial loading of offset registers together with $\overline{\text{SDEN}}$. Refer to Figure 6 & 7 for details.

D_{8-0} — 9 - bit wide input data bus.

RCLK — Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN}}$ is set low. Synchronizes the $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ and $\overline{\text{PRAE}}$ flags. RCLK and WCLK are independent of each other.

$\overline{\text{REN}}$ — Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN}}$ is set to low. This also advances the Read pointer of the queue.

$\overline{\text{OE}}$ — Setting $\overline{\text{OE}}$ low activates the data output drivers. Setting $\overline{\text{OE}}$ high deactivates the data output drivers (High-Z). $\overline{\text{OE}}$ does not control advancement of Read pointer.

Q_{8-0} — 9 - bit wide output data bus.

FWFT/SDI — Selects FWFT timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{\text{LOAD}}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{\text{SDEN}}$. In FWFT mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ is used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ are used instead of $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$. Refer to Table 9 for all flags status.

$\overline{\text{SDEN}}$ — If serial programming is selected, setting $\overline{\text{SDEN}}$ and $\overline{\text{LOAD}}$ low enables serial data to be written into offset registers during the low to high transition of WCLK. During serial programming, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flags status is invalid. Refer Figure 6 & 7 for details.

$\overline{\text{RET}}$ — Data previously read from the queue can be retransmitted by asserting $\overline{\text{RET}}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue. Refer to Diagram 7 & 8 for details.

Pin Functions (Continued)

$\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ — In Standard mode, queue is full when $\overline{\text{FULL}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. In FWFT mode, queue is full when $\overline{\text{DRDY}}$ goes high during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. Refer to Table 8 & 9 for behavior of $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$.

$\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ — In Standard mode, queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. In FWFT mode, queue is empty when $\overline{\text{QRDY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. Refer to Table 8 & 9 for behavior of $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$.

$\overline{\text{PRAF}}$ — In Synchronous mode, queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{\text{PRAF}}$. In Asynchronous timing mode, $\overline{\text{PRAF}}$ is triggered by both WCLK and RCLK. Refer to Table 8 & 9 for behavior of $\overline{\text{PRAF}}$.

$\overline{\text{PRAE}}$ — In Synchronous mode, queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty+offset) or programmed offset values determine the status of $\overline{\text{PRAE}}$. In Asynchronous timing mode, $\overline{\text{PRAE}}$ is triggered by both WCLK and RCLK. Refer to Table 8 & 9 for behavior of $\overline{\text{PRAE}}$.

$\overline{\text{HALF}}$ — Queue is more than half full when $\overline{\text{HALF}}$ goes low during the low to high transition of WCLK. $\overline{\text{HALF}}$ goes high during low to high transition of RCLK when queue is less than half full. Refer to Table 8 & 9 for details.

$\overline{\text{LOAD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	$\overline{\text{SDEN}}$	WCLK	RCLK	FQ281 FQ271 FQ261 Selection / Sequence
0	0	1	1	↑	X	Parallel write to offset registers: Empty Offset (Low Byte) Empty Offset (High Byte) Full Offset (Low Byte) Full Offset (High Byte) → Parallel write to registers: 1. $\overline{\text{PRAE}}$ Low Byte 2. $\overline{\text{PRAE}}$ High Byte 3. $\overline{\text{PRAF}}$ Low Byte 4. $\overline{\text{PRAF}}$ High Byte
0	1	0	1	X	↑	Parallel read from offset registers: Empty Offset (Low Byte) Empty Offset (High Byte) Full Offset (Low Byte) Full Offset (High Byte) → Parallel read from registers: 1. $\overline{\text{PRAE}}$ Low Byte 2. $\overline{\text{PRAE}}$ High Byte 3. $\overline{\text{PRAF}}$ Low Byte 4. $\overline{\text{PRAF}}$ High Byte
0	1	1	0	↑	X	Serial shift into registers: 32 bits for the FQ281 30 bits for the FQ271 28 bits for the FQ261 1 bit for each rising WCLK edge Starting with Empty Offset (Low Byte) Ending with Full Offset (High Byte)
X	1	1	1	X	X	No Operation
1	0	X	X	↑	X	Write Memory
1	X	0	X	X	↑	Read Memory
1	1	1	X	X	X	No Operation

Figure 6. Programmable Flag Offset Programming Sequence (FQ281, FQ271 and FQ261)

$\overline{\text{LOAD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	$\overline{\text{SDEN}}$	WCLK	RCLK	FQ291 Selection / Sequence
0	0	1	1	↑	X	Parallel write to offset registers: Empty Offset (Low Byte) Empty Offset (Mid Byte) Empty Offset (High Byte) Full Offset (Low Byte) Full Offset (Mid Byte) Full Offset (High Byte) Parallel write to registers: 1. $\overline{\text{PRAE}}$ Low Byte 2. $\overline{\text{PRAE}}$ Mid Byte 3. $\overline{\text{PRAE}}$ High Byte 4. $\overline{\text{PRAF}}$ Low Byte 5. $\overline{\text{PRAF}}$ Mid Byte 6. $\overline{\text{PRAF}}$ High Byte
0	1	0	1	X	↑	Parallel read from offset registers: Empty Offset (Low Byte) Empty Offset (High Byte) Empty Offset (Mid Byte) Full Offset (Low Byte) Full Offset (Mid Byte) Full Offset (High Byte) Parallel read from registers: 1. $\overline{\text{PRAE}}$ Low Byte 2. $\overline{\text{PRAE}}$ Mid Byte 3. $\overline{\text{PRAE}}$ High Byte 4. $\overline{\text{PRAF}}$ Low Byte 5. $\overline{\text{PRAF}}$ Mid Byte 6. $\overline{\text{PRAF}}$ High Byte
0	1	1	0	↑	X	Serial shift into registers: 34 bits for the FQ291 1 bit for each rising WCLK edge Starting with Empty Offset (Low Byte) Ending with Full Offset (High Byte)
X	1	1	1	X	X	No Operation
1	0	X	X	↑	X	Write Memory
1	X	0	X	X	↑	Read Memory
1	1	1	X	X	X	No Operation

Figure 7. Programmable Flag Offset Programming Sequence (FQ291)

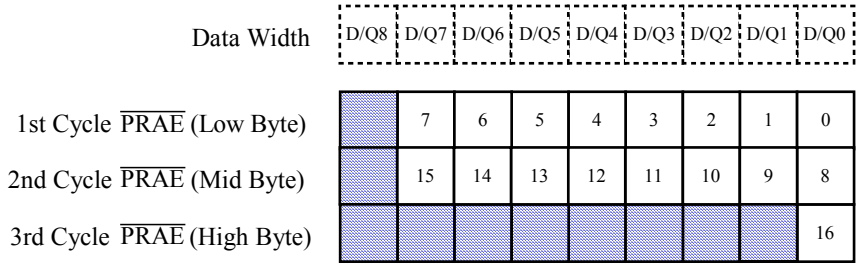
Device	$\overline{PRAF}$ Programming (bits)		$\overline{PRAE}$ Programming (bits)	
FQ291	D/Q_{7-0} D/Q_{7-0} D/Q_0	Low Byte Mid Byte High Byte	D/Q_{7-0} D/Q_{7-0} D/Q_0	Low Byte Mid Byte High Byte
FQ281	D/Q_{7-0} D/Q_{7-0}	Low Byte High Byte	D/Q_{7-0} D/Q_{7-0}	Low Byte High Byte
FQ271	D/Q_{7-0} D/Q_{6-0}	Low Byte High Byte	D/Q_{7-0} D/Q_{6-0}	Low Byte High Byte
FQ261	D/Q_{7-0} D/Q_{5-0}	Low Byte High Byte	D/Q_{7-0} D/Q_{5-0}	Low Byte High Byte

	FQ291	FQ281 FQ271 FQ261
Low Byte	DV = 7FH, if LOAD = 0 DV = FFH, if LOAD = 1	DV = 7FH, if LOAD = 0 DV = FFH, if LOAD = 1
Mid Byte	DV = 00H, if LOAD = 0 DV = 03H, if LOAD = 1	N/A
High Byte	DV = 00H	DV = 00H, if LOAD = 0 DV = 03H, if LOAD = 1

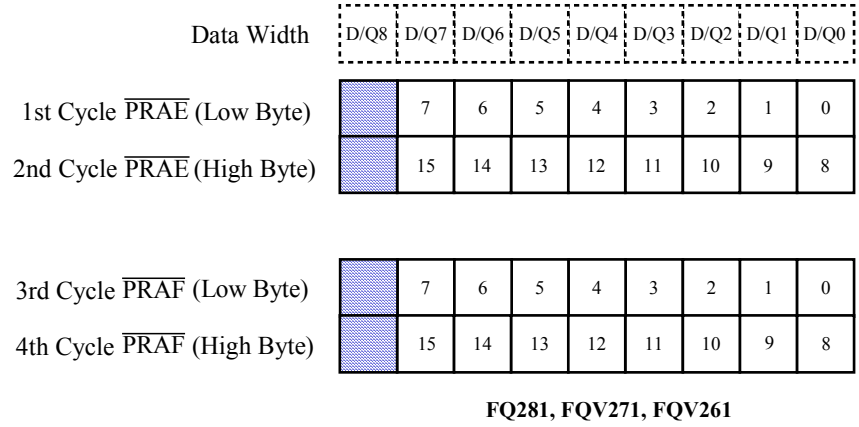
Table 6. Parallel Offset Register Data Mapping and Default Values

Device	Standard Mode	FWFT Mode
FQ291	131,072 x 9	131,073 x 9
FQ281	65,536 x 9	65,537 x 9
FQ271	32,768 x 9	32,769 x 9
FQ261	16,384 x 9	16,385 x 9

Table 7. Maximum Depth of Queue for Standard and FWFT Mode



FQ291



FQ281, FQV271, FQV261

# of Bits for Offset Registers
17 bits for FQ291 16 bits for FQ281 15 bits for FQ271 14 bits for FQ261
Note: Don't Care applies to all unused bits for both High Byte and Low Byte

Figure 8. Parallel Offset Write/Read Cycle Diagram

FQ291	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y[1]	H	H	H	L	H
(y+1) to 65,536	H	H	H	H	H
65,537 to [131,072-(x+1)]	H	H	L	H	H
(131,072-x[2]) to 131,071	H	L	L	H	H
131,072	L	L	L	H	H

FQ281	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y[1]	H	H	H	L	H
(y+1) to 32,768	H	H	H	H	H
32,769 to [65,536-(x+1)]	H	H	L	H	H
(65,536-x[2])to 65,535	H	L	L	H	H
65,536	L	L	L	H	H

FQ271	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y[1]	H	H	H	L	H
(y+1) to 16,384	H	H	H	H	H
16,385 to [32,768-(x+1)]	H	H	L	H	H
(32,768-x[2])to 32,767	H	L	L	H	H
32,768	L	L	L	H	H

FQ261	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y[1]	H	H	H	L	H
(y+1) to 8,192	H	H	H	H	H
8,193 to [16,384-(x+1)]	H	H	L	H	H
(16,384 –x[2])to 16,383	H	L	L	H	H
16,384	L	L	L	H	H

NOTES:
1. y = $\overline{\text{PRAE}}$ offset; Default Values: y = 127 when parallel offset loading is selected or y = 1,023 when serial offset loading is selected.
2. x = $\overline{\text{PRAF}}$ offset; Default Values: x = 127 when parallel offset loading is selected or x = 1,023 when serial offset loading is selected.

Table 8. Status Flags (Standard Mode)

FQ291	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 65,537	L	H	H	H	L
65,538 to [131,073-(x+1)]	L	H	L	H	L
(131,073-x[2]) to 131,072	L	L	L	H	L
131,073	H	L	L	H	L

FQ281	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 32,769	L	H	H	H	L
32,770 to [65,537-(x+1)]	L	H	L	H	L
(65,537-x [2])to 65,536	L	L	L	H	L
65,537	H	L	L	H	L

FQ271	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 16,385	L	H	H	H	L
16,386 to [32,769-(x+1)]	L	H	L	H	L
(32,768-x[2]) to 32,768	L	L	L	H	L
32,769	H	L	L	H	L

FQ261	$\overline{DRDY}$	$\overline{PRAF}$	$\overline{HALF}$	$\overline{PRAE}$	$\overline{QRDY}$
0	L	H	H	L	H
1 to y[1]	L	H	H	L	L
(y+2) to 8,193	L	H	H	H	L
8,192 to [16,385-(x+1)]	L	H	L	H	L
(16,384 -x[2]) to 16,384	L	L	L	H	L
16,385	H	L	L	H	L

NOTES:
1. y = $\overline{PRAE}$ offset; Default Values: y = 127 when parallel offset loading is selected or y = 1,023 when serial offset loading is selected.
2. x = $\overline{PRAF}$ offset; Default Values: x = 127 when parallel offset loading is selected or x = 1,023 when serial offset loading is selected.

Table 9. Status Flags (FWFT Mode)

Timing Diagrams

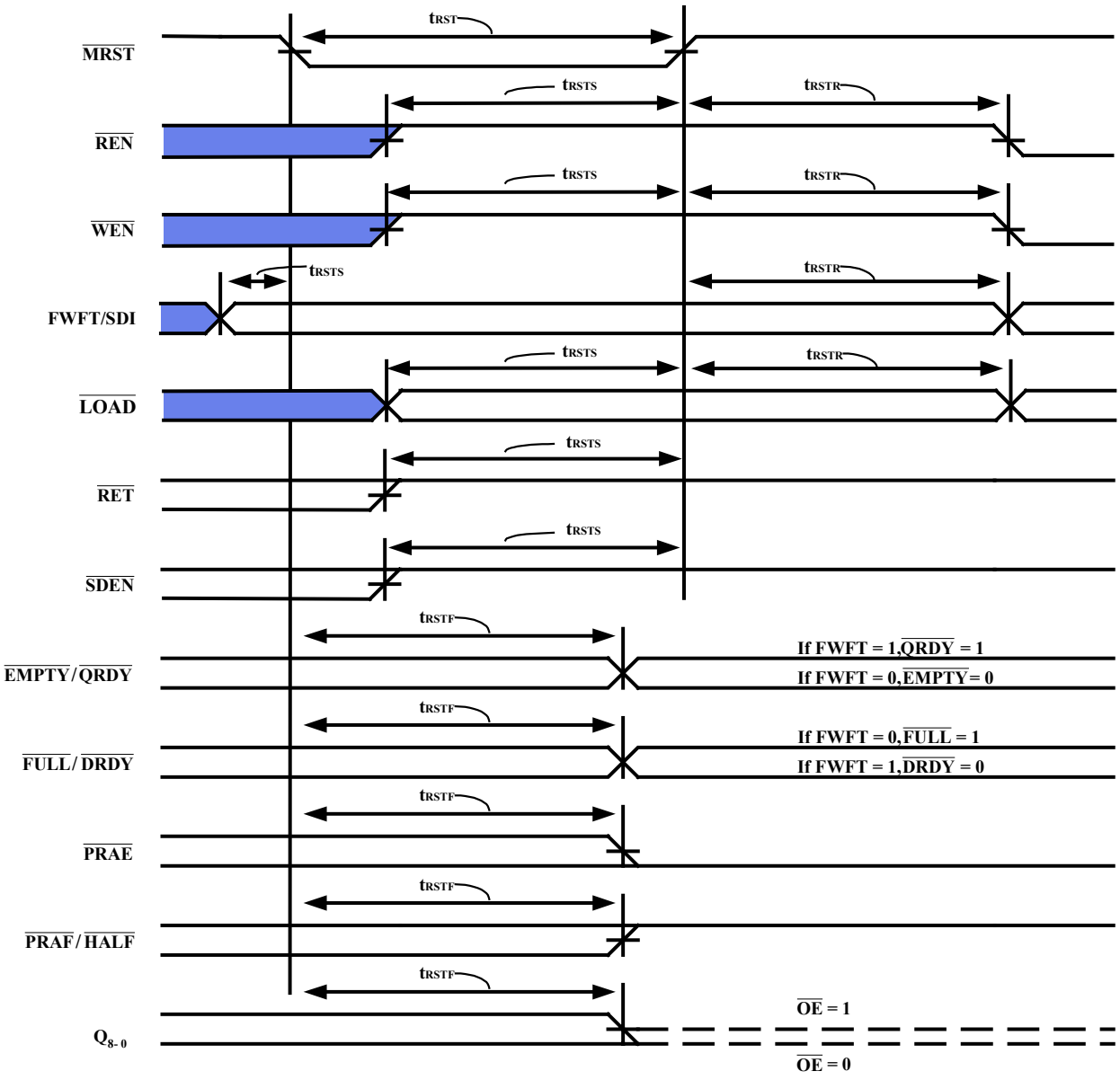


Diagram 1. Master Reset Timing

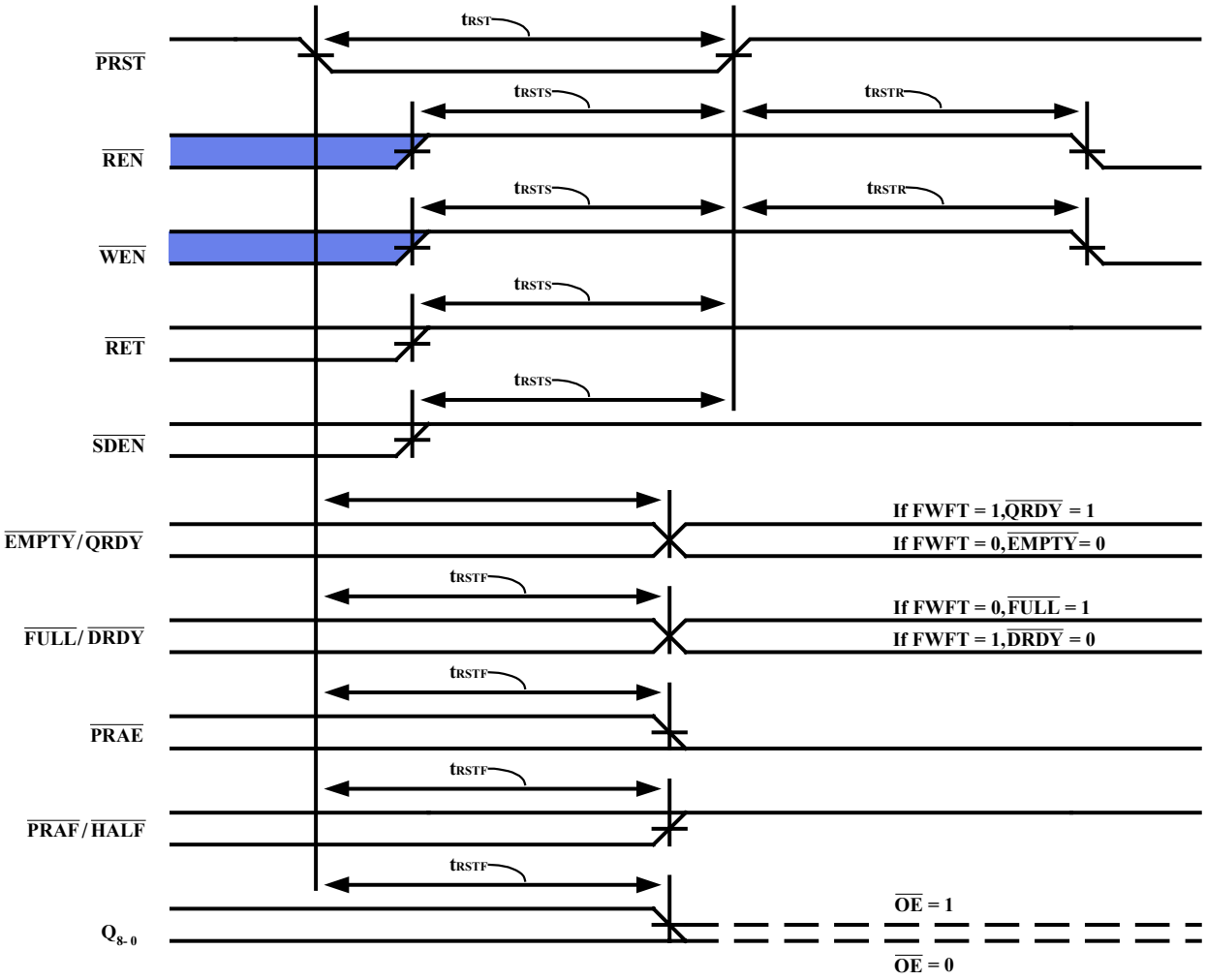


Diagram 2. Partial Reset Timing

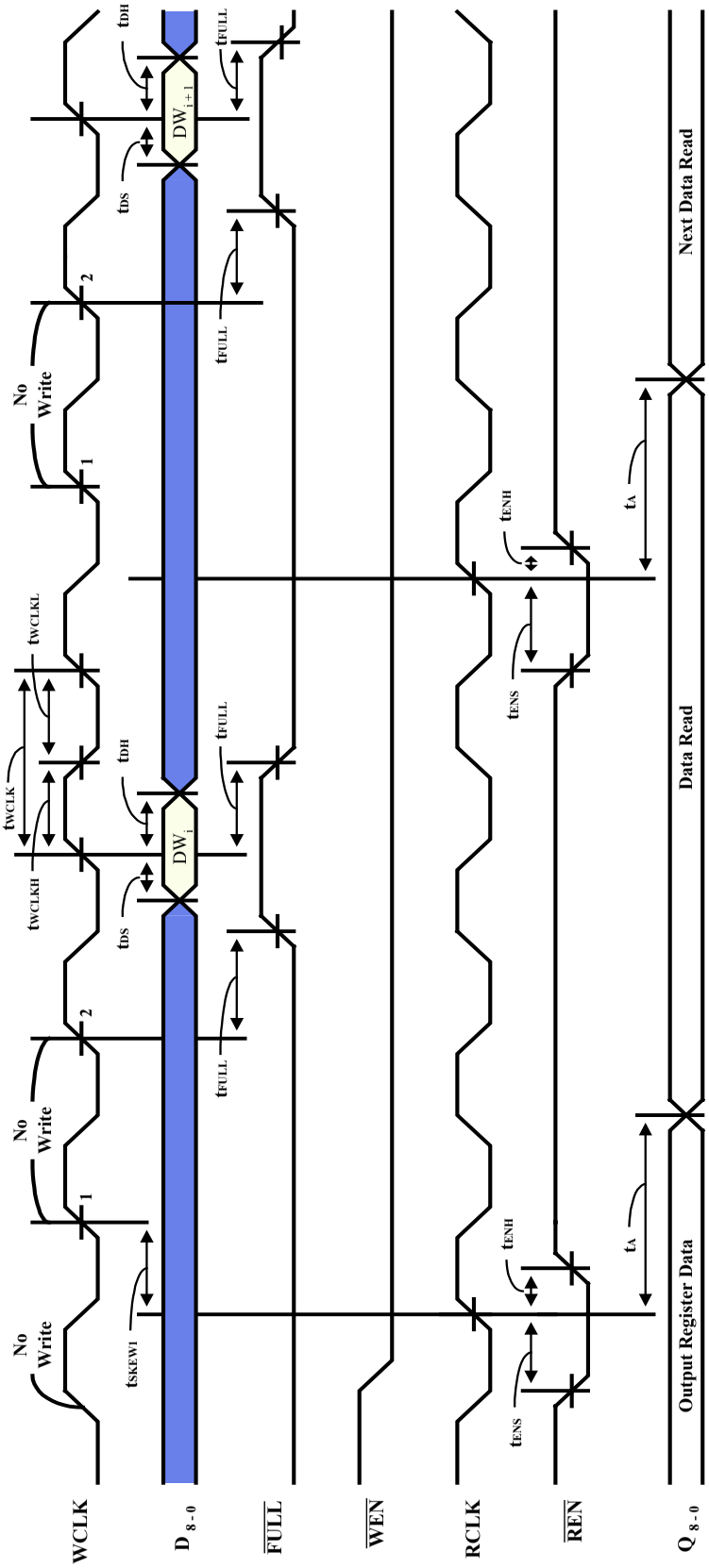
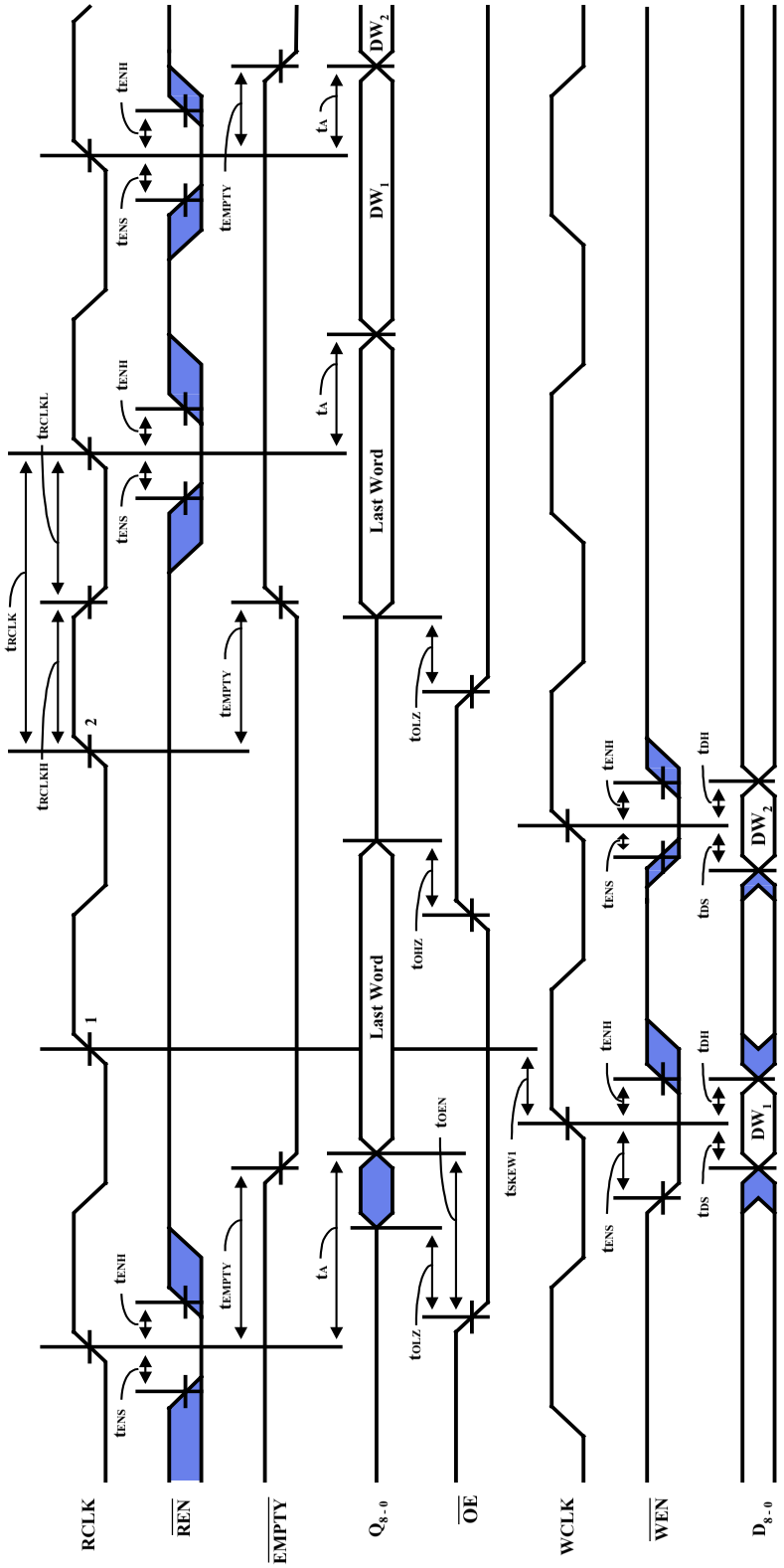


Diagram 3. Write Cycle and Full Flag Timing (Standard Mode)

NOTES:

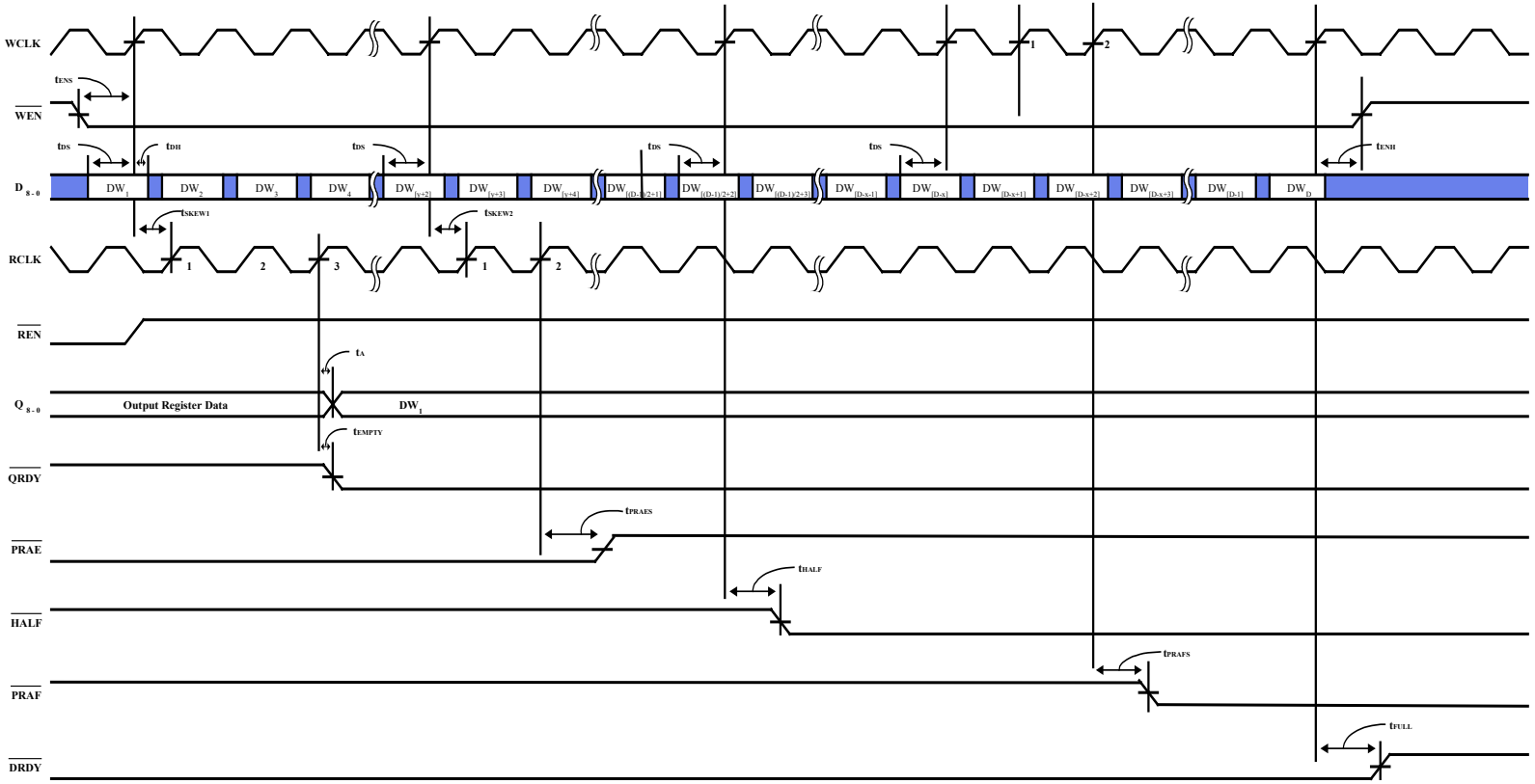
1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW1}, $\overline{FULL}$ will go high (after one WCLK cycle plus t_{FULL}). If t_{SKEW1} is not met, then $\overline{FULL}$ will assert 1 or more WCLK cycles.
2. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.



NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW1}, $\overline{EMPTY}$ will go high (after RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.
2. $\overline{LOAD}$ = High.
3. First word latency: $t_{SKEW1} + t_{EMPTY} + 1 * t_{RCLK}$.

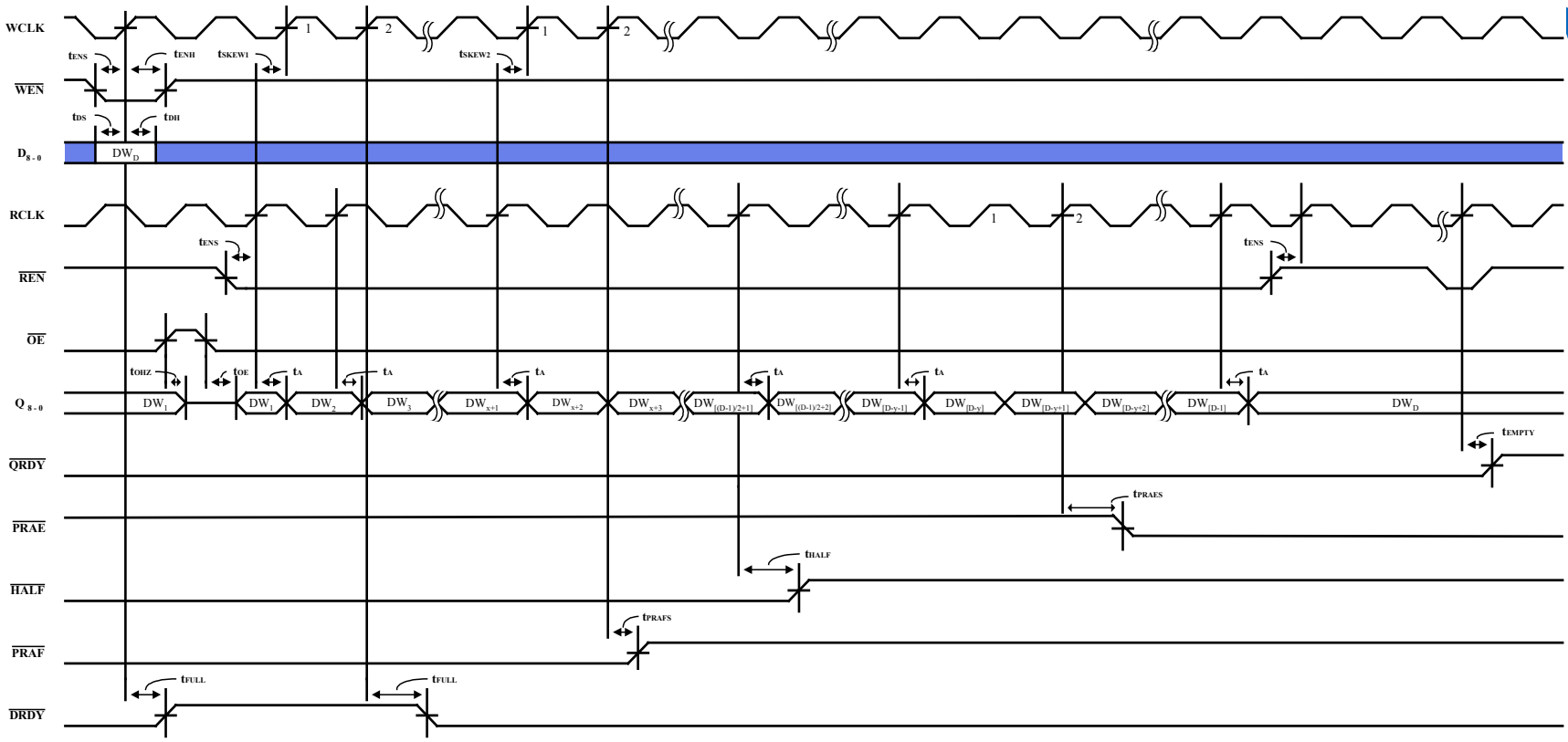
Diagram 4. Read Cycle, Empty Flag and First Data Word Latency Timing (Standard Mode)



NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW1}, $\overline{QRDY}$ will go low (after two RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{QRDY}$ will assert 1 or more RCLK cycles.
2. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW2}, $\overline{PRAE}$ will go high (after one RCLK cycle plus t_{PRAES}). If t_{SKEW2} is not met, then $\overline{PRAE}$ will assert 1 or more RCLK cycles.
3. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.
4. y = $\overline{PRAE}$ offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 7 for Depth.
6. First word latency: $t_{SKEW1} + t_{EMPTY} + 2 * t_{RCLK}$

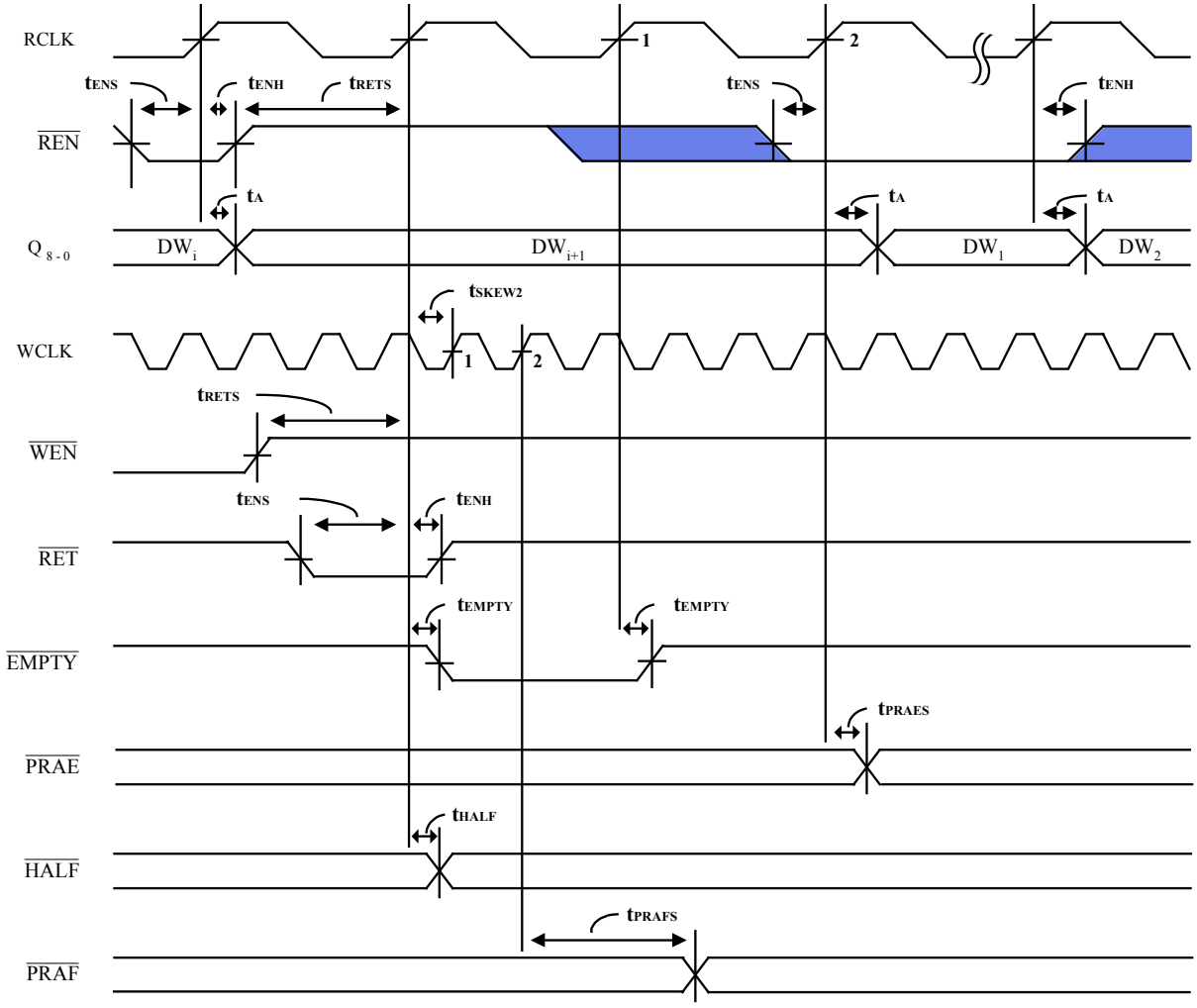
Diagram 5. Write Timing (FWFT Mode)



NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW1}, $\overline{QRDY}$ will go low (after two RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{QRDY}$ will assert 1 or more RCLK cycles.
2. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW2}, $\overline{PRAE}$ will go high (after one RCLK cycle plus t_{PRAES}). If t_{SKEW2} is not met, then $\overline{PRAE}$ will assert 1 or more RCLK cycles.
3. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.
4. y = $\overline{PRAE}$ offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 7 for Depth.
6. First word latency: $t_{SKEW1} + t_{EMPTY} + 2 * t_{RCLK}$

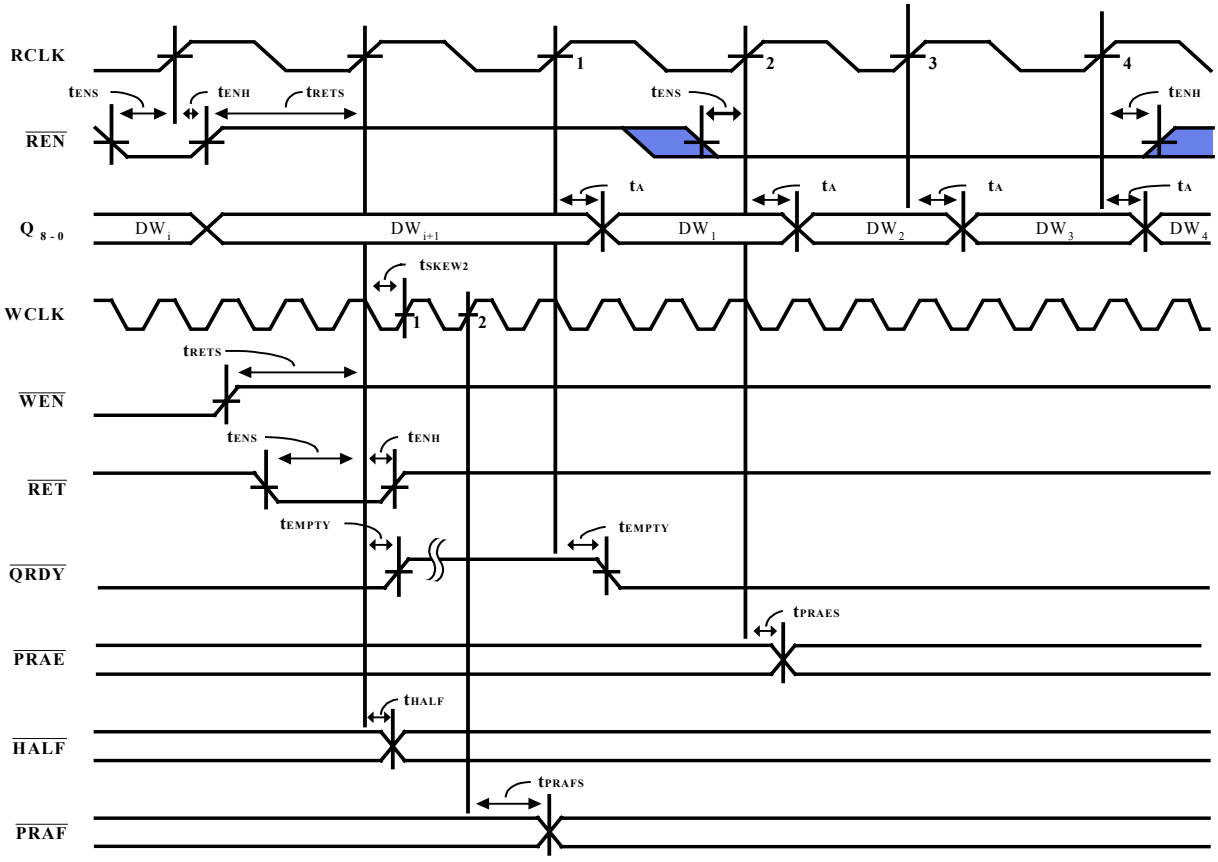
Diagram 6. Read Timing (FWFT Mode)



NOTES:

1. Upon completion of retransmit setup, a read operation can begin only after $\overline{\text{EMPTY}}$ returns high.
2. $\overline{\text{OE}}$ = Low.
3. DW_i = Words written to the queue after $\overline{\text{MRST}}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than 2 words written to the queue for a retransmit setup to be valid.
5. $\overline{\text{EMPTY}}$ goes high at 1 RCLK cycle + t_{EMPTY}.

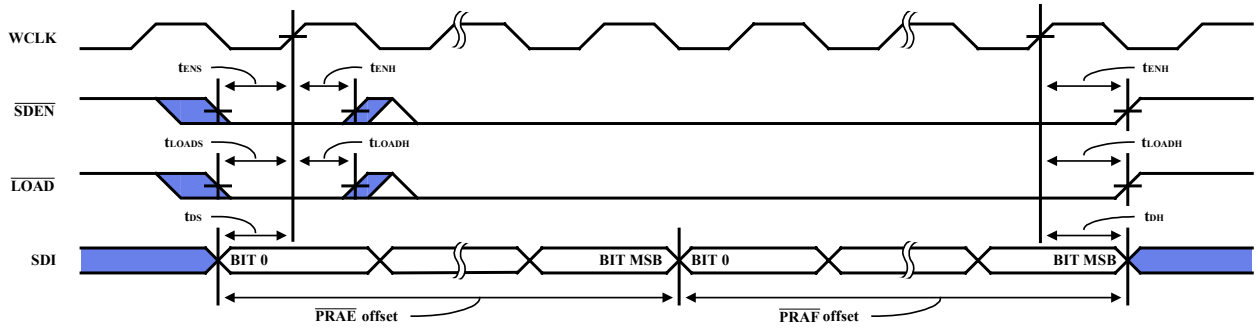
Diagram 7. Retransmit Timing (Standard Mode)



NOTES:

1. Upon completion of retransmit setup, a read operation can begin only after $\overline{QRDY}$ returns low.
2. $\overline{OE}$ = Low.
3. DW_i = Words written to the queue after $\overline{MRST}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than 2 words written to the queue for a retransmit setup to be valid.
5. Please refer to Table 7 for Depth.
6. D = 65,536 for all devices.
7. $\overline{EMPTY}$ goes high at 1 RCLK cycle + t_{EMPTY}.

Diagram 8. Retransmit Timing (FWFT Mode)



*Refer to Table 10.

Diagram 9. Serial Loading of Programmable Flag Registers (Standard and FWFT Mode)

	FQV291	FQV281	FQV271	FQV261
MSB	16	15	14	13

Table 10. Reference Table for Diagram 9

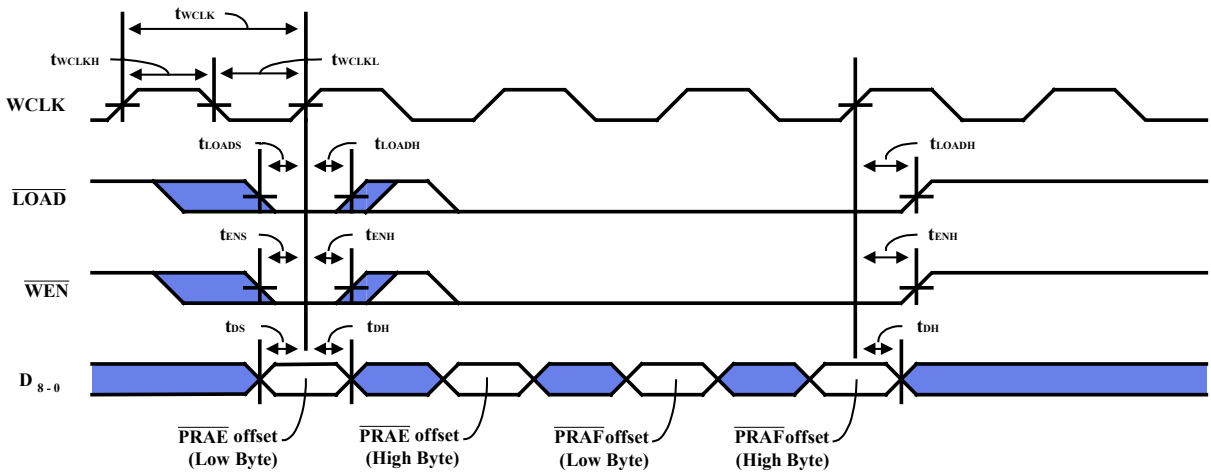


Diagram 10. Parallel Loading of Programmable Flag Registers for FQ281, FQ271 and FQ261 (Standard and FWFT Mode)

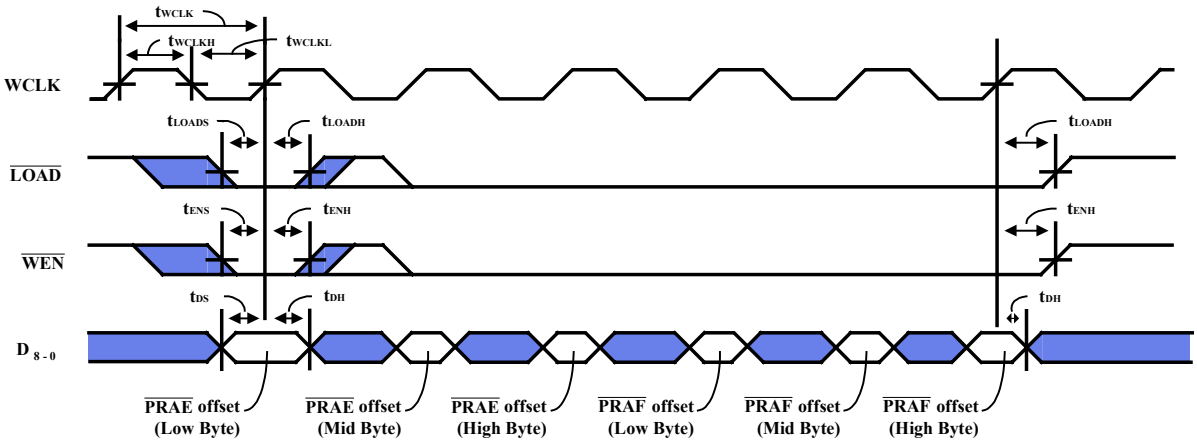


Diagram 11. Parallel Loading of Programmable Flag Registers for FQ291 (Standard and FWFT Mode)

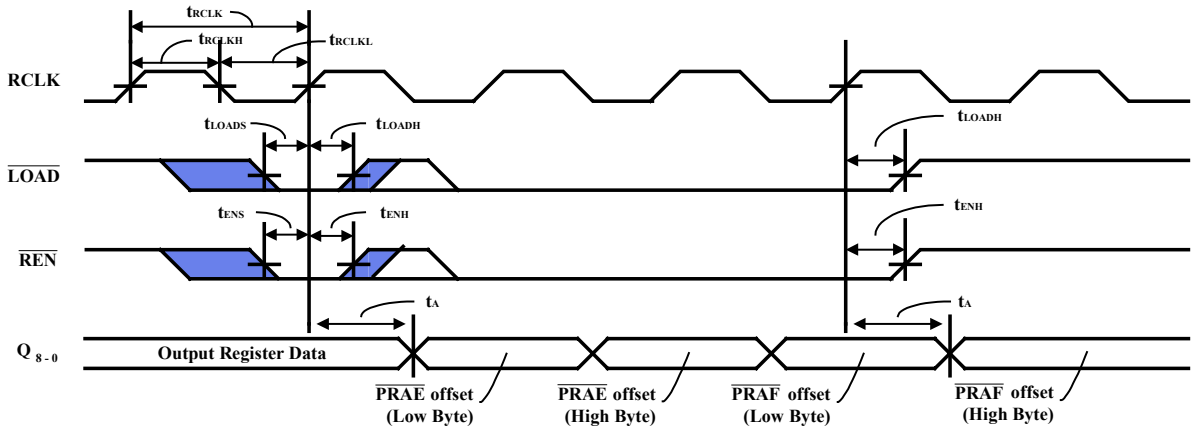


Diagram 12. Parallel Read of Programmable Flag Registers for FQ281, FQ271 and FQ261 (Standard and FWFT Mode)

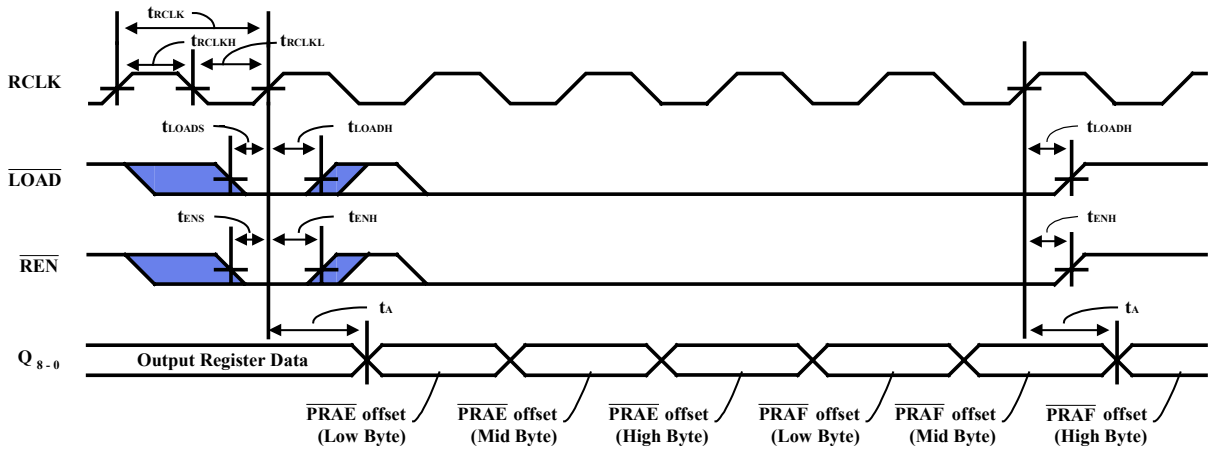
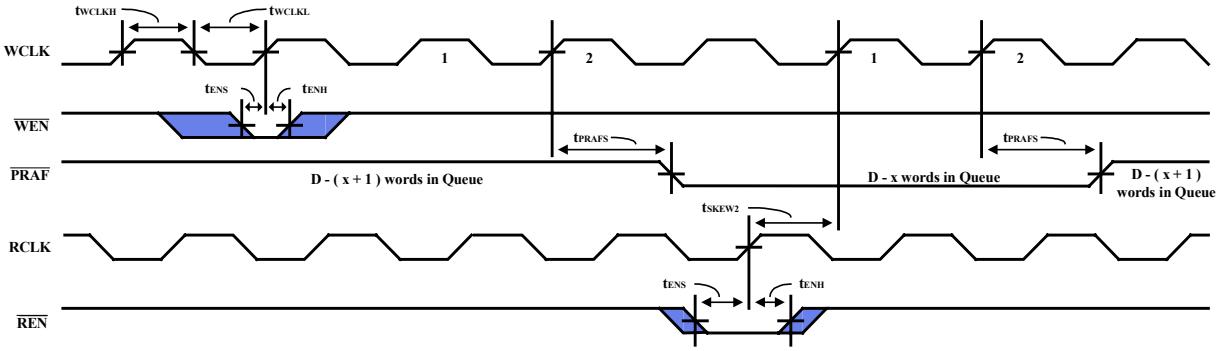
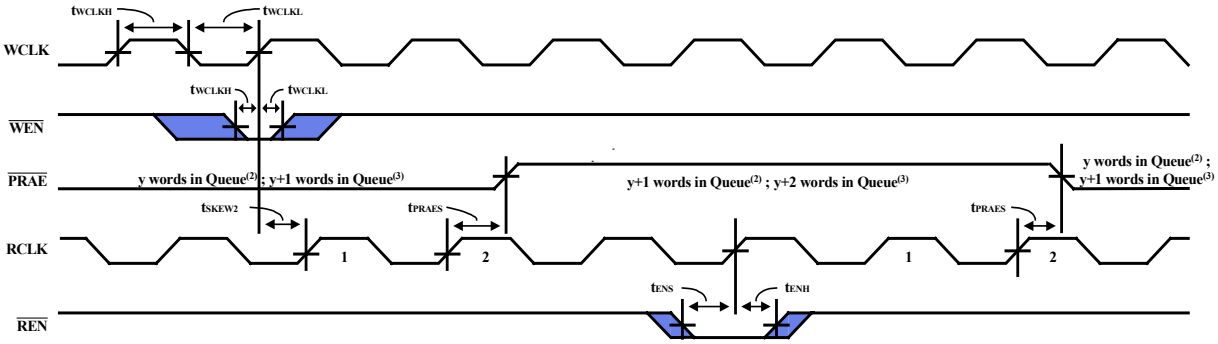


Diagram 13. Parallel Read of Programmable Flag Registers for FQ291 (Standard and FWFT Mode)



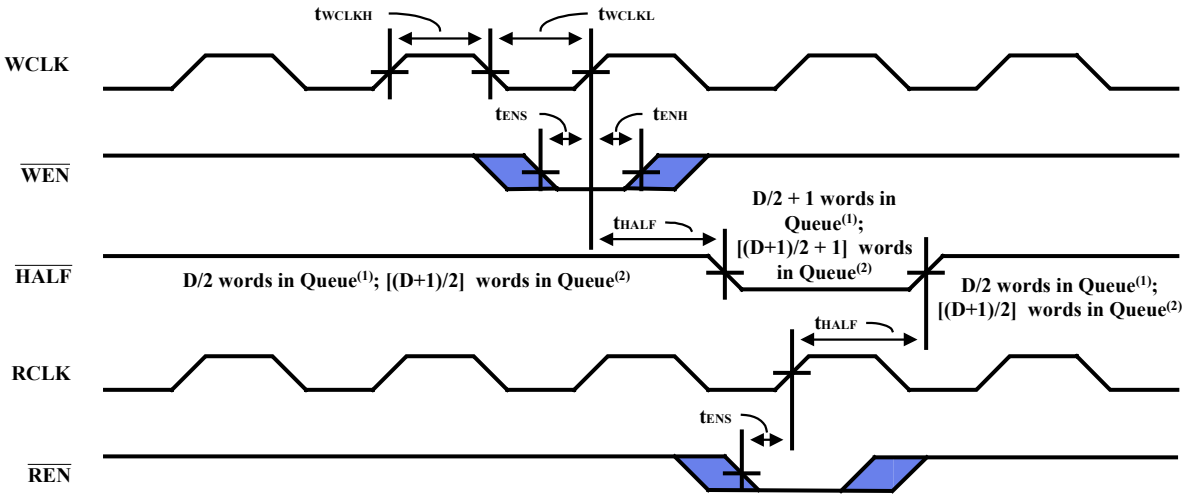
NOTES:
1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth. Please refer to Table 7 for Depth.
3. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW2}, $\overline{\text{PRAF}}$ will go high (after on WCLK cycle plus t_{PRAFS}). If t_{SKEW2} is not met, then $\overline{\text{PRAF}}$ will assert 1 or more WCLK cycles.
4. $\overline{\text{PRAF}}$ synchronizes to the rising edge of WCLK only.

Diagram 14. Synchronous Programmable Almost-Full Flag Timing (Standard and FWFT Mode)



NOTES:
1. y = $\overline{\text{PRAE}}$ offset.
2. For Standard Mode.
3. For FWFT Mode.
4. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW2}, $\overline{\text{PRAE}}$ will go high (after one RCLK cycle plus t_{PRAES}). If t_{SKEW2} is not met, then $\overline{\text{PRAE}}$ will assert 1 or more RCLK cycles.
5. $\overline{\text{PRAE}}$ synchronizes to the rising edge of RCLK only.

Diagram 15. Synchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Mode)



NOTES:
1. For Standard Mode.
2. For FWFT Mode.
3. Refer to Table 7 for Depth.

Diagram 16. Half-Full Flag Timing (Standard and FWFT Mode)

Order Information:

HBA Device Family	Device Type	Power	Speed (ns)*	Package**	Temperature Range
XX	XXX	X	XX	XX	X
FQ	**291** (131,072 x 9)	Low	**10** – 100 MHz	**PF**	Blank – Commercial (0°C to 70°C)
	281 (65,536 x 9)		**15** – 66 MHz	**TF**	**I** – Industrial (-40° to 85°C)
	271 (32,768 x 9)		**20** – 50 MHz		
	261 (16,384 x 9)				

***Speed –** Slower speeds available upon request.
****Package** – 64 pin Plastic Thin Quad Flat Pack (TQFP), 64 pin Slim Thin Quad Flat Pack (STQFP)

Example:

FQ281L10TF (64k x 9, 10ns, Commercial temp)
FQ271L20PFI (32k x 9, 20ns, Industrial temp)

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