

AZP92

PECL/ECL $\div 1$, $\div 2$ Clock Generation Chip with Selectable Enable

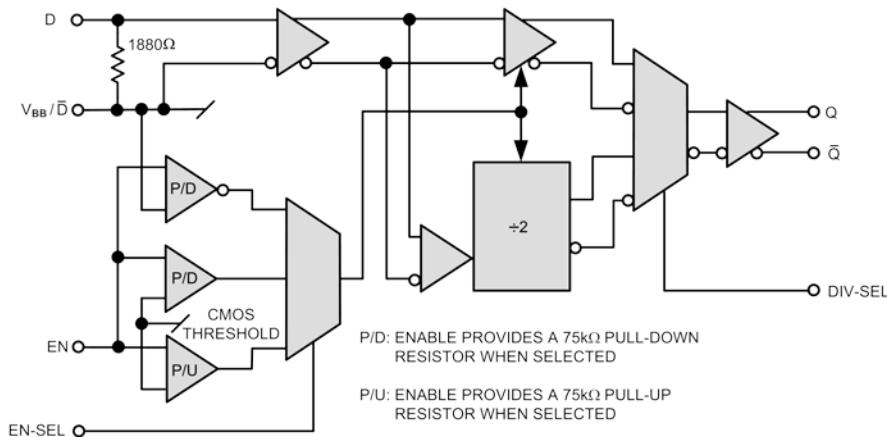
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DESCRIPTION

The [AZP92](#) is a $\div 1$ or $\div 2$ clock generation part specifically designed to accommodate Colpitts or Pierce based oscillators. Features are incorporated to reduce board components. A voltage reference and input biasing allows for easy oscillator interface.

The AZP92 provides a $\div 2$ mode of operation for more frequency options and is selectable with a single connection. A selectable enable is also provided which doubles as a reset when the AZP92 is in $\div 2$ mode. With a single connection, the enable can be selected to operate as active high or active low.

BLOCK DIAGRAM



FEATURES

- 3.0V to 5.5V Operation
- Selectable Divide Ratio
- Selectable Enable Polarity and Threshold (CMOS or PECL)
- High Bandwidth
 - 1.5+ GHz ($\div 1$)
 - 3.0+ GHz ($\div 2$)
- -145 dBc/Hz ($\div 1$) Typical Noise Floor
- -151 dBc/Hz ($\div 2$) Typical Noise Floor

APPLICATIONS

- Colpitts or Pierce based oscillators

PACKAGE AVAILABILITY

- MLP8
 - Green/RoHS Compliant/Pb-Free

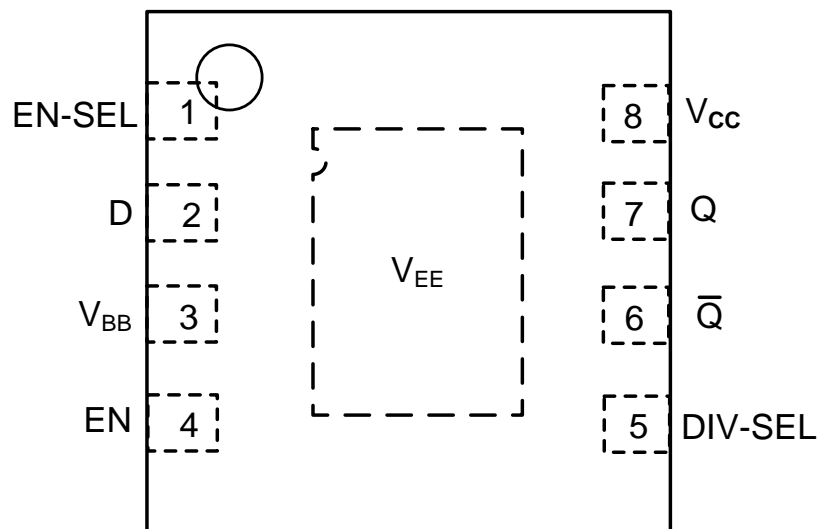
Part Number (PN)	Package	Marking
AZP92NAG ¹	MLP8	PIG <Date Code> ²

¹ [Tape & Reel](#) - Add 'R1' at end of PN for 7in (1k parts), 'R2' (2.5k) for 13in

² See www.azmicrotek.com for [date code format](#)

PIN DESCRIPTION AND CONFIGURATION**Table 1 - Pin Description**

Pin	Name	Type	Function
1	EN-SEL	Input	Enable Polarity Select
2	D	Input	Data Input
3	V _{BB}	Input	Reference Voltage
4	EN	Input	Output Enable
5	DIV-SEL	Input	Divide Select
6	Q̄	Output	Inverted PECL Output
7	Q	Output	PECL Output
8	V _{CC}	Power	Positive Supply
9	V _{EE}	Power	Negative Supply

**Figure 1 - Pin Configuration**

ENGINEERING NOTES

The AZP92 is a specialized $\div 1$ or $\div 2$ clock generation part including an enable/reset function. The divide ratio is selected with the DIV-SEL pin/pad. When DIV-SEL is open (NC), the AZP92 functions as a standard receiver. If DIV-SEL is connected to V_{EE} , it functions as a $\div 2$ divider.

A selectable enable is provided which also functions as a reset when the $\div 2$ mode is selected. Enable (EN) functionality is selected with the EN-SEL pin/pad which has three valid states: open (NC), V_{EE} , or connected to V_{EE} via a 20k Ω resistor. Leaving EN-SEL open or connecting it to V_{EE} will select the EN pin/pad to function as an active high CMOS/TTL enable. When EN-SEL is open, an internal 75k Ω pull-up resistor is selected which enables the outputs whenever EN is left open. When EN-SEL is connected to V_{EE} , an internal 75k Ω pull-down resistor is selected which disables the outputs whenever EN is left open.

Connecting the EN-SEL to V_{EE} with a 20k Ω resistor will select the EN pin/pad to function as an active low PECL/ECL enable with an internal 75k Ω pull-down resistor. In this mode, outputs are enabled when EN is left open (NC). This default logic condition can be overridden by connecting the EN to V_{CC} with an external resistor of $\leq 20k\Omega$. Refer to the enable truth table on the next page for detailed operation.

The AZP92 provides a V_{BB} with an 1880 Ω internal bias resistor from D to V_{BB} . This feature allows AC coupling with minimal external components. The V_{BB} pin supports 1.5mA sink/source current and should be bypassed to ground or V_{CC} with a 0.01 μ F capacitor.

Table 2 - Divide Truth Table

DIV-SEL	\div -Ratio
NC	$\div 1$
V_{EE} ¹	$\div 2$

¹ DIV-SEL connection must be $\leq 1\Omega$.

Table 3 - Enable Truth Table

EN-SEL	EN	Q	Q
NC	CMOS Low or V_{EE}	Low	High
	CMOS High, V_{CC} or NC	Data	Data
V_{EE}	CMOS Low, V_{EE} or NC	Low	High
	CMOS High or V_{CC}	Data	Data
20k Ω to V_{EE}	PECL Low, V_{EE} or NC	Low	High
	PECL High or V_{CC}	Data	Data

Figure 2 illustrates the timing sequences for the AZP92 in the $\div 1$ mode which is determined by leaving the DIV-SEL open (NC). It also illustrates the enable in the active High mode being controlled by a CMOS signal. This mode is determined by leaving the EN-SEL open (NC).

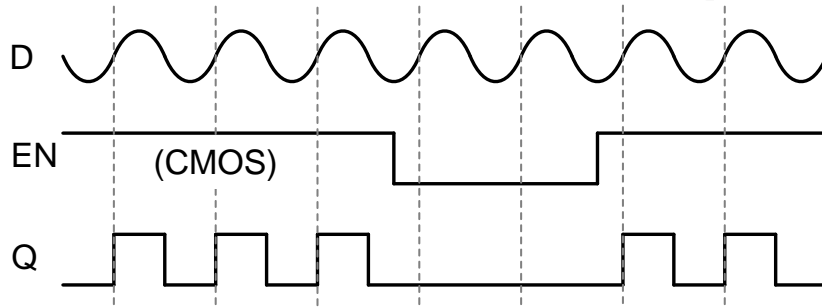


Figure 2 - Timing Diagram

Figure 3 illustrates the timing sequences for the AZP92 in the $\div 2$ mode which is determined by connecting the DIV-SEL to V_{EE} . It also illustrates the enable in the active Low mode being controlled by a PECL signal. This mode is determined by connecting the EN-SEL to V_{EE} via 20k Ω resistor.

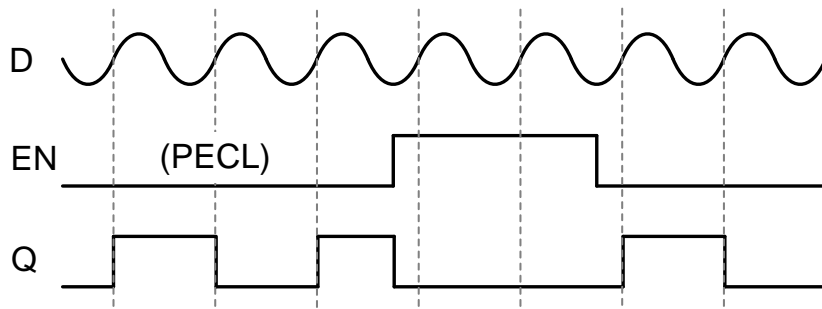


Figure 3 - Timing Diagram

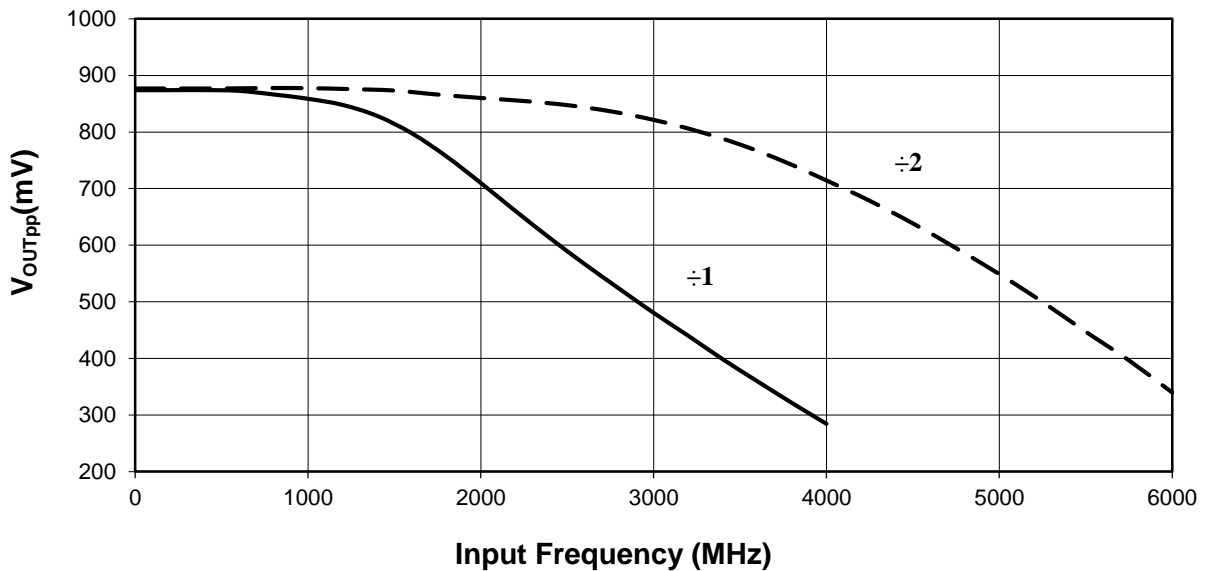


Figure 4 - Typical Large Signal Output Swing

Measured with 750mv D input, Q/Q each terminated to $V_{CC}-2V$ via 50 Ω resistors

PERFORMANCE DATA**Table 4 - Absolute Maximum Ratings**

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V _{CC}	PECL Power Supply	V _{EE} = 0V	0 to + 6.0	V
V _{I,PECL}	PECL Input Voltage	V _{EE} = 0V	0 to + 6.0	V
V _{EE}	ECL Power Supply	V _{CC} = 0V	-6.0 to 0	V
V _{I,ECL}	ECL Input Supply	V _{CC} = 0V	-6.0 to 0	V
I _{HGOUT}	Output Current	Continuous	50	mA
		Surge	100	
T _A	Operating Temperature Range	-	-40 to +85	°C
T _{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD _{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD _{MM}	Machine Model Electro Static Discharge	-	200	V
ESD _{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

Table 5 - 100K ECL DC Characteristics

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage ¹	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V _{OL}	Output LOW Voltage ¹	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V _{IH}	Input HIGH Voltage D,EN (ECL) ²	-1165	-390	-1165	-390	-1165	-390	-1165	-390	mV
	Input HIGH Voltage EN (CMOS) ³	V _{EE} + 2000	V _{CC}	V _{EE} + 2000	V _{CC}	V _{EE} + 2000	V _{CC}	V _{EE} + 2000	V _{CC}	mV
V _{IL}	Input LOW Voltage D,EN (ECL) ²	-2250	-1475	-2250	-1475	-2250	-1475	-2250	-1475	mV
	Input LOW Voltage EN (CMOS) ³	V _{EE}	V _{EE} + 800	V _{EE}	V _{EE} + 800	V _{EE}	V _{EE} + 800	V _{EE}	V _{EE} + 800	mV
V _{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I _{IH}	Input HIGH Current EN		150		150		150		150	μA
I _{IL}	Input LOW Current EN (ECL) ²	0.5		0.5		0.5		0.5		μA
	Input LOW Current EN (CMOS) ³	-150		-150		-150		-150		
I _{EE}	Power Supply Current ⁴		31		31		31		34	mA

¹ Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

² EN-SEL connected to V_{EE} through a 20kΩ resistor

³ EN-SEL connected to V_{EE} or left open (NC)

⁴ DIV-SEL left open (NC)

Table 6 - 100K LVPECL DC Characteristics

100K LVPECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +3.3\text{V}$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	2215	2420	2275	2420	2275	2420	2275	2420	mV
V_{OL}	Output LOW Voltage ^{1,2}	1400	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage D,EN (ECL) ³	2135	2910	2135	2910	2135	2910	2135	2910	mV
	Input HIGH Voltage EN (CMOS) ⁴	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D,EN (ECL) ³	1050	1825	1050	1825	1050	1825	1050	1825	mV
	Input LOW Voltage EN (CMOS) ⁴	GND	800	GND	800	GND	800	GND	800	mV
V_{BB}	Reference Voltage ¹	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	μA
I_{IL}	Input LOW Current EN (ECL) ³	0.5		0.5		0.5		0.5		μA
	Input LOW Current EN (CMOS) ⁴	-150		-150		-150		-150		
I_{EE}	Power Supply Current ⁵		31		31		31		34	mA

¹ For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value

² Specified with each output terminated through 50 Ω resistors to $V_{CC} - 2\text{V}$.

³ EN-SEL connected to V_{EE} through a 20k Ω resistor

⁴ EN-SEL connected to V_{EE} or left open (NC)

⁵ DIV-SEL left open (NC)

Table 7 - 100K PECL DC Characteristics

100K PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage ^{1,2}	3100	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage D,EN (ECL) ³	3835	4610	3835	4610	3835	4610	3835	4610	mV
	Input HIGH Voltage EN (CMOS) ⁴	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D,EN (ECL) ³	2750	3525	2750	3525	2750	3525	2750	3525	mV
	Input LOW Voltage EN (CMOS) ⁴	GND	800	GND	800	GND	800	GND	800	mV
V_{BB}	Reference Voltage ¹	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	μA
I_{IL}	Input LOW Current EN (ECL) ³	0.5		0.5		0.5		0.5		μA
	Input LOW Current EN (CMOS) ⁴	-150		-150		-150		-150		
I_{EE}	Power Supply Current ⁵		31		31		31		34	mA

¹ For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value

² Specified with each output terminated through 50 Ω resistors to $V_{CC} - 2\text{V}$.

³ EN-SEL connected to V_{EE} through a 20k Ω resistor

⁴ EN-SEL connected to V_{EE} or left open (NC)

⁵ DIV-SEL left open (NC)

Table 8 - AC Characteristics

AC Characteristics ($V_{EE} = -3.0\text{V}$ to -5.5V ; $V_{CC} = \text{GND}$ or $V_{EE} = \text{GND}$; $V_{CC} = +3.0\text{V}$ to $+5.5\text{V}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Delay													
	D to Q/Qb ¹			450			450			450			450	ps
	D to Q _{HG} /Q _{bHG} ¹			600			600			600			600	ps
t_{SKEW}	Duty Cycle Skew ²		5	20		5	20		5	20		5	20	ps
V_{pp} (AC)	Input Swing ³ Differential	150		1000	150		1000	150		1000	150		1000	mV
	Input Swing ³ Single Ended	300		2000	300		2000	300		2000	300		2000	
t_r/t_f	Output Rise/Fall ¹ (20% - 80%)	80		200	80		200	80		200	80		200	ps

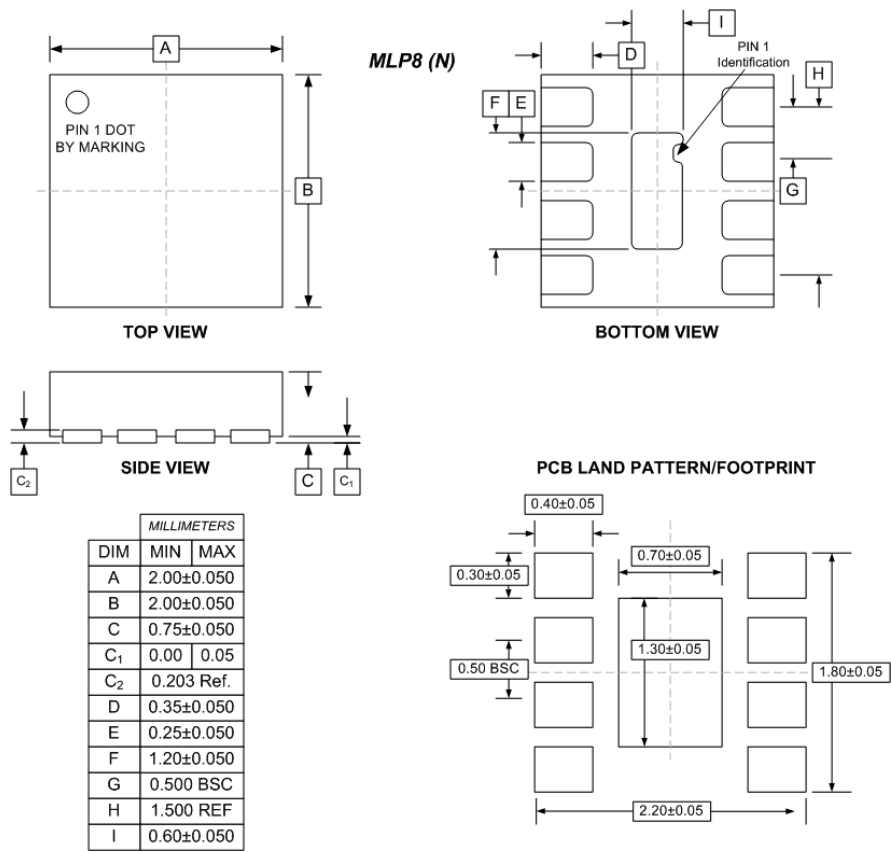
¹ Specified with each output terminated through 50 Ω resistors to $V_{CC} - 2\text{V}$.

² Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

³ V_{pp} is the peak-to-peak differential input swing for which AC parameters are guaranteed.

⁴ Range valid for AC coupled signals only

PACKAGE DIAGRAM
MLP8
Green/RoHS compliant/Pb-Free
MSL=1



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