AZEBP53Q

Evaluation Board for AZP53 Low Phase Noise Buffers

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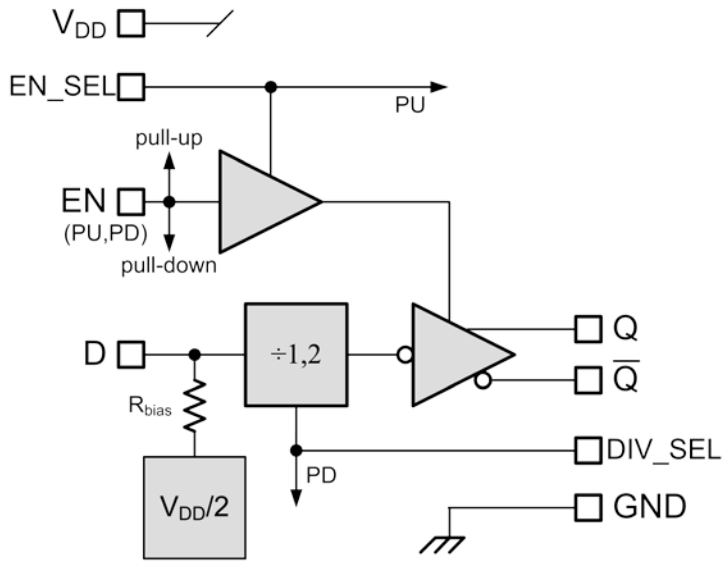
DESCRIPTION

The AZEBP53Q evaluation board is a multi-layer PCB assembly containing the AZP53 low phase noise buffer and supporting components. They provide an excellent platform for initial design verification and validation of phase noise. All signal paths are designed for 50Ω impedance matched operation.

The AZP53 is a sine wave/CMOS to LVPECL buffer/divider optimized for very low phase noise (-165dBc/Hz). It is particularly useful in converting crystal or SAW based oscillators into LVPECL outputs for up 800MHz of bandwidth. For greater bandwidth, refer to the AZP63.

The AZP53 is one of a family of parts that provide options of fixed ÷1, fixed ÷2 and selectable ÷1, ÷2 modes as well as active high enable or active low enable to oscillator designers. Refer to Table 2 for the comparison of parts within the AZP5x and AZP63 family.

BLOCK DIAGRAM



FEATURES

- LVPECL outputs optimized for very low phase noise (-165dBc/Hz)
- Up to 800MHz bandwidth
- Selectable ÷1, ÷2 output
- Selectable Enable logic
- 3.0V to 3.6V operation

APPLICATIONS

- Converting crystal or SAW based oscillators to LVPECL output

BOARD CONFIGURATION

- Board is initially populated with a standard factory configuration as noted in this datasheet
- Board comes standard with an installed AZP53Q part
  - SON8 (1.5mm x 1.0mm)
  - Other packages available upon request

PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin Description for AZP53Q

Pin	Name	Type	Function
1	Q	Output	LVPECL Output
2	$\overline{Q}$	Output	LVPECL Output
3	EN	Input	Enable
4	GND	Power	Negative Supply
5	D	Input	Sine or CMOS Input
6	EN_SEL	Input	Enable Select
7	DIV_SEL	Input	Divide Select
8	V_{DD}	Power	Positive Supply

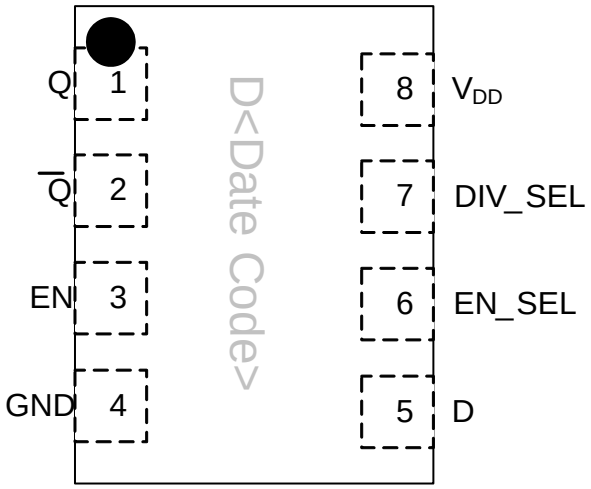


Figure 1 – Pin Configuration for AZP53Q

ENGINEERING NOTES

FUNCTIONALITY

The AZP53 is an instance of a family of parts that provide options of fixed ÷1, fixed ÷2 and selectable ÷1, ÷2 modes as well as active high enable or active low enable to oscillator designers. Table 2 details the differences between the parts to assist designers in selecting the optimal part for their design.

Table 3 lists the specific AZP53 functional operation.

Table 2 - AZP51-54 & AZP63 Family

Part Number	Divide Ratio	EN Logic	EN pull-up/pull-down	Bandwidth
AZP51	÷1	active HIGH	Pull-up	> 800MHz
AZP52	÷2	active HIGH	Pull-up	> 800MHz
AZP53	Selectable ÷1 or ÷2	selectable	selectable	> 800MHz
AZP54	÷1	active LOW	Pull-down	> 800MHz
AZP63	Selectable ÷1 or ÷2	selectable	selectable	≥ 1GHz

Table 3 - AZP53 Functional Operations, ÷1 mode

	Inputs			Outputs	
Part Number	**EN_SEL**	**EN**	**D**	**Q**	**$\overline{Q}$**
AZP53	High, NC[1]	Low, NC[1]	Low	Low	High
			High	High	Low
		High	X[2]	Z[3]	Z[3]
	Low	High, NC[1]	Low	Low	High
			High	High	Low
		Low	X[2]	Z[3]	Z[3]
	DIV_SEL			**Divide Ratio**	
	Low, NC[1]			÷1	
	High			÷2	

[1] Not connected

[2] Don't care

[3] Tri-State

EVALUATION BOARD

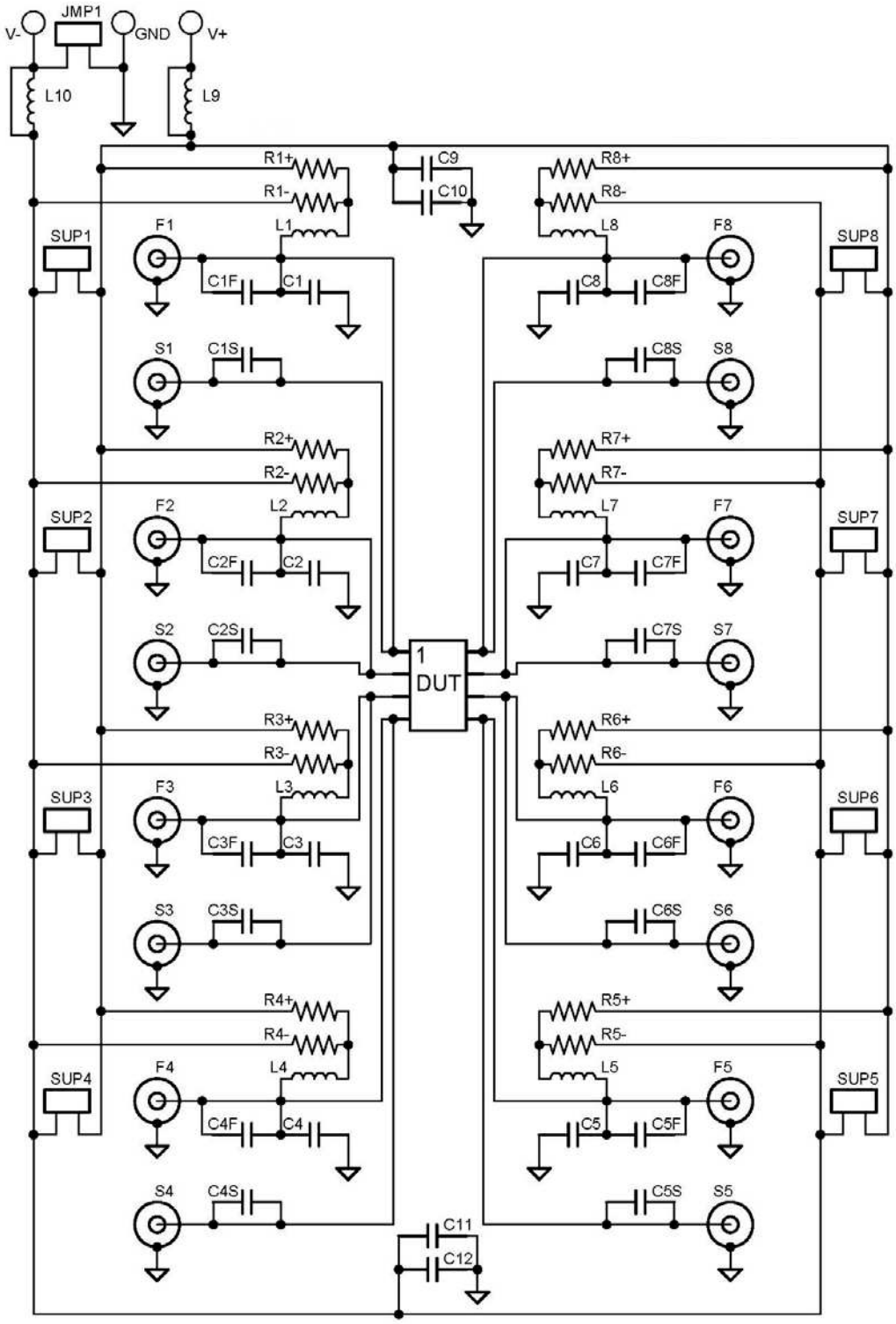


Figure 2 - Evaluation Board Schematic

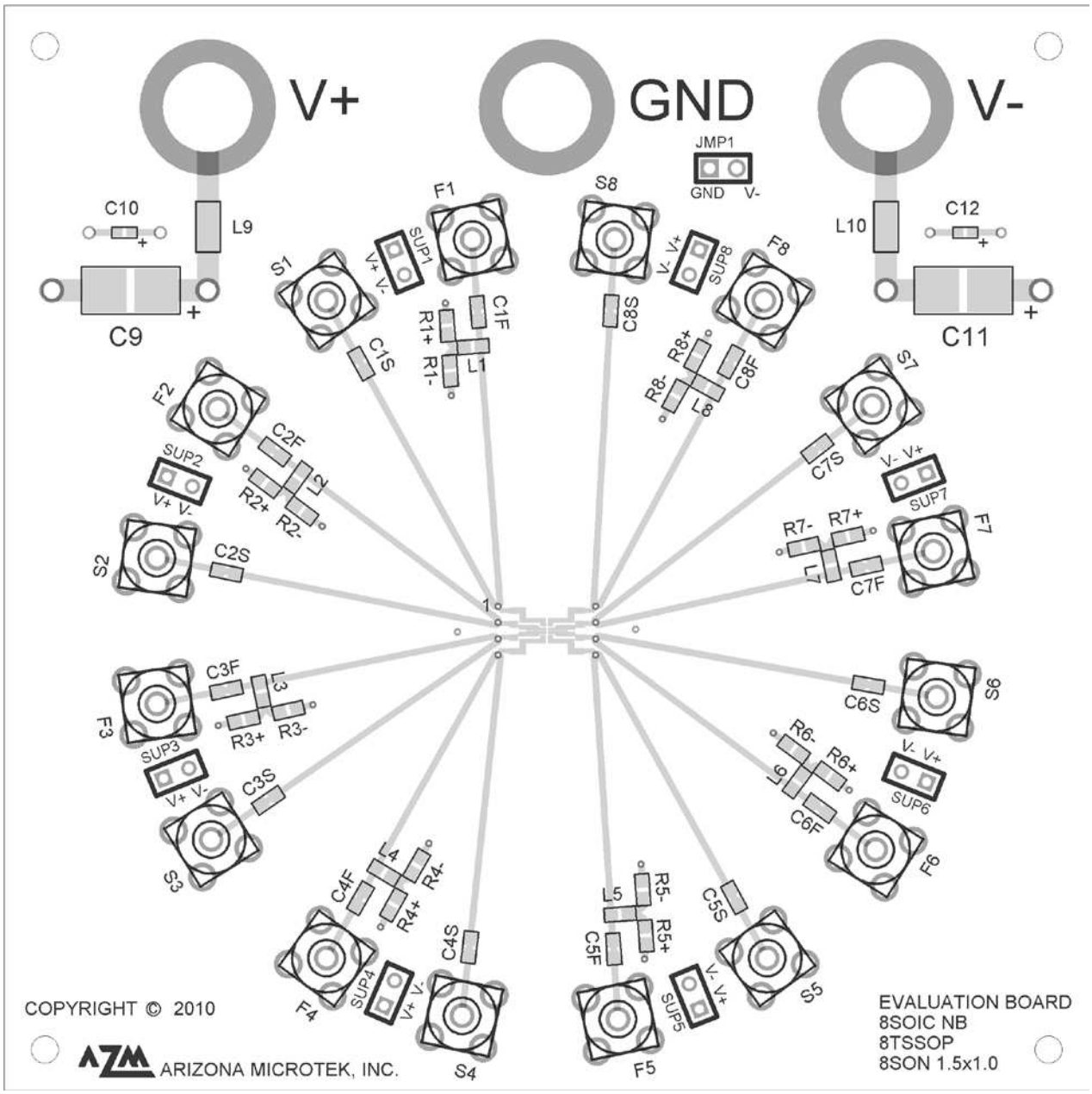


Figure 3 - Evaluation Board, Top View

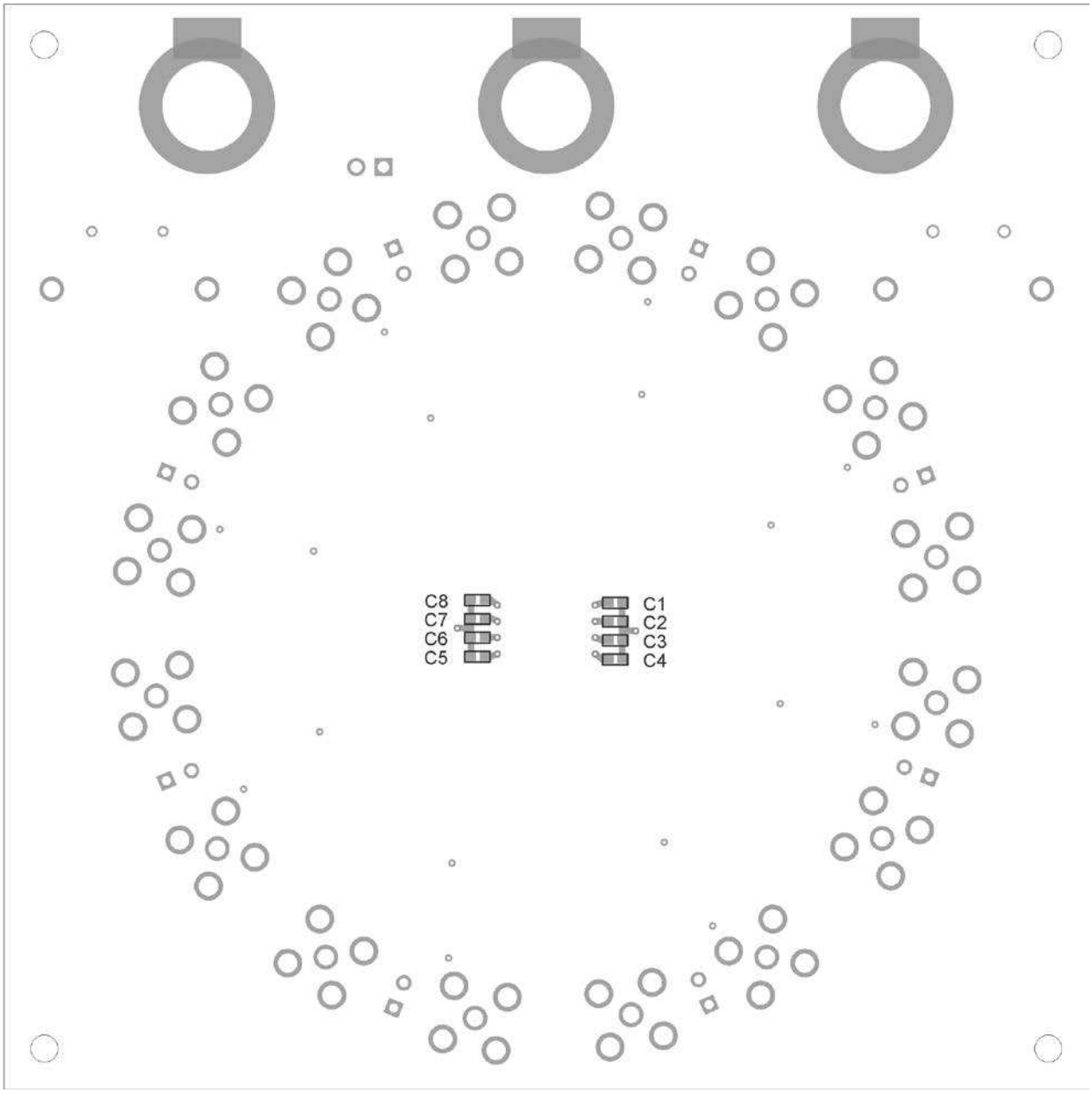


Figure 4 - Evaluation Board, Bottom View

PARTS LIST

Table 4 lists the factory installed parts and jumpers. As shipped, the AZEBP53Q supports single supply operation. Later sections illustrate how to configure the board for dual supply operation.

Other parts on the board are not installed, allowing the customer to customize the board for their internal needs.

Table 4 – Evaluation Parts List

Factory Installed

Reference Designator	Part	Notes
V+	Banana Jack	V_{DD} Supply
V-	Banana Jack	GND (single supply)
JMP1	Wire jumper between the two terminals of JMP1	AZEBP53Q factory wired for single supply operation.
SUP8	Wire jumper between SUP8, V+ pin and center pin of F8.	V_{DD} applied to DUT Pin 8
SUP4	Wire jumper between SUP4, V- pin and center pin of F4.	GND/V_{SS} applied to DUT Pin 4
C9, C11	22µF, 16 V tantalum capacitor	3.5x2.8mm
C4, C8, C10, C12, L5, C1F, C2F, C5F	0.01µF ceramic capacitor	0402 Surface Mount
F1, F2, F5	Female SMA connector	Amphenol 901-144-8RFX or equivalent
DUT	AZP53Q	1.5x1.0mm package (EBP53)
R2-,R1-	200Ω Resistor	0402 Surface Mount
R5-	50Ω Resistor	0402 Surface Mount

Customer Installed (as required)

Reference Designator	Part	Notes
R1+ to R8+, R3- to R4-, R6- to R8-	Resistor	0402 or 0603 Surface Mount
C1-C3, C7	Capacitor	0402 or 0603 Surface Mount
C3F, C4F, C6F – C8F, C1S – C8S	Capacitor	0402 or 0603 Surface Mount
L9, L10	Inductor or Ferrite Bead	1206 Surface Mount
F3, F4, F6 – F8, S1 – S8	Female SMA connector	Amphenol 901-144-8RFX or equivalent

AZEBP53Q Connections and Operating Modes

Divide Mode Connections

The DIV_SEL pin controls the divide by one (÷1) and divide by two (÷2) mode selection.

Table 5 - Divide Mode Connections

Divide Mode	DIV_SEL (Pin 7) logic	Jumper
÷1 (Factory Default)	No Connect	None
÷1	Low	Jumper across the two pins of R7-.
		Jumper across the two pins of L7.
÷2	High	Jumper across the two pins of R7+.
		Jumper across the two pins of L7.

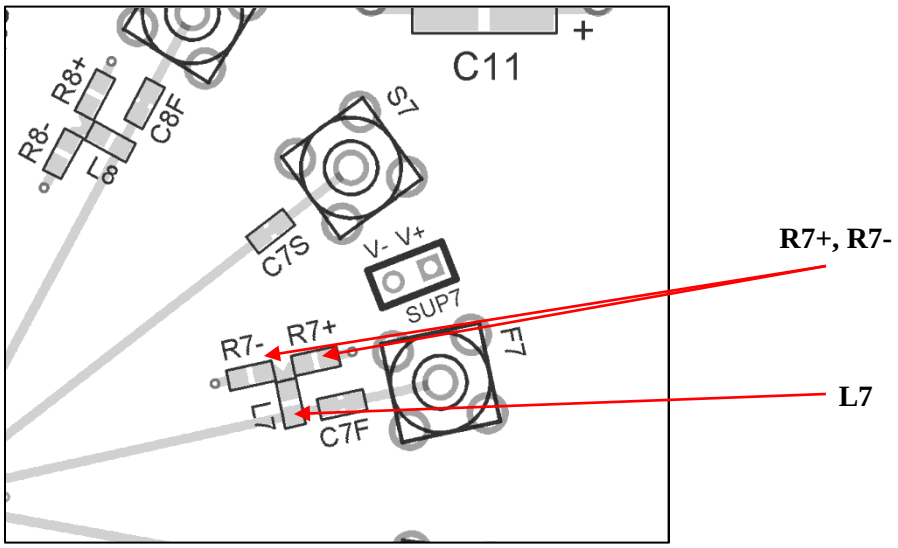


Figure 5 - Divide Mode Jumpers

ENABLE SELECT CONNECTIONS

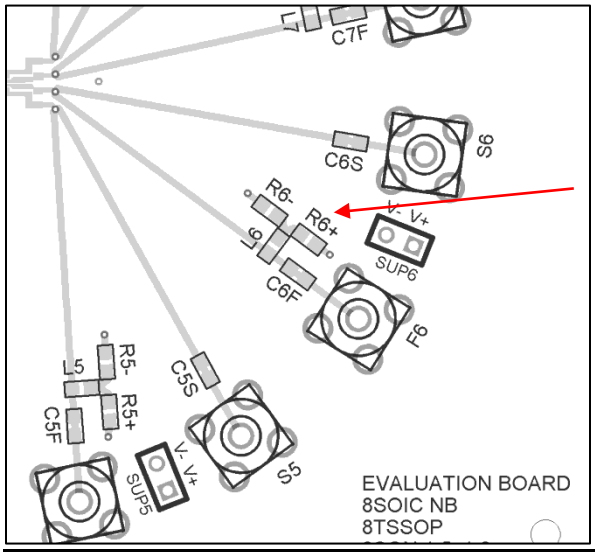
The EN_SEL pin controls the logic polarity of the enable (EN) pin.

Table 6 - Enable Select Jumpers

Enable (EN, Pin 3) Mode	EN_SEL (Pin 6) logic	Jumper
Active Low[1] (Factory Default)	No Connect	None
Active Low[1]	High	Jumper across the two pins of R6+.
		Jumper across the two pins of L6.
Active High[2]	Low	Jumper across the two pins of R6-.
		Jumper across the two pins of L6.

[1] Active Low: Outputs are enabled when EN Low or no connect, tri-state when EN high.

[2] Active High: Outputs are enabled when EH High or no connect, tri-state when EN low.



R6+, R6-, L6

Figure 6 - Enable Select Wiring

POWER SUPPLY CONNECTIONS

The evaluation board supports two methods of power supply connection. One method uses a single +3.3 V supply connected between V_{DD} and GND. The other method uses dual supplies, +2.0 V connected to V_{DD} and -1.3 V connected to V_{SS} (IC Ground). Dual supply operation (V_{DD}=+2.0V, V_{SS}=-1.3V) enables direct coupling to 50Ω test equipment loads.

The AZEBP53Q is factory configured for a single +3.3 V Supply.

Table 7 - Power Supply Jumpers

Supply Type	Voltage	Connect to PCB Pin	Jumper
Single +3.3 V Supply (Factory Default)	V_{DD} (+3.3 V)	V+	Jumper between the center pin of F8 and the V+ pin of SUP8.
	GND	GND, V-	Jumper across the two pins of JMP1
			Jumper between the center pin of F4 and the V- pin of SUP4.
Dual Supply (+2.0, -1.3 V)	V_{DD} (+2.0 V)	V+	Jumper between the center pin of F8 and the V+ pin of SUP8.
	GND	GND	-
	V_{SS} (-1.3 V)	V-	Jumper between the center pin of F4 and the V- pin of SUP4.

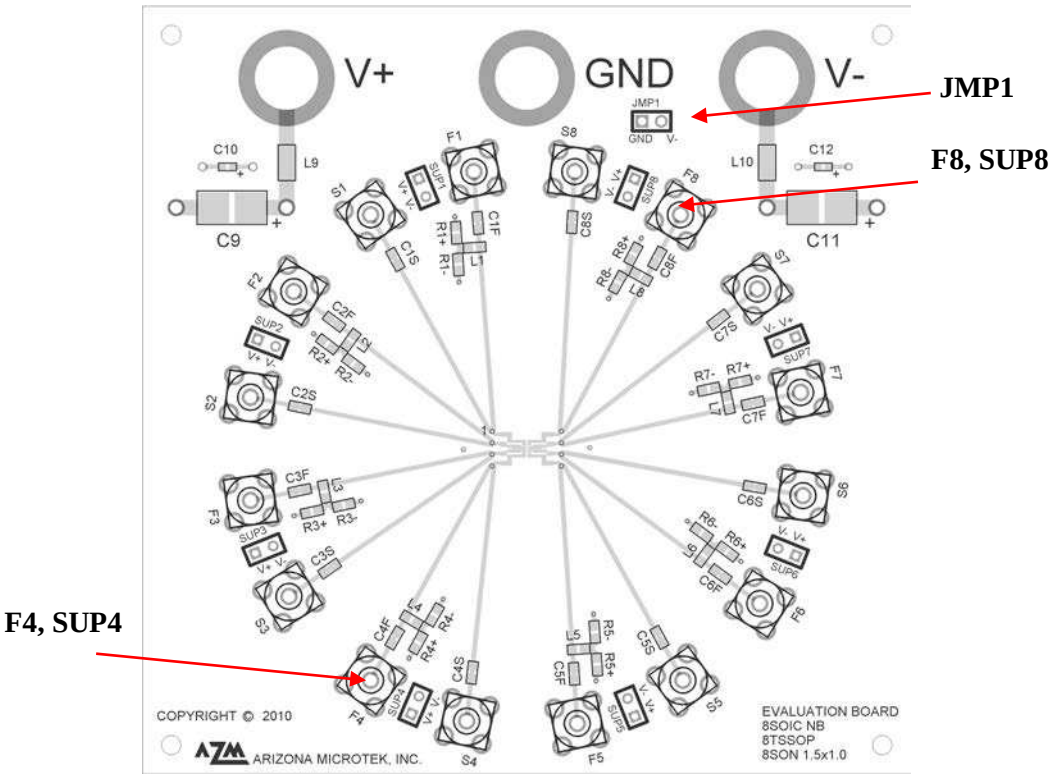


Figure 7 – Power Supply Wiring

SINGLE SUPPLY LVPECL OUTPUT TERMINATION *(FACTORY DEFAULT)*

Most RF and phase noise test sets use AC coupled inputs. Figure 10 shows evaluation board interfacing to test equipment, meeting both DC and AC termination requirements. On-board 200Ω resistors (R1-, R2-) form the required DC loads. The test equipment 50Ω input impedance provides the AC termination through C1F and C2F. The parallel combination of the on-board 200Ω and test equipment 50Ω resistors results in a net 40Ω AC load termination, which is close enough to 50Ω for almost all measurement purposes.

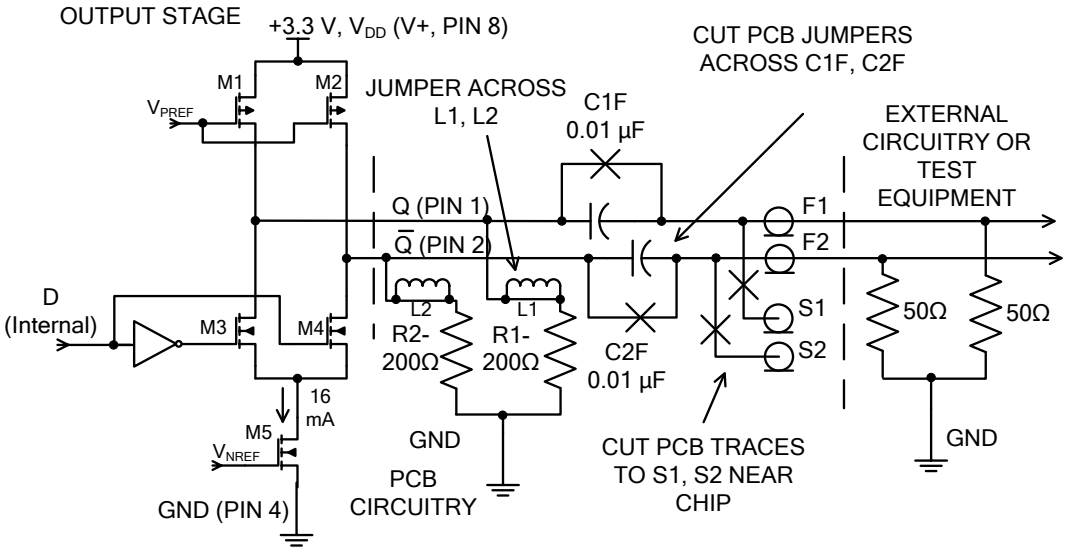


Figure 8 - Single Supply Output Schematic

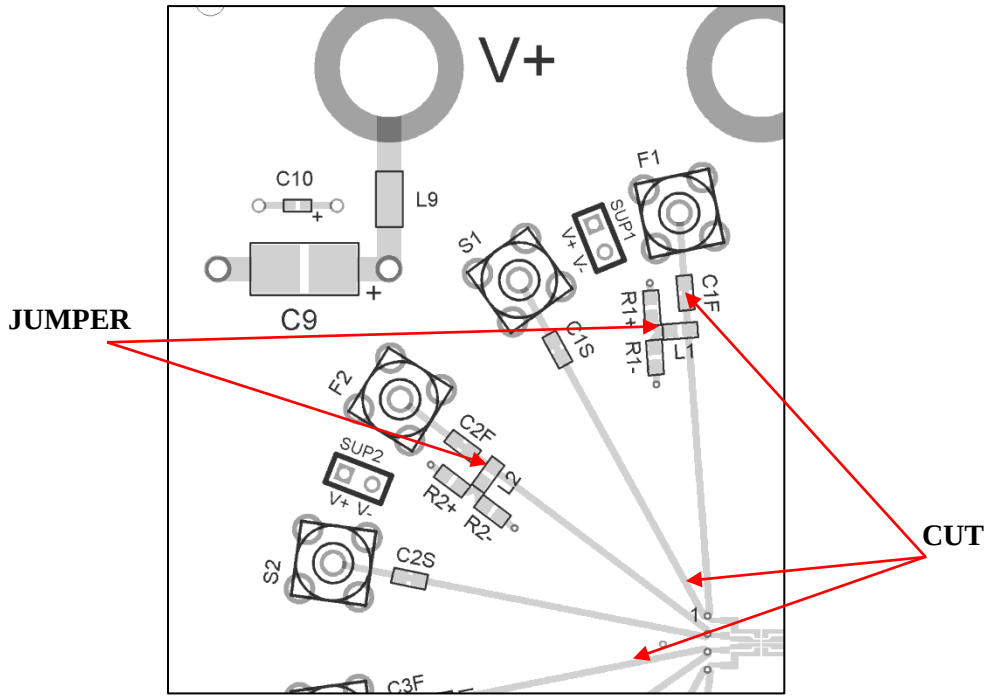


Figure 9 - Single Supply Output Wiring

DUAL SUPPLY LVPECL OUTPUT TERMINATION *(OPTIONAL CONFIGURATION)*

The AZP53 design contains LVPECL compatible current drive output stages to maximize switching speed shown in Figure 8. Two current source PMOS transistors (M1-M2) feed the output pins. M5 is an NMOS current source which is switched by M3 and M4. When M4 is on, M5 takes current from M2. The associated output voltage swings match LVPECL levels when external 50Ω resistors terminate the outputs. Both outputs should always be terminated identically to avoid waveform distortion and circulating current caused by unsymmetrical loads. This rule should be followed even if only one output is in use.

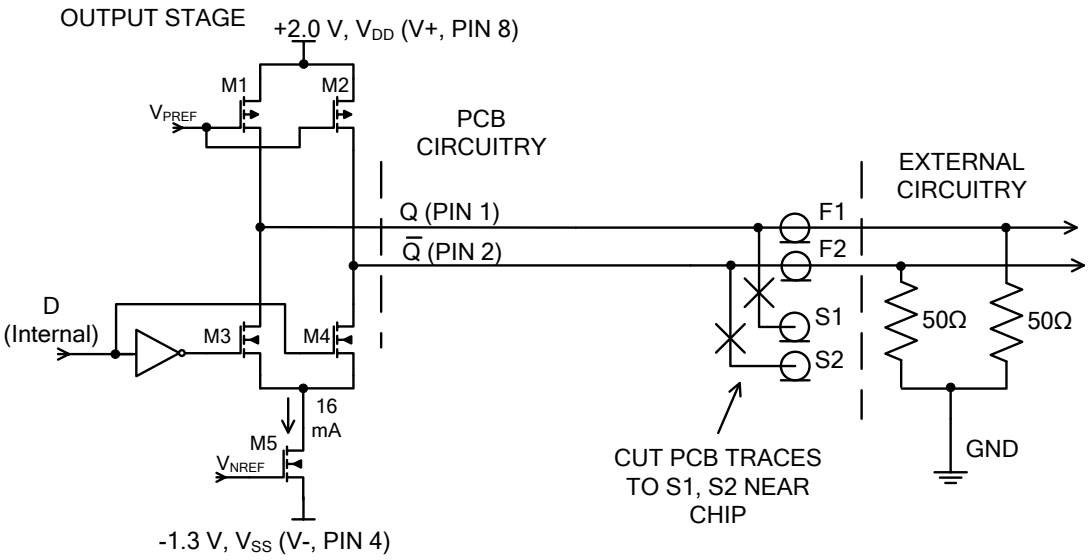


Figure 10 - Dual Supply Output Schematic

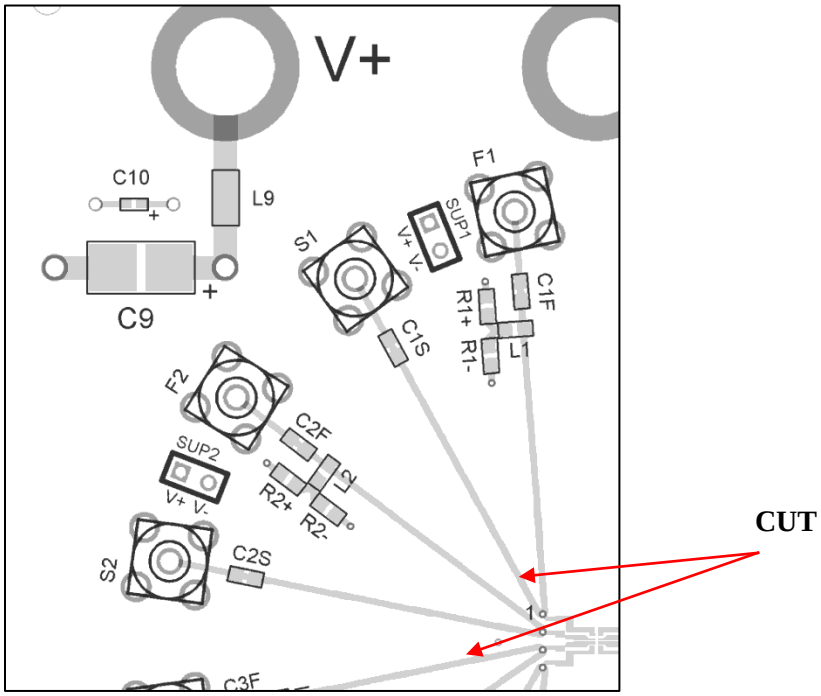


Figure 11 - Dual Supply LVPECL Output Wiring

SINGLE SUPPLY FOUR RESISTOR TERMINATION (*OPTIONAL CONFIGURATION*)

The four resistor technique eliminates the need for two power supplies and provides a Thevenin equivalent 50Ω termination. However the external circuitry must be high impedance to maintain the 50Ω loading.

R1+, R1-, R2+ and R2- are customer installed items

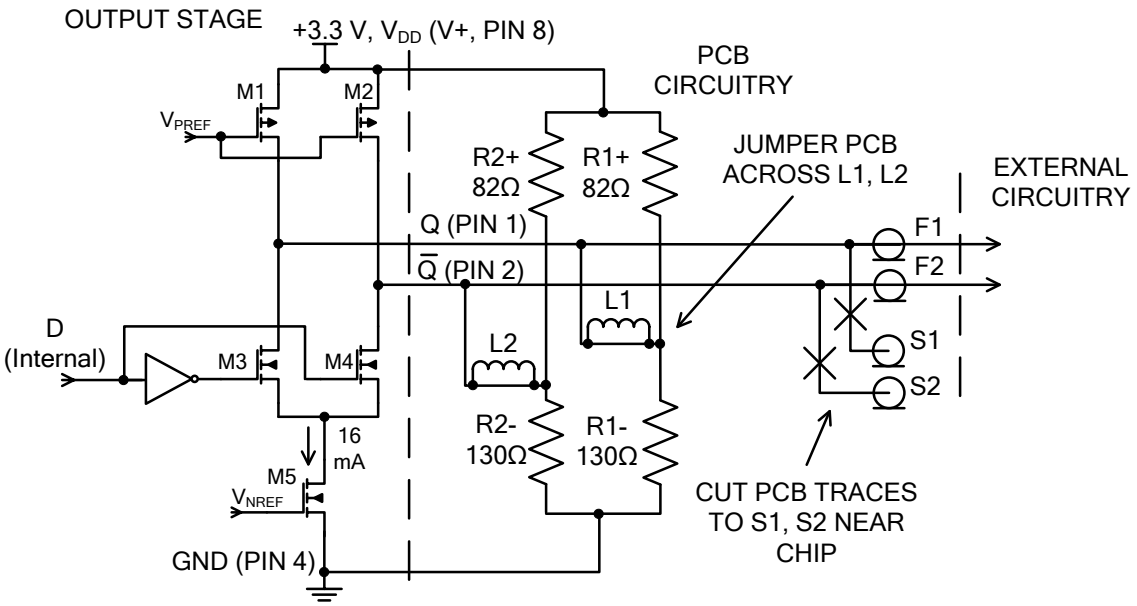


Figure 12 - Single Supply Four Resistor Schematic

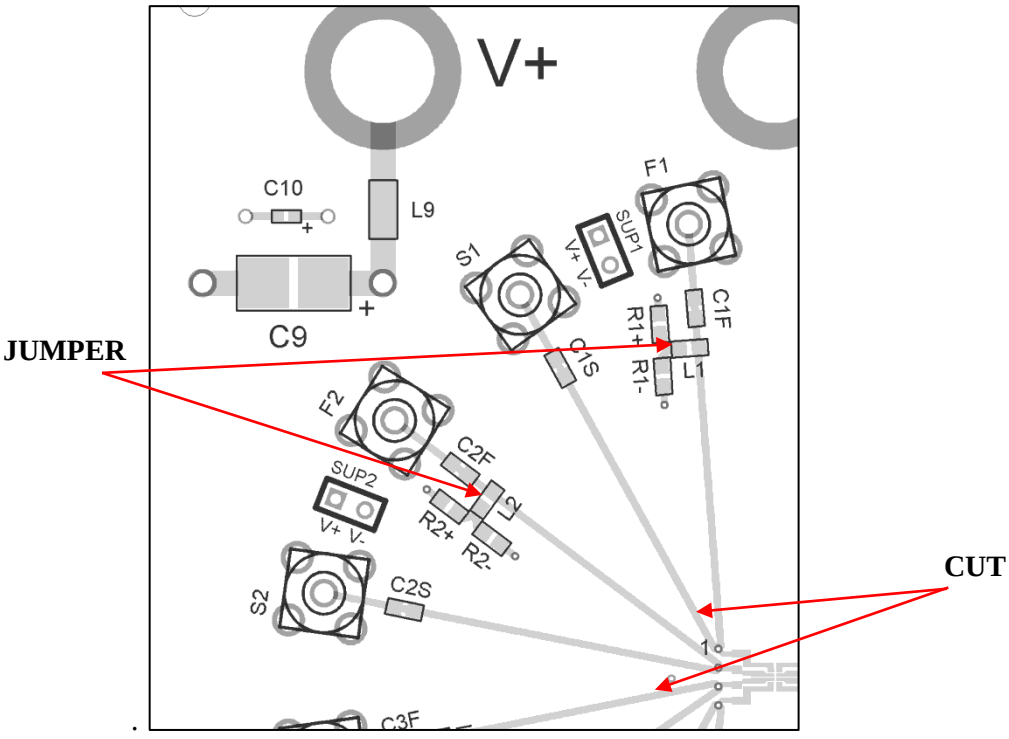


Figure 13 - Single Supply Four Resistor Wiring

INPUT CONNECTION

The AZP53 input terminal bias is $V_{DD}/2$ fed by an internal 10kΩ resistor. For clock applications, the input signal should be AC coupled into the D or $\overline{D}$ input to maintain a 50% duty cycle on the outputs. The input can be driven to any voltage between 0V and V_{DD} without damage or waveform degradation. The values of C5F, L5 and R5- depend on the specific application. C5F is typically 0.01µF, L5 (capacitor) is also typically 0.01µF and R5- is typically 50Ω.

R5-, C5F, and L5 are factory default installed items.

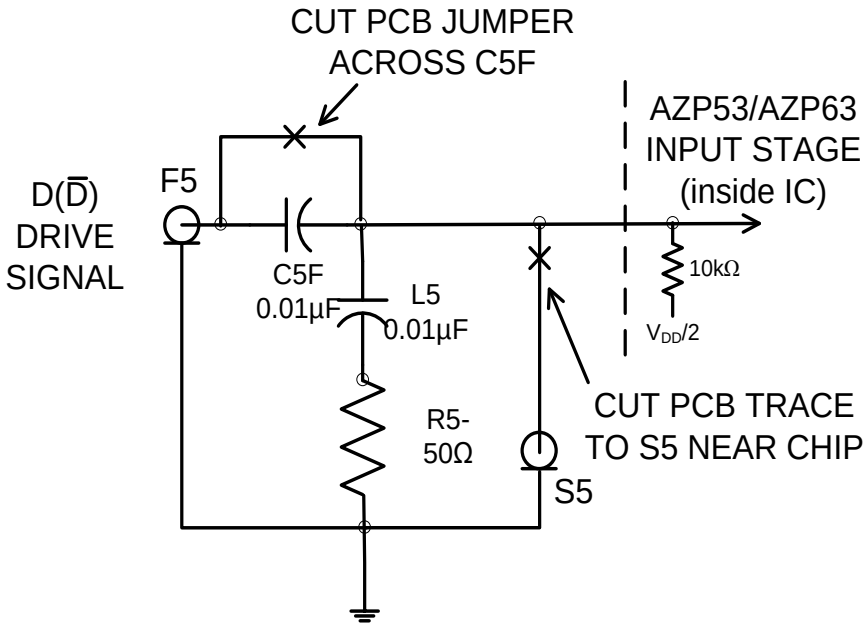


Figure 14 - Input Connection Schematic

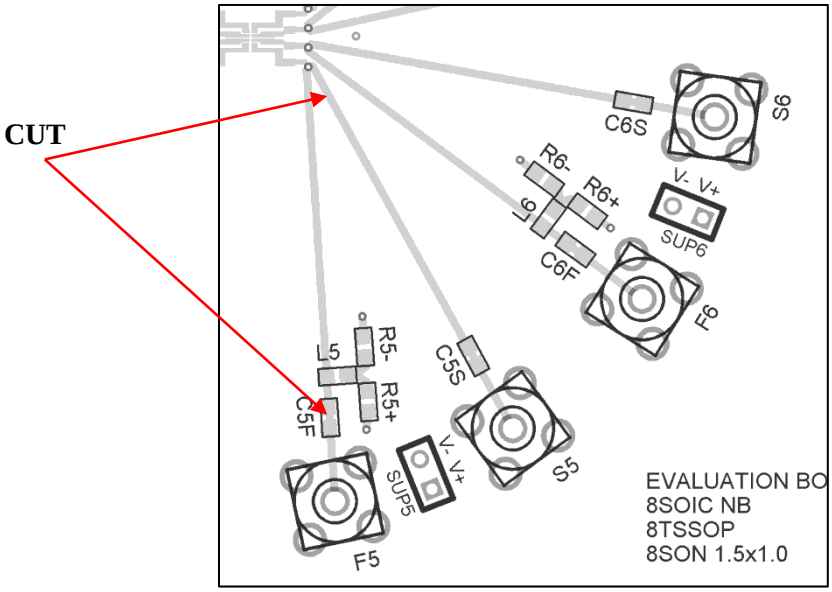


Figure 15 - Input Connection Wiring