AZ100LVEL33

PECL/ECL ÷4 Divider

www.azmicrotek.com

DESCRIPTION

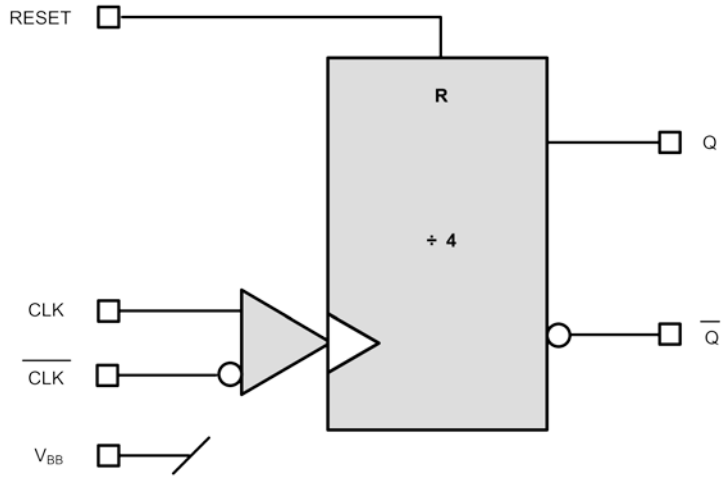
The AZ100LVEL33 is an integrated ÷4 divider. The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random logic state; the reset allows for the synchronization of multiple AZ100LVEL33's in a system.

The AZ100LVEL33 is a direct replacement for the On Semiconductor MC100EL/LVEL33

FEATURES

- 5.0+ GHz toggle frequency
- 470ps propagation delay
- Internal input pulldown resistors
- 3.0V to 5.5V power supply

BLOCK DIAGRAM



APPLICATIONS

- General Applications

PACKAGE AVAILABILITY

- MLP8
- MSOP8
- SOIC8
- Green/RoHS Compliant/Pb-Free

Part Number (PN)	Package	Marking
AZ100LVEL33NG[1]	MLP 8	C3G <Date Code>[2]
AZ100LVEL33TG[1]	MSOP 8	AZHGLV33[2]
AZ100LVEL16DG[1]	SOIC 8	AZM100GLVEL33[2]

[1] Tape & Reel - Add 'R1' at end of PN for 7in (1k parts), 'R2' (2.5k) for 13in

[2] See www.azmicrotek.com for date code format

PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin Description for AZ100LVEL33N

Pin	Name	Type	Function
1	RESET	Input	Asynchronous Reset
2	CLK	Input	Clock Input
3	$\overline{CLK}$	Input	Inverting Clock Input
4	V_{BB}	Output	Reference Voltage
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}$	Output	Inverting PECL Output
7	Q	Output	PECL Output
8	V_{CC}	Power	Positive Supply

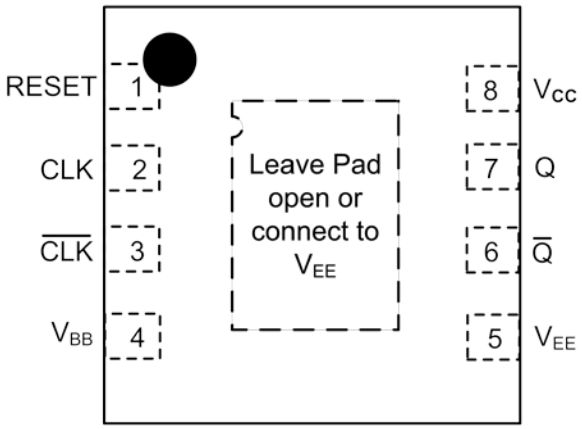


Figure 1 - Pin Configuration AZ100LVEL33N

Table 2 - Pin Description for AZ100LVEL33T & AZ100LVEL33D

Pin	Name	Type	Function
1	RESET	Input	Asynchronous Reset
2	CLK	Input	Clock Input
3	$\overline{CLK}$	Input	Inverting Clock Input
4	V_{BB}	Output	Reference Voltage
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}$	Output	Inverting PECL Output
7	Q	Output	PECL Output
8	V_{CC}	Power	Positive Supply

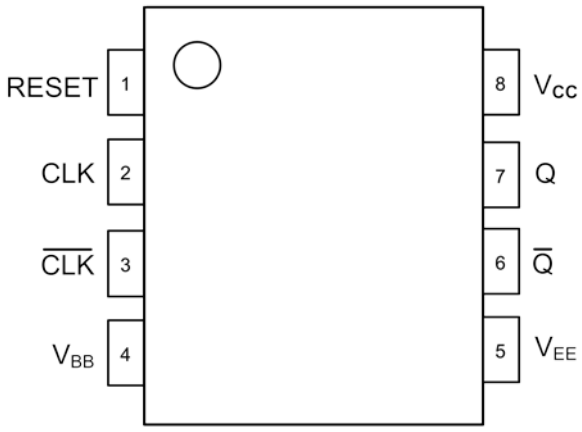


Figure 2 - Pin Configuration AZ100LVEL33T & AZ100LVEL33D

ENGINEERING NOTES

The AZ100LVEL33 provides a V_{BB} output for single-ended use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the CLK/$\overline{CLK}$ differential input pair. The input signal is then fed to the other CLK/$\overline{CLK}$ input. The V_{BB} pin should be used only as a bias for the AZ100LVEL32 as its sink/source capability is limited. When used, the V_{BB} pin should be bypassed to ground via a 0.01µF capacitor.

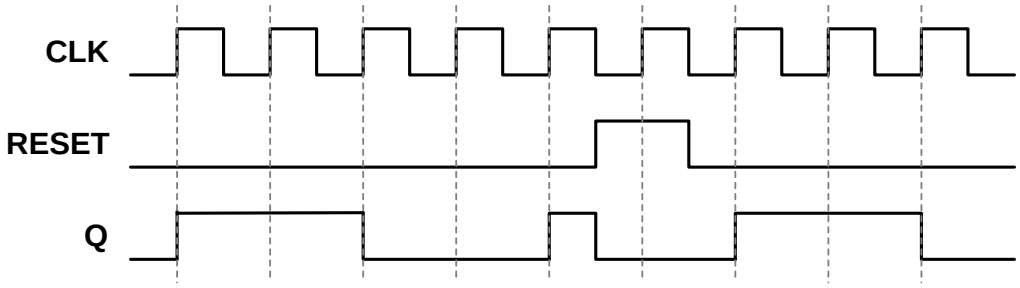


Figure 3 - Timing Diagram

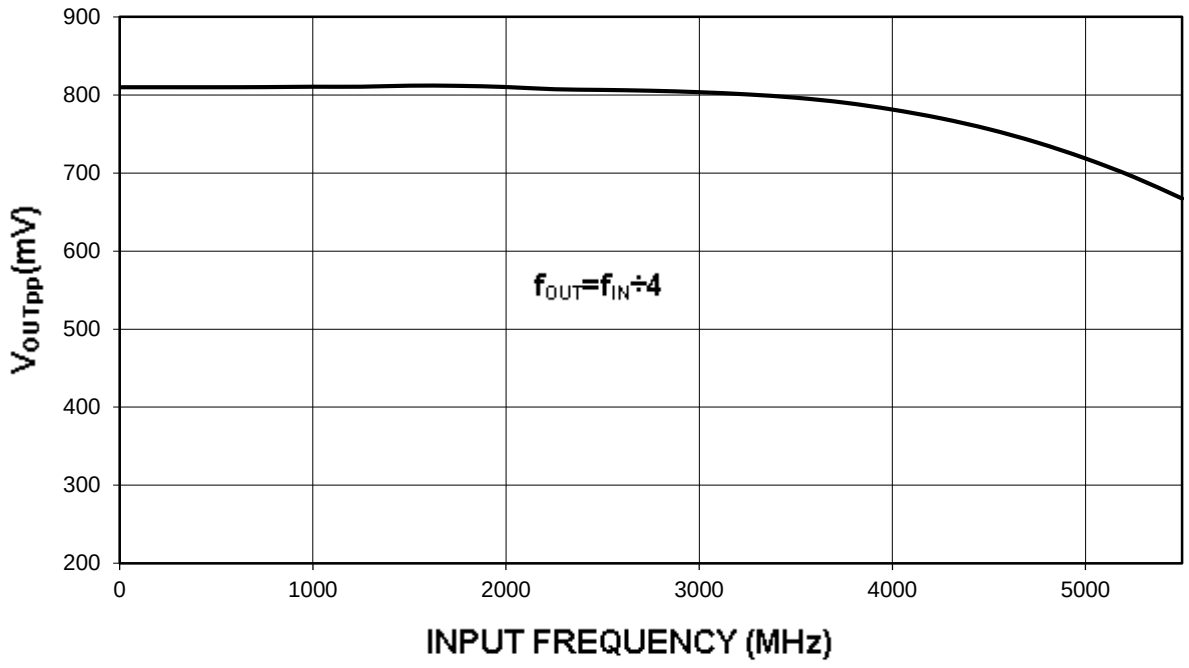


Figure 4 - Typical Large Signal Output Swing

Measured with 750mV input, output terminated to V_{CC}-2V via 50Ω resistors

PERFORMANCE DATA

Table 3 – Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to + 6.0	V
V_{I_PECL}	PECL Input Voltage	V_{EE} = 0V	0 to + 6.0	V
V_{EE}	ECL Power Supply	V_{CC} = 0V	-6.0 to 0	V
V_{I_ECL}	ECL Input Supply	V_{CC} = 0V	-6.0 to 0	V
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range	-	-40 to +85	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

Table 4 - ECL DC Characteristics

ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V_{OL}	Output LOW Voltage[1]	-1830	-1555	-1810	-1620	-1810	-1620	-1810	-1620	mV
V_{IH}	Input HIGH Voltage	-1165	-880	-1165	-880	-1165	-880	-1165	-880	mV
V_{IL}	Input LOW Voltage	-1810	-1475	-1810	-1475	-1810	-1475	-1810	-1475	mV
V_{BB}	Reference Voltage	-1380	-1260	-1380	-1260	-1380	-1260	-1380	-1260	mV
I_{IH}	Input HIGH Current		150		150		150		150	µA
I_{IL}	Input LOW Current CLK	-150		-150		-150		-150		µA
	Input LOW Current RESET	0.5		0.5		0.5		0.5		
I_{EE}	Power Supply Current		33		33		33		37	mA

[1] Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

Table 5 - LVPECL DC Characteristics

LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215	2420	2275	2420	2275	2420	2275	2420	mV
V_{OL}	Output LOW Voltage[1,2]	1470	1745	1490	1680	1490	1680	1490	1680	mV
V_{IH}	Input HIGH Voltage[1]	2135	2420	2135	2420	2135	2420	2135	2420	mV
V_{IL}	Input LOW Voltage[1]	1490	1825	1490	1825	1490	1825	1490	1825	mV
V_{BB}	Reference Voltage[1]	1920	2040	1920	2040	1920	2040	1920	2040	mV
I_{IH}	Input HIGH Current		150		150		150		150	µA
I_{IL}	Input LOW Current CLK	-150		-150		-150		-150		µA
	Input LOW Current RESET	0.5		0.5		0.5		0.5		
I_{EE}	Power Supply Current		33		33		33		37	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value

2 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

Table 6 - PECL DC Characteristics

PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3170	3445	3190	3380	3190	3380	3190	3380	mV
V_{IH}	Input HIGH Voltage[1]	3835	4120	3835	4120	3835	4120	3835	4120	mV
V_{IL}	Input LOW Voltage[1]	3190	3525	3190	3525	3190	3525	3190	3525	mV
V_{BB}	Reference Voltage[1]	3620	3740	3620	3740	3620	3740	3620	3740	mV
I_{IH}	Input HIGH Current		150		150		150		150	µA
I_{IL}	Input LOW Current CLK	-150		-150		-150		-150		µA
	Input LOW Current RESET	0.5		0.5		0.5		0.5		
I_{EE}	Power Supply Current		33		33		33		37	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value

2 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC}=GND or V_{EE}=GND; V_{CC} = +3.0V to +5.5V)

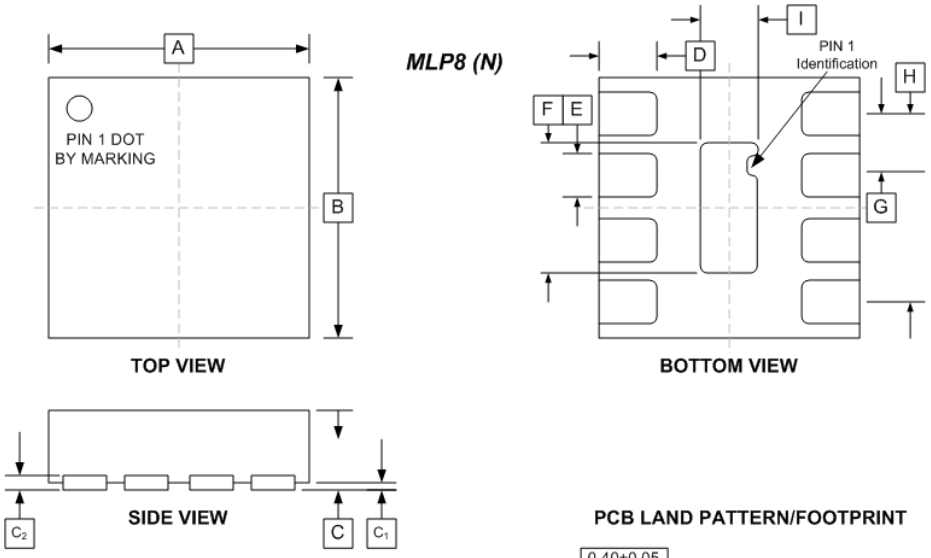
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency	4.2			4.2			4.2			4.2			GHz
t_{PLH}/t_{PHL}	Propagation Delay													
	CLK/ to Q/[1]	360	450	540	320	460	550	380	470	560	400	490	580	ps
	RESET to Q/[1]	310	460	610	340	460	580	360	460	560	380	480	580	ps
t_{SKEW}	Duty Cycle Skew[2]			20			20			20			20	ps
V_{PP} (AC)	Input Swing[1]	150		1000	150		1000	150		1000	150		1000	mV
V_{CMR}	Common Mode Range[2]	V_{EE}+		V_{CC} -	V_{EE}+		V_{CC} -	V_{EE}+		V_{CC} -	V_{EE}+		V_{CC} -	
	V_{PP} < 500mV	1.2		0.4	1.1		0.4	1.1		0.4	1.1		0.4	V
	V_{PP} ≥ 500mV	1.4		0.4	1.3		0.4	1.3		0.4	1.3		0.4	V
t_r/t_f	Output Rise/Fall[1] (20%-80%)	100		260	100		260	100		260	100		260	ps

V_{PP} is the peak-to-peak differential input swing for which AC parameters are guaranteed.

2 V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that V_{PP} is within the differential input swing range specified

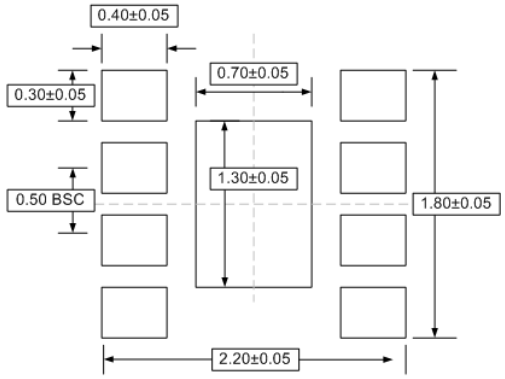
PACKAGE DIAGRAM

MLP8
Green/RoHS compliant/Pb-Free
MSL=1



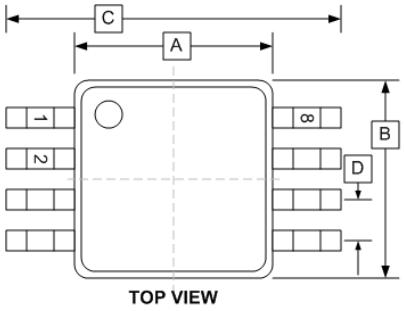
	MILLIMETERS	
DIM	MIN	MAX
A	2.00±0.050	
B	2.00±0.050	
C	0.75±0.050	
C_1	0.00	0.05
C_2	0.203 Ref.	
D	0.35±0.050	
E	0.25±0.050	
F	1.20±0.050	
G	0.500 BSC	
H	1.500 REF	
I	0.60±0.050	

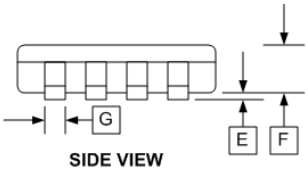
PCB LAND PATTERN/FOOTPRINT



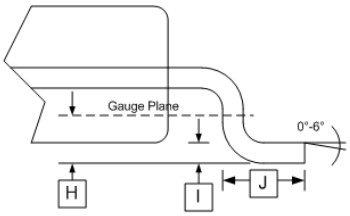
PACKAGE DIAGRAM

MSOP8
Green/RoHS compliant/Pb-Free
MSL=1





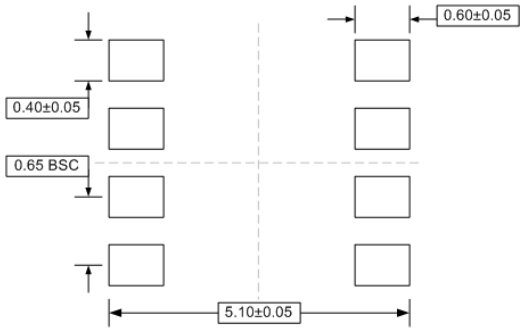
MSOP8 (T)



	INCHES	
DIM	MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0256 TYP	
E	0.004±0.002	
F	0.034±0.002	
G	0.009±0.014	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	

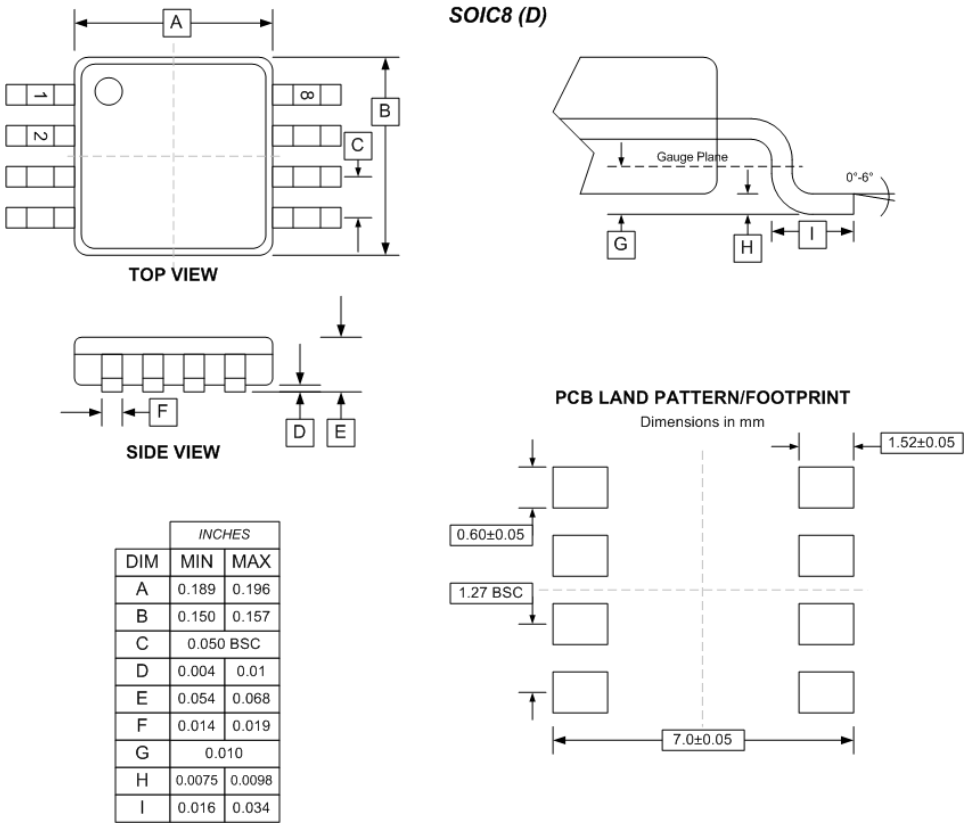
PCB LAND PATTERN/FOOTPRINT

Dimensions in mm



PACKAGE DIAGRAM

SOIC8
Green/RoHS compliant/Pb-Free
MSL=1



	INCHES	
DIM	MIN	MAX
A	0.189	0.196
B	0.150	0.157
C	0.050 BSC	
D	0.004	0.01
E	0.054	0.068
F	0.014	0.019
G	0.010	
H	0.0075	0.0098
I	0.016	0.034