AZ100LVEL16VV

ARIZONA MICROTEK

Dual Frequency PECL/ECL Oscillator Gain Stage & Buffer with Enable

www.azmicrotek.com

DESCRIPTION

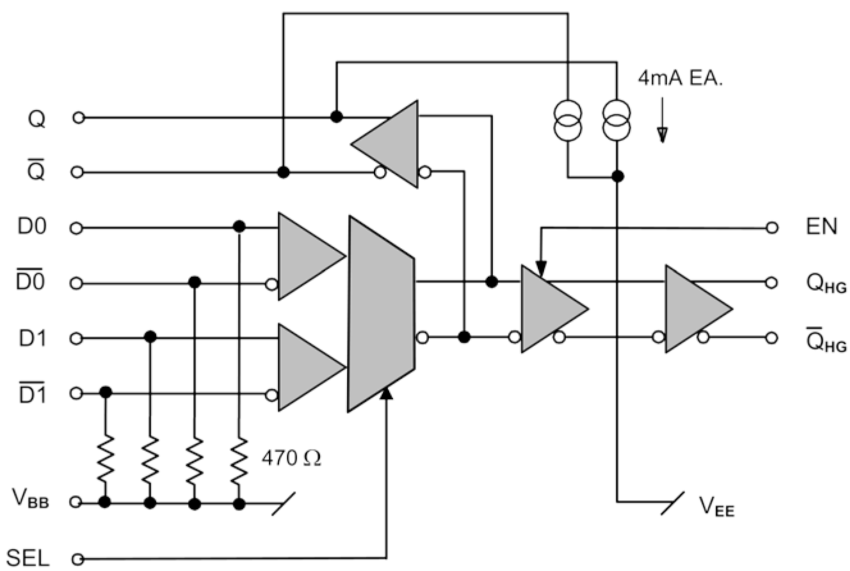
The AZ100LVEL16VV is a specialized oscillator gain stage with two selectable data input pairs and a high gain output buffer including an enable. Selectable data input pairs permit switching between two different oscillator frequencies. The $Q_{HG}/\overline{Q}_{HG}$ outputs have a voltage gain several times greater than the $Q/\overline{Q}$ outputs. An enable allows continuous oscillator operation by only controlling the $Q_{HG}/\overline{Q}_{HG}$ outputs.

The AZ100LVEL16VV also provides a reference voltage (V_{BB}) with internal biasing resistors to each input to minimize external components.

FEATURES

- Minimizes External Components
- High Bandwidth for ≥1GHz
- Similar Operation as AZ100LVEL16VR except with selectable data input pairs
- -147 dBc/Hz Typical Noise Floor

BLOCK DIAGRAM



APPLICATIONS

- Dual frequency oscillators
- Crystal or saw oscillators that require minimal external components.

PACKAGE AVAILABILITY

- MLP16
  - Green/RoHS Compliant/Pb-Free

Order Number	Package	Marking
AZ100LVEL16VRL[1]	MLP16	AZM+16K <Date Code>[2]

[1] Tape & Reel - Add 'R1' at end of PN for 7in (1k parts), 'R2' (2.5k) for 13in

[2] See www.azmicrotek.com for date code format

PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin Description AZ100LVEL16VTNA+

Pin	Name	Type	Function
1	D0	Input	Data Input
2	$\overline{D0}$	Input	Inverting Data Input
3	D1	Input	Data Input
4	$\overline{D1}$	Input	Inverting Data Input
5	V_{BB}	Output	Reference Voltage
6	NC	-	N/A
7	V_{EE}	Power	Negative Supply
8	NC	-	N/A
9	EN	Input	Output Enable
10	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
11	Q_{HG}	Output	High Gain PECL Output
12	SEL	Input	Data Input Select
13	V_{CC}	Power	Positive Supply
14	NC	-	N/A
15	Q	Output	PECL Output
16	$\overline{Q}$	Output	Inverting PECL Output

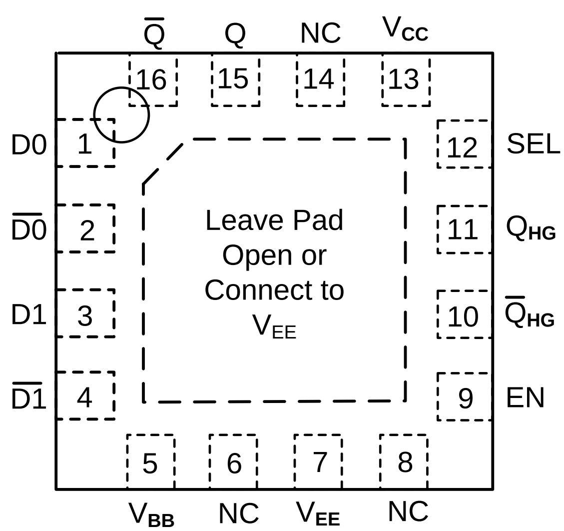


Figure 1 - Pin Configuration

ENGINEERING NOTES

The AZ100LVEL16VV is a specialized oscillator gain stage with two selectable data input pairs and a high gain output buffer including an enable. The $Q_{HG}/\overline{Q}_{HG}$ outputs have a voltage gain several times greater than the $Q/\overline{Q}$ outputs.

The AZ100LVEL16VV provides two selectable data input pairs that permit switching between two different oscillator frequencies. When the select pin (SEL) is LOW or open (NC) data from the $D0/\overline{D0}$ is selected. When the SEL pin is HIGH data from the $D1/\overline{D1}$ is selected. Allowing continuous oscillator operation, the (EN) enable works with either data input pair. When EN is HIGH or open (NC), input data is passed to both sets of outputs. When EN is LOW, the $Q_{HG}/\overline{Q}_{HG}$ outputs will be forced LOW/HIGH respectively, while input data will continue to be passed to the $Q/\overline{Q}$ outputs. The EN and SEL inputs can be driven with an ECL/PECL signal or a full supply swing CMOS type logic signal.

The AZ100LVEL16VV also provides a V_{BB} with a 1.5mA sink/source current. Each data input is separately connected to V_{BB} with a 470Ω internal bias resistor. Bypassing V_{BB} to ground with a 0.01 μF capacitor is recommended.

Each $Q/\overline{Q}$ output has a 4 mA on-chip pull-down current source. External resistors may also be used to increase pull-down current of the $Q/\overline{Q}$ to a maximum of 25mA each (includes a 4 mA on-chip current source).

Table 2 - Truth Table

EN	CS-SEL	Q	$\overline{Q}$	Q_{HG}	$\overline{Q}_{HG}$
High/Open	Low/Open	$D0/\overline{D0}$	$D0/\overline{D0}$	$D0/\overline{D0}$	$D0/\overline{D0}$
High/Open	High	$D1/\overline{D1}$	$D1/\overline{D1}$	$D1/\overline{D1}$	$D1/\overline{D1}$
Low	Low/Open	$D0/\overline{D0}$	$D0/\overline{D0}$	Low	High
Low	High	$D1/\overline{D1}$	$D1/\overline{D1}$	Low	High

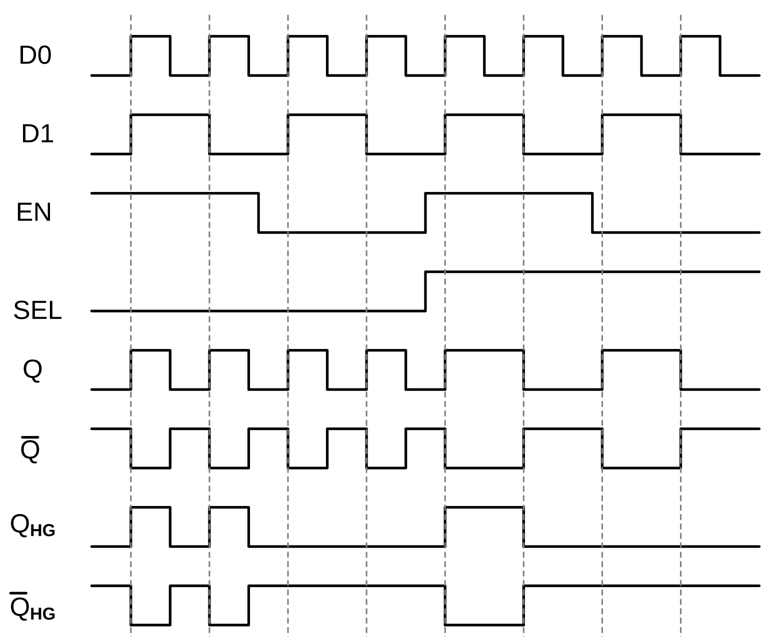


Figure 2 - Timing Diagram

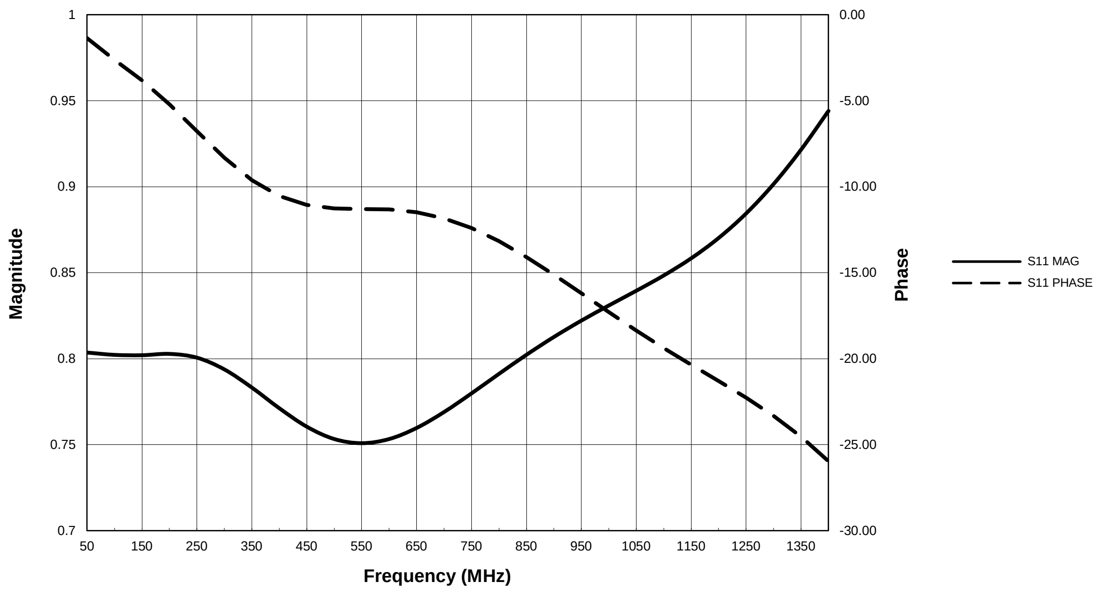


Figure 3 - S11

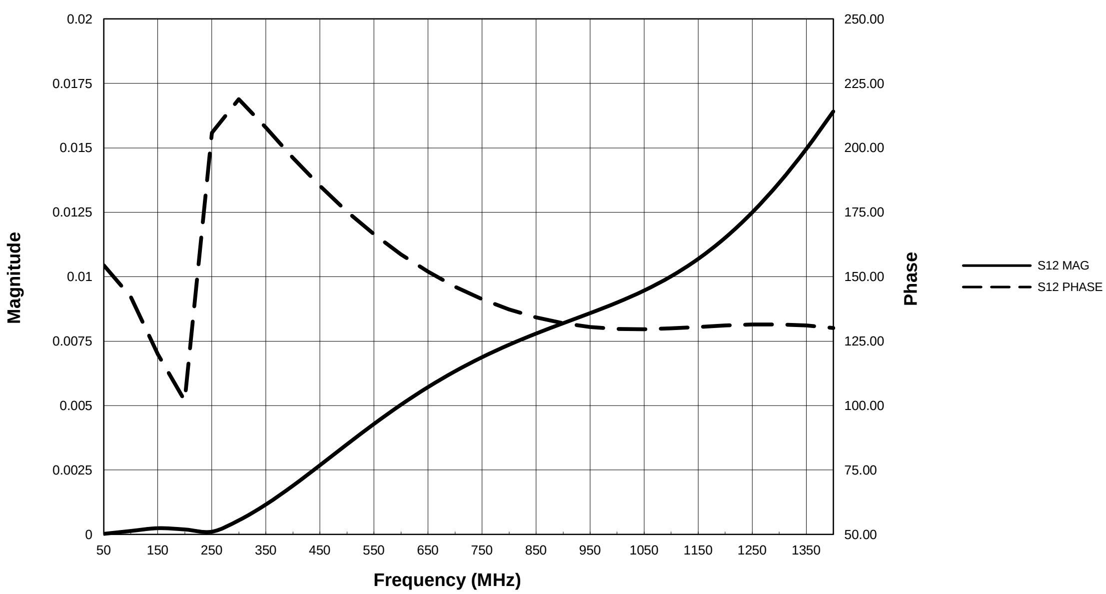


Figure 4 - S12

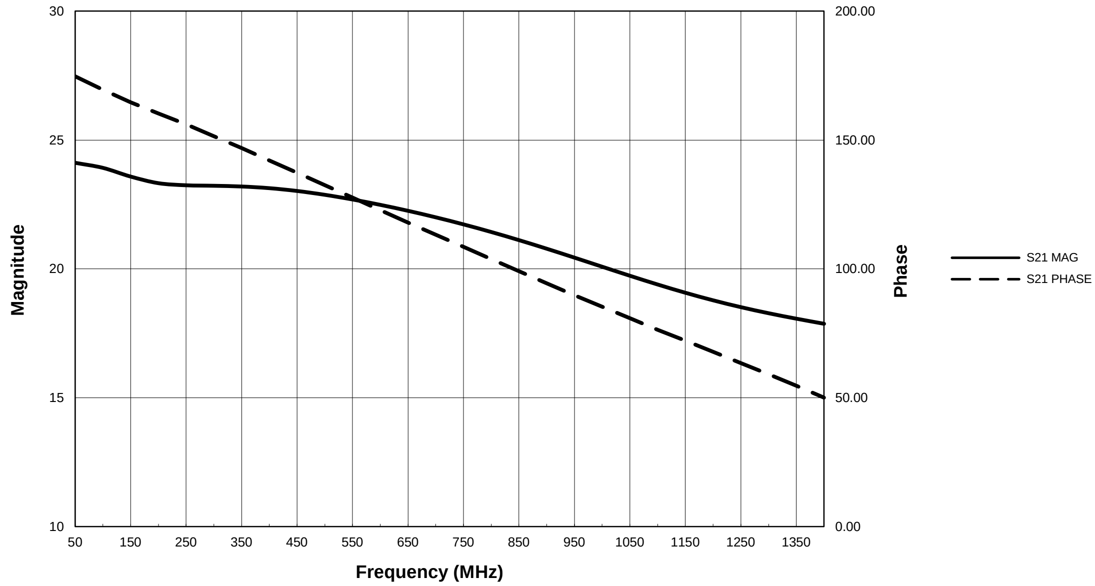


Figure 5 – S21

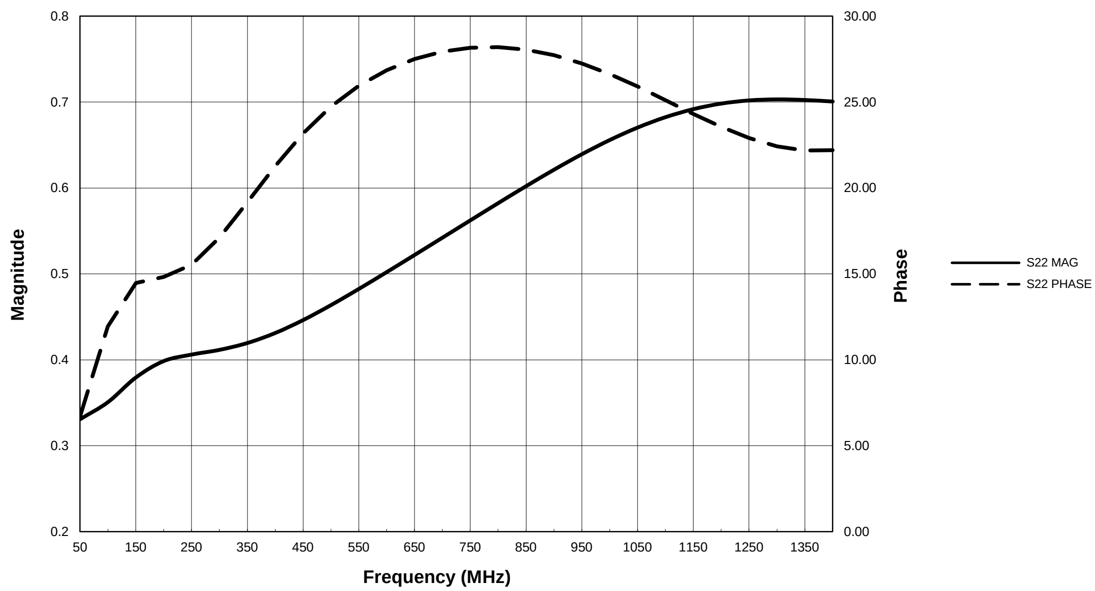


Figure 6 – S22

PERFORMANCE DATA

Table 3 – Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to + 6.0	V
V_{D_PECL}	PECL D Input Voltage	Referenced to V_{BB}	±0.75	V
V_{EN_PECL}	PECL D Input Voltage	V_{EE} = 0V	0 to + 6.0	V
V_{EE}	ECL Power Supply	V_{CC} = 0V	-6.0 to 0	V
V_{D_ECL}	ECL D Input Voltage	Referenced to V_{BB}	±0.75	V
V_{EN_ECL}	ECL D Input Voltage	V_{CC} = 0V	-6.0 to 0	V
I_{OUT}	Output Current	Continuous Q	25	mA
		Surge Q	50	
		Continuous Q_{HG}	50	
		Surge Q_{HG}	100	
T_A	Operating Temperature Range	-	-40 to +85	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

Table 4 - ECL DC Characteristics

ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
V_{OL}	Output LOW Voltage[1]	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
	Input HIGH Voltage EN,SEL	-1165	V_{CC}	-1165	V_{CC}	-1165	V_{CC}	-1165	V_{CC}	
V_{IL}	Input LOW Voltage D	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
	Input LOW Voltage EN,SEL	V_{EE}	-1475	V_{EE}	-1475	V_{EE}	-1475	V_{EE}	-1475	
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IH}	Input HIGH Current EN,SEL		150		150		150		150	μA
I_{IL}	Input LOW Current EN,SEL	-100		-100		-100		-100		μA
I_{EE}	Power Supply Current[1]		47		47		47		51	mA

1 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

Table 5 - LVPECL DC Characteristics

LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2255	2465	2275	2465	2275	2465	2275	2465	mV
V_{OL}	Output LOW Voltage[1,2]	1375	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage D	2135	2560	2135	2560	2135	2560	2135	2560	mV
	Input HIGH Voltage EN,SEL	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	
V_{IL}	Input LOW Voltage D	1050	1825	1400	1825	1400	1825	1400	1825	mV
	Input LOW Voltage EN,SEL	V_{EE}	1825	V_{EE}	1825	V_{EE}	1825	V_{EE}	1825	
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW[3] Current EN	-400		-400		-400		-400		µA
I_{EE}	Power Supply Current[2]		47		47		47		51	mA

1 Voltage levels vary 1:1 with V_{CC}

2 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

3 Specified with EN and SEL forced to V_{EE}

Table 6 - PECL DC Characteristics

PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3955	4165	3975	4165	3975	4165	3975	4165	mV
V_{OL}	Output LOW Voltage[1,2]	3075	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage D	3835	4260	3835	4260	3835	4260	3835	4260	mV
	Input HIGH Voltage EN,SEL	3835	V_{CC}	3835	V_{CC}	3835	V_{CC}	3835	V_{CC}	
V_{IL}	Input LOW Voltage D	3100	3525	3100	3525	3100	3525	3100	3525	mV
	Input LOW Voltage EN,SEL	V_{EE}								
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN	-1000		-1000		-1000		-1000		µA
I_{EE}	Power Supply Current[2]		47		47		47		51	mA

1 Voltage levels vary 1:1 with V_{CC}

2 Specified with each output terminated through 50Ω resistors to V_{CC} - 2V.

3 Specified with EN and SEL forced to V_{EE}

Table 7 - AC Characteristics

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC}=GND or V_{EE}=GND; V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Delay													
	D to Q/Qb			400			400			400			400	ps
	D to Q_{HG}/Qb_{HG}			550			550			550			550	ps
t_{SKEW}	Duty Cycle Skew[1]		5	20		5	20		5	20		5	20	ps
Vpp (AC)	Input Swing[2]	80		1000	80		1000	80		1000	80		1000	mV
t_r/t_f	Output Rise/Fall (20% - 80%)	100		260	100		260	100		260	100		260	ps

1 Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

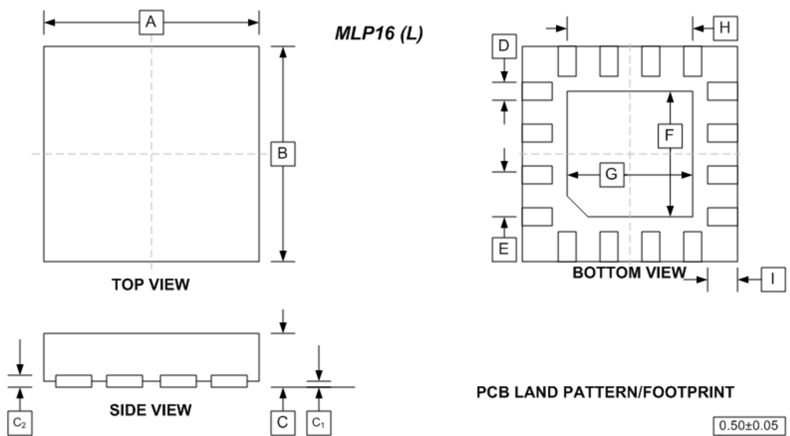
2 V_{PP} is the peak-to-peak differential input swing for which AC parameters are guaranteed. The device has a voltage gain of ≈20 to Q/ outputs and a voltage gain of ≈100 to $Q_{HG}/_{HG}$ outputs.

PACKAGE DIAGRAM

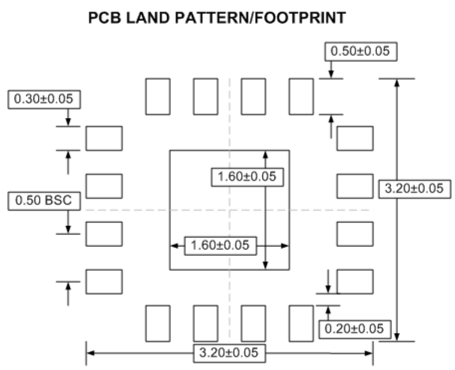
MLP16

Green/RoHS compliant/Pb-Free

MSL=1



DIM	MILLIMETERS	
	MIN	MAX
A	3.00±0.050	
B	3.00±0.050	
C	0.85±0.050	
C_1	0.00	0.05
C_2	0.203 REF	
D	0.23±0.050	
E	0.50 BSC	
F	1.55±0.050	
G	1.55±0.050	
H	1.500 Ref	
I	0.40±0.050	



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