

# AZ100LVEL16VT



## PECL/ECL Oscillator Gain Stage & Buffer with Selectable Enable

[www.azmicrotek.com](http://www.azmicrotek.com)

### DESCRIPTION

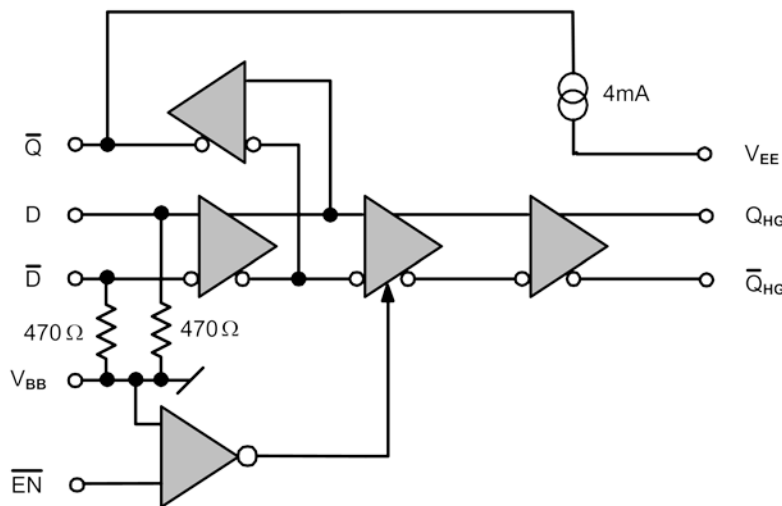
The [AZ100LVEL16VT](#) is a specialized oscillator gain stage with a high gain output buffer including an enable function. The  $Q_{HG}/\bar{Q}_{HG}$  outputs have voltage gain several times greater than the Q output. It provides a  $Q_{HG}/\bar{Q}_{HG}$  enable that allows continuous oscillator operation via the Q outputs.

The AZ100LVEL16VT also provides a 4mA internal pull-down current source for Q outputs. Internal input biasing further reduces the number of needed external components.

### FEATURES

- Minimizes External Components
- High Bandwidth for  $\geq 1\text{GHz}$
- Similar Operation as [AZ100LVEL16VR](#) except in Disabled Condition,  $Q_{HG}$  is High
- -147 dBc/Hz Typical Noise Floor

### BLOCK DIAGRAM



### APPLICATIONS

- Crystal or saw oscillators that require minimal external components.

### PACKAGE AVAILABILITY

- MLP8
  - Green/RoHS Compliant/Pb-Free

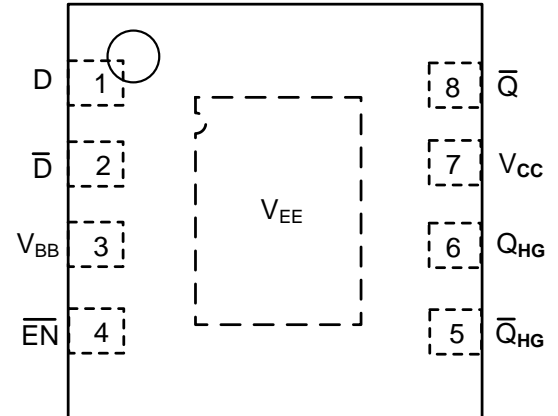
Order Number	Package	Marking
AZ100LVEL16VTNA <sup>1</sup>	MLP8	P9+ <Date Code> <sup>2</sup>
AZ100LVEL16VTNB <sup>1</sup>	MLP8	P8+ <Date Code> <sup>2</sup>

<sup>1</sup> [Tape & Reel](#) - Add 'R1' at end of PN for 7in (1k parts), 'R2' (2.5k) for 13in

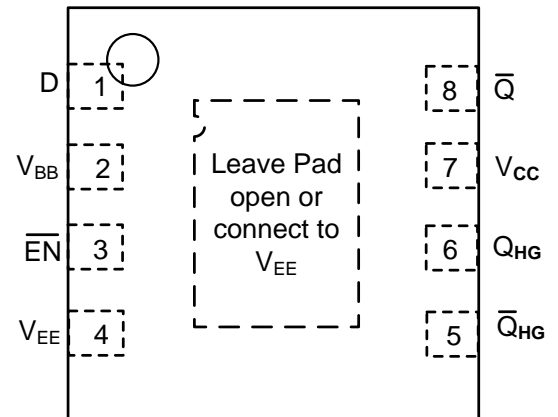
<sup>2</sup> See [www.azmicrotek.com](http://www.azmicrotek.com) for [date code format](#)

**PIN DESCRIPTION AND CONFIGURATION****Table 1 - Pin Description AZ100LVEL16VTNA+**

Pin	Name	Type	Function
1	D	Input	Data Input
2	$\bar{D}$	Input	Inverting Data Input
3	$V_{BB}$	Output	Reference Voltage
4	EN	Input	Output Enable
5	$Q_{HG}$	Output	High Gain Inverting PECL Output
6	$Q_{HG}$	Output	High Gain PECL Output
7	$V_{CC}$	Power	Positive Supply
8	$\bar{Q}$	Output	Inverting PECL Output
9	$V_{EE}$	Power	Negative Supply

**Figure 1 - Pin Configuration for AZ100LVEL16VTNA+****Table 2 - Pin Description AZ100LVEL16VTNB+**

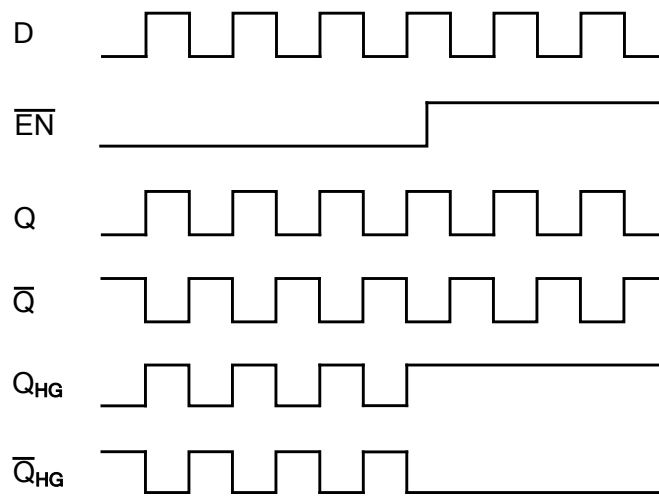
Pin	Name	Type	Function
1	D	Input	Data Input
2	$V_{BB}$	Output	Reference Voltage
3	EN	Input	Output Enable
4	$V_{EE}$	Power	Negative Supply
5	$Q_{HG}$	Output	High Gain Inverting PECL Output
6	$Q_{HG}$	Output	High Gain PECL Output
7	$V_{CC}$	Power	Positive Supply
8	$\bar{Q}$	Output	Inverting PECL Output
9	NC	-	N/A

**Figure 2 - Pin Configuration for AZ100LVEL16VTNB+**

**ENGINEERING NOTES**

The AZ100LVEL16VT is a specialized oscillator gain stage with a high gain output buffer including an enable. The  $Q_{HG}/\bar{Q}_{HG}$  outputs have a voltage gain several times greater than the Q output. When the EN input is LOW, the Q and  $Q_{HG}/\bar{Q}_{HG}$  outputs follow the data inputs. When EN is HIGH, the  $Q_{HG}$  output is forced high and the  $\bar{Q}_{HG}$  output is forced low.

For the AZ100LVEL16VTNA, both D and  $\bar{D}$  inputs are brought out and tied to the  $V_{BB}$  pin through 470 $\Omega$  internal bias resistors. In the AZ100LVEL16VTNB, the D input is internally tied directly to the  $V_{BB}$  pin and the  $\bar{D}$  input is tied to the  $V_{BB}$  pin through a 470 $\Omega$  internal bias resistor. Bypassing  $V_{BB}$  to ground with a 0.01  $\mu$ F capacitor is recommended.



**Figure 3 -Timing Diagram**

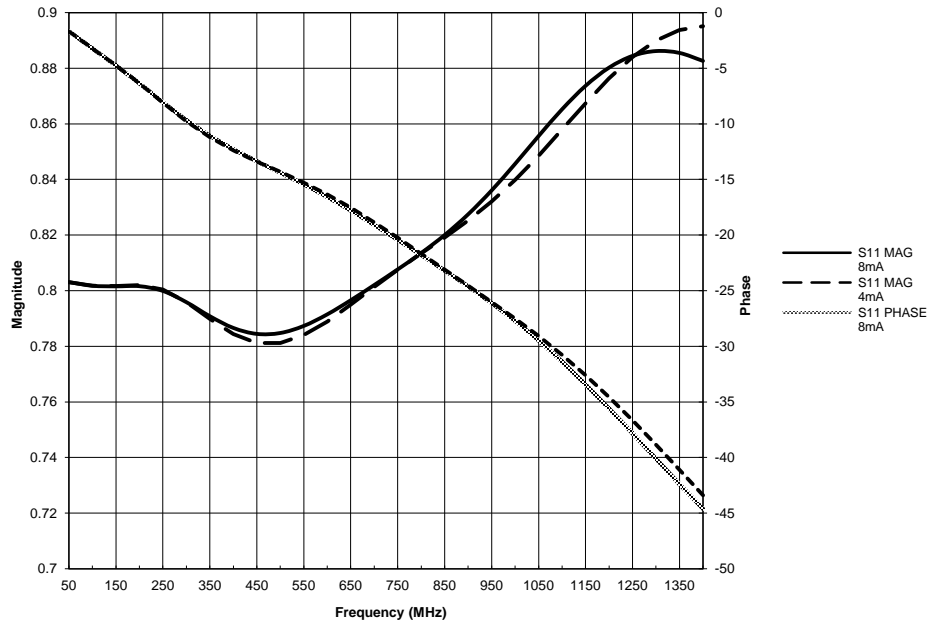


Figure 4 - S11

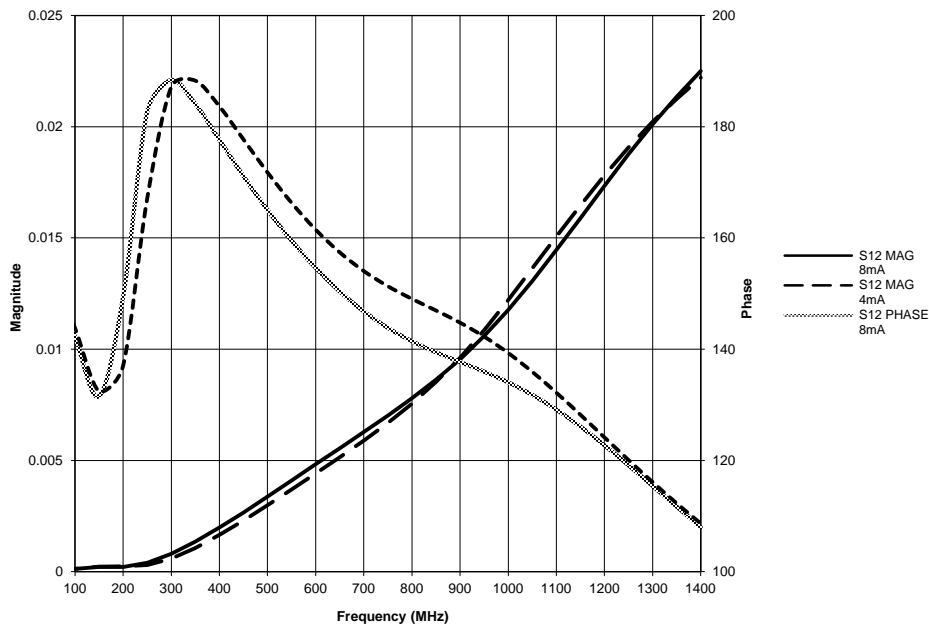


Figure 5 - S12

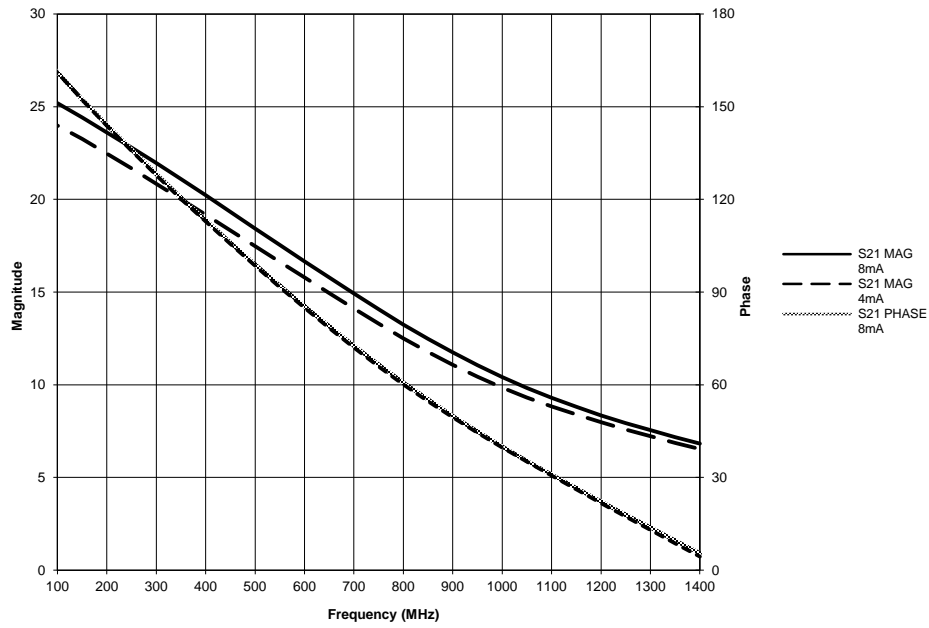


Figure 6 – S21

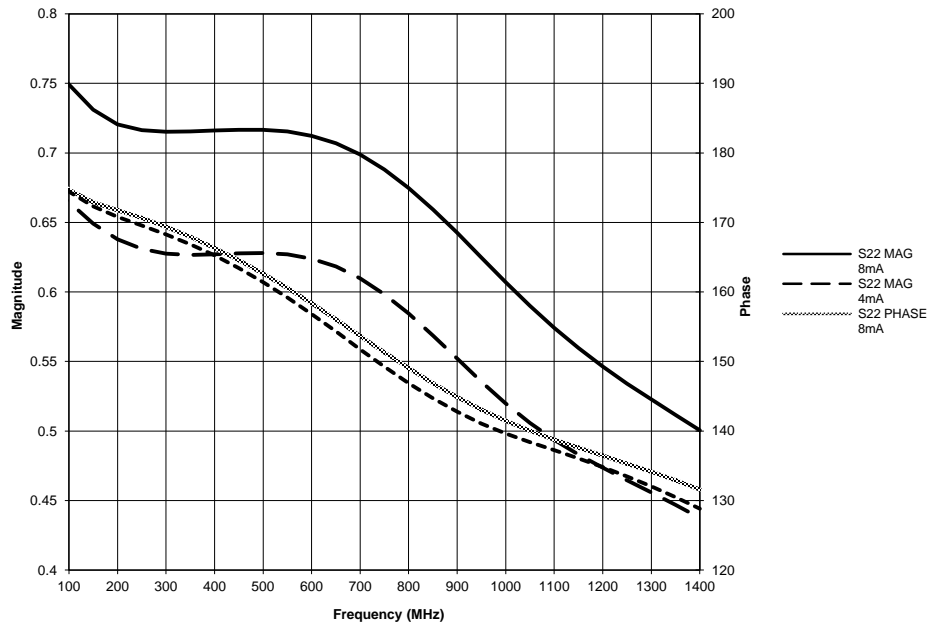


Figure 7 – S22

**PERFORMANCE DATA**

Table 3 – Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V <sub>CC</sub>	PECL Power Supply	V <sub>EE</sub> = 0V	0 to + 6.0	V
V <sub>D_PECL</sub>	PECL D Input Voltage	Referenced to V <sub>BB</sub>	±0.75	V
V <sub>EN_PECL</sub>	PECL D Input Voltage	V <sub>EE</sub> = 0V	0 to + 6.0	V
V <sub>EE</sub>	ECL Power Supply	V <sub>CC</sub> = 0V	-6.0 to 0	V
V <sub>D_ECL</sub>	ECL D Input Voltage	Referenced to V <sub>BB</sub>	±0.75	V
V <sub>EN_ECL</sub>	ECL D Input Voltage	V <sub>CC</sub> = 0V	-6.0 to 0	V
I <sub>OUT</sub>	Output Current	Continuous Q	25	mA
		Surge Q	50	
		Continuous Q <sub>HG</sub>	50	
		Surge Q <sub>HG</sub>	100	
T <sub>A</sub>	Operating Temperature Range	-	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-	-65 to +150	°C
ESD <sub>HBM</sub>	Human Body Model Electro Static Discharge	-	2500	V
ESD <sub>MM</sub>	Machine Model Electro Static Discharge	-	200	V
ESD <sub>CDM</sub>	Charged Device Model Electro Static Discharge	-	2000	V

Table 4 - ECL DC Characteristics

ECL DC Characteristics (V<sub>EE</sub> = -3.0V to -5.5V, V<sub>CC</sub> = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>1</sup>	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
V <sub>OL</sub>	Output LOW Voltage <sup>1</sup>	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V <sub>IH</sub>	Input HIGH Voltage D,EN	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
V <sub>IL</sub>	Input LOW Voltage D,EN	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
V <sub>BB</sub>	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I <sub>IH</sub>	Input HIGH Current EN		150		150		150		150	µA
I <sub>IL</sub>	Input LOW Current EN	0.5		0.5		0.5		0.5		µA
I <sub>EE</sub>	Power Supply Current <sup>1</sup>		48		48		48		54	mA

<sup>1</sup> Specified with each output terminated through 50Ω resistors to V<sub>CC</sub> - 2V.

Table 5 - LVPECL DC Characteristics

LVPECL DC Characteristics ( $V_{EE} = \text{GND}$ ,  $V_{CC} = +3.3\text{V}$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	2255	2465	2275	2465	2275	2465	2275	2465	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	1375	1745	1400	1680	1400	1680	1400	1680	mV
$V_{IH}$	Input HIGH Voltage D,EN	2135	2560	2135	2560	2135	2560	2135	2560	mV
$V_{IL}$	Input LOW Voltage D,EN	1400	1825	1400	1825	1400	1825	1400	1825	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	1910	2050	1910	2050	1910	2050	1910	2050	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	μA
$I_{IL}$	Input LOW Current EN	0.5		0.5		0.5		0.5		μA
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		54	mA

<sup>1</sup> For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value

<sup>2</sup> Specified with each output terminated through 50Ω resistors to  $V_{CC} - 2\text{V}$ .

Table 6 - PECL DC Characteristics

PECL DC Characteristics ( $V_{EE} = \text{GND}$ ,  $V_{CC} = +5.0\text{V}$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	3955	4165	3975	4165	3975	4165	3975	4165	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	3075	3445	3100	3380	3100	3380	3100	3380	mV
$V_{IH}$	Input HIGH Voltage D,EN	3835	4260	3835	4260	3835	4260	3835	4260	mV
$V_{IL}$	Input LOW Voltage D,EN	3100	3525	3100	3525	3100	3525	3100	3525	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	3610	3750	3610	3750	3610	3750	3610	3750	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	μA
$I_{IL}$	Input LOW Current EN	0.5		0.5		0.5		0.5		μA
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		54	mA

<sup>1</sup> For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value

<sup>2</sup> Specified with each output terminated through 50Ω resistors to  $V_{CC} - 2\text{V}$ .

Table 7 - AC Characteristics

AC Characteristics ( $V_{EE} = -3.0V$  to  $-5.5V$ ;  $V_{CC}=GND$  or  $V_{EE}=GND$ ;  $V_{CC} = +3.0V$  to  $+5.5V$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{PLH}/t_{PHL}$	Propagation Delay													
	D to Q <sup>1</sup>			350			350			350			350	ps
	D to Q <sub>HG</sub> <sup>2</sup>			450			450			450			450	ps
$t_{SKEW}$	Duty Cycle Skew <sup>3</sup>		5	20		5	20		5	20		5	20	ps
V <sub>pp</sub> (AC)	Input Swing <sup>4</sup> Differential	80		1000	80		1000	80		1000	80		1000	mV
	Input Swing <sup>4</sup> Single Ended	160		1500	160		1500	160		1500	160		1500	
$t_r/t_f$	Output Rise/Fall <sup>1,2</sup> (20% - 80%)	100		240	100		240	100		240	100		240	ps

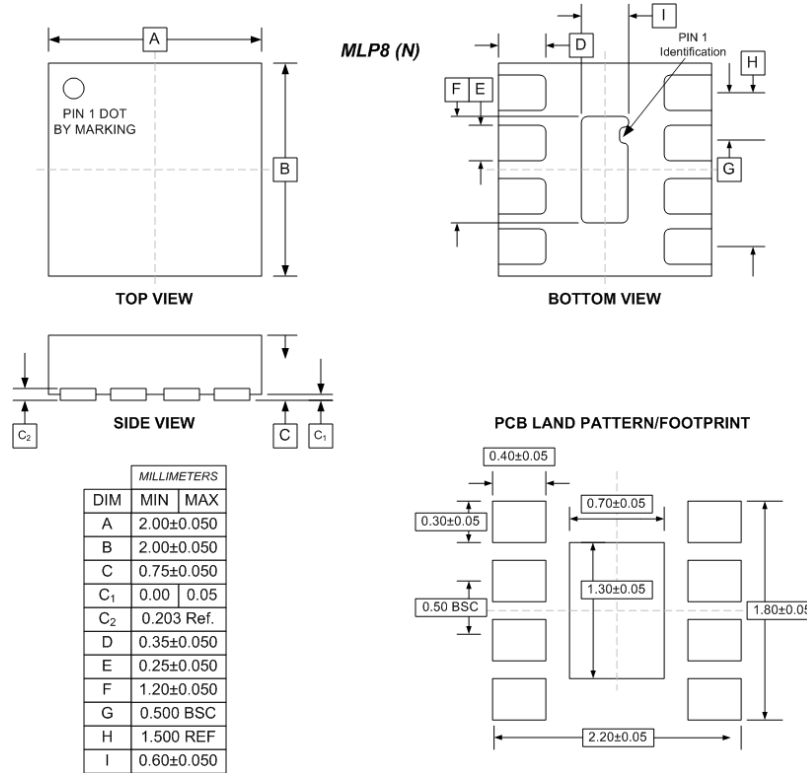
<sup>1</sup> Specified with each output terminated through 50Ω resistors to  $V_{CC} - 2V$ .

<sup>2</sup> Specified with each output terminated through 50Ω resistors to  $V_{CC} - 2V$ .

<sup>3</sup> Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.

<sup>4</sup> The peak-to-peak input swing is the range for which AC parameters are guaranteed. D and D<sup>-</sup> must remain within the range of ± 750 mV with respect to  $V_{BB}$ . The device has a voltage gain of ~20 to the Q<sup>-</sup> outputs and a voltage gain of ~100 to the Q<sub>HG</sub>/Q<sup>-</sup><sub>HG</sub> outputs.

**PACKAGE DIAGRAM**  
MLP8  
Green/RoHS compliant/Pb-Free  
MSL=1



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