AZ100ELT22

Dual CMOS/TTL to Differential PECL Translator

www.azmicrotek.com

DESCRIPTION

The AZ100ELT22 is a dual CMOS/TTL to differential PECL translator. Because PECL (Positive ECL) levels are used, only V_{CC} and ground are required. The small outline packaging and the low skew, dual gate design of the AZ100ELT22 makes it ideal for applications that require the translation of a clock and a data signal.

The AZ100ELT22 is a direct replacement for the ON Semi MC100ELT22, MC100LVELT22 and Micrel SY89322V

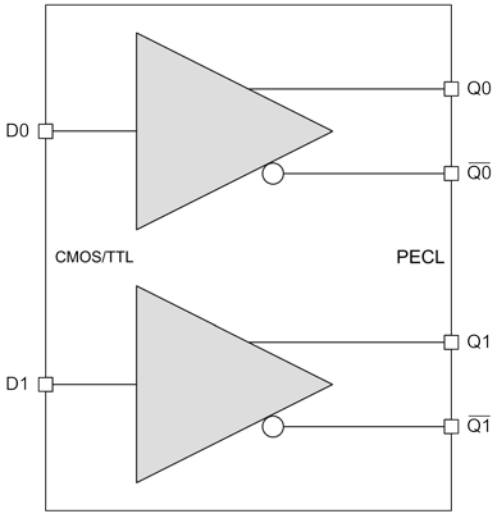
FEATURES

- 0.5ns typical propagation delay
- <100ps typical output to output skew
- Differential PECL outputs
- Flow through pinouts

APPLICATIONS

- LVCMOS/LVTTL to LVPECL translations
- CMOS/TTL to PECL translations

BLOCK DIAGRAM



PACKAGE AVAILABILITY

- MSOP8
  - Green/RoHS/Pb-Free
- SOIC8
  - Green/RoHS/Pb-Free

Order Number	Package	Marking
AZ100ELT22DG[1]	SOIC8	HT22G[2]
AZ100ELT22TG[1]	MSOP8	HT22G[2]

[1] Tape & Reel - Add 'R1' at end of order number for 7in (1k parts), 'R2' (2.5k) for 13in

[2] See www.azmicrotek.com for date code format

www.azmicrotek.com
+1-480-962-5881
Request a Sample

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Mesa, AZ 85204 USA

May 2012, Rev 2.0

PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin Description

Pin	Name	Type	Function
1	Q0	Output	PECL Output
2	$\overline{Q0}$	Output	PECL Output
3	Q1	Output	PECL Output
4	$\overline{Q1}$	Output	PECL Output
5	GND	Power	Negative Supply
6	D1	Input	Data Input
7	D0	Input	Data Input
8	V_{CC}	Power	Positive Supply

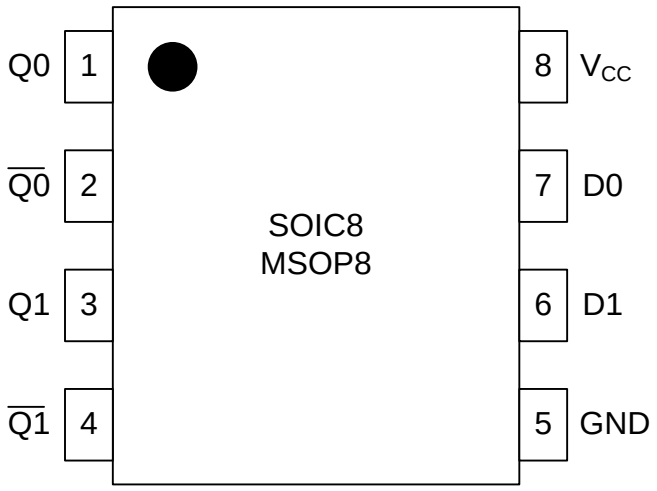


Figure 1 - Pin Configuration SOIC8/MSOP8

ENGINEERING NOTES

When the D input is left floating, the Q output is forced HIGH, and the $\overline{Q}$ output is forced LOW.

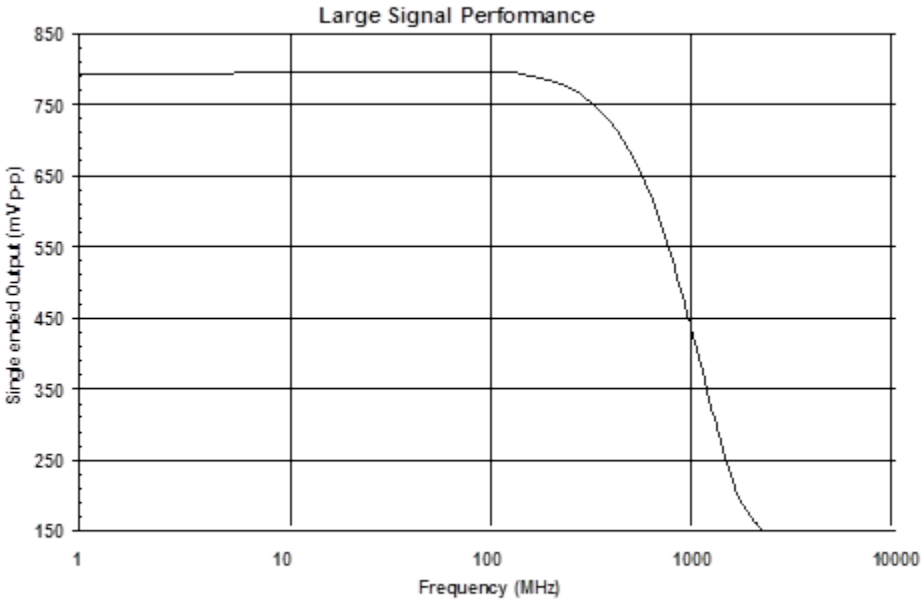


Figure 2 – AZ100ELT22 Large Signal Bandwidth

PERFORMANCE DATA

Table 2 – Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	DC Power Supply	(V_{EE} = 0V)	0 to +8.0	V
V_{IN}	Input Voltage	(V_{EE} = 0V)	0 to +6.0	V
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range		-40 to +85	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C
ESD_{HBM}	Human Body Model		2500	V
ESD_{MM}	Machine Model		200	V
ESD_{CDM}	Charged Device Model		2500	V

Table 3 – TTL/CMOS Input DC Characteristics

TTL/CMOS Input DC Characteristics (GND = 0.0V, V_{CC} = +3.3V to 5.5V)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7V			15	µA
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}			20	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V			-0.1	mA
V_{IK}	Input Clamp Diode Voltage	I_{IN} = -18mA			-1.2	V
V_{IH}	Input HIGH Voltage		2			V
V_{IL}	Input LOW Voltage				0.8	V

Table 4 - LVPECL DC Characteristics

LVPECL DC Characteristics (GND = 0.0V, V_{CC} = +3.3V)

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	2160		2420	2205		2420	2235	2345	2420	2255		2420	mV
V_{OL}	Output LOW Voltage[1,2]	1470		1745	1490		1680	1490	1595	1680	1490		1680	mV
I_{CC}	Power Supply Current[3]			24			24			24			25	mA

[1] Each output is terminated through a 50Ω resistor to V_{CC} - 2V.

[2] Output parameters vary 1:1 with V_{CC}

[3] I_{CC} measurements must be done with outputs open

Table 5 - PECL DC Characteristics

PECL DC Characteristics (GND = 0.0V, V_{CC} = +5.0V)

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	3860		4120	3905		4120	3935	4045	4120	3955		4120	mV
V_{OL}	Output LOW Voltage[1,2]	3170		3445	3190		3380	3190	3295	3380	3190		3380	mV
I_{EE}	Power Supply Current[3]			24			24			24			25	mA

1 Each output is terminated through a 50Ω resistor to V_{CC} - 2V.

2 Output parameters vary 1:1 with V_{CC}

3 I_{CC} measurements must be done with outputs open

Table 6 - AC Characteristics

AC Characteristics (GND = 0.0V, V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Delay to Output[1]	100		550	100		550	100		550	100		550	ps
t_r/t_f	Output Rise/Fall Times Q (20%-80%)	80		250	80		250	80		250	80		250	ps
f_{max}	Maximum Frequency[2]	800			800			800			800			MHz

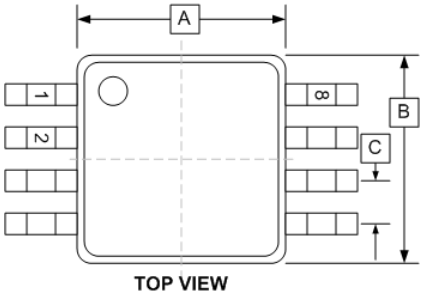
1 Propagation delay is measured from +1.5V on the input to 50% of the PECL output swing

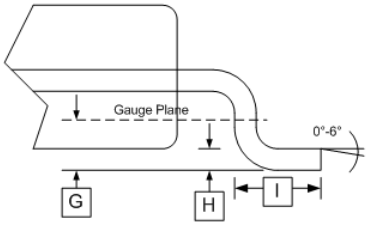
2 Output as -3dB

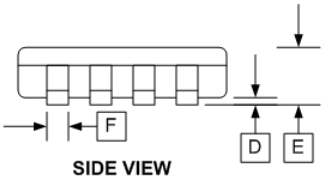
PACKAGE DIAGRAM

SOIC8
Green/RoHS compliant/Pb-Free
MSL=1

SOIC8 (D)



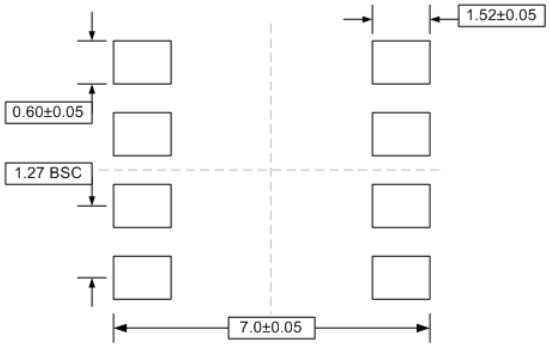




	INCHES	
DIM	MIN	MAX
A	0.189	0.196
B	0.150	0.157
C	0.050 BSC	
D	0.004	0.01
E	0.054	0.068
F	0.014	0.019
G	0.010	
H	0.0075	0.0098
I	0.016	0.034

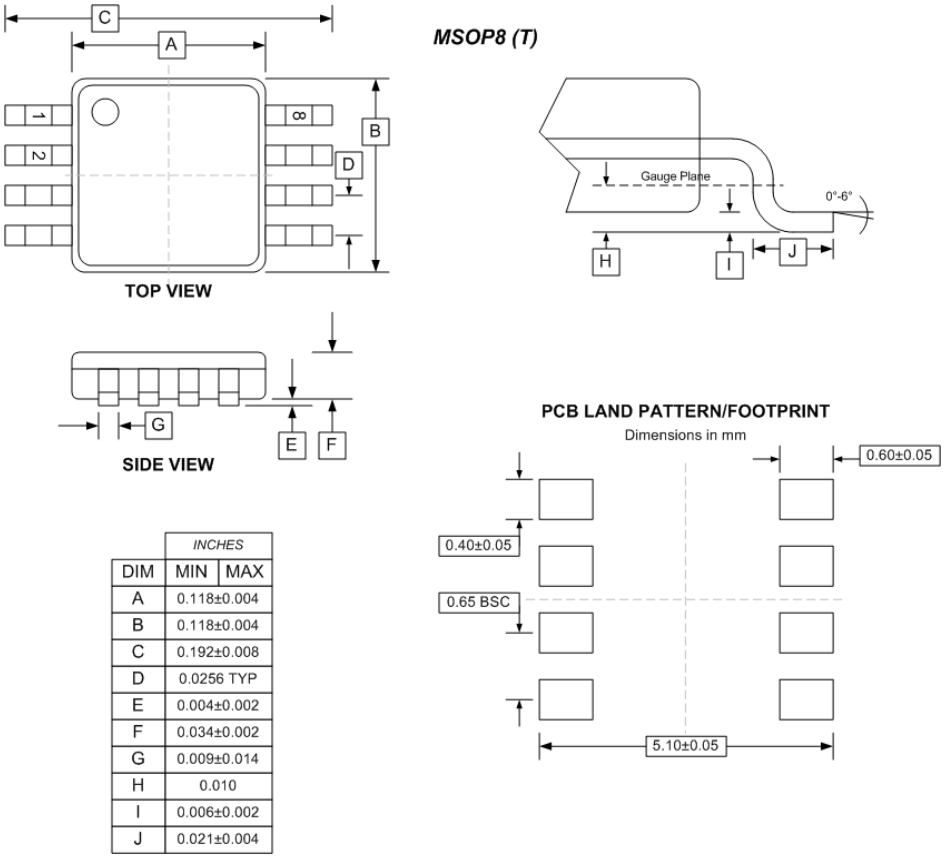
PCB LAND PATTERN/FOOTPRINT

Dimensions in mm



PACKAGE DIAGRAM

MSOP8
Green/RoHS compliant/Pb-Free
MSL=1



DIM	INCHES MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0256 TYP	
E	0.004±0.002	
F	0.034±0.002	
G	0.009±0.014	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	