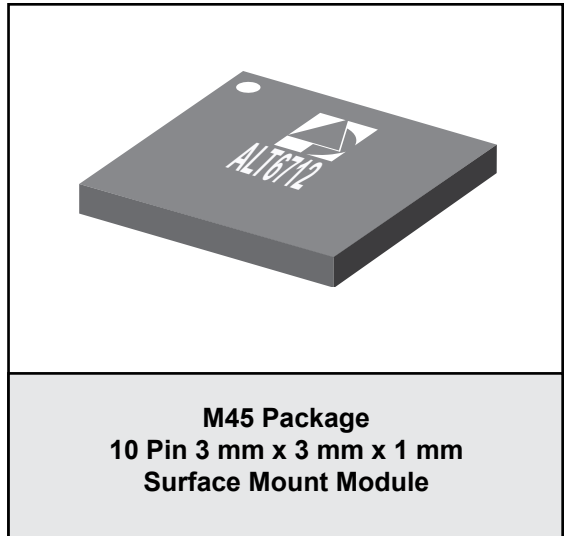


FEATURES

- LTE Compliant
- 4th Generation HELP™ technology
- High Efficiency (LTE MPR = 0 dB):
 - 34 % @ P_{OUT} = +27.5 dBm
 - 17 % @ P_{OUT} = +16 dBm
 - 10 % @ P_{OUT} = +6 dBm
- Low Quiescent Current: 4 mA
- Low Leakage Current in Shutdown Mode: 4 μA
- Internal Voltage Regulator
- Integrated “daisy chainable” directional coupler with CPL_{IN} and CPL_{OUT} port.
- Internal DC blocks on all RF ports
- Optimized for a 50 Ω System
- 1.8 V Control Logic
- RoHS Compliant Package, 260 °C MSL-3



APPLICATIONS

- Band 12 & 17 LTE Wireless Devices

PRODUCT DESCRIPTION

The ALT6712 HELP4™ PA is a 4th generation HELP™ product for LTE devices operating in UMTS 700 MHz Bands 12 and 17. This PA incorporates ANADIGICS’ HELP4™ technology to deliver exceptional efficiency at low power levels and low quiescent current without the need for external voltage regulators or converters. The device is manufactured using advanced InGaP-Plus™ HBT technology offering state-of-the-art reliability, temperature stability, and ruggedness. Three selectable bias modes that optimize efficiency for different output power levels and a shutdown mode with low leakage current increase handset talk and standby time. A “daisy chainable” directional coupler is integrated in the module, thus eliminating the need of an external coupler. The self-contained 3 mm x 3 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency, and linearity in a 50 Ω system.

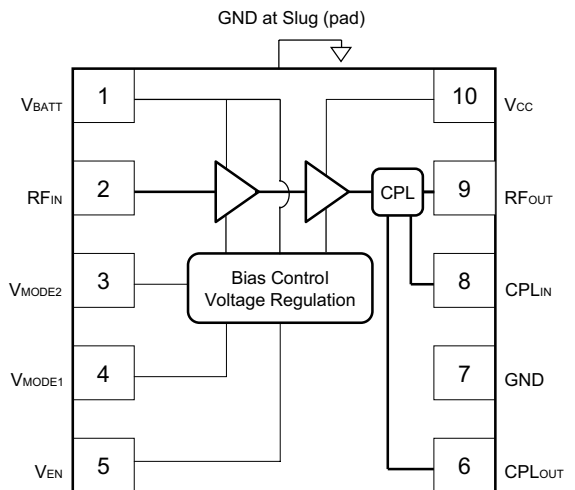


Figure 1: Block Diagram

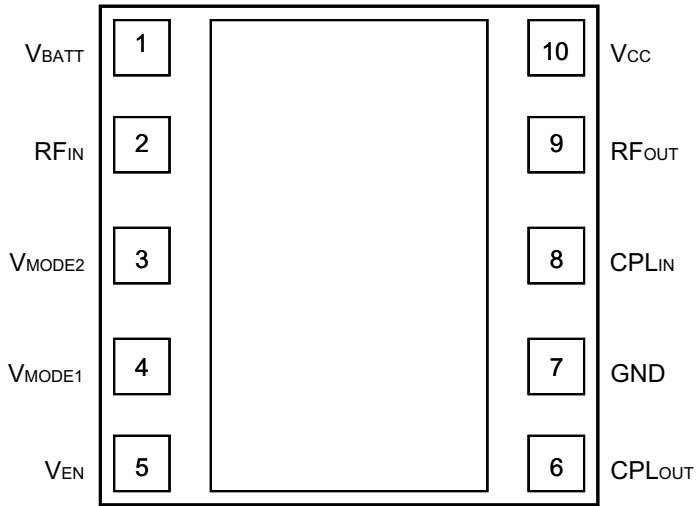


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V_{BATT}	Battery Voltage
2	RF_{IN}	RF Input
3	V_{MODE2}	Mode Control Voltage 2
4	V_{MODE1}	Mode Control Voltage 1
5	V_{EN}	PA Enable Voltage
6	CPL_{OUT}	Coupler Output
7	GND	Ground
8	CPL_{IN}	Coupler Input
9	RF_{OUT}	RF Output
10	V_{CC}	Supply Voltage

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{CC})	0	+5	V
Battery Voltage (V_{BATT})	0	+6	V
Control Voltages (V_{MODE1} , V_{MODE2} , V_{EN})	0	+3.5	V
RF Input Power (P_{IN})	-	+10	dBm
Storage Temperature (T_{STG})	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	698	-	716	MHz	
Supply Voltage (V_{CC})	+3.1	+3.4	+4.35	V	$P_{OUT} < +27.5$ dBm
Enable Voltage (V_{EN})	+1.35 0	+1.8 -	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage (V_{MODE1} , V_{MODE2})	+1.35 0	+1.8 -	+3.1 +0.5	V	Low Bias Mode High Bias Mode
LTE/UMTS Power ^(1, 2)					
LTE (MPR=0), HPM	-	27.5	-	dBm	TS 36.101 Rel 8 for LTE
LTE (MPR=0), MPM	-	16	-		
LTE (MPR=0), LPM	-	6	-		
Case Temperature (T_c)	-40	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

- (1) LTE waveform characteristics: 10 MHz QPSK, 12 RB.
(2) For operation at +105 °C, P_{OUT} is derated by 1.0 dB.

Table 4: Electrical Specifications - LTE Operation (MPR = 0 dB waveform, 10 MHz QPSK, 12 RB)
(T_C = +25 °C, V_{CC} = +3.4 V, V_{BATT} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P _{OUT}	V _{MODE1}	V _{MODE2}
Gain	26 16 8	29 19 11	32 22 14	dB	+27.5 dBm +16 dBm +6 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
LTE to LTE, E-UTRA	- - -	-40 -39 -44	-35 -35 -35	dBc	+27.5 dBm +16 dBm +6 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
UTRA ACLR1	- - -	-41 -40 -44	-37 -36 -38	dBc	+27.5 dBm +16 dBm +6 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
UTRA ACLR2	- - -	-64 -64 -66	-40 -40 -40	dBc	+27.5 dBm +16 dBm +6 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency ⁽¹⁾	30 14 8	34 17 10	- - -	%	+27.5 dBm +16 dBm +6 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Quiescent Current (I _{cq}) Low Bias Mode	-	4	5.5	mA	through V _{BATT} and V _{CC} pins	1.8 V	1.8 V
Mode Control Current	-	0.08	0.15	mA	through V _{MODE} pins, V _{MODE1,2} = +1.8 V		
Enable Current	-	0.1	0.2	mA	through V _{EN} pin		
BATT Current	-	0.8	1.5	mA	through V _{BATT} pin, V _{MODE1,2} = +1.8 V		
Leakage Current	-	4	10	μA	V _{BATT} = +4.35 V, V _{CC} = +4.35 V V _{EN} = 0 V, V _{MODE1,2} = 0 V		
Noise Power	- - -	-131 -140 -145	- - -	dBm/Hz	746 - 768 MHz GPS Band, 1574 - 1577 MHz ISM Band, 2400 - 2483.5 MHz		
Harmonics 2fo 3fo, 4fo	- - -	-47 -62	- - -	dBc	P _{OUT} ≤ +27.5 dBm		
Coupling Factor	-	20	-	dB			
Directivity	-	21	-	dB			
Daisy Chain Insertion Loss	-	<0.36	-	dB	698 to 2620 MHz Pin 8 through 9, Shutdown Mode		
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	P _{OUT} ≤ +27.5 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		
Phase Delta: HPM - LPM HPM - MPM MPM - LPM	- - - -	-68 138 153	- - -	Deg			

Notes:

(1) ACLR and Efficiency measured at 707 MHz.

APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: <http://www.anadigics.com>

Shutdown Mode

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the V_{EN} , V_{MODE1} and V_{MODE2} voltages.

Bias Modes

The power amplifier may be placed in either Low, Medium or High Bias modes by applying the appropriate logic level (see Operating Ranges table)

to the V_{MODE} pins. The Bias Control table below lists the recommended modes of operation for various applications.

Three operating modes are recommended to optimize current consumption. High Bias/High Power operating mode is for P_{OUT} levels ≥ 16 dBm. At ~ 16 dBm - 6 dBm, the PA could be switched to Medium Power Mode. For P_{OUT} levels ≤ -6 dBm, the PA could be switched to Low Power Mode for extremely low current consumption.

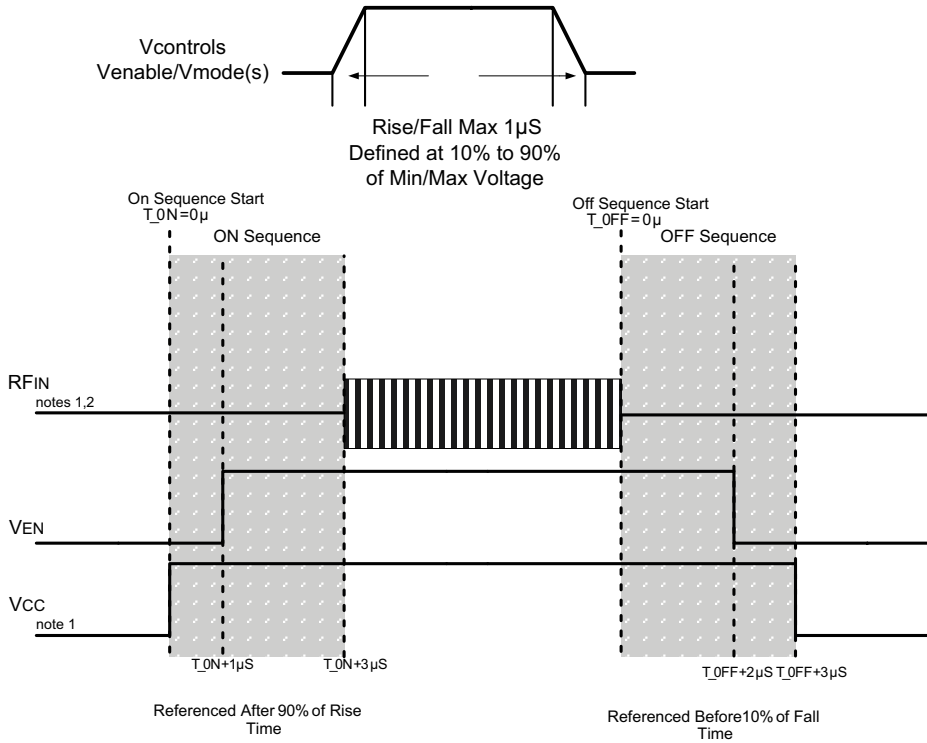


Figure 3: Recommended ON/OFF Timing Sequence

Notes:

- (1) Level might be changed after RF is ON.
- (2) RF OFF defined as $P_{IN} \leq -30$ dBm.
- (3) Switching simultaneously between V_{MODE} and V_{EN} is not recommended.

Table 5: Bias Control

APPLICATION	P _{OUT} LEVELS	BIAS MODE	V _{EN}	V _{MODE1}	V _{MODE2}	V _{CC}	V _{BATT}
Low power (Low Bias Mode)	< +6 dBm	Low	+1.8 V	+1.8 V	+1.8 V	3.1 - 4.35 V	≥ 3.1 V
Med power (Medium Bias Mode)	> 6 dBm < +16 dBm	Low	+1.8 V	+1.8 V	0 V	3.1 - 4.35 V	≥ 3.1 V
High power (High Bias Mode)	> +16 dBm	High	+1.8 V	0 V	0 V	3.1 - 4.35 V	≥ 3.1 V
Shutdown	-	Shutdown	0 V	0 V	0 V	3.1 - 4.35 V	≥ 3.1 V

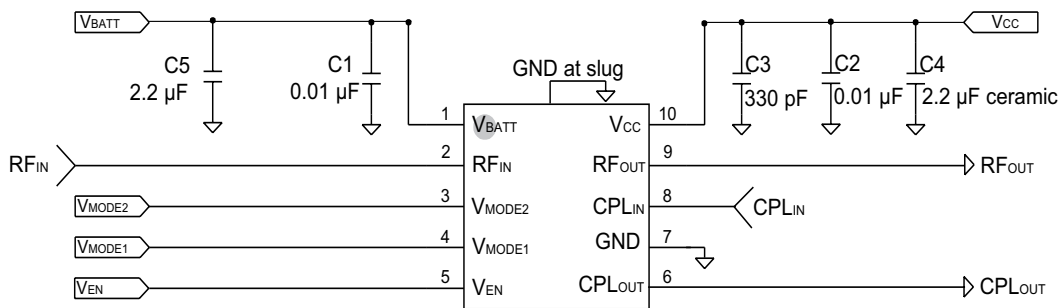
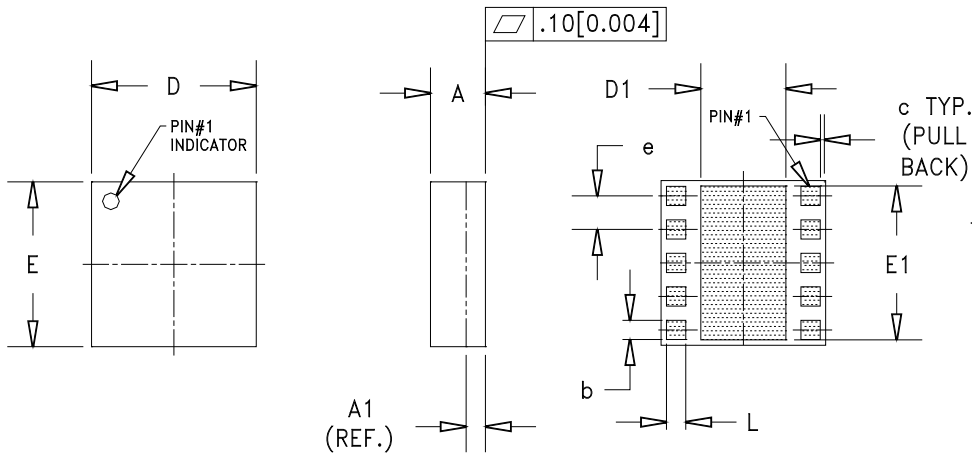


Figure 4: Evaluation Board Schematic

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.91	1.03	1.13	0.035	0.041	0.044	-
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						-
b	0.32	0.35	0.40	0.013	0.014	0.016	3
c	-	0.10	-	-	0.004	-	-
D	2.88	3.00	3.12	0.113	0.118	0.123	-
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	2.88	3.00	3.12	0.113	0.118	0.123	-
E1	2.70	2.75	2.85	0.106	0.108	0.112	3
e	-	0.60	-	-	0.024	-	3
L	0.32	0.35	0.40	0.013	0.014	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
5. LAMINATE CONTROL DRAWING SPECIFIED BY PART NUMBER.

Figure 5: M45 Package Outline - 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module

TOP BRAND

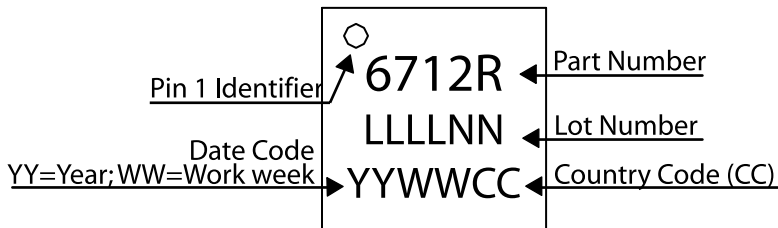
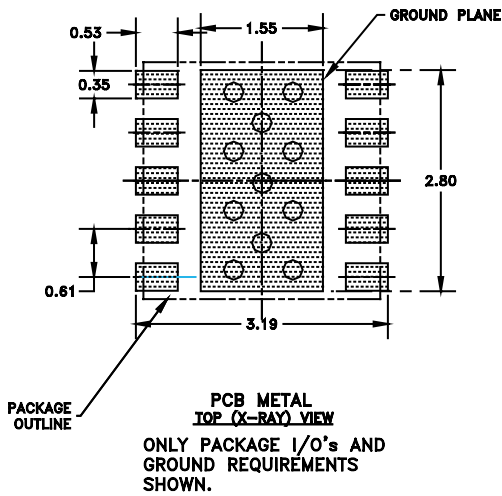


Figure 6: Branding Specification - M45 Package

PCB AND STENCIL DESIGN GUIDELINE



NOTES:

- (1) OUTLINE DRAWING REFERENCE: P8002478_E
- (2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
- (3) DIMENSIONS IN MILLIMETERS.
- (4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.
- (5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)

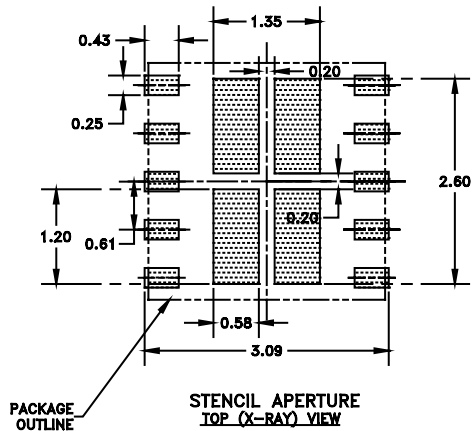
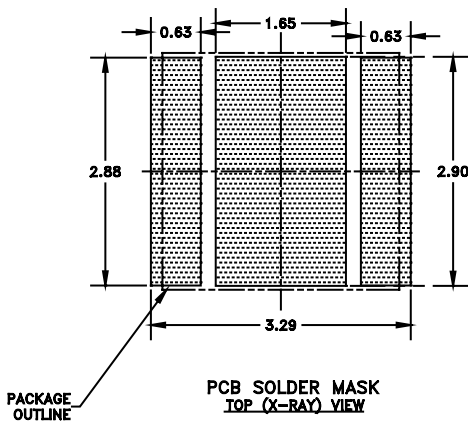
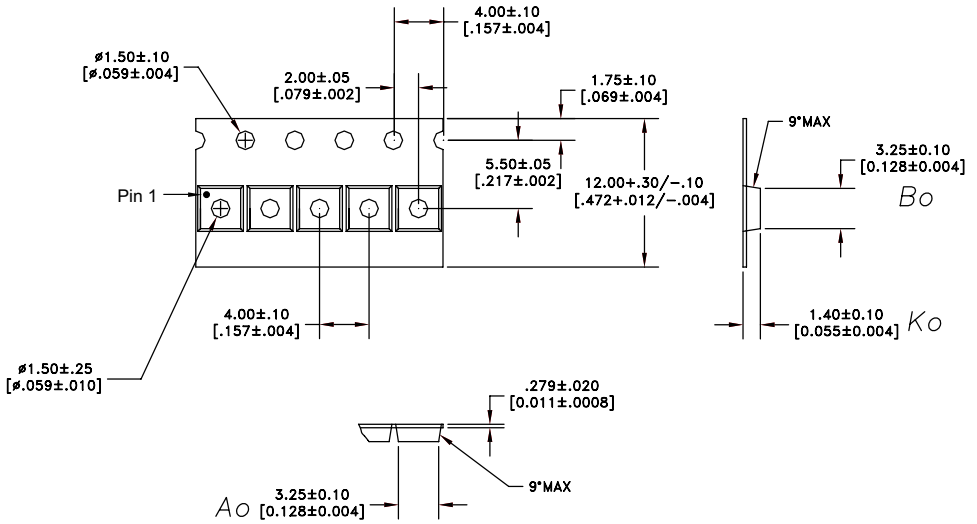


Figure 7: Recommended PCB Layout Information

COMPONENT PACKAGING



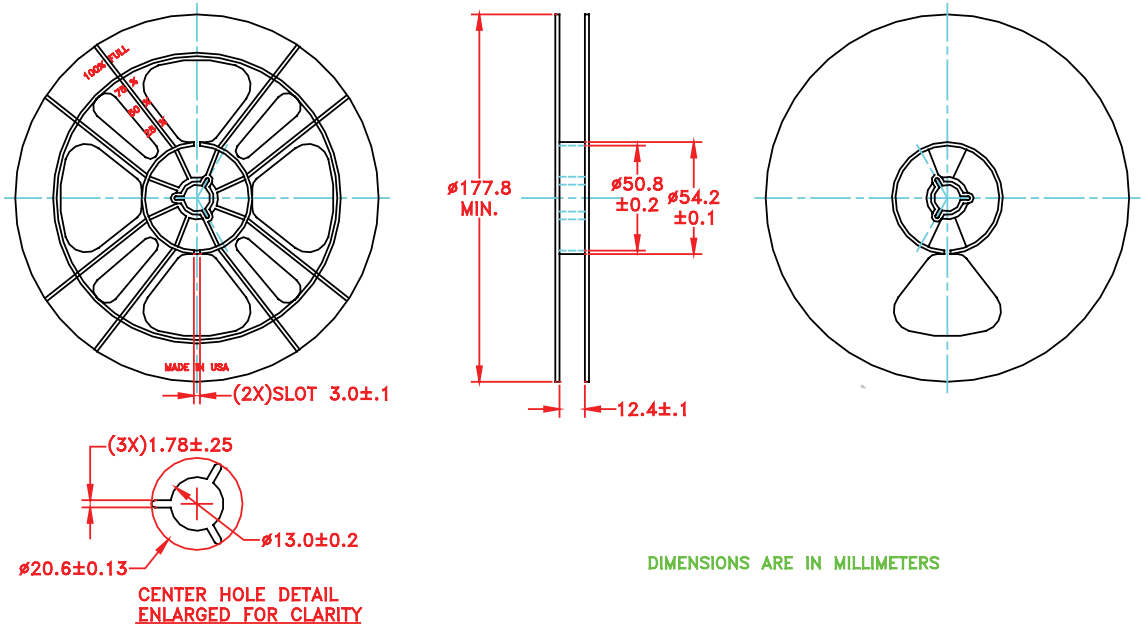
NOTES:

- 1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)
100% RECYCLABLE.

DIMENSIONS ARE IN MILLIMETERS [INCHES]

DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

Figure 8: Carrier Tape



NOTES:

- 1. MATERIAL: BLACK CARBON POLYSTYRENE
- SURFACE RESISTIVITY: 1×10^4 TO 1×10^6 ohms/square

DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

Table 9: Reel

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ALT6712RM45Q7	-40 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
ALT6712RM45P9	-40 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Partial Tape and Reel



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