

FEATURES

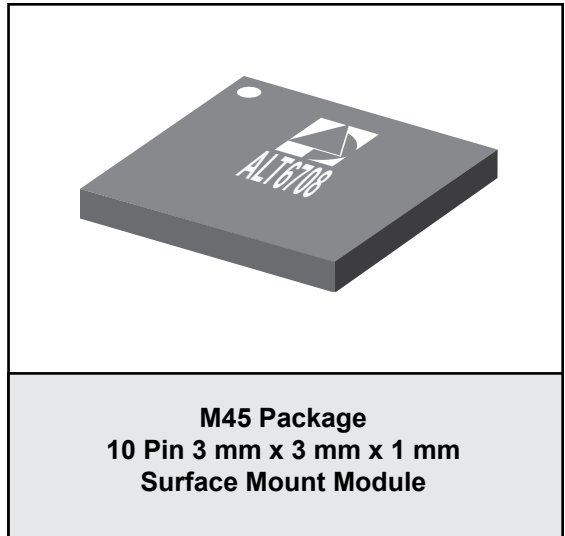
- HSPA, LTE Compliant
- 4th Generation HELP™ technology
- High Efficiency (R99 waveform):
 - 40 % @ P_{OUT} = +28.8 dBm
 - 26 % @ P_{OUT} = +17 dBm
 - 17 % @ P_{OUT} = +13.5 dBm
 - 18 % @ P_{OUT} = +7.5 dBm
 - 10 % @ P_{OUT} = +3.5 dBm
- Low Quiescent Current: 3 mA
- Low Leakage Current in Shutdown Mode: <5 μA
- Internal Voltage Regulator
- Integrated “daisy chainable” directional coupler with CPL_{IN} and CPL_{OUT} port.
- Internal DC Blocks on all RF ports
- Optimized for a 50 Ω System
- 1.8V Control Logic
- RoHS Compliant Package, 260 °C MSL-3

APPLICATIONS

- Band 8 LTE Wireless Devices
- Band 8 (EGSM) WCDMA/HSPA Wireless Devices

PRODUCT DESCRIPTION

The ALT6708 HELP4™ PA is a 4th generation HELP™ product for LTE and WCDMA devices operating in UMTS900 (Band 8) . This PA incorporates ANADIGICS’ HELP4™ technology to deliver exceptional efficiency at low power levels and low quiescent current without the need for external voltage regulators or converters. The device is manufactured using advanced InGaP-Plus™ HBT technology offering state-of-the-art reliability, temperature stability, and ruggedness. Three selectable bias modes that optimize efficiency for different output power levels and a shutdown mode with low leakage current increase handset talk and standby time. A “daisy chainable” directional coupler is



integrated in the module, thus eliminating the need of an external coupler. The self-contained 3 mm x 3 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency, and linearity in a 50 Ω system.

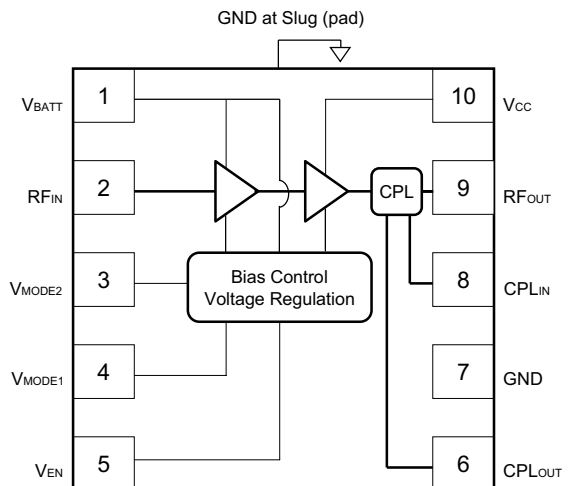


Figure 1: Block Diagram

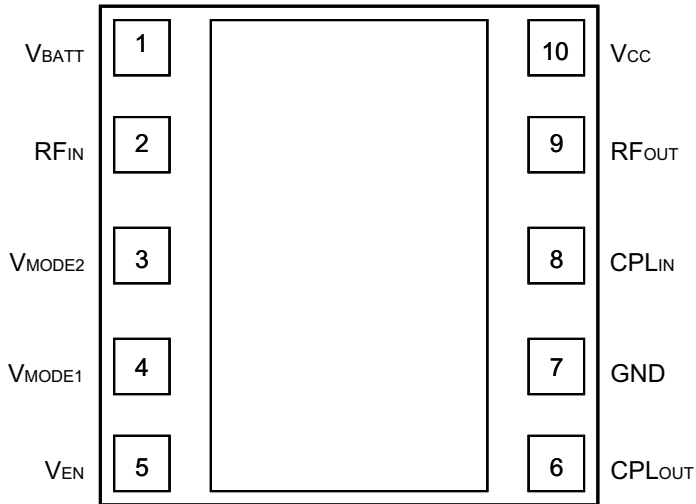


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	VBATT	Battery Voltage
2	RFIN	RF Input
3	VMODE2	Mode Control Voltage 2
4	VMODE1	Mode Control Voltage 1
5	VEN	PA Enable Voltage
6	CPLOUT	Coupler Output
7	GND	Ground
8	CPLIN	Coupler Input
9	RFOUT	RF Output
10	VCC	Supply Voltage

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{CC})	0	+5	V
Battery Voltage (V_{BATT})	0	+6	V
Control Voltages (V_{MODE1} , V_{MODE2} , V_{EN})	0	+3.5	V
RF Input Power (P_{IN})	-	+10	dBm
Storage Temperature (T_{STG})	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	880	-	915	MHz	
Supply Voltage (V_{CC})	+3.1	+3.4	+4.35	V	$P_{OUT} < +28.8$ dBm
Enable Voltage (V_{EN})	+1.35 0	+1.8 -	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage (V_{MODE1} , V_{MODE2})	+1.35 0	+1.8 -	+3.1 +0.5	V	Low Bias Mode High Bias Mode
WCDMA/UMTS Output Power ^(1, 3)					
R99 WCDMA, HPM	28.0	28.8	-	dBm	3GPP TS 34.121-1, Rel 8 Table C.11.1.3, SUBTEST 1
HSPA (MPR=0), HPM	26.9	27.7	-		
LTE ⁽²⁾	26.9	27.7	-		
R99 WCDMA, MPM	-	17.0	-		
LTE ⁽²⁾ & HSPA (MPR=0), MPM	-	16.0	-		
R99 WCDMA, LPM	-	7.5	-		
LTE ⁽²⁾ & HSPA (MPR=0), LPM		6.5			TS 36.101 Rel 8 for LTE
Case Temperature (T_C)	-40	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

- (1) For operation at 3.1 V, P_{OUT} is derated by 0.8 dB.
- (2) LTE waveform characteristics: up to 15MHz, QPSK, RB = 16.
- (3) For Operation at +105 °C, P_{OUT} is derated by 1.0 dB.

Table 4: Electrical Specifications - LTE Operation (RB = 12, START = 0, QPSK)
(T_c = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P _{OUT}	V _{MODE1}	V _{MODE2}
Gain	25 14 9	27.5 17.5 12.5	31 21 16	dB	P _{OUT} = +27.7 dBm P _{OUT} = +16 dBm P _{OUT} = +6.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR E-UTRA at ± 10 MHz offset	- - -	-39 -39 -40	-35 -35 -35	dBc	P _{OUT} = +27.7 dBm P _{OUT} = +16 dBm P _{OUT} = +6.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR UTRA at ± 7.5 MHz offset	- - -	-39 -40 -40	-36.5 -36.5 -36.5	dBc	P _{OUT} = +27.7 dBm P _{OUT} = +16 dBm P _{OUT} = +6.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR UTRA at ± 12.5 MHz offset	- - -	-59 -60 -60	-40 -40 -40	dBc	P _{OUT} = +27.7 dBm P _{OUT} = +16 dBm P _{OUT} = +6.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency	31 18 12	35 22 17	- - -	%	P _{OUT} = +27.7 dBm P _{OUT} = +16 dBm P _{OUT} = +6.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Quiescent Current (I _{cq}) Low Bias Mode	-	2.8	4.5	mA	through V _{CC} pin	1.8 V	1.8 V
Mode Control Current	-	0.06	0.15	mA	through V _{MODE} pins, V _{MODE1,2} = +1.8 V		
Enable Current	-	0.03	0.1	mA	through V _{EN} pin, V _{EN} = +1.8 V		
BATT Current	-	0.8	1.5	mA	through V _{BATT} pin, V _{MODE1,2} = +1.8 V		
Leakage Current	-	<5	10	μA	V _{BATT} = V _{CC} = +4.35 V, V _{EN} = 0 V, V _{MODE1,2} = 0 V		
Noise in Receive Band	-	-133	-	dBm/Hz	925 MHz to 960 MHz		
Harmonics 2fo 3fo, 4fo	- - -	-50 -58	-35 -45	dBc	P _{OUT} ≤ +27.7 dBm		
Input Impedance	-	-	2:1	VSWR			
Coupling Factor	-	20	-	dB			
Directivity	-	20	-	dB			
Coupler IN_OUT Daisy Chain Insertion Loss	-	0.35	-	dB	698 MHz to 2620 MHz Pin 6-8, Shutdown Mode		
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	P _{OUT} ≤ +27.7 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

Notes:

(1) ACLR and Efficiency measured at 897.5 MHz.

Table 5: Electrical Specifications - WCDMA Operation (R99 Modulation)
(T_C = +25 °C, V_{CC} = +3.4 V, V_{BATT} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P _{OUT}	V _{MODE1}	V _{MODE2}
Gain	25 14 9	27.5 17.5 12.5	31 21 16	dB	P _{OUT} = +28.8 dBm P _{OUT} = +17 dBm P _{OUT} = +7.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR1 at 5 MHz offset ⁽¹⁾	- - -	-41 -42 -41	-36.5 -36.5 -36.5	dBc	P _{OUT} = +28.8 dBm P _{OUT} = +17 dBm P _{OUT} = +7.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR2 at 10 MHz offset	- - -	-55 -57 -59	-48 -48 -48	dBc	P _{OUT} = +28.8 dBm P _{OUT} = +17 dBm P _{OUT} = +7.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency ⁽¹⁾	36 22 - 13 -	40 26 17 18 10	- - - - -	%	P _{OUT} = +28.8 dBm P _{OUT} = +17 dBm P _{OUT} = +13.5 dBm P _{OUT} = +7.5 dBm P _{OUT} = +3.5 dBm	0 V 1.8 V 1.8 V 1.8 V 1.8 V	0 V 0 V 0 V 1.8 V 1.8 V
Spurious Output Level (all spurious outputs)	-	-	<-70	dBc	P _{OUT} ≤ +28.8 dBm In-band land VSWR < 5:1 Out-of-band load VSWR < 10 : 1 Applies over all operating ranges		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

Notes:

(1) ACLR and Efficiency measured at 897.5 MHz.

PERFORMANCE DATA PLOTS:
(WCDMA Operation at 897.5 MHz and 50 Ω system)

Figure 4: WCDMA Gain (dB) over Temperature
(V_{BATT} = V_{CC} = +3.4 V)

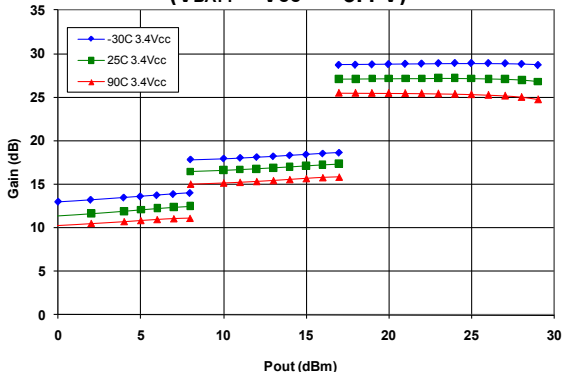


Figure 5: WCDMA Gain (dB) over Voltage
(T_c = 25 °C)

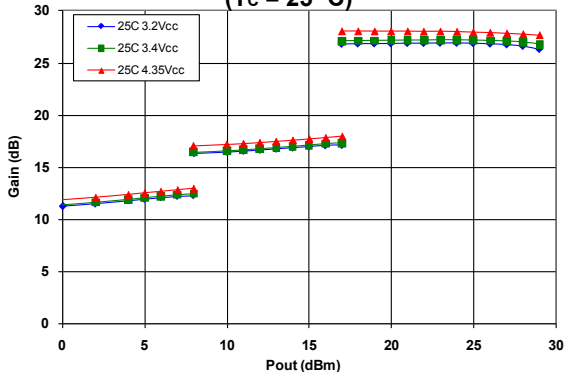


Figure 6: WCDMA PAE (%) over Temperature
(V_{BATT} = V_{CC} = +3.4 V)

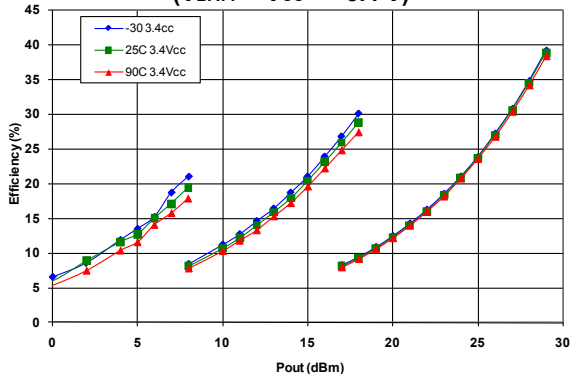


Figure 7: WCDMA PAE (%) over Voltage
(T_c = 25 °C)

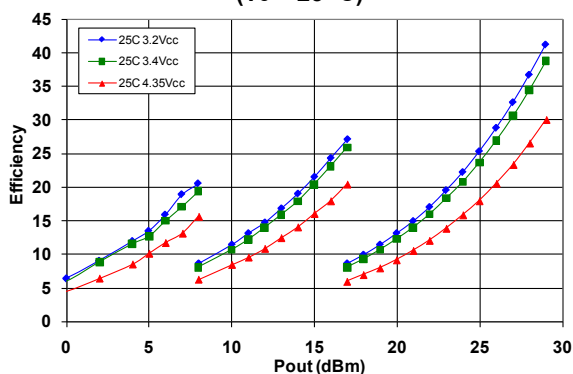


Figure 8: WCDMA ACLR1 (dBc) over Temperature
(V_{BATT} = V_{CC} = +3.4 V)

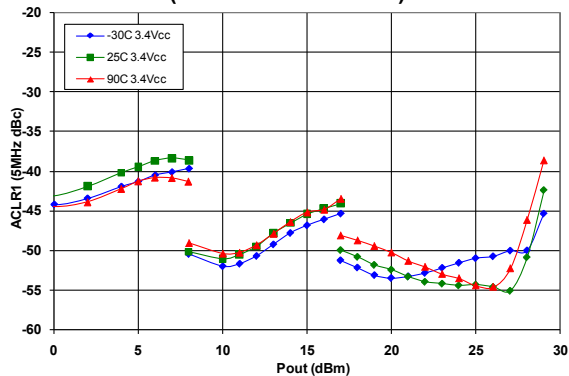
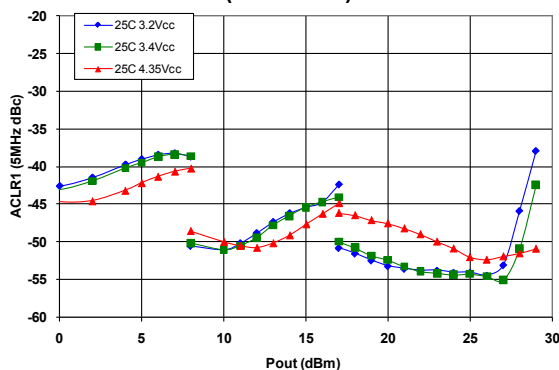


Figure 9: WCDMA ACLR1 (dBc) over Voltage
(T_c = 25 °C)



APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: <http://www.anadigics.com>

Shutdown Mode

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the V_{EN} , V_{MODE1} and V_{MODE2} voltages.

Bias Modes

The power amplifier may be placed in either Low, Medium or High Bias modes by applying the appropriate logic level (see Operating Ranges table)

to the V_{MODE} voltages. The Bias Control table below lists the recommended modes of operation for various applications.

Three operating modes are recommended to optimize current consumption. High Bias/High Power operating mode is for P_{OUT} levels ≥ 16 dBm. At ~ 17 dBm - 6.5 dBm, the PA should be "Mode Switched" to Medium Power Mode. For P_{OUT} levels $\leq \sim 7.5$ dBm, the PA can be switched to Low Power Mode for even lower quiescent current consumption.

Table 6: Bias Control

APPLICATION	P_{OUT} LEVELS	BIAS MODE	V_{EN}	V_{MODE1}	V_{MODE2}	V_{CC}	V_{BATT}
Low power (Low Bias Mode)	$\leq +7.5$ dBm	Low	+1.8 V	+1.8 V	+1.8 V	3.1 - 4.35 V	> 3.1 V
Med power (Medium Bias Mode)	$> +6.5$ dBm $\leq +17$ dBm	Low	+1.8 V	+1.8 V	0 V	3.1 - 4.35 V	> 3.1 V
High power (High Bias Mode)	$> +16$ dBm	High	+1.8 V	0 V	0 V	3.1 - 4.35 V	> 3.1 V
Shutdown	-	Shutdown	0 V	0 V	0 V	3.1 - 4.35 V	> 3.1 V

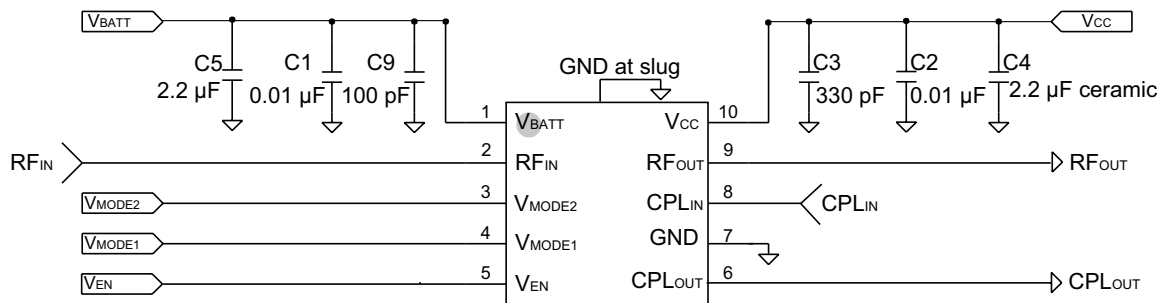
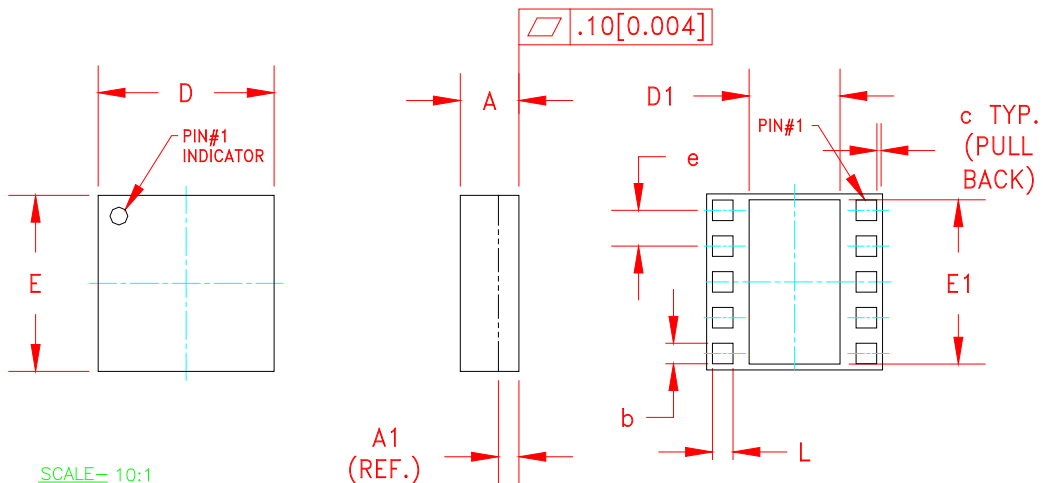


Figure 10: Evaluation Board Schematic

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.91	1.03	1.13	0.035	0.041	0.044	—
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						—
b	0.32	0.35	0.40	0.013	0.014	0.016	3
c	—	0.10	—	—	0.004	—	—
D	2.88	3.00	3.12	0.113	0.118	0.123	—
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	2.88	3.00	3.12	0.113	0.118	0.123	—
E1	2.70	2.75	2.85	0.106	0.108	0.112	3
e	0.60			0.024			3
L	0.32	0.35	0.40	0.013	0.014	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
5. LAMINATE CONTROL DRAWING SPECIFIED BY PART NUMBER.

Figure 11: M45 Package Outline - 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module

TOP BRAND

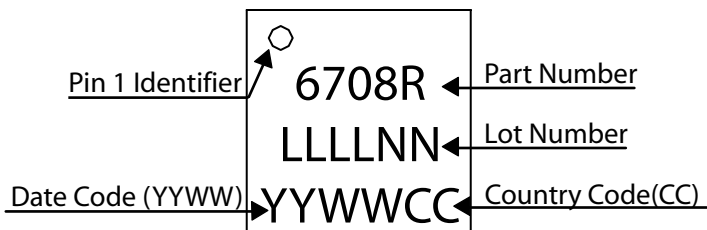
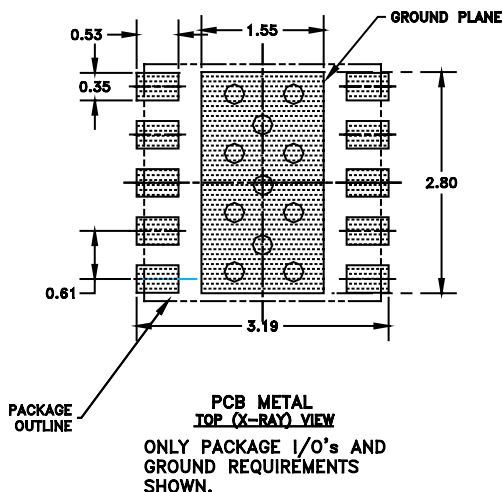


Figure 12: Branding Specification - M45 Package

PCB AND STENCIL DESIGN GUIDELINE



NOTES:

- (1) OUTLINE DRAWING REFERENCE: P8002478_E
- (2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
- (3) DIMENSIONS IN MILLIMETERS.
- (4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.
- (5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)

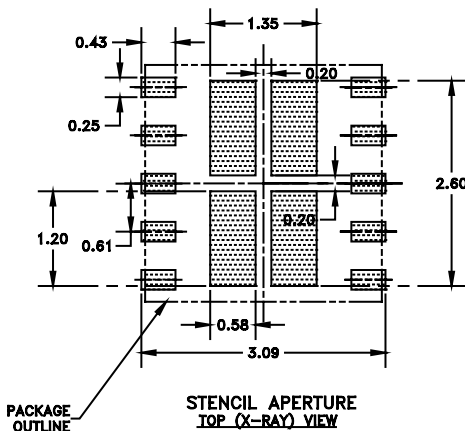
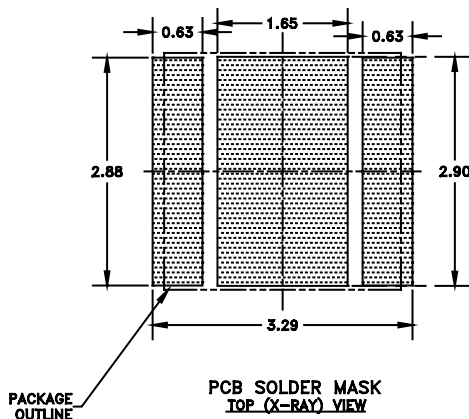


Figure 13: Recommended PCB Layout Information

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ALT6708RM45Q7	-40 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
ALT6708RM45P9	-40 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Partial Tape and Reel

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