



Device Overview

The 89HPES48H12G3 is a 48-lane, 12-port system interconnect switch optimized for PCI Express Gen3 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Features

◆ High Performance Non-Blocking Switch Architecture

- 48-lane 12-port PCIe switch
 - Six x8 ports switch ports each of which can bifurcate to two x4 ports (total of twelve x4 ports)
- Integrated SerDes supports 8.0 GT/s Gen3, 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
- Delivers up to 96 GBps (768 Gbps) of switching capacity
- Supports 128 Bytes to 2 KB maximum payload size
- Low latency cut-through architecture
- Supports one virtual channel and eight traffic classes

◆ Standards and Compatibility

- PCI Express Base Specification 3.0 compliant
- Implements the following optional PCI Express features
 - Advanced Error Reporting (AER) on all ports
 - End-to-End CRC (ECRC)
 - Access Control Services (ACS)
 - Power Budgeting Enhanced Capability
 - Device Serial Number Enhanced Capability
 - Sub-System ID and Sub-System Vendor ID Capability
 - Internal Error Reporting ECN
 - Atomic operations ECN
 - TLP processing hints ECN
 - Latency Tolerance Reporting (LTR) ECN
 - Optimized Buffer Flush/Fill (OBFF) ECN
 - ARI ECN
 - VGA and ISA enable
 - L0s and L1 ASPM

◆ Port Configurability

- x4 and x8 ports
 - Ability to merge adjacent x4 ports to create a x8 port
- Automatic per port link width negotiation (x8 → x4 → x2 → x1)
- Crosslink support
- Automatic lane reversal

- Autonomous and software managed link width and speed control
- Per lane SerDes configuration
 - Full back channel equalization support
 - Rx, 5 tap DFE
 - Rx, single tap has pulse shaping
 - Rx CTLE compensates for up to 25db @ 4G/s
 - Tx De-emphasis
 - Tx pre-shoot
 - Programmable Drive strength
 - Tx Margin

◆ Switch Partitioning

- IDT proprietary feature that creates logically independent switches in the device
- Supports up to 12 fully independent switch partitions
- Configurable downstream port device numbering
- Supports dynamic reconfiguration of switch partitions
 - Dynamic port reconfiguration — downstream, upstream
 - Dynamic migration of ports between partitions
 - Movable upstream port within and between switch partitions

◆ Initialization / Configuration

- Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
- Common switch configurations are supported with pin strapping (no external components)
- Supports in-system Serial EEPROM initialization/programming

◆ Quality of Service (QoS)

- Port arbitration
 - Round robin
- Request metering
 - IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput
- High performance switch core architecture
 - Combined Input Output Queued (CIOQ) switch architecture with large buffers

◆ Clocking

- Supports 100 MHz reference clock frequency
- Flexible port clocking modes
 - Common clock
 - Non-common clock
 - Local port clock with SSC and port reference clock input

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◆ Hot-Plug and Hot Swap

- Hot-plug controller on all ports
 - *Hot-plug supported on all downstream switch ports*
- All ports support hot-plug using low-cost external SMBus I/O expanders
- Configurable presence detect supports card and cable applications
- GPE output pin for hot-plug event notification
 - *Enables SCI/SMI generation for legacy operating system support*
- Hot swap capable I/O

◆ Power Management

- Supports D0, D3hot and D3 power management states
- Active State Power Management (ASPM)
 - *Supports L0, L0s, L1, L2/L3 Ready and L3 link states*
 - *Configurable L0s and L1 entry timers allow performance/power-savings tuning*
- Supports PCI Express Power Budgeting Capability
- SerDes power savings
 - *Supports low swing / half-swing SerDes operation*
 - *SerDes optionally turned-off in D3hot*
 - *SerDes associated with unused ports are turned-off*
 - *SerDes associated with unused lanes are placed in a low power state*

◆ 9 General Purpose I/O

◆ Reliability, Availability and Serviceability (RAS)

- ECRC support
- AER on all ports
- SECDED ECC protection on all internal RAMs
- End-to-end data path parity protection
- Checksum Serial EEPROM content protected
- Autonomous link reliability (preserves system operation in the presence of faulty links)
- Ability to generate an interrupt (INTx or MSI) on link up/down transitions

◆ Test and Debug

- On-die scope
- On-chip link activity and status outputs available for several ports including the upstream ports
- Per port link activity and status outputs available using external SMBus I/O expander for all remaining ports
- SerDes test modes
- Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

◆ Power Supplies

- Requires three power supply voltages (1.0V, 1.8V, and 3.3V)
- No power sequencing requirements

◆ Packaged in a 27mm x 27mm 676-ball Flip Chip BGA with 1mm ball spacing

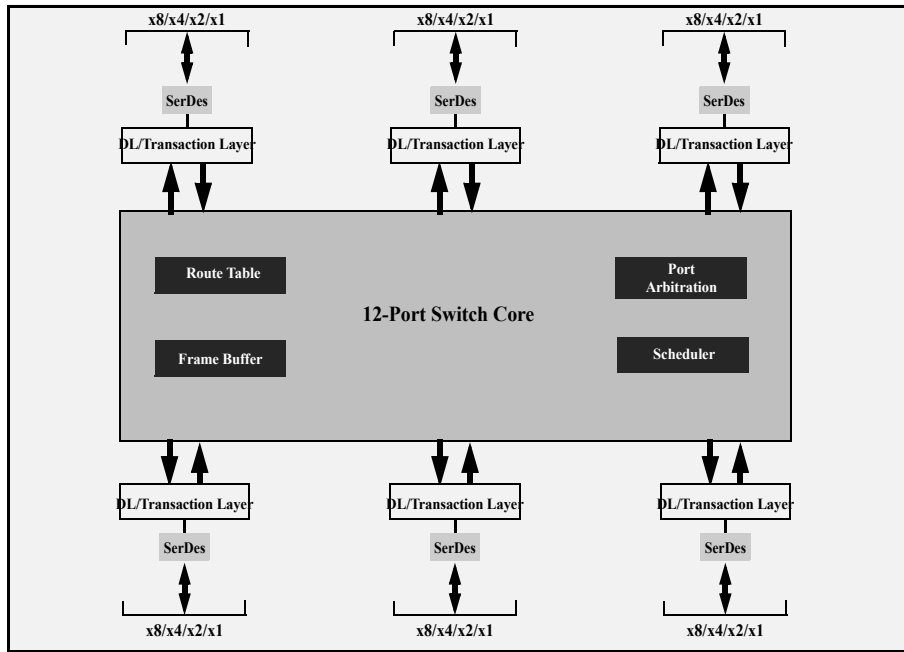
Product Description

Utilizing standard PCI Express Gen3 interconnect, the PES48H12G3 provides the most efficient system interconnect switching solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 96 GBps (768 Gbps) of aggregated, full-duplex switching capacity through 48 integrated serial lanes, using proven and robust IDT technology. Each lane is capable of 8 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base specification 3.0.

The PES48H12G3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 3.0. The PES48H12G3 can operate either as a store and forward or cut-through switch. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

The PES48H12G3 is a *partitionable* PCIe switch. This means that in addition to operating as a standard PCI express switch, the PES48H12G3 ports may be partitioned into groups that logically operate as completely independent PCIe switches. Figure 2 illustrates a three partition PES48H12G3 configuration.

Block Diagram



48 PCI Express Lanes
Up to 6 x8 ports or 12 x4 Ports

Figure 2 Internal Block Diagram

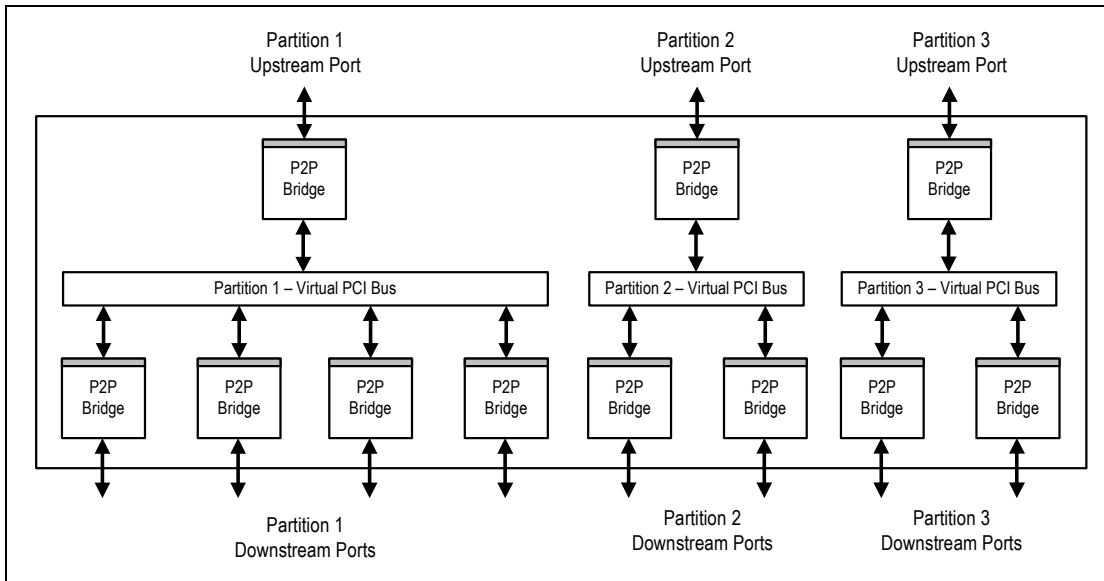


Figure 2 Example of Usage of Switch Partitioning

SMBus Interface

The PES48H12G3 contains an SMBus master interface. This master interface allows the default configuration register values of the PES48H12G3 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Two pins make up the SMBus master interface: an SMBus clock pin and an SMBus data pin. Four pins make up the SMBus slave interface: an SMBus clock pin and an SMBus data pin plus two address pins, SSMBADDR[2,1]. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	0
2	SSMBADDR[2]	0
3	1	0
4	0	0
5	1	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 2, the master and slave SMBuses may only be used in a split configuration.

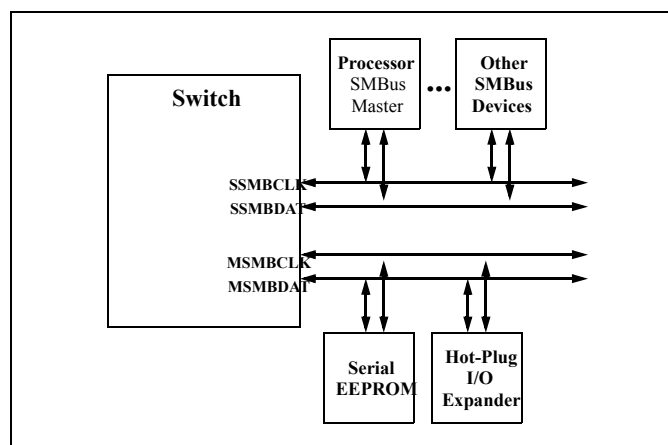


Figure 2 Split SMBus Interface Configuration

The switch's SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required.

Hot-Plug Interface

The PES48H12G3 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES48H12G3 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES48H12G3 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES48H12G3. In response to an I/O expander interrupt, the PES48H12G3 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES48H12G3 provides 9 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES48H12G3. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE00RP[3:0] PE00RN[3:0]	I	PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pairs for port 0.
PE00TP[3:0] PE00TN[3:0]	O	PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pairs for port 0.
PE01RP[3:0] PE01RN[3:0]	I	PCI Express Port 1 Serial Data Receive. Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE01TP[3:0] PE01TN[3:0]	O	PCI Express Port 1 Serial Data Transmit. Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE02RP[3:0] PE02RN[3:0]	I	PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pairs for port 2.
PE02TP[3:0] PE02TN[3:0]	O	PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pairs for port 2.
PE03RP[3:0] PE03RN[3:0]	I	PCI Express Port 3 Serial Data Receive. Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE03TP[3:0] PE03TN[3:0]	O	PCI Express Port 3 Serial Data Transmit. Differential PCI Express transmit pairs for port 3. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE04RP[3:0] PE04RN[3:0]	I	PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pairs for port 4.
PE04TP[3:0] PE04TN[3:0]	O	PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pairs for port 4.
PE05RP[3:0] PE05RN[3:0]	I	PCI Express Port 5 Serial Data Receive. Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE05TP[3:0] PE05TN[3:0]	O	PCI Express Port 5 Serial Data Transmit. Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE06RP[3:0] PE06RN[3:0]	I	PCI Express Port 6 Serial Data Receive. Differential PCI Express receive pairs for port 6.
PE06TP[3:0] PE06TN[3:0]	O	PCI Express Port 6 Serial Data Transmit. Differential PCI Express transmit pairs for port 6.
PE07RP[3:0] PE07RN[3:0]	I	PCI Express Port 7 Serial Data Receive. Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.
PE07TP[3:0] PE07TN[3:0]	O	PCI Express Port 7 Serial Data Transmit. Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.
PE08RP[3:0] PE08RN[3:0]	I	PCI Express Port 8 Serial Data Receive. Differential PCI Express receive pairs for port 8.
PE08TP[3:0] PE08TN[3:0]	O	PCI Express Port 8 Serial Data Transmit. Differential PCI Express transmit pairs for port 8.
PE09RP[3:0] PE09RN[3:0]	I	PCI Express Port 9 Serial Data Receive. Differential PCI Express receive pairs for port 9. When port 8 is merged with port 9, these signals become port 8 receive pairs for lanes 4 through 7.
PE09TP[3:0] PE09TN[3:0]	O	PCI Express Port 9 Serial Data Transmit. Differential PCI Express transmit pairs for port 9. When port 8 is merged with port 9, these signals become port 8 transmit pairs for lanes 4 through 7.
PE12RP[3:0] PE12RN[3:0]	I	PCI Express Port 12 Serial Data Receive. Differential PCI Express receive pairs for port 12.
PE12TP[3:0] PE12TN[3:0]	O	PCI Express Port 12 Serial Data Transmit. Differential PCI Express transmit pairs for port 12.
PE13RP[3:0] PE13RN[3:0]	I	PCI Express Port 13 Serial Data Receive. Differential PCI Express receive pairs for port 13. When port 12 is merged with port 13, these signals become port 12 receive pairs for lanes 4 through 7.
PE13TP[3:0] PE13TN[3:0]	O	PCI Express Port 13 Serial Data Transmit. Differential PCI Express transmit pairs for port 13. When port 12 is merged with port 13, these signals become port 12 transmit pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GCLKN[1:0] GCLKP[1:0]	I	Global Reference Clock. Differential reference clock input pairs. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is 100MHz. Note: Both pairs of the Global Reference Clocks must be connected to and derived from the same clock source. Refer to the Overview section of Chapter 3 in the PES48H12G3 User Manual for additional details.
P[2,0]CLKN P[2,0]CLKP	I	Port Reference Clock. Differential reference clock pair associated with ports 0 and 2. ¹

Table 3 Reference Clock Pins

¹ Unused port clock pins should be connected to Vss on the board.

Signal	Type	Name/Description
MSMBCLK	I/O	Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	Master SMBus Data. This bidirectional signal is used for data on the master SMBus.
SSMBADDR[2,1]	I	Slave SMBus Address. These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	Slave SMBus Clock. This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	Slave SMBus Data. This bidirectional signal is used for data on the slave SMBus.

Table 4 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART0PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART1PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART2PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART3PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[4]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function — Reserved 2nd Alternate function pin name: POLINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output.

Table 5 General Purpose I/O Pins (Part 1 of 2)

Signal	Type	Name/Description
GPIO[5]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output.
GPIO[6]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[8]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: IO expander interrupt.

Table 5 General Purpose I/O Pins (Part 2 of 2)

Signal	Type	Name/Description
CLKMODE[2:0]		Clock Mode. These signals determine the port clocking mode used by ports of the device.
P01MERGEN	I	Port 0 and 1 Merge. P01MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P23MERGEN	I	Port 2 and 3 Merge. P23MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	Port 4 and 5 Merge. P45MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
P67MERGEN	I	Port 6 and 7 Merge. P67MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port.

Table 6 System Pins (Part 1 of 2)

Signal	Type	Name/Description
P89MERGEN	I	Port 8 and 9 Merge. P89MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 8 is merged with port 9 to form a single x8 port. The Serdes lanes associated with port 9 become lanes 4 through 7 of port 8. When this pin is high, port 8 and port 9 are not merged, and each operates as a single x4 port.
P1213MERGEN	I	Port 12 and 13 Merge. P1213MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 12 is merged with port 13 to form a single x8 port. The Serdes lanes associated with port 13 become lanes 4 through 7 of port 12. When this pin is high, port 12 and port 13 are not merged, and each operates as a single x4 port.
PERSTN	I	Global Reset. Assertion of this signal resets all logic inside PES48H12G3.
RSTHALT	I	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, PES48H12G3 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	Switch Mode. These configuration pins determine the PES48H12G3 switch operating mode. Note: These pins should be static and not change following the negation of PERSTN. 0x0 - Single partition with port 0 selected as the upstream port 0x1 - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port 0x2 through 0x7 - Reserved 0x8 - Single partition with port 0 selected as the upstream port (i.e., port 2 disabled) 0x9 - Single partition with port 2 selected as the upstream port (i.e., port 0 disabled) 0xA - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port (i.e., port 2 disabled) 0xB - Single partition with Serial EEPROM initialization and port 2 selected as the upstream port (i.e., port 0 disabled) 0xC - Multi-partition 0xD - Multi-partition with Serial EEPROM initialization 0xE - Reserved 0xF - Reserved

Table 6 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	JTAG Clock. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	JTAG Data Input. This is the serial data input to the boundary scan logic or JTAG Controller.

Table 7 Test Pins (Part 1 of 2)

Signal	Type	Name/Description
JTAG_TDO	O	JTAG Data Output. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	JTAG Mode. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	JTAG Reset. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 7 Test Pins (Part 2 of 2)

Signal	Type	Name/Description
V _{DD} CORE	I	Core V_{DD}. Power supply for core logic (1.0V).
V _{DD} I/O	I	I/O V_{DD}. LVTTTL I/O buffer power supply (3.3V).
V _{DD} PEA	I	PCI Express Analog Power. Serdes analog power supply (1.0V).
V _{DD} PEHA	I	PCI Express Analog High Power. Serdes analog power supply (1.8V).
V _{SS}	I	Ground.

Table 8 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any of these pins left floating can cause a slight increase in power consumption. Finally, unused Serdes (Rx and Tx) pins should be left floating.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
PCI Express Interface	PE00RN[3:0]	I	PCIe Differential ²	Serial Link		
	PE00RP[3:0]	I				
	PE00TN[3:0]	O				
	PE00TP[3:0]	O				
	PE01RN[3:0]	I				
	PE01RP[3:0]	I				
	PE01TN[3:0]	O				
	PE01TP[3:0]	O				
	PE02RN[3:0]	I				
	PE02RP[3:0]	I				
	PE02TN[3:0]	O				
	PE02TP[3:0]	O				
	PE03RN[3:0]	I				
	PE03RP[3:0]	I				
	PE03TN[3:0]	O				
	PE03TP[3:0]	O				
	PE04RN[3:0]	I				
	PE04RP[3:0]	I				
	PE04TN[3:0]	O				
	PE04TP[3:0]	O				
	PE05RN[3:0]	I				
	PE05RP[3:0]	I				
	PE05TN[3:0]	O				
	PE05TP[3:0]	O				
	PE06RN[3:0]	I				
	PE06RP[3:0]	I				
	PE06TN[3:0]	O				
	PE06TP[3:0]	O				
	PE07RN[3:0]	I				
	PE07RP[3:0]	I				
	PE07TN[3:0]	O				
	PE07TP[3:0]	O				
PE08RN[3:0]	I					
PE08RP[3:0]	I					

Table 9 Pin Characteristics (Part 1 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes	
PCI Express Interface (Cont.)	PE08TN[3:0]	O	PCIe Differential	Serial Link			
	PE08TP[3:0]	O					
	PE09RN[3:0]	I					
	PE09RP[3:0]	I					
	PE09TN[3:0]	O					
	PE09TP[3:0]	O					
	PE12RN[3:0]	I					
	PE12RP[3:0]	I					
	PE12TN[3:0]	O					
	PE12TP[3:0]	O					
	PE13RN[3:0]	I					
	PE13RP[3:0]	I					
	PE13TN[3:0]	O					
	PE13TP[3:0]	O					
	GCLKN[1:0]	I	HCSL	Diff. Clock Input		Refer to Table 16	
	GCLKP[1:0]	I					
P00CLKN, P00CLKP	I						
P02CLKN, P02CLKP	I						
SMBus	MSMBCLK	I/O	LVTTTL	STI ³		pull-up on board	
	MSMBDAT	I/O		STI		pull-up on board	
	SSMBADDR[2:1]	I		Input	pull-up		
	SSMBCLK	I/O		STI		pull-up on board	
	SSMBDAT	I/O		STI		pull-up on board	
General Purpose I/O	GPIO[8:0]	I/O	LVTTTL	STI, High Drive	pull-up		
System Pins	CLKMODE[1:0]	I	LVTTTL	Input	pull-up		
	CLKMODE[2]	I			pull-down		
	P01MERGEN	I			pull-down		
	P23MERGEN	I			pull-down		
	P45MERGEN	I			pull-down		
	P67MERGEN	I			pull-down		
	P89MERGEN	I			pull-down		
	P1213MERGEN	I			pull-down		
	PERSTN	I			STI		
	RSTHALT	I			Input	pull-down	
	SWMODE[3:0]	I	pull-down				

Table 9 Pin Characteristics (Part 2 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
EJTAG / JTAG	JTAG_TCK	I	LVTTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	

Table 9 Pin Characteristics (Part 3 of 3)

- ¹. Internal resistor values for pull-up and pull-down are in the range 27K – 34K Ω with 30K Ω being typical.
- ². All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.
- ³. Schmitt Trigger Input (STI).

Logic Diagram — PES48H12G3

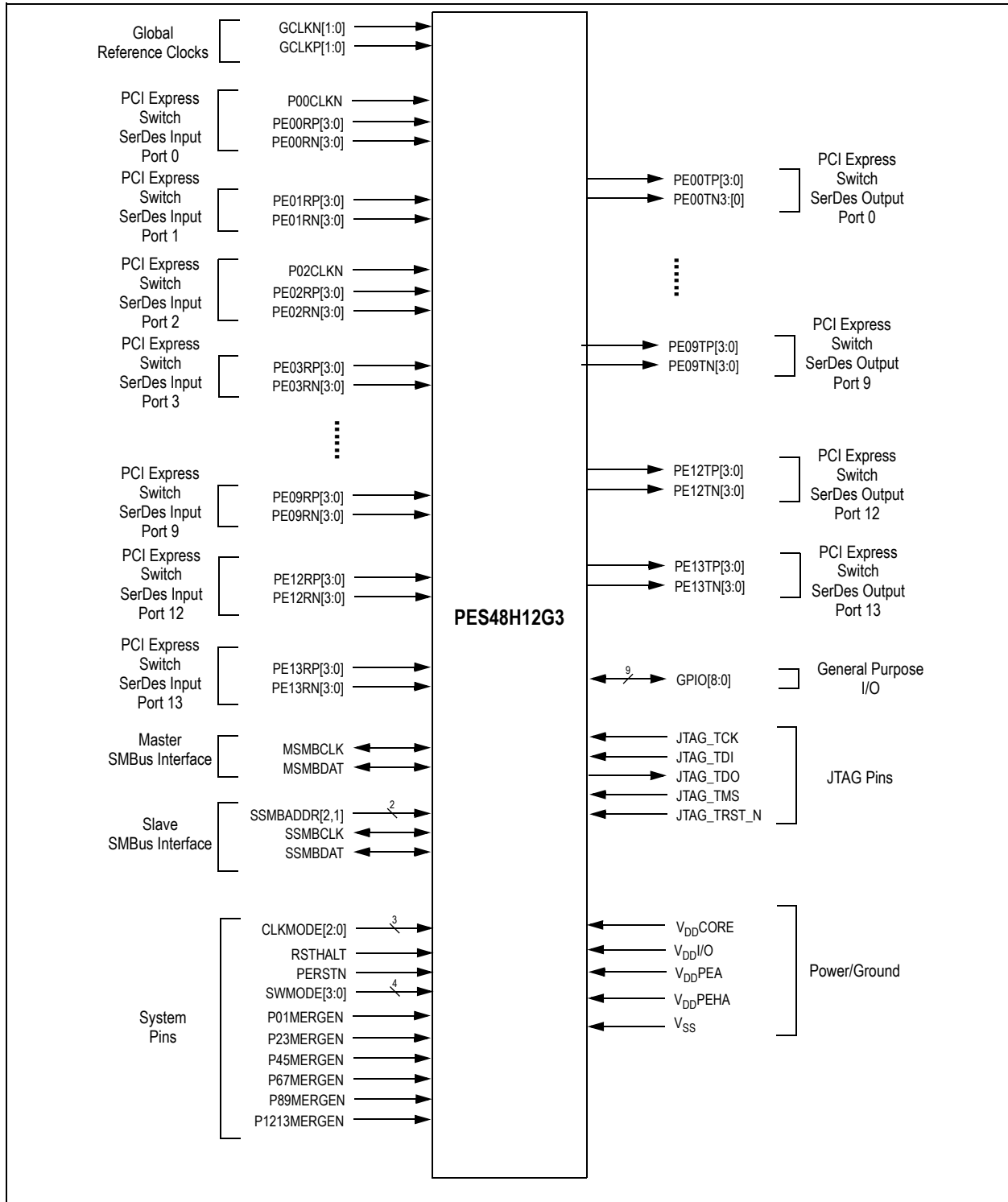


Figure 2 PES48H12G3 Logic Diagram

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 10 PES48H12G3 Operating Temperatures

Thermal Considerations

This section describes thermal considerations for the PES48H12G3 (27mm² FCBGA676 package). The data in Table 11 below contains information that is relevant to the thermal performance of the PES48H12G3 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
		85	°C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	11.7	°C/W	Zero air flow
		7.7	°C/W	1 m/S air flow
		6.3	°C/W	2 m/S air flow
		5.5	°C/W	3 m/S air flow
		5.1	°C/W	4 m/S air flow
		4.9	°C/W	5 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	2.7	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.15	°C/W	
P	Power Dissipation of the Device	17.01	Watts	Maximum

Table 11 Thermal Specifications for PES48H12G3, 27x27 mm FCBGA676 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 11. Consequently, the effective junction to ambient thermal resistance (q_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$q_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired q_{JA} becomes a known entity to the system designer. How to achieve the desired q_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of q_{JC} (value provided in Table 11), thermal resistance of the chosen adhesive (q_{CS}), that of the heat sink (q_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

Electrical Specifications

Absolute Maximum Ratings

Note: All voltage values, except differential voltages, are measured with respect to ground pins.

Parameter	Value	Unit
Supply voltage range V_{DDCORE}	-0.5 to 1.35	V
Supply voltage range V_{DDPEA}	-0.5 to 1.35	V
Supply voltage range V_{DDPEHA}	-0.5 to 2.5	V
Supply voltage range $V_{DDI/O}$	-0.5 to 4.0	V
Voltage range Differential I/O	-0.5 to $V_{DDPEHA} + 0.5$	V
3.3V Control IO	-0.5 to $V_{DDI/O} + 0.5$	V
ESD requirements: Electrostatic discharge Human body model	± 2000	V
ESD requirements: Charged-Device Model (CDM)	± 500	V
ESD requirements: Machine model	± 200	V
Storage ambient temperature	-55 to 150	°C

Table 12 Absolute Maximum Ratings

Warning: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Description	Min	Typical	Max	Unit
Power-Supply Pin Requirements					
V_{DDCORE}	1.0V DC digital core supply voltage	0.95	1.0	1.1	V
V_{DDPEA}^1	1.0V DC analog supply voltage	0.95	1.0	1.1	V
V_{DDPEHA}^2	1.8V DC analog high supply voltage	1.71	1.8	1.98	V
$V_{DDI/O}$	3.3V DC supply voltage for SMBus/JTAG/IO	3.0	3.3	3.6	V

Table 13 Recommended Operating Conditions

¹: V_{DDPEA} should have no more than $25mV_{peak-peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.

²: V_{DDPEHA} should have no more than $50mV_{peak-peak}$ AC power supply noise superimposed on the 1.8V nominal DC value.

Power-Up/Power-Down Sequence

There are no power-up or power-down sequence requirements for the various operating supply voltages for this device. Therefore, power supplies can be ramped up and ramped down in any order.

Power Consumption

Table 14 below lists power consumption values under typical and maximum operating conditions.

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.8V	Max 1.98V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
8/8/8/8/8/8 (Full Swing)	mA	4950	7425	3499	4024	1792	2061	72	94		
	Watts	4.95	8.17	3.5	4.43	3.23	4.08	0.24	0.34	11.91	17.01

Table 14 PES48H12G3 Power Consumption

Note 1: The above power consumption assumes that all ports are functioning at Gen3 (8.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in V_{DDPEA} and V_{DDPEHA} . Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 3 ports out of 16 are turned off, then the power savings for each of the above two power rails can be calculated quite simply as 3/16 multiplied by the power consumption indicated in the above table.

Note 2: Using a port in Gen2 mode (5.0GT/S) results in approximately TBD % power savings for each power rail: V_{DDPEA} and V_{DDPEHA} .

Note 3: Using a port in Gen1 mode (2.5GT/S) results in approximately TBD % power savings for each power rail: V_{DDPEA} and V_{DDPEHA} .

DC Specifications

Parameter	Description	Min	Typical	Max	Unit
3.3V I/O Requirements					
V_{IL_VDDIO}	Digital Input Signal Voltage Low Level	-0.3	—	0.8	V
V_{IH_VDDIO}	Digital Input Signal Voltage High Level	2.1	—	$V_{DDIO} + 0.3$	V
$V_{OL_VDDIO_HP}$	Digital Output Signal Voltage Low Level, High Power, $I_{OL}=4mA^{1,2}$	—	—	0.4	V
$V_{OL_VDDIO_LP}$	Digital Output Signal Voltage Low Level, Low Power, $I_{OL}=350\mu A$	—	—	0.4	V
V_{HYS_VDDIO}	Hysteresis of Schmitt Trigger Input	0.1	—	—	V

Table 15 DC Specification

¹. VOL low power and high power state is controlled via an external pull-up design in the end-application.

². Applies to JTAG input pins.

Clock Specifications

The PES48H12G3 includes differential input clock buffers which are compatible with HCSL-type drivers and are designed to work with IDT standard 100 MHz PCIe reference clock generator devices (for information on IDT's Clock/Timing products, contact www.idt.com/go/clockhelp).

The standard 100 MHz PCIe input reference clock electrical specifications are shown in Table 16.

Parameter	Description	100 MHz Input		Unit
		Min	Max	
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns
Falling Edge Rate	Falling Edge Rate	0.6	4.0	V/ns
V _{IH}	Differential Input High Voltage	+150		mV
V _{IL}	Differential Input Low Voltage		-150	mV
V _{CROSS}	Absolute crossing point voltage	+250	+550	mV
V _{CROSSDELTA}	Variation of V _{cross} over all rising clock edges		+140	mV
V _{RS}	Ring-back voltage margin	-100	+100	mV
V _{STABLE}	Time before V _{RS} is allowed	500		ps
V _{PERIODAVG}	Average Clock Period Accuracy	-300	+2800	ppm
V _{PERIODABS}	Absolute Period (including Jitter and Spread Spectrum modulation)	9.847	10.203	ns
T _{CCJITTER}	Cycle to Cycle jitter		150	ps
V _{MAX}	Absolute Max input voltage		+1.15	V
V _{MIN}	Absolute Min input voltage		-0.3	V
Duty Cycle	Duty Cycle	40	60	%
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching		20	%
Z _{C-DC}	Clock source DC impedance	40	60	W

Table 16 Input Reference Clock Buffer Electrical Specifications

AC Electrical Specifications

Note: For the tables in this section, please refer to PCI Express Base Specification 3.0 for setup and measurement conditions.

PCI Express Transmitter Specifications

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
BW _{TX-PLL}	Tx PLL BW for 2.5 GT/s	1.5	22	—	—	—	—	MHz	
BW _{TX-PKG-PLL1}	Tx PLL bandwidth corresponding to PKG _{TX-PLL1} specified below.	—	—	8	16	2	4	MHz	
BW _{TX-PKG-PLL2}	Tx PLL bandwidth corresponding to PKG _{TX-PLL2} specified below.	—	—	5	16	2	5	MHz	
PKG _{TX-PLL1}	Tx PLL peaking	—	—	—	3.0	—	2.0	dB	
PKG _{TX-PLL2}	Tx PLL peaking	—	—	—	1.0	—	1.0	dB	

Table 17 PLL Specifications

¹: Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0. Note that the values in this table apply to both Tx and Rx since both use the same PLL.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
V _{TX-DIFF-PP}	Differential p-p Tx voltage swing	0.8	1.2	0.8	1.2	See V _{TX-FS-NO-EQ} in Table 21		VPP	Defined by register settings in compliance with PCI Express Specification.
			1.8		>1.8		>1.8		Absolute maximum swing value across all possible register settings.
V _{TX-DIFF-PP-LOW}	Low power differential p-p Tx voltage swing	0.4	1.2	0.4	1.2	See V _{TX-RS-NO-EQ} in Table 21		VPP	Defined by register settings in compliance with PCI Express Specification.
			1.8		1.8		1.8		Absolute maximum swing value across all possible register settings.
V _{TX-DE-RATIO-3.5dB}	Tx de-emphasis level ratio	2.5	4.5	2.5	4.5	See Table 21		dB	Programmable over a wide range with included registers.
V _{TX-DE-RATIO-6dB}	Tx de-emphasis level	5.0	7.0	5.0	7.0	See Table 21		dB	Programmable over a wide range with included registers.
V _{TX-CM-AC-PP}	Tx AC peakpeak common mode voltage (5.0 GT/s)	—	—	—	150	—	150	mVPP	

Table 18 Transmitter Voltage and Current Specifications (Part 1 of 2)

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
V _{TX-CM-AC-P}	Tx AC peak common mode voltage (2.5 GT/s)	20	20	—	—	—	—	mV	
I _{TX-SHORT}	Transmitter short-circuit current limit	—	90	—	90	—	90	mA	
V _{TX-DC-CM}	Transmitter DC common-mode voltage	0	3.6	0	3.6	0	3.6	V	
V _{TX-CM-DC-ACTIVE-IDLE-DELTA}	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle.	0	100	0	100	0	100	mV	
V _{TX-CM-DC-LINE-DELTA}	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	25	0	25	0	25	mV	
V _{TX-IDLE-DIFF-AC-P}	Electrical Idle Differential Peak Output Voltage	0	20	0	20	0	20	mV	
V _{TX-IDLE-DIFF-DC}	DC Electrical Idle Differential Output Voltage	—	—	0	5	0	5	mV	
V _{TX-RCV-DETECT}	The amount of voltage change allowed during Receiver Detection	—	600	—	600	—	600	mV	

Table 18 Transmitter Voltage and Current Specifications (Part 2 of 2)

¹: Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
UI	Unit Interval	399.88	400.12	199.94	200.06	124.96	125.03	ps	
T _{MIN-PULSE}	Instantaneous lone pulse width	—	—	0.9	—	See Table 21		UI	
T _{TX-EYE}	Transmitter Eye including all jitter sources	0.75	—	0.75	—	See Table 21		UI	
T _{TX-EYE-MEDIAN-to-MAX-JITTER}	Maximum time between the jitter median and max deviation from the median	—	0.125	—	—	—	—	UI	
T _{TX-HF-DJ-DD}	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	See Table 21		UI	
T _{TX-LF-RMS}	Tx RMS jitter < 1.5 MHz	—	—	—	3.0	See Table 21		ps RMS	
T _{RF-MISMATCH}	Tx rise/fall mismatch	—	—	—	0.1	—	—	UI	
T _{TX-IDLE-MIN}	Minimum time spent in Electrical Idle	20	—	20	—	20	—	ns	

Table 19 Transmitter Timing and Jitter Specifications (Part 1 of 2)

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid Electrical Idle after sending an EIOS	—	8	—	8	—	8	ns	
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition to valid diff signaling after leaving Electrical Idle	—	8	—	8	—	8	ns	
L _{TX-SKEW}	Lane-to-Lane Output Skew	—	500 ps + 2 UI	—	500 ps + 4 UI	—	500 ps + 6 UI	ps	

Table 19 Transmitter Timing and Jitter Specifications (Part 2 of 2)

¹ Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
T _{RES-ISI-5GBPS}	Residual Deterministic ISI Jitter at output pins after a signal has passed through a 60-inch FR4 trace at 5Gbps	—	—	—	0.25	—	—	U _l _{pkpk}	
T _{RES-ISI-8GBPS}	Residual Deterministic ISI Jitter at output pins after a signal has passed through a 40-inch FR4 trace at 8Gbps	—	—	—	—	—	0.25	U _l _{pkpk}	
RL _{TX-DIFF}	Tx package plus Si differential return loss	10	—	10 for 0.05 - 1.25GHz	—	10 for 0.05 - 1.25GHz	—	dB	
				8 for >1.25 - 2.5GHz	—	8 for >1.25 - 2.5GHz	—		
				—	—	4 for 2.5 - 4GHz	—		
RL _{TX-CM}	Tx package plus Si common mode return loss	6	—	6 for 0.05 - 2.5GHz	—	6 for 0.05 - 2.5GHz	—	dB	
						3 for 2.5GHz - 4GHz	—		
Z _{TX-DIFF-DC}	DC differential Tx impedance	80	120	—	120	—	120	Ω	
C _{TX}	AC Coupling Capacitor	75	265	75	265	176	265	nF	

Table 20 Miscellaneous Transmitter Specifications

¹ Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen3 8.0GT/s		Unit	Notes
		Min ¹	Max ¹		
V _{TX-FS-NO-EQ}	Full swing Tx voltage with no TxEq	800	1300	mVPP	Defined by register settings in compliance with PCI Express Specification. See V _{TX-DIFF-PP} in Table 18 for absolute maximum swing value.
V _{TX-RS-NO-EQ}	Reduced swing Tx voltage with no TxEq	—	1300	mVPP	Defined by register settings in compliance with PCI Express Specification. See V _{TX-DIFF-PP-LOW} in Table 18 for absolute maximum swing value.
V _{TX-EIEOS-FS}	Min swing during EIEOS for full swing	250	—	mVPP	Programmable over a wide range with included registers.
V _{TX-EIEOS-RS}	Min swing during EIEOS for reduced swing	232	—	mVPP	Programmable over a wide range with included registers.
V _{TX-BOOST-FS}	Tx boost ratio for full swing	8.0	—	dB	Programmable over a wide range with included registers.
V _{TX-BOOST-RS}	Tx boost ratio for reduced swing	2.5	—	dB	Programmable over a wide range with included registers.
T _{TX-UTJ}	Tx uncorrelated total jitter	—	31.25	ps PP @ 10 ⁻¹²	
T _{TX-UDJDD}	Tx uncorrelated deterministic jitter	—	12	ps PP	
T _{TX-UPW-TJ}	Total uncorrelated PWJ	—	24	ps PP @ 10 ⁻¹²	
T _{TX-UPW-DJDD}	Deterministic DjDD uncorrelated PWJ	—	10	ps PP	
T _{TX-DDJ}	Data dependent jitter	—	18	ps PP	
EQ _{TX-COEFF-RES}	Tx coefficient resolution	1/63	1/24	N/A	
ps _{21TX}	Pseudo package loss	-3.0	—	dB	
Preshoot_3.5dB	Preshoot (P7, P8, P9)	2.5	4.5	dB	
Preshoot_1.9dB	Preshoot (P5)	0.9	2.9	dB	
Preshoot_2.5dB	Preshoot (P6)	1.5	3.5	dB	
Deemphasis_3.5dB	Deemphasis (P1, P8)	2.5	4.5	dB	
Deemphasis_6dB	Deemphasis (P0, P7)	4.5	7.5	dB	
Deemphasis_2.5dB	Deemphasis (P3)	1.5	3.5	dB	
Deemphasis_4.4dB	Deemphasis (P2)	2.9	5.9	dB	

Table 21 Gen3-specific Transmitter Specifications

¹. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen2 5.0 GT/s		Unit	Notes
		Min ¹	Max ¹		
UI	Unit interval without SSC	199.94	200.06	ps	
T _{RX-HF-RMS}	1.5 – 100 MHz RMS jitter	—	4.2	ps RMS	
T _{RX-HF-DJ-DD}	Max Dj impinging on Rx under tolerancing	—	88	ps	
T _{RX-LF-RMS}	10 kHz to 1.5 MHz RMS jitter	—	8.0	ps RMS	
T _{RX-MIN-PULSE}	Minimum single pulse applied at Rx	120	—	ps	
V _{RX-MIN-MAXRATIO}	Min/max pulse voltage ratio seen over an time interval of 2 UI	—	5		
V _{RX-EYE}	Receive eye voltage opening	100	—	mVPP diff	
V _{RX-CM-CH-SRC}	Common mode noise from Rx	—	300	mVPP	

Table 22 Gen 2 Tolerancing Limits for Data Clocked Rx Architecture

¹. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

PCI Express Receiver Specifications

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
V _{RX-DIFF-PP-DC}	Differential Rx peak-peak voltage for data clocked Rx architecture	0.175	1.2	0.100	1.2	0.175	2.0	V	Extended specification of this device.
		Closed eye	2.0	Closed eye	2.0	Closed eye	2.0		
V _{RX-MAX-MIN-RATIO}	Min/Max pulse voltage on consecutive UI	—	—	—	5	—	—		
V _{RX-CM-AC-P}	Rx AC common mode voltage	—	150	—	150	—	75 mV (EH <100 mVPP) 125 mV (EH ≥ 100 mVPP) See Table 4.22 in the PCIe Base Specification 3.0	mVP	

Table 23 Receiver Voltage and Current Specifications (Part 1 of 2)

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
V _{RX-IDLE-DET-DIFFp-p}	Electrical Idle Detect Threshold	65	175	65	175	65	175	mV	Programmable over a wide range with included registers

Table 23 Receiver Voltage and Current Specifications (Part 2 of 2)

¹: Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
UI	Unit Interval	399.88	400.12	199.94	200.06	124.96	125.03	ps	
T _{RX-EYE}	Receiver eye time opening	0.40	—	—	—	See Tables 4.22 and 4.23 in the PCIe Base Specification 3.0		UI	
T _{RX-TJ-DC}	Max Rx inherent timing error	—	—	—	0.34			UI	
T _{RX-DJ-DD-DC}	Max Rx inherent deterministic timing error	—	—	—	0.24			UI	
T _{RX-EYE-MEDIAN-to-MAX-JITTER}	Max time delta between median and deviation from median	—	0.3	—	—	—	—	UI	
T _{RX-MIN-PULSE}	Minimum width pulse at Rx	—	—	0.6	—	—	—	UI	
T _{RX-GND_FLOAT}	Rx termination ground float time	—	—	—	—	—	500	µs	
T _{RX-IDLE-DET-DIFF-ENTERTIME}	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	10	—	10	—	10	ms	
L _{RX-SKEW}	Lane to Lane input skew	—	20	—	8	—	6	ns	

Table 24 Receiver Timing and Jitter Specifications

¹: Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min ¹	Max ¹	Min ¹	Max ¹	Min ¹	Max ¹		
RL _{RX-DIFF}	Rx package plus Si differential return loss	10	—	10 for 0.05 - 1.25GHz	—	10 for 0.05 - 1.25GHz	—	dB	
				8 for >1.25 - 2.5GHz		8 for >1.25 - 2.5GHz			
				5 for 2.5GHz - 4GHz		—			
RL _{RX-CM}	Common mode Rx return loss	6	—	6 for 0.05 - 2.5GHz	—	6 for 0.05 - 2.5GHz	—	dB	
				5 for 2.5GHz - 4GHz		—			
Z _{RX-DC}	Receiver DC single ended impedance	40	60	40	60	—	—	Ω	
Z _{RX-DIFF-DC}	DC differential impedance	80	120	—	—	—	—	Ω	
Z _{RX-HIGH-IMP-DC-POS}	DC Input CM Input Impedance for V>0 during Reset or power down	10 k or 20 k	—	10 k or 20 k	—	10 k or 20 k	—	Ω	
Z _{RX-HIGH-IMP-DC-NEG}	DC Input CM Input Impedance for V < 0 during Reset or power down	1.0 k	—	1.0 k	—	1.0 k	—	Ω	

Table 25 Miscellaneous Receiver Specifications

¹ Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[8:0] ¹	Tpw ²	None	50	—	ns	

Table 26 GPIO AC Timing Characteristics

¹ GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

² The values for this symbol were determined by calculation, not by testing.

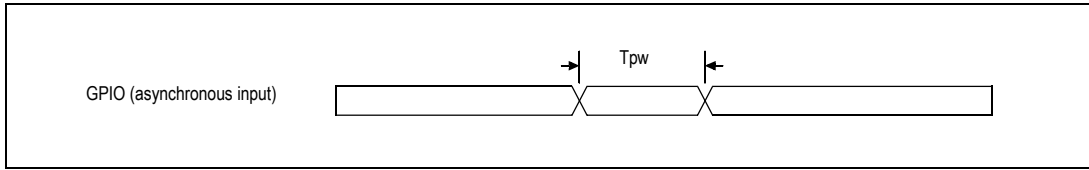


Figure 2 GPIO AC Timing Waveform

JTAG AC Timing Specifications

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 2.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS ¹ , JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c ²		—	20	ns	
JTAG_TRST_N	Tpw_16d ²	none	25.0	—	ns	

Table 27 JTAG AC Timing Characteristics

¹ The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

² The values for this symbol were determined by calculation, not by testing.

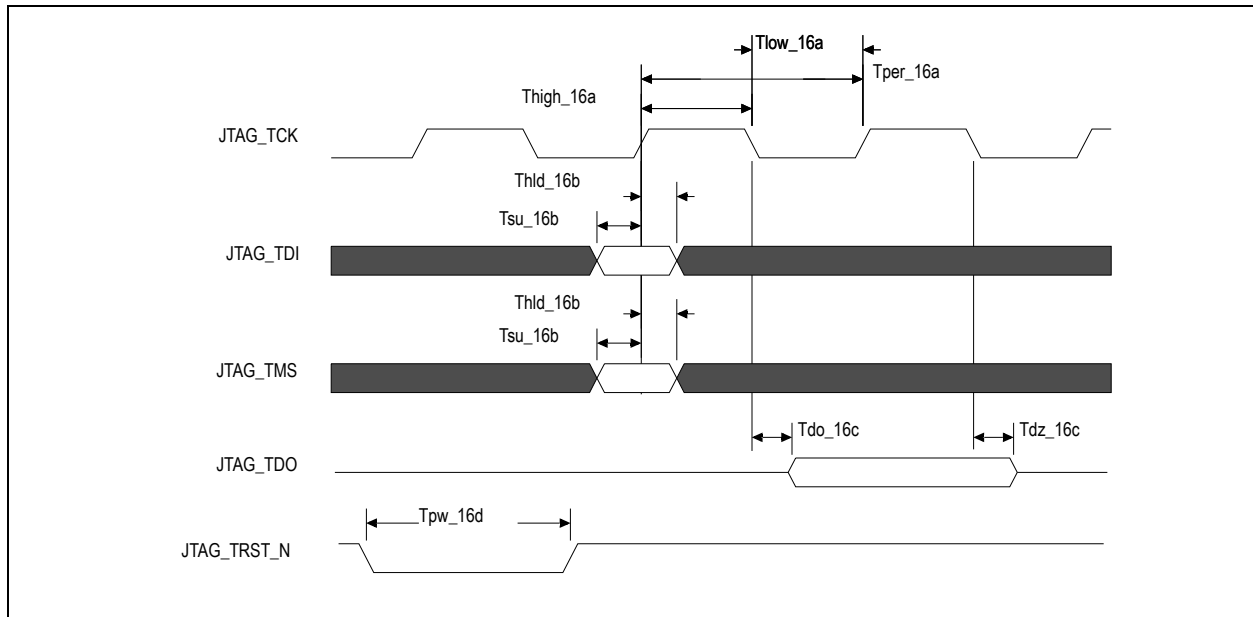


Figure 2 JTAG AC Timing Waveform

SMBus Characterization

Symbol	Parameter	Slow SMBus ¹		
		3.0V	3.3V	3.6V
DC Parameter for SDA Pin				
V _{IL}	Input Low	1.5	1.6	1.7
V _{IH}	Input High	1.6	1.7	1.9
V _{OL@4mA}	Output Low	245	230	220
V _{OL@3mA}	Output Low	185	175	165
V _{OL@6mA}	Output Low	380	350	330
V _{OL@1mA}	Output Low	65	65	65
V _{OL@3350uA}	Output Low	30	30	30
I _{OL@0.4V}		6.4	7	7.4
I _{Pullup}	Current Source	—	—	—
I _{IL_Leak}	Input Low Leakage	0	0.1	.01
I _{IH_Leak}	Input High Leakage	0	0.1	.01
DC Parameter for SCL Pin				
V _{IL (V)}	Input Low	1.5	1.6	1.7

Table 28 SMBus DC Characterization Data

Symbol	Parameter	Slow SMBus ¹		
		3.0V	3.3V	3.6V
V _{IH} (V)	Input High	1.6	1.7	1.9
I _{IL_Leak}	Input Low Leakage	0	0.1	0.1
I _{IH_Leak}	Input High Leakage	0	0.1	0.1

Table 28 SMBus DC Characterization Data

¹. Data at room and hot temperature.

Symbol	Parameter	SMBus @3.3V ±10% ¹		Unit
		Min	Max	
F _{SCL}	Clock frequency	6	625	KHz
T _{BUF}	Bus free time between Stop and Start	3.7	—	μs
T _{HD:STA}	Start condition hold time	1.2	—	μs
T _{SU:STA}	Start condition setup time	1.2	—	μs
T _{SU:STO}	Stop condition setup time	1.2	—	μs
T _{HD:DAT}	Data hold time	1.2	—	ns
T _{SU:DAT}	Data setup time	1.2	—	ns
T _{TIMEOUT}	Detect clock low time out	—	74.7	ms
T _{LOW}	Clock low period	3.7	—	μs
T _{HIGH}	Clock high period	3.7	—	μs
T _F	Clock/Data fall time	—	68.4	ns
T _R	Clock/Data rise time	—	127.6	ns
T _{POR@10kHz}	Time which a device must be operational after power-on reset	20	—	ms

Table 29 SMBus AC Timing Data

¹: Data at room and hot temperature.

PES48H12G3 Package Pinout, 27x27mm 676-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES48H12G3 (27x27mm) device. Note: NC stands for No Connection.

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
A1	V _{SS}		B1	V _{SS}		C1	V _{SS}	
A2	V _{SS}		B2	V _{SS}		C2	V _{SS}	
A3	V _{DD} IO		B3	V _{DD} IO		C3	V _{SS}	
A4	V _{SS}		B4	V _{SS}		C4	V _{SS}	
A5	PE08TP3		B5	PE08TN3		C5	V _{SS}	
A6	PE08TP2		B6	PE08TN2		C6	V _{SS}	
A7	V _{SS}		B7	V _{SS}		C7	V _{SS}	
A8	PE08TP1		B8	PE08TN1		C8	V _{SS}	
A9	PE08TP0		B9	PE08TN0		C9	V _{SS}	
A10	V _{SS}		B10	V _{SS}		C10	V _{SS}	
A11	PE03TP3		B11	PE03TN3		C11	V _{SS}	
A12	PE03TP2		B12	PE03TN2		C12	V _{SS}	
A13	V _{SS}		B13	V _{SS}		C13	V _{SS}	
A14	PE03TP1		B14	PE03TN1		C14	V _{SS}	
A15	PE03TP0		B15	PE03TN0		C15	V _{SS}	
A16	V _{SS}		B16	V _{SS}		C16	V _{SS}	
A17	PE02TP3		B17	PE02TN3		C17	V _{SS}	
A18	PE02TP2		B18	PE02TN2		C18	V _{SS}	
A19	V _{SS}		B19	V _{SS}		C19	V _{SS}	
A20	PE02TP1		B20	PE02TN1		C20	V _{SS}	
A21	PE02TP0		B21	PE02TN0		C21	V _{SS}	
A22	V _{DD} IO		B22	V _{DD} IO		C22	V _{SS}	
A23	MSMBDAT		B23	MSMBCLK		C23	JTAG_TDO	
A24	JTAG_TMS		B24	PERSTN		C24	JTAG_TDI	
A25	CLKMODE1		B25	SSMBDAT		C25	SSMBCLK	
A26	JTAG_TCK		B26	SSMBADDR2		C26	SSMBADDR1	

Table 30 PES48H12G3 676-pin Signal Pin-out (Part 1 of 9)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
D1	V _{DD} IO		E1	V _{SS}		F1	PE09TP0	
D2	V _{DD} IO		E2	V _{SS}		F2	PE09TN0	
D3	V _{SS}		E3	V _{SS}		F3	V _{SS}	
D4	V _{SS}		E4	V _{SS}		F4	PE09RN0	
D5	PE08RN3		E5	PE08RP3		F5	PE09RP0	
D6	PE08RN2		E6	PE08RP2		F6	V _{SS}	
D7	V _{SS}		E7	V _{SS}		F7	V _{SS}	
D8	PE08RN1		E8	PE08RP1		F8	V _{DD} PEHA	
D9	PE08RN0		E9	PE08RP0		F9	NC	
D10	V _{SS}		E10	V _{SS}		F10	V _{DD} PEHA	
D11	PE03RN3		E11	PE03RP3		F11	V _{DD} PEA	
D12	PE03RN2		E12	PE03RP2		F12	NC	
D13	NC		E13	V _{SS}		F13	GCLKP0	
D14	PE03RN1		E14	PE03RP1		F14	V _{DD} PEA	
D15	PE03RN0		E15	PE03RP0		F15	P02CLKP	
D16	V _{SS}		E16	V _{SS}		F16	NC	
D17	PE02RN3		E17	PE02RP3		F17	V _{DD} PEA	
D18	PE02RN2		E18	PE02RP2		F18	V _{DD} PEA	
D19	V _{SS}		E19	V _{SS}		F19	V _{DD} PEHA	
D20	PE02RN1		E20	PE02RP1		F20	V _{SS}	
D21	PE02RN0		E21	PE02RP0		F21	V _{SS}	
D22	JTAG_TRST_N		E22	PE01RP3		F22	PE01RP2	
D23	V _{SS}		E23	PE01RN3		F23	PE01RN2	
D24	V _{SS}		E24	V _{SS}		F24	V _{SS}	
D25	V _{DD} IO		E25	PE01TN3		F25	PE01TN2	
D26	V _{DD} IO		E26	PE01TP3		F26	PE01TP2	

Table 30 PES48H12G3 676-pin Signal Pin-out (Part 2 of 9)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
G1	PE09TP1		H1	V _{SS}		J1	PE09TP2	
G2	PE09TN1		H2	V _{SS}		J2	PE09TN2	
G3	V _{SS}		H3	V _{SS}		J3	V _{SS}	
G4	PE09RN1		H4	V _{SS}		J4	PE09RN2	
G5	PE09RP1		H5	V _{SS}		J5	PE09RP2	
G6	V _{SS}		H6	V _{DD} PEA		J6	V _{DD} PEA	
G7	V _{SS}		H7	V _{DD} PEA		J7	V _{DD} PEA	
G8	V _{DD} PEHA		H8	V _{DD} PEA		J8	V _{DD} PEA	
G9	NC		H9	V _{SS}		J9	V _{SS}	
G10	V _{DD} PEHA		H10	V _{SS}		J10	V _{SS}	
G11	V _{DD} PEA		H11	V _{DD} CORE		J11	V _{DD} CORE	
G12	V _{SS}		H12	V _{DD} CORE		J12	V _{DD} CORE	
G13	GCLKN0		H13	V _{SS}		J13	V _{SS}	
G14	V _{DD} PEA		H14	V _{SS}		J14	V _{SS}	
G15	P02CLKN		H15	V _{DD} CORE		J15	V _{DD} CORE	
G16	NC		H16	V _{DD} CORE		J16	V _{DD} CORE	
G17	V _{DD} PEA		H17	V _{SS}		J17	V _{SS}	
G18	V _{DD} PEA		H18	V _{SS}		J18	V _{SS}	
G19	V _{DD} PEHA		H19	V _{DD} PEA		J19	V _{DD} PEA	
G20	V _{SS}		H20	V _{DD} PEA		J20	V _{DD} PEA	
G21	V _{SS}		H21	V _{DD} PEA		J21	V _{DD} PEA	
G22	V _{SS}		H22	PE01RP1		J22	PE01RP0	
G23	V _{SS}		H23	PE01RN1		J23	PE01RN0	
G24	V _{SS}		H24	V _{SS}		J24	V _{SS}	
G25	V _{SS}		H25	PE01TN1		J25	PE01TN0	
G26	V _{SS}		H26	PE01TP1		J26	PE01TP0	

Table 30 PES48H12G3 676-pin Signal Pin-out (Part 3 of 9)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
K1	PE09TP3		L1	V _{SS}		M1	PE04TP0	
K2	PE09TN3		L2	V _{SS}		M2	PE04TN0	
K3	V _{SS}		L3	V _{SS}		M3	V _{SS}	
K4	PE09RN3		L4	V _{SS}		M4	PE04RN0	
K5	PE09RP3		L5	V _{SS}		M5	PE04RP0	
K6	V _{DD} PEA		L6	V _{DD} PEHA		M6	V _{SS}	
K7	V _{DD} PEA		L7	V _{DD} PEHA		M7	V _{SS}	
K8	V _{DD} PEA		L8	V _{DD} PEHA		M8	V _{SS}	
K9	V _{SS}		L9	V _{SS}		M9	V _{SS}	
K10	V _{SS}		L10	V _{SS}		M10	V _{SS}	
K11	V _{DD} CORE		L11	V _{DD} CORE		M11	V _{DD} CORE	
K12	V _{DD} CORE		L12	V _{DD} CORE		M12	V _{DD} CORE	
K13	V _{SS}		L13	V _{SS}		M13	V _{SS}	
K14	V _{SS}		L14	V _{SS}		M14	V _{SS}	
K15	V _{DD} CORE		L15	V _{DD} CORE		M15	V _{DD} CORE	
K16	V _{DD} CORE		L16	V _{DD} CORE		M16	V _{DD} CORE	
K17	V _{SS}		L17	V _{SS}		M17	V _{SS}	
K18	V _{SS}		L18	V _{SS}		M18	V _{SS}	
K19	V _{DD} PEA		L19	V _{DD} PEHA		M19	V _{DD} PEHA	
K20	V _{DD} PEA		L20	NC		M20	P00CLKN	
K21	V _{DD} PEA		L21	V _{DD} PEA		M21	P00CLKP	
K22	V _{SS}		L22	PE00RP3		M22	PE00RP2	
K23	V _{SS}		L23	PE00RN3		M23	PE00RN2	
K24	V _{SS}		L24	V _{SS}		M24	V _{SS}	
K25	V _{SS}		L25	PE00TN3		M25	PE00TN2	
K26	V _{SS}		L26	PE00TP3		M26	PE00TP2	

Table 30 PES48H12G3 676-pin Signal Pin-out (Part 4 of 9)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
N1	PE04TP1		P1	V _{SS}		R1	PE04TP2	
N2	PE04TN1		P2	V _{SS}		R2	PE04TN2	
N3	V _{SS}		P3	V _{SS}		R3	V _{SS}	
N4	PE04RN1		P4	V _{SS}		R4	PE04RN2	
N5	PE04RP1		P5	V _{SS}		R5	PE04RP2	
N6	V _{DD} PEA		P6	NC		R6	NC	
N7	V _{DD} PEA		P7	NC		R7	NC	
N8	V _{DD} PEA		P8	V _{DD} PEA		R8	V _{DD} PEA	
N9	V _{SS}		P9	V _{SS}		R9	V _{SS}	
N10	V _{SS}		P10	V _{SS}		R10	V _{SS}	
N11	V _{DD} CORE		P11	V _{DD} CORE		R11	V _{DD} CORE	
N12	V _{DD} CORE		P12	V _{DD} CORE		R12	V _{DD} CORE	
N13	V _{SS}		P13	V _{SS}		R13	V _{SS}	
N14	V _{SS}		P14	V _{SS}		R14	V _{SS}	
N15	V _{DD} CORE		P15	V _{DD} CORE		R15	V _{DD} CORE	
N16	V _{DD} CORE		P16	V _{DD} CORE		R16	V _{DD} CORE	
N17	V _{SS}		P17	V _{SS}		R17	V _{SS}	
N18	V _{SS}		P18	V _{SS}		R18	V _{SS}	
N19	V _{DD} PEHA		P19	V _{DD} PEA		R19	V _{DD} PEA	
N20	NC		P20	V _{DD} PEA		R20	V _{DD} PEA	
N21	NC		P21	V _{DD} PEA		R21	V _{DD} PEA	
N22	NC		P22	PE00RP1		R22	PE00RP0	
N23	NC		P23	PE00RN1		R23	PE00RN0	
N24	V _{SS}		P24	V _{SS}		R24	V _{SS}	
N25	V _{SS}		P25	PE00TN1		R25	PE00TN0	
N26	V _{SS}		P26	PE00TP1		R26	PE00TP0	

Table 30 PES48H12G3 676-pin Signal Pin-out (Part 5 of 9)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
T1	PE04TP3		U1	V _{SS}		V1	PE05TP0	
T2	PE04TN3		U2	V _{SS}		V2	PE05TN0	
T3	V _{SS}		U3	V _{SS}		V3	V _{SS}	
T4	PE04RN3		U4	V _{SS}		V4	PE05RN0	
T5	PE04RP3		U5	V _{SS}		V5	PE05RP0	
T6	V _{DD} PEA		U6	V _{DD} PEHA		V6	V _{DD} PEA	
T7	V _{DD} PEA		U7	V _{DD} PEHA		V7	V _{DD} PEA	
T8	V _{DD} PEA		U8	V _{DD} PEHA		V8	V _{DD} PEA	
T9	V _{SS}		U9	V _{SS}		V9	V _{SS}	
T10	V _{SS}		U10	V _{SS}		V10	V _{SS}	
T11	V _{DD} CORE		U11	V _{DD} CORE		V11	V _{DD} CORE	
T12	V _{DD} CORE		U12	V _{DD} CORE		V12	V _{DD} CORE	
T13	V _{SS}		U13	V _{SS}		V13	V _{SS}	
T14	V _{SS}		U14	V _{SS}		V14	V _{SS}	
T15	V _{DD} CORE		U15	V _{DD} CORE		V15	V _{DD} CORE	
T16	V _{DD} CORE		U16	V _{DD} CORE		V16	V _{DD} CORE	
T17	V _{SS}		U17	V _{SS}		V17	V _{SS}	
T18	V _{SS}		U18	V _{SS}		V18	V _{SS}	
T19	V _{DD} PEHA		U19	V _{SS}		V19	V _{DD} PEA	
T20	V _{DD} PEHA		U20	V _{SS}		V20	V _{DD} PEA	
T21	V _{DD} PEHA		U21	V _{SS}		V21	V _{DD} PEA	
T22	V _{SS}		U22	PE13RP3		V22	PE13RP2	
T23	V _{SS}		U23	PE13RN3		V23	PE13RN2	
T24	V _{SS}		U24	V _{SS}		V24	V _{SS}	
T25	V _{SS}		U25	PE13TN3		V25	PE13TN2	
T26	V _{SS}		U26	PE13TP3		V26	PE13TP2	

Table 30 PES48H12G3 676-pin Signal Pin-out (Part 6 of 9)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
W1	PE05TP1		Y1	V _{SS}		AA1	PE05TP2	
W2	PE05TN1		Y2	V _{SS}		AA2	PE05TN2	
W3	V _{SS}		Y3	V _{SS}		AA3	V _{DD} IO	
W4	PE05RN1		Y4	V _{SS}		AA4	PE05RN2	
W5	PE05RP1		Y5	V _{SS}		AA5	PE05RP2	
W6	V _{DD} PEA		Y6	V _{SS}		AA6	V _{SS}	
W7	V _{DD} PEA		Y7	V _{SS}		AA7	V _{SS}	
W8	V _{DD} PEA		Y8	V _{DD} PEA		AA8	V _{DD} PEA	
W9	V _{SS}		Y9	V _{DD} PEHA		AA9	V _{DD} PEHA	
W10	V _{SS}		Y10	V _{DD} PEA		AA10	V _{DD} PEA	
W11	V _{DD} CORE		Y11	NC		AA11	V _{DD} PEA	
W12	V _{DD} CORE		Y12	NC		AA12	V _{DD} PEA	
W13	V _{SS}		Y13	V _{DD} PEHA		AA13	V _{DD} PEHA	
W14	V _{SS}		Y14	GCLKN1		AA14	GCLKP1	
W15	V _{DD} CORE		Y15	NC		AA15	V _{SS}	
W16	V _{DD} CORE		Y16	NC		AA16	V _{SS}	
W17	V _{SS}		Y17	V _{DD} PEA		AA17	V _{DD} PEA	
W18	V _{SS}		Y18	V _{DD} PEHA		AA18	V _{DD} PEHA	
W19	V _{DD} PEA		Y19	V _{DD} PEA		AA19	V _{DD} PEA	
W20	V _{DD} PEA		Y20	V _{SS}		AA20	V _{SS}	
W21	V _{DD} PEA		Y21	V _{SS}		AA21	V _{SS}	
W22	V _{SS}		Y22	PE13RP1		AA22	PE13RP0	
W23	V _{SS}		Y23	PE13RN1		AA23	PE13RN0	
W24	V _{SS}		Y24	V _{SS}		AA24	V _{SS}	
W25	V _{SS}		Y25	PE13TN1		AA25	PE13TN0	
W26	V _{SS}		Y26	PE13TP1		AA26	PE13TP0	

Table 30 PES48H12G3 676-pin Signal Pin-out (Part 7 of 9)

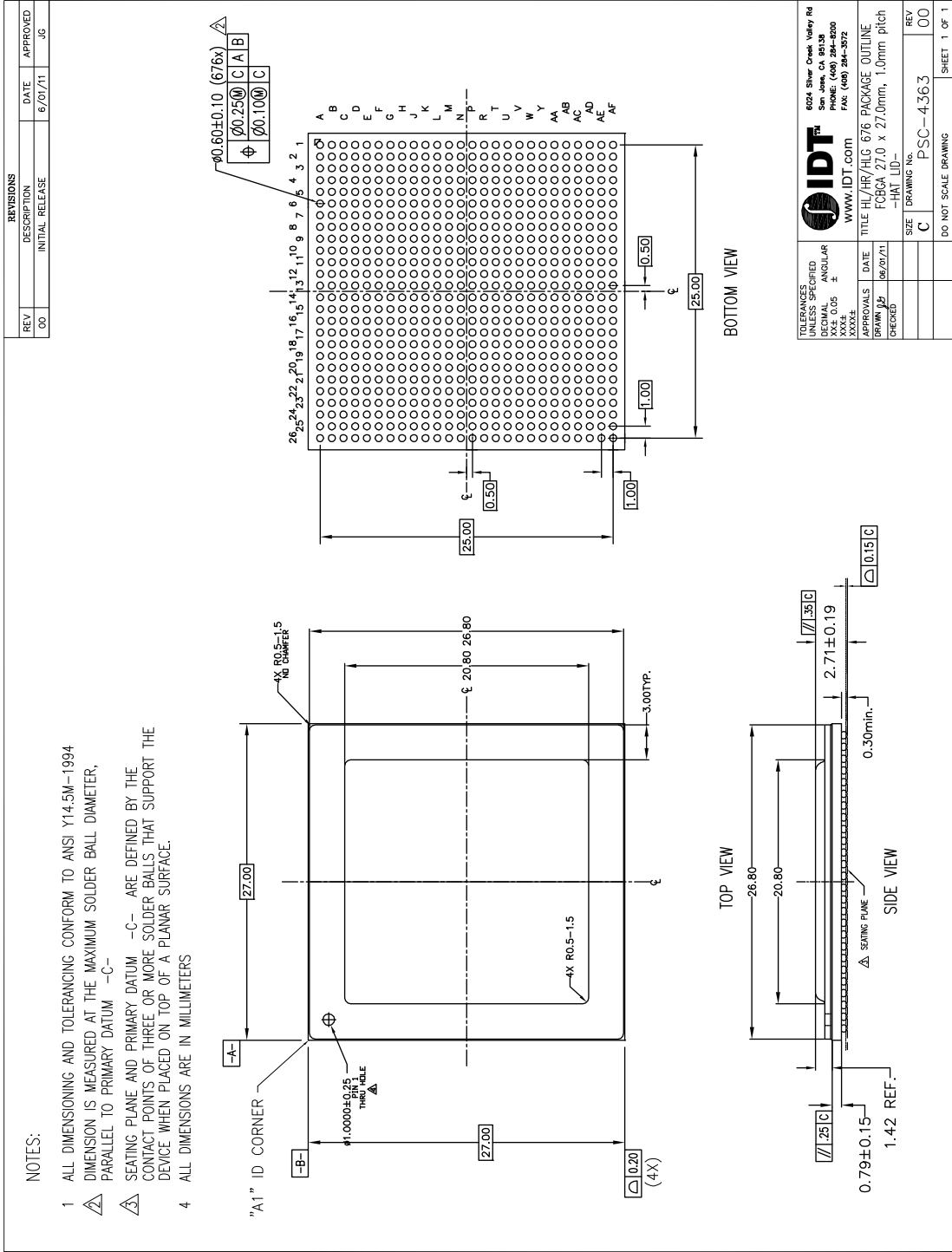
Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
AB1	PE05TP3		AC1	V _{DD} IO		AD1	V _{DD} IO	
AB2	PE05TN3		AC2	V _{DD} IO		AD2	P23MERGEN	
AB3	V _{DD} IO		AC3	V _{SS}		AD3	P1213MERGEN	
AB4	PE05RN3		AC4	V _{SS}		AD4	NC	
AB5	PE05RP3		AC5	CLKMODE2		AD5	SWMODE0	
AB6	PE06RP0		AC6	PE06RN0		AD6	V _{SS}	
AB7	PE06RP1		AC7	PE06RN1		AD7	V _{SS}	
AB8	V _{SS}		AC8	V _{SS}		AD8	V _{SS}	
AB9	PE06RP2		AC9	PE06RN2		AD9	V _{SS}	
AB10	PE06RP3		AC10	PE06RN3		AD10	V _{SS}	
AB11	V _{SS}		AC11	V _{SS}		AD11	V _{SS}	
AB12	PE07RP0		AC12	PE07RN0		AD12	V _{SS}	
AB13	PE07RP1		AC13	PE07RN1		AD13	V _{SS}	
AB14	V _{SS}		AC14	V _{SS}		AD14	V _{SS}	
AB15	PE07RP2		AC15	PE07RN2		AD15	V _{SS}	
AB16	PE07RP3		AC16	PE07RN3		AD16	V _{SS}	
AB17	V _{SS}		AC17	V _{SS}		AD17	V _{SS}	
AB18	PE12RP0		AC18	PE12RN0		AD18	V _{SS}	
AB19	PE12RP1		AC19	PE12RN1		AD19	V _{SS}	
AB20	V _{SS}		AC20	V _{SS}		AD20	V _{SS}	
AB21	PE12RP2		AC21	PE12RN2		AD21	V _{SS}	
AB22	PE12RP3		AC22	PE12RN3		AD22	V _{SS}	
AB23	V _{SS}		AC23	V _{SS}		AD23	V _{SS}	
AB24	V _{DD} IO		AC24	V _{DD} IO		AD24	V _{DD} IO	
AB25	V _{SS}		AC25	GPIO04	1	AD25	GPIO05	2
AB26	V _{SS}		AC26	GPIO08	1	AD26	GPIO06	

Table 30 PES48H12G3 676-pin Signal Pin-out (Part 8 of 9)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
AE1	P01Mergen		AE19	PE12TN1		AF11	V _{SS}	
AE2	P67Mergen		AE20	V _{SS}		AF12	PE07TP0	
AE3	P89Mergen		AE21	PE12TN2		AF13	PE07TP1	
AE4	V _{DDIO}		AE22	PE12TN3		AF14	V _{SS}	
AE5	SWMODE1		AE23	V _{SS}		AF15	PE07TP2	
AE6	PE06TN0		AE24	V _{DDIO}		AF16	PE07TP3	
AE7	PE06TN1		AE25	GPIO02		AF17	V _{SS}	
AE8	V _{SS}		AE26	GPIO07		AF18	PE12TP0	
AE9	PE06TN2		AF1	CLKMODE0		AF19	PE12TP1	
AE10	PE06TN3		AF2	P45Mergen		AF20	V _{SS}	
AE11	V _{SS}		AF3	RSTHALT		AF21	PE12TP2	
AE12	PE07TN0		AF4	SWMODE2		AF22	PE12TP3	
AE13	PE07TN1		AF5	SWMODE3		AF23	V _{SS}	
AE14	V _{SS}		AF6	PE06TP0		AF24	GPIO01	1
AE15	PE07TN2		AF7	PE06TP1		AF25	GPIO00	1
AE16	PE07TN3		AF8	V _{SS}		AF26	GPIO03	1
AE17	V _{SS}		AF9	PE06TP2				
AE18	PE12TN0		AF10	PE06TP3				

Table 30 PES48H12G3 676-pin Signal Pin-out (Part 9 of 9)

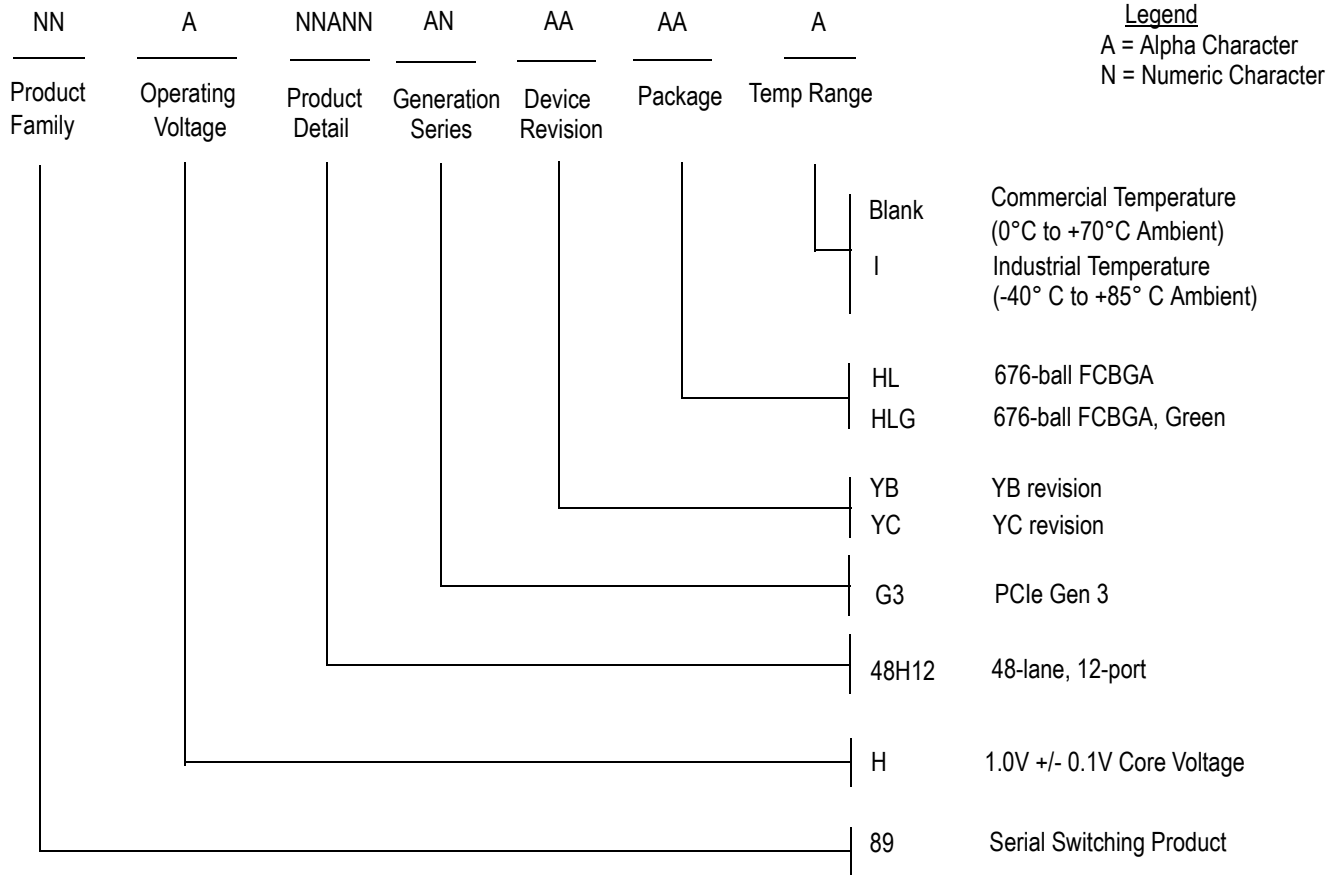
PES48H12G3 Package Drawing — 676-Pin HL676/HLG676



Revision History

March 12, 2013: Initial publication of final data sheet.

Ordering Information



Legend

A = Alpha Character
N = Numeric Character

Valid Combinations

89H48H12G3YBHL	676-ball FCBGA package, Commercial Temp.	89H48H12G3YCHL	676-ball FCBGA package, Commercial Temp.
89H48H12G3YBHLG	676-ball Green FCBGA package, Commercial Temp.	89H48H12G3YCHLG	676-ball Green FCBGA package, Commercial Temp.
89H48H12G3YBHLI	676-ball FCBGA package, Industrial Temp.	89H48H12G3YCHLI	676-ball FCBGA package, Industrial Temp.
89H48H12G3YBHLGI	676-ball Green FCBGA package, Industrial Temp.	89H48H12G3YCHLGI	676-ball Green FCBGA package, Industrial Temp.



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