ICS87159
1-TO-8 LVPECL-TO-HCSL ÷1, ÷2, ÷4 CLOCK GENERATOR

GENERAL DESCRIPTION

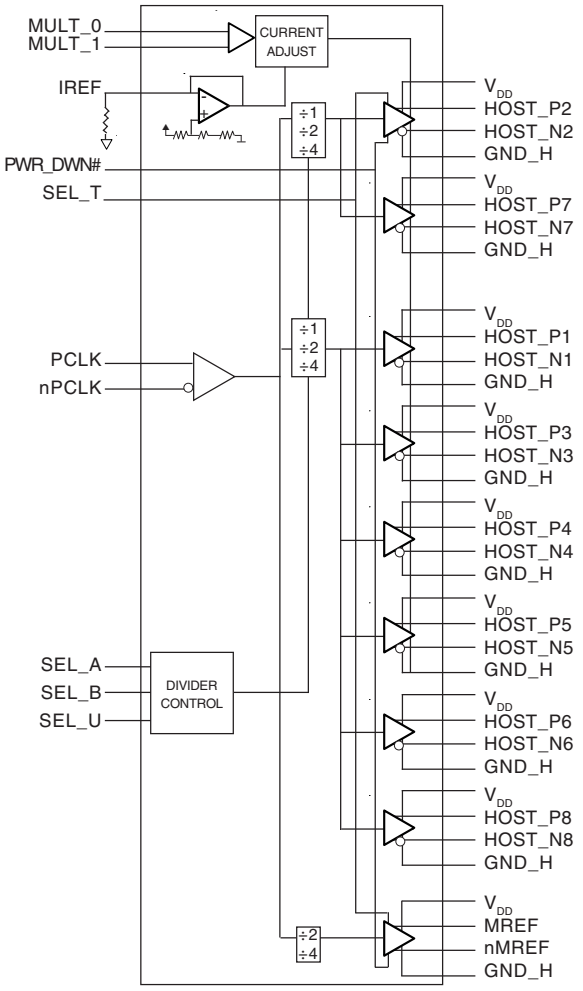
The ICS87159 is a high performance 1-to-8 Differential-to-HCSL/LVCMOS Clock Generator. The ICS87159 has one differential input (which can accept LVDS, LVPECL, LVHSTL, SSTL, HCSL), eight differential HCSL output pairs and two complementary LVCMOS/LVTTL outputs. The eight HCSL output pairs can be configured for divide-by-1, 2, and 4 or high impedance by use of select pins. The two complementary LVCMOS/LVTTL outputs can be configured for divide by 2, divide by 4, high impedance, or driven low for low power operation.

The primary use of the ICS87159 is in *Intel® E8870 chipsets that use *Intel® Pentium 4 processors. The ICS87159 converts the differential clock from the main system clock into HCSL clocks used by *Intel® Pentium 4 processors. However, the ICS87159 is a highly flexible, general purpose device that operates up to 600MHz and can be used in any situation where Differential-to-HCSL translation is required.

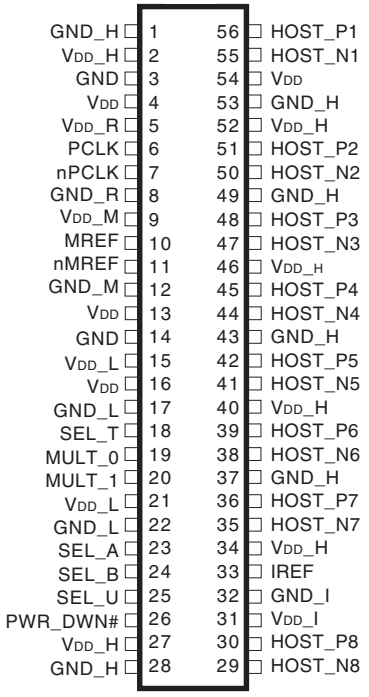
FEATURES

- Eight HCSL outputs
- Two LVCMOS outputs
- LVPECL clock input pair
- PCLK, nPCLK supports the following input types: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 600MHz
- Output skew: 110ps (maximum)
- Propagation delay: 3.6ns (maximum)
- 3.3V operating supply
- 0°C to 85°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



56-Lead TSSOP
6.1mm x 14.0mm x .92mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 28, 37, 43, 49, 53	GND_H	Power		Power supply ground for the differential HOST clock outputs.
2, 27, 34 40, 46, 52	V_{DD}_H	Power		Positive supply pins for the differential HOST clock outputs.
3, 14	GND	Power		Power supply ground.
4, 13, 16, 54	V_{DD}	Power		Positive supply pins.
5	V_{DD}_R	Power		Positive supply pin for LVPECL reference clock inputs.
6	PCLK	Input		Non-inverting differential LVPECL clock input.
7	nPCLK	Input		Inverting differential LVPECL clock input.
8	GND_R	Power		Power supply ground for LVPECL inputs.
9	V_{DD}_M	Power		Positive supply pin for MREF clock outputs.
10, 11	MREF, nMREF	Output		Single ended clocks provided as a reference clock to a memory clock driver. LVCMOS / LVTTL clock output.
12	GND_M	Power		Power supply ground for MREF clock outputs.
15	V_{DD}_L	Power		Positive supply pin for logic input pins.
17, 22	GND_L	Power		Power supply ground for logic input pins.
18	SEL_T	Input	Pulldown	Active high input tristates all outputs. LVCMOS / LVTTL interface levels.
19	MULT_0	Input	Pulldown	The logic setting on these two pins selects the multiplying factor of the IREF reference current for the HOST pair outputs. LVCMOS / LVTTL interface levels.
20	MULT_1	Input	Pullup	The logic setting on these two pins selects the multiplying factor of the IREF reference current for the HOST pair outputs. LVCMOS / LVTTL interface levels.
21	V_{DD}_L	Power		Positive supply pin for logic input pins.
23, 24, 25	SEL_A, _B, _U	Input	Pulldown	Selects desired output frequencies. LVCMOS / LVTTL interface levels.
26	PWR_DWN#	Input	Pullup	Asynchronous active-low LVTTL power-down signal forces MREF outputs low, tristates HOST_N outputs, and drives HOST_P output currents to 2xIREF. LVCMOS / LVTTL interface levels.
29, 30	HOST_N8, HOST_P8	Output		Differential output pairs. HCSL interface levels.
31	V_{DD}_I	Power		Positive supply pin for IREF current reference input.
32	GND_I	Power		Power supply ground for IREF current reference input.
33	IREF	Input		A fixed precision resistor from this pin to ground provides a reference current used for differential current-mode HOST clock outputs.
35, 36	HOST__N7 HOST__P7	Output		Differential output pairs. HCSL interface levels.
38, 39	HOST_N6, HOST_P6	Output		Differential output pairs. HCSL interface levels.
41, 42	HOST__N5, HOST__P5	Output		Differential output pairs. HCSL interface levels.
44, 45	HOST _N4, HOST _P4	Output		Differential output pairs. HCSL interface levels.

continued on next page...

Number	Name	Type		Description
47, 48	HOST_N3, HOST_P3	Output		Differential output pairs. HCSL interface levels.
50, 51	HOST _N2, HOST_P2	Output		Differential output pairs. HCSL interface levels.
55, 56	HOST_N1, HOST_P1	Output		Differential output pairs. HCSL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	LVCMOS Output Impedance			22		Ω

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs					Outputs								
MR/OE_P/OE_N#	_T	_A	_B	_Y	H_P2/H_N2	H_P1/H_N1	H_P3/H_N3	H_P4/H_N4	H_P5/H_N5	H_P6/H_N6	H_P8/H_N8	H_P7/H_N7	MREF_P/MREF_N
1	0	0	0	0	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 4
1	0	0	0	1	Hi Z	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	Hi Z	÷ 4
1	0	0	1	0	÷ 4	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 4	÷ 4
1	0	0	1	1	÷ 4	÷ 4	÷ 4	÷ 4	÷ 4	÷ 4	÷ 4	÷ 4	÷ 4
1	0	1	0	0	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	÷ 4
1	0	1	0	1	Hi Z	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	Hi Z	÷ 4
1	0	1	1	0	÷ 2	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	÷ 2	÷ 4
1	0	1	1	1	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2
1	1	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z
0	X	X	X	X	H_P1 = 2xIREF H_N1 = Hi Z	H_P2 = 2xIREF H_N2 = Hi Z	H_P3 = 2xIREF H_N3 = Hi Z	H_P4 = 2 x IREF H_N4 = Hi Z	H_P5 = 2xIREF H_N5 = Hi Z	H_P6 = 2xIREF H_N6 = Hi Z	H_P5 = 2xIREF H_N5 = Hi Z	H_P1 = 2xIREF H_N1 = Hi Z	MREF_P = low MREF_N = low

TABLE 3B. FUNCTION TABLE

Inputs		Board Target Trace/Term Z	Reference R, IREF = V_{DD}/(3*Rr)	Output Current	V_{OH} @ 50Ω environment
MULT_0	MULT_1				
0	0	50Ω	Rr = 475 1%, IREF = 2.32mA	IOH = 5*IREF	0.6
0	1	50Ω	Rr = 475 1%, IREF = 2.32mA	IOH = 6*IREF	0.7
1	0	50Ω	Rr = 475 1%, IREF = 2.32mA	IOH = 4*IREF	0.5
1	1	50Ω	Rr = 475 1%, IREF = 2.32mA	IOH = 7*IREF	0.8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	58.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Operating Supply Current			48		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	mV
V_{IL}	Input Low Voltage			-0.3		0.8	mV
I_{IH}	Input High Current	MULT_1, PWR_DWN#	V_{DD} = V_{IN} = 3.465V			5	µA
		SEL_A, SEL_B, SEL_T, SEL_U, MULT_0	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	MULT_1, PWR_DWN#	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		SEL_A, SEL_B, SEL_T, SEL_U MULT_0	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

All parameters measured at 200MHz in, 100MHz out on HOST_XX and 50MHz out on MREF.
Current adjust set for V_{OH} = 0.7V. Measurements refer to HOST_XX outputs only.
NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Paramter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK, nPCLK	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	PCLK, nPCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

All parameters measured at 200MHz in, 100MHz out on HOST_XX and 50MHz out on MREF.
Current adjust set for V_{OH} = 0.7V. Measurements refer to HOST_XX outputs only.
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK, nPCLK is V_{DD} + 0.3V.

TABLE 4D. HCSL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{OH}	Output Current		12.9		14.9	mA
V_{OH}	Output High Voltage	RREF = 475Ω, RLOAD = 50Ω		0.7		V
V_{OL}	Output Low Voltage	RREF = 475Ω, RLOAD = 50Ω		0.03		V
I_{OZ}	High Impedance Leakage Current		-10		10	µA
V_{OX}	Output Crossover Voltage		280		430	V

TABLE 5A. HCSL AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				600	MHz
t_{PD}	Propagation Delay; NOTE 1		3.0	3.3	3.6	ns
*t*sk(o)	Output Skew; NOTE 2, 4, 5			65	110	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				500	ps
*t*jit(cc)	Cycle-to-Cycle Jitter				150	ps
t_R/ t_F	Output Rise/Fall Time	20% to 80%	125		800	ps
odc	Output Duty Cycle		48		52	%

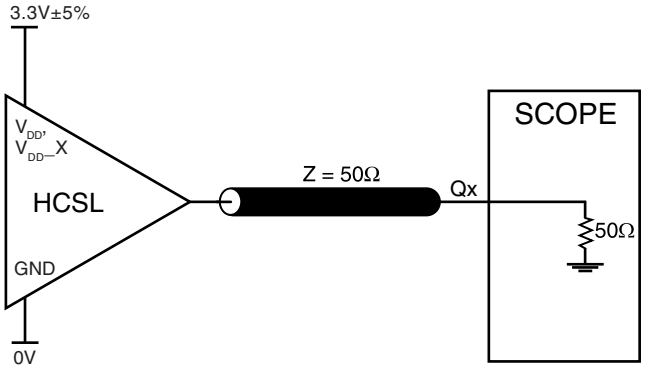
All parameters measured at 200MHz in, 100MHz out on HOST_XX and 50MHz out on MREF.
Current adjust set for V_{OH} = 0.7V. Measurements refer to HOST_XX outputs only.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: Maximum value calculated at +3σ from typical.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. LVCMOS/LVTTL AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 85°C

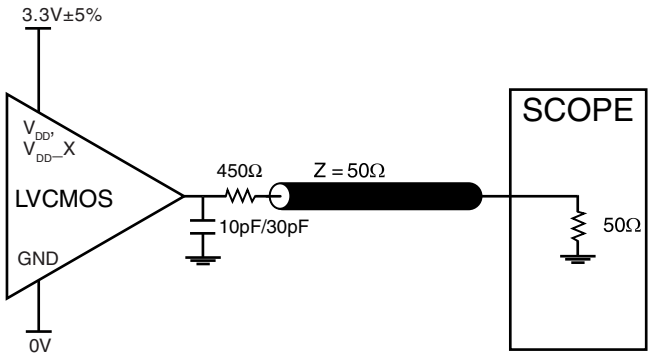
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				300	MHz
t_{PD}	Propagation Delay	Measured at V_{DD}/2	2.85	3.35	3.85	ns
*t*jit(cc)	Cycle-to-Cycle Jitter	C_L = 10pF/30pF			150	ps
t_R	Output Rise Time	0.4V to 2.4V, C_L = 10pF	0.4			ns
		0.4V to 2.4V, C_L = 30pF			1.8	ns
t_F	Output Fall Time	0.4V to 2.4V, C_L = 10pF	0.4			ns
		0.4V to 2.4V, C_L = 30pF			2	ns
odc	Output Duty Cycle	C_L = 10pF/30pF	48		52	%

All parameters measured at 200MHz in, 100MHz out on HOST_XX and 50MHz out on MREF.
Current adjust set for V_{OH} = 0.7V. Measurements refer to MREF outputs only.

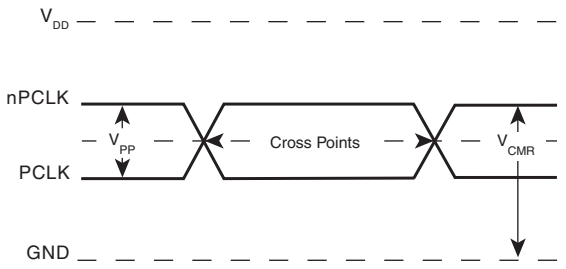
PARAMETER MEASUREMENT INFORMATION



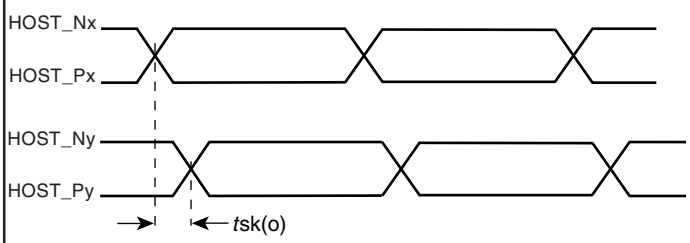
3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT



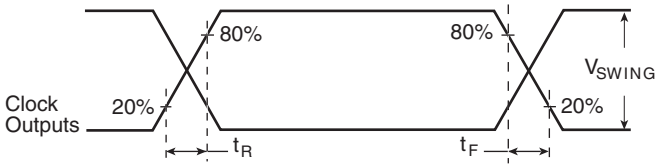
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



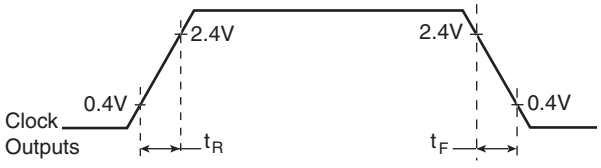
DIFFERENTIAL INPUT LEVEL



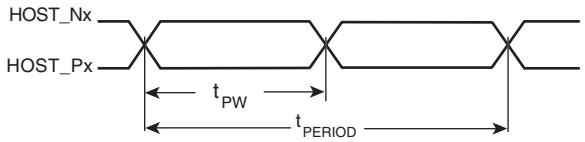
OUTPUT SKEW



HCSL OUTPUT RISE/FALL TIME

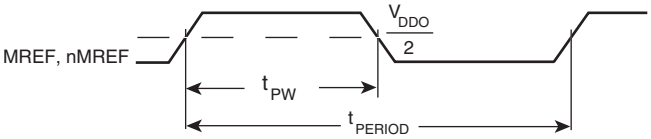


LVCMOS OUTPUT RISE/FALL TIME



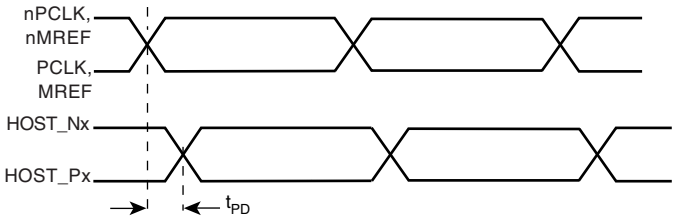
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

HCSL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



PROPAGATION DELAY

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

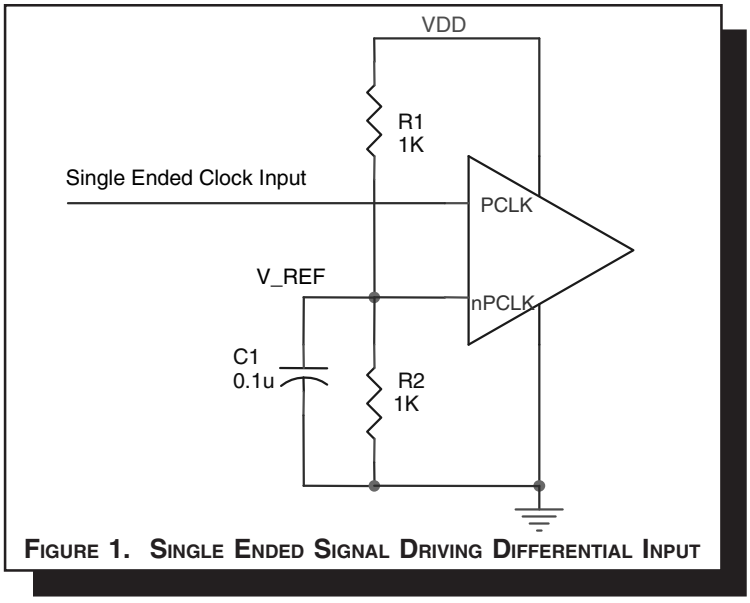


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

PCLK/nPCLK INPUT:
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

HCSL OUTPUT
All unused HCSL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

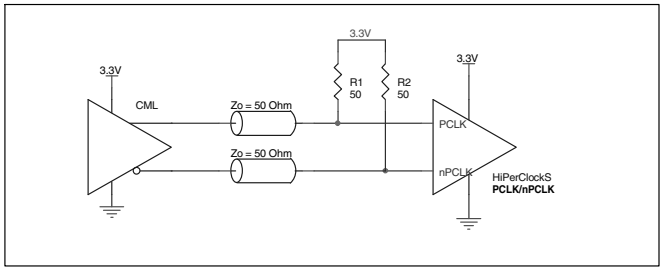


FIGURE 2A. PCLK/nPCLK INPUT DRIVEN BY A CML DRIVER

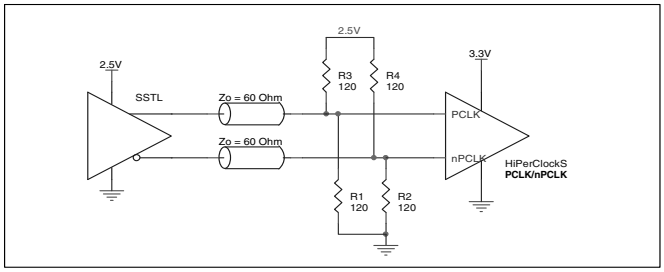


FIGURE 2B. PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER

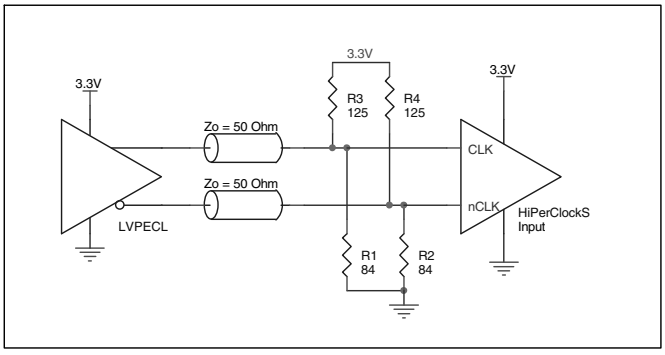


FIGURE 2C. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

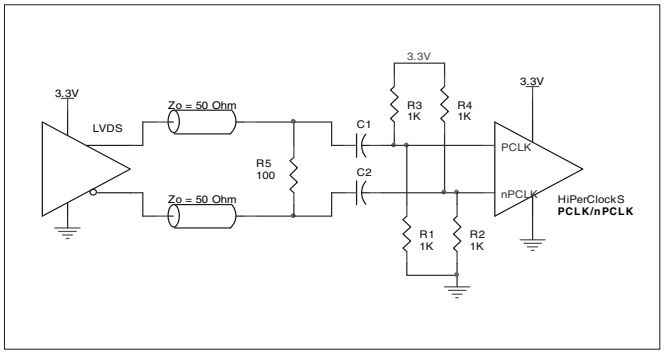


FIGURE 2D. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

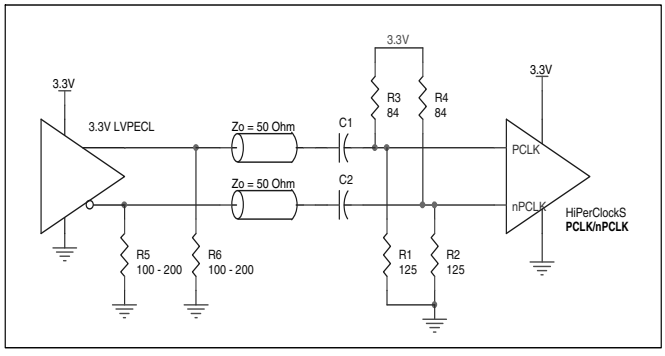


FIGURE 2E. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

SCHEMATIC EXAMPLE

Figure 3 shows an example of the ICS87159 LVPECL to HCSL Clock Generator schematic.

In this example, the ICS87159 is configured as follows:

PWR_DWN# = 1
Mult_[1:0] = 10, Rref = 475Ω, IREF = 2.32mA, I_{OH} = 6*IREF
SEL_[A,B,U] = 000, MREF = PECL ÷ 4, all HOST outputs = PECL ÷ 2
SEL_T = 0, Output Enable

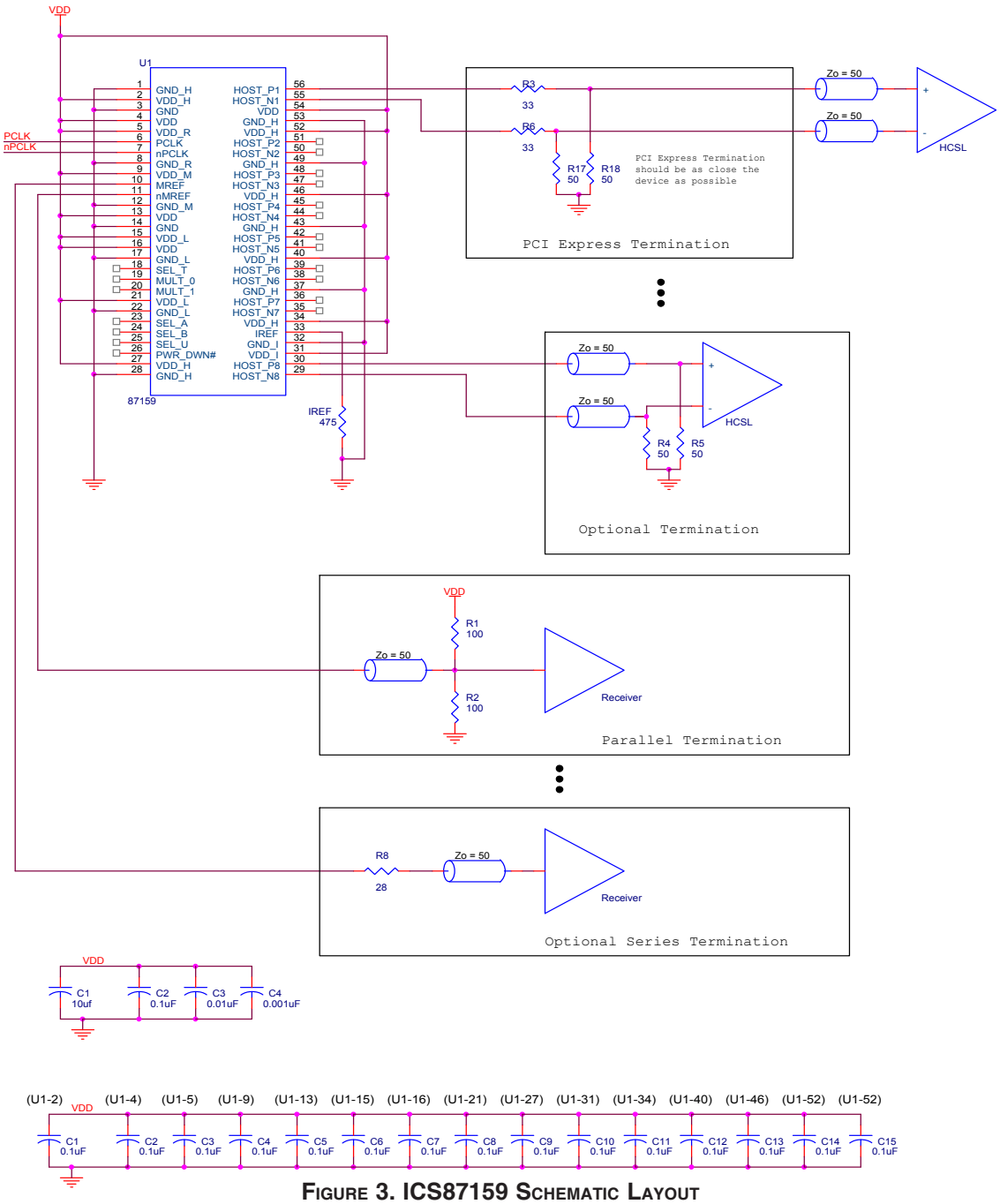


FIGURE 3. ICS87159 SCHEMATIC LAYOUT

Power and Ground

This section provides a layout guide related to power, ground and placement of bypass capacitors for a high-speed digital IC. This layout guide is a general recommendation. The actual board design will depend on the component types being used, the board density and cost constraints. The description assumes that the board has clean power and ground planes. The principle is to minimize the ESR between the clean power/ground plane and the IC power/ground pin.

A low ESR bypass capacitor should be used on each power pin. The value of bypass capacitors ranges from 0.01uF to 0.1uF. The bypass capacitors should be located as close to the power pin as possible. It is preferable to locate the bypass capacitor on the same side as the IC. *Figure 4* shows suggested capacitor placement. Placing the bypass capacitor on the same side as IC allows the capaci-tor to have direct contact with the IC power pin. This can avoid any vias between the bypass capacitor and the IC power pins.

The vias should be place at the Power/Ground pads. There should be minimum one via per pin. Increase the number of vias from the Power/Ground pads to Power/Ground planes can improve the conductivity.

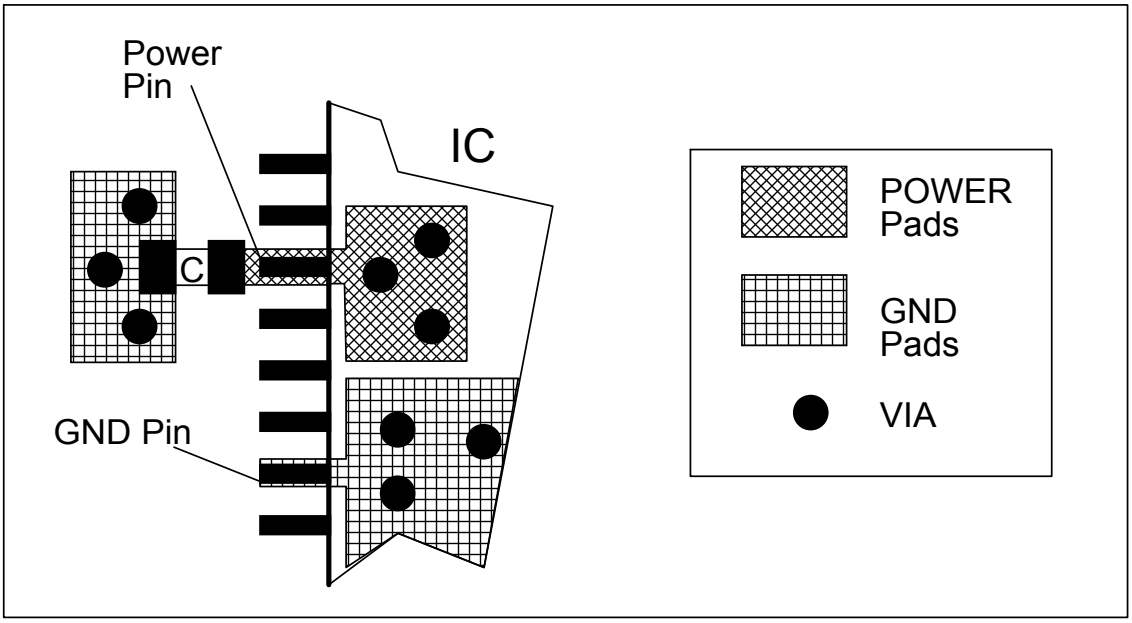


FIGURE 4. RECOMMENDED LAYOUT OF BYPASS CAPACITOR PLACEMENT

LOGIC CONTROL INPUT

The logic input control signals are 3.3V LVCMOS compatible. The logic control input contains ESD diodes and either pull-up or pull-down resistor as shown in *Figure 5.* The data sheet provides pull-up or pull-down information for each input pin. Leaving the input floating will set the control logic to default setting.

To set logic high, the input pin connected directly to V_{DD}. To set logic low, the control input connect directly to ground. For control signal source from the driver that has different power supply, a series current resistor of greater than 100 Ohm is required for random power on sequence.

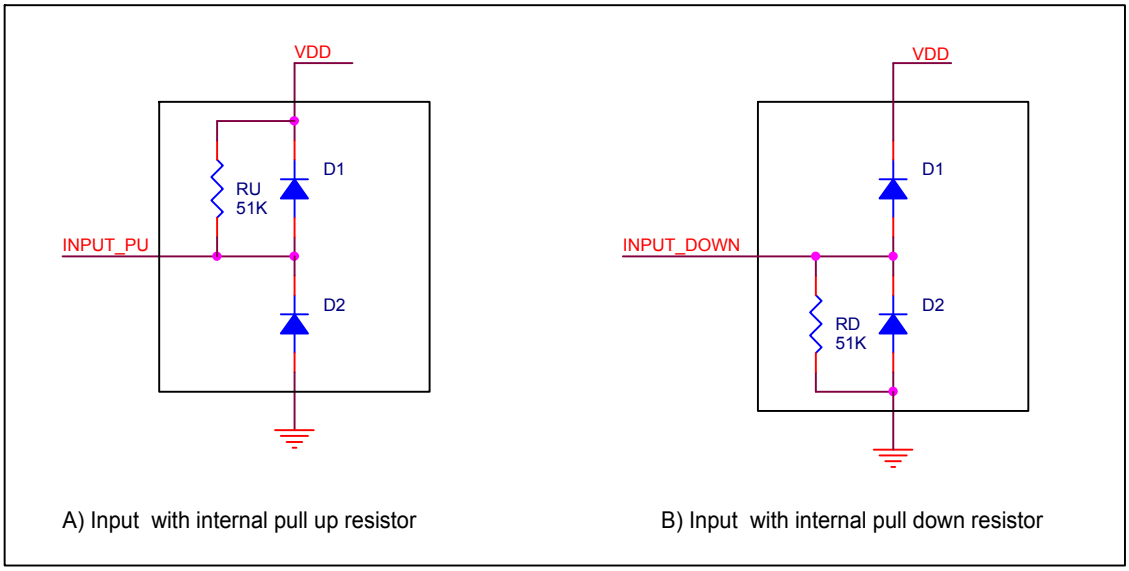


FIGURE 5. LOGIC INPUT CONTROLS

HCSL DRIVER TERMINATION

The HCSL is a differential constant current source driver. The output current is set by control pins MULT_[1:0] and the value of resistor Rref.

In the characteristic impedance of 50 Ohm environment, the match load 50 Ohm resistors R4 and R5 are terminated at the receiving end of the transmission line. The 33 Ohm series resistor R6 and R7 should be located as close to the driver pins as possible. For the clock traces that required very low skew should have equal length.

Other general rules of high-speed digital design also should be followed. Some check points are listed as follows:

- Avoid sharp angles on the clock trace. Sharp angle turn causes the characteristic impedance change on the transmission lines.
- Keep the clock trace on same layer. Whenever possible, avoid any vias on the middle clock traces. Any via on middle the trace can affect the trace characteristic impedance and hence degrade signal quality.
- There should be sufficient space between the clock traces that have different frequencies to avoid cross talk.
- No other signal trace is routed between the clock trace pair.
- Transmission line should not be routed across the split plane on the adjacent layer.

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 56 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	80.2°C/W	68.5°C/W	62.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	58.2°C/W	52.4°C/W	50°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87159 is: 2631

PACKAGE OUTLINE - G SUFFIX FOR 56 LEAD TSSOP

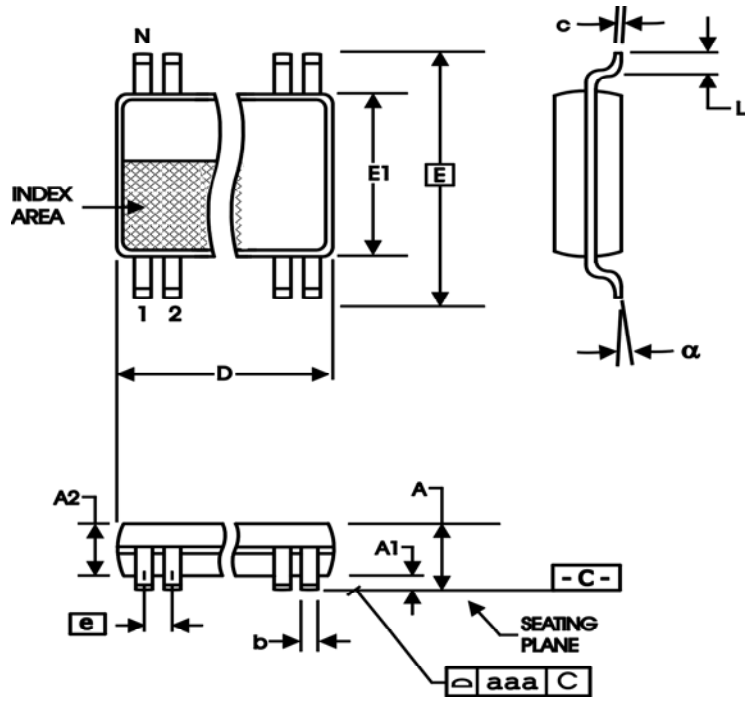


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	56	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.17	0.27
c	0.09	0.20
D	13.90	14.10
E	8.10 BASIC	
E1	6.00	6.20
e	0.50 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87159AG	ICS87159AG	56 Lead TSSOP	tube	0°C to 85°C
87159AGT	ICS87159AG	56 Lead TSSOp	1000 tape & reel	0°C to 85°C
87159AGLF	ICS87159AGLF	56 lead "Lead-Free" TSSOP	tube	0°C to 85°C
87159AGLFT	ICS87159AGLF	56 lead "Lead-Free" TSSOP	1000 tape & reel	0°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	1 15	Features Section - added Lead-Free bullet. Ordering Information Table - added Lead-Free part number and note.	3/21/05
A		8	Added *Recommendations for Unused Input and Output Pins.*	1/17/06
B	T8	15 17	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	7/25/10

We've Got Your Timing Solution.

www.IDT.com

6024 Silver Creek Valley Road
San Jose, CA 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775

Tech Support
netcom@idt.com