



÷1/÷2 DIFFERENTIAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

ICS87021I

GENERAL DESCRIPTION

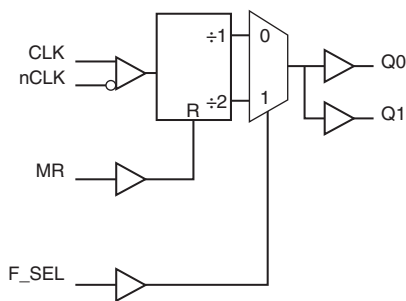


The ICS87021I is a high performance ÷1/÷2 Differential-to-LVCMOS/LVTTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The CLK, nCLK pair can accept most standard differential input levels. Guaranteed part-to-part skew characteristics make the ICS87021I ideal for those clock distribution applications demanding well defined performance and repeatability.

FEATURES

- Two single-ended LVCMOS/LVTTL outputs
- One differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 250MHz
- Additive phase jitter, RMS: 0.18ps (typical)
- Output skew: 50ps (maximum)
- Part-to-part skew: 450ps (maximum)
- Propagation delay: 3.4ns (maximum)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Availalbe in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT

CLK	1	8	VDD
nCLK	2	7	Q0
MR	3	6	Q1
F_SEL	4	5	GND

ICS87021I

8-Lead SOIC

3.90mm x 4.90mm x 1.375mm package body

M Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK	Input	Pulldown	Non-inverting differential clock input.
2	nCLK	Input	Pullup	Inverting differential clock input.
3	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels. See Table 3.
4	F_SEL	Input	Pulldown	Selects divider value for Qx outputs as described in Table 3. LVCMOS / LVTTTL interface levels.
5	GND	Power		Power supply ground.
6	Q1	Output		Singled-ended output. LVCMOS/LVTTTL interface levels.
7	Q0	Output		Singled-ended output. LVCMOS/LVTTTL interface levels.
8	V _{DD}	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance (per output)	V _{DD} = 3.465V		24		pF
		V _{DD} = 2.625V		16		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{OUT}	Output Impedance	V _{DD} = 3.465V		9		Ω

TABLE 3. FUNCTION TABLE

MR	F_SEL	Divide Value
1	X	Reset: Q0, Q1 outputs low
0	0	÷1
0	1	÷2

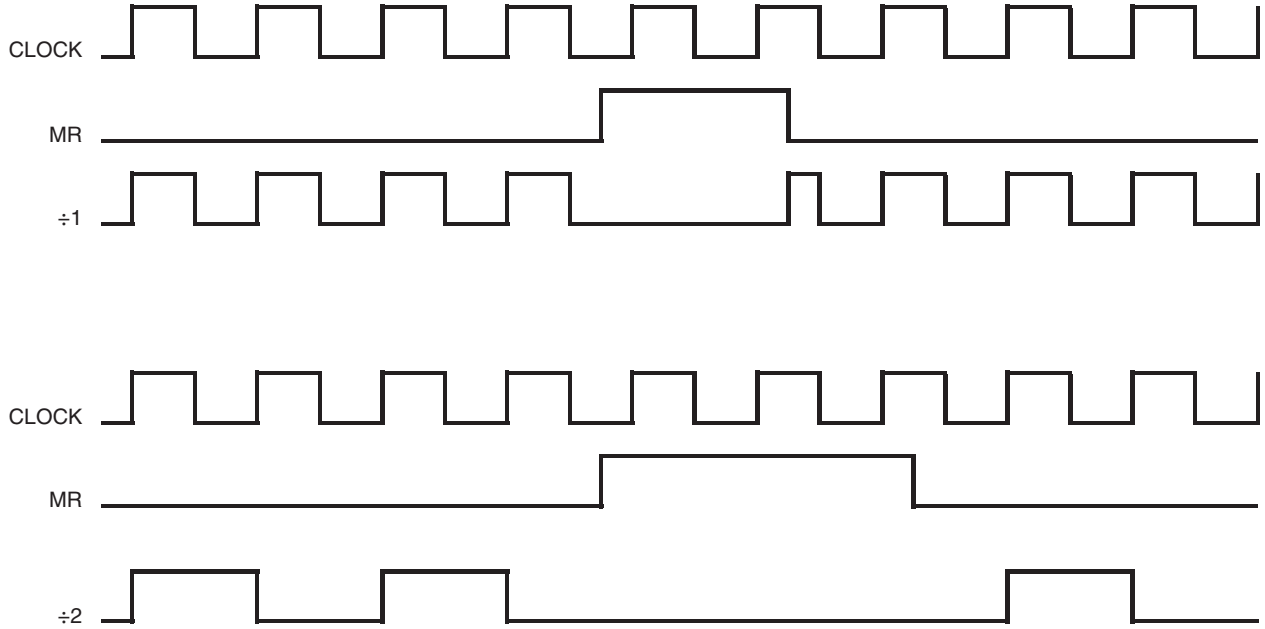


FIGURE 1. TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5$ V
Outputs, V_O	-0.5V to $V_{DD} + 0.5$ V
Package Thermal Impedance, θ_{JA}	103°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				60	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				35	mA

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		1.3		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.7	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465$ V			150	μ A
I_{IL}	Input Low Current	$V_{DD} = 3.465$ V, $V_{IN} = 0$ V	-5			μ A
V_{OH}	Output High Voltage; NOTE 1	$V_{DD} = 3.465$ V	2.6			V
V_{OL}	Output Low Voltage; NOTE 1	$V_{DD} = 3.465$ V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information section, "3.3V Output Load Test Circuit" diagram.

TABLE 4D. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		1.1		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.5	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 2.625$ V			150	μ A
I_{IL}	Input Low Current	$V_{DD} = 2.625$ V, $V_{IN} = 0$ V	-5			μ A
V_{OH}	Output High Voltage; NOTE 1	$V_{DD} = 2.625$ V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	$V_{DD} = 2.625$ V			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information section, "2.5V Output Load Test Circuit" diagram.

TABLE 4E. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$ OR $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		150	μA
		nCLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		5	μA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5		μA
		nCLK	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150		μA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: Common mode voltage is defined as V_{IH} .

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	CLK to Qx	2.1		3.4	ns
f_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	250MHz, Integration Range: 12kHz – 20MHz		0.18		ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				450	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 4				50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		700	ps
odc	Output Duty Cycle; NOTE 5	$F_{out} \leq 133\text{MHz}$	45		55	%
		$F_{out} > 133\text{MHz}$	40		60	%

NOTE 1: Measured from the differential input crossing point to the output at $V_{DD}/2$.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions.

NOTE 5: Output Duty Cycle assuming 50% input duty cycle.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

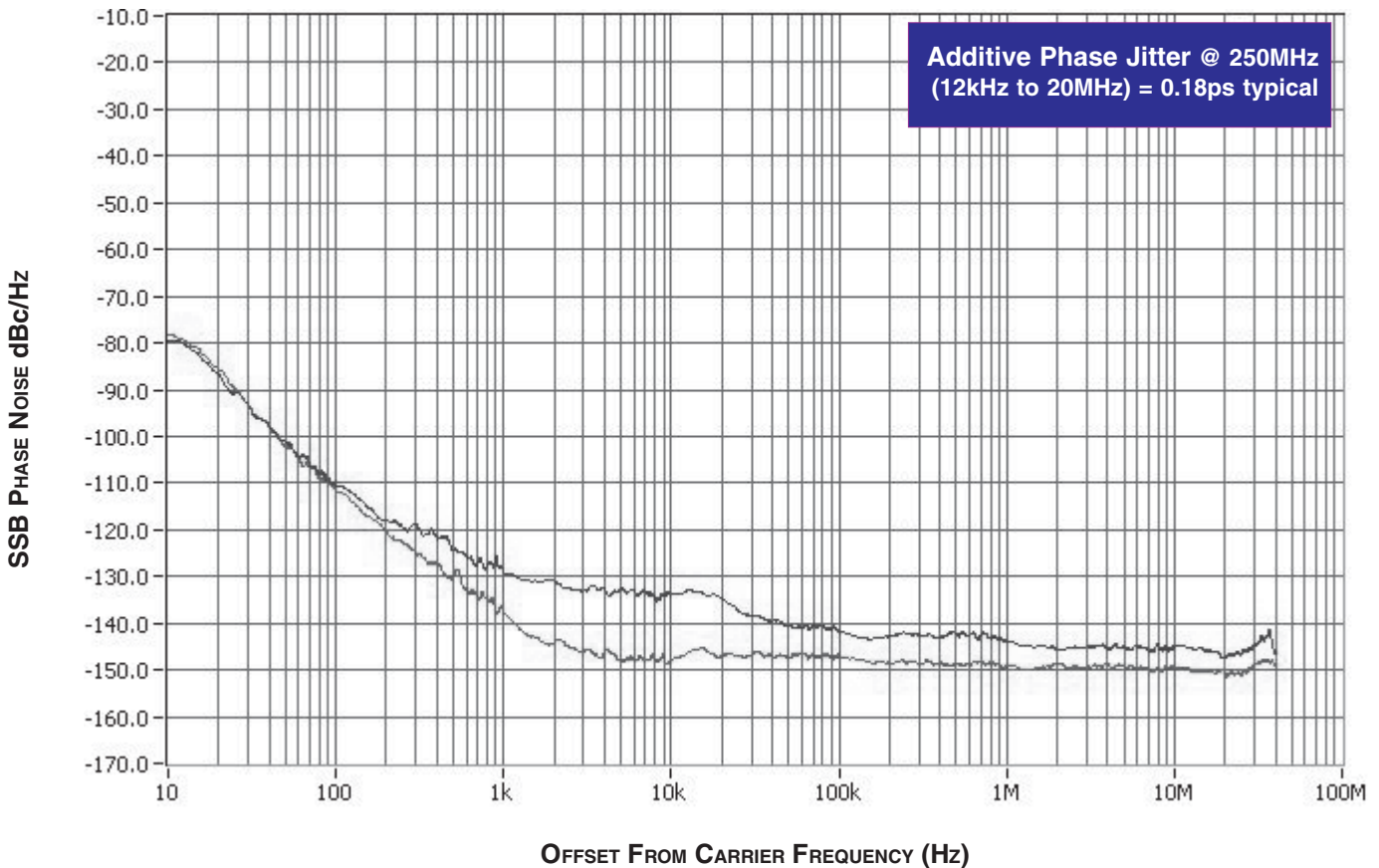
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	CLK to Qx	2.7		3.4	ns
f_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	250MHz, Integration Range: 12kHz – 20MHz		0.3		ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				450	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 4				25	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		700	ps
odc	Output Duty Cycle; NOTE 5	$F_{out} \leq 133\text{MHz}$	45		55	%
		$F_{out} > 133\text{MHz}$	40		60	%

For NOTES, please see above Table 5A.

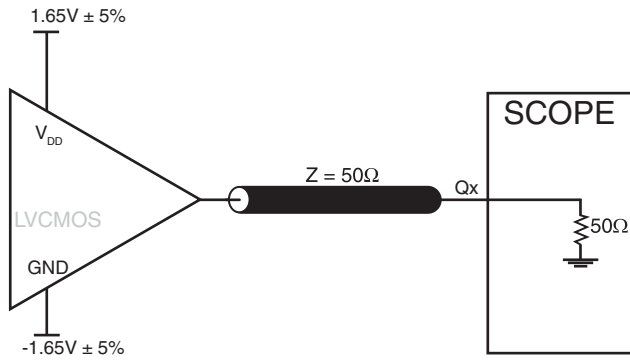
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz

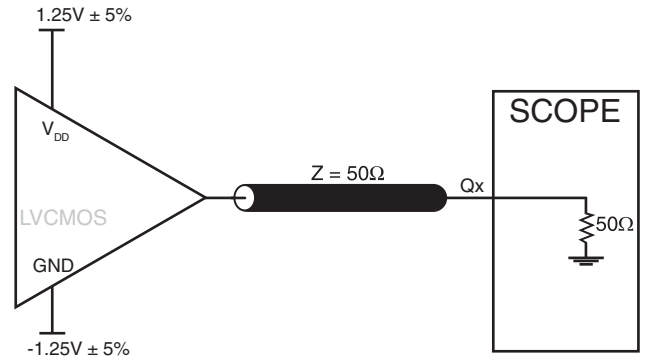
band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



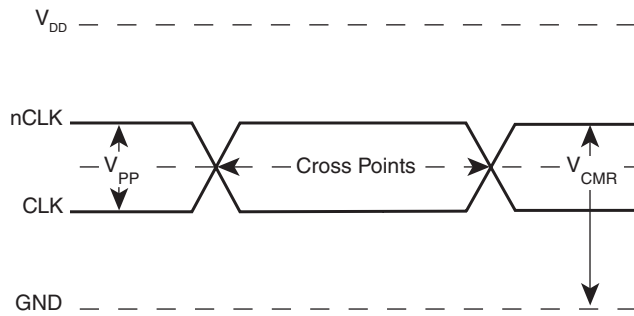
PARAMETER MEASUREMENT INFORMATION



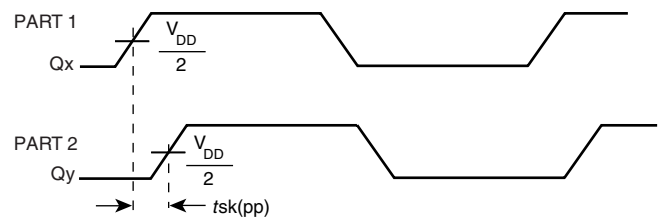
3.3V OUTPUT LOAD AC TEST CIRCUIT



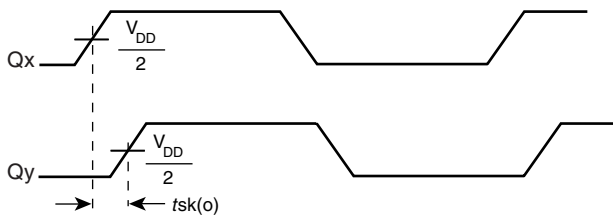
2.5V OUTPUT LOAD AC TEST CIRCUIT



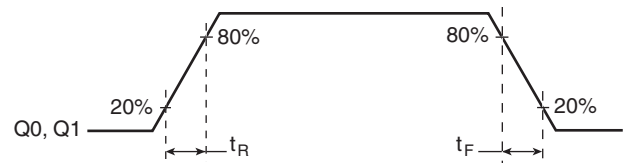
DIFFERENTIAL INPUT LEVEL



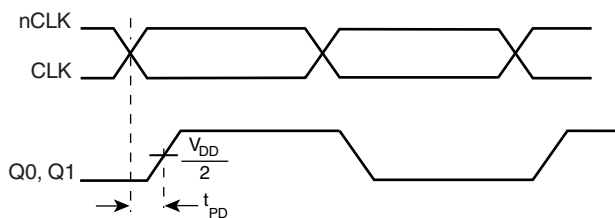
PART-TO-PART SKEW



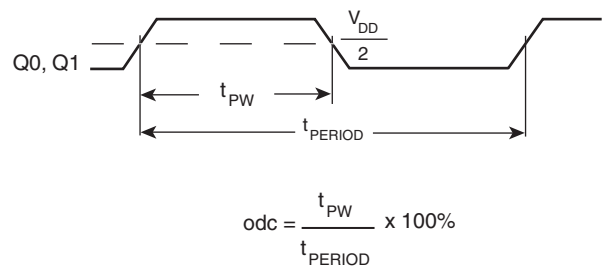
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

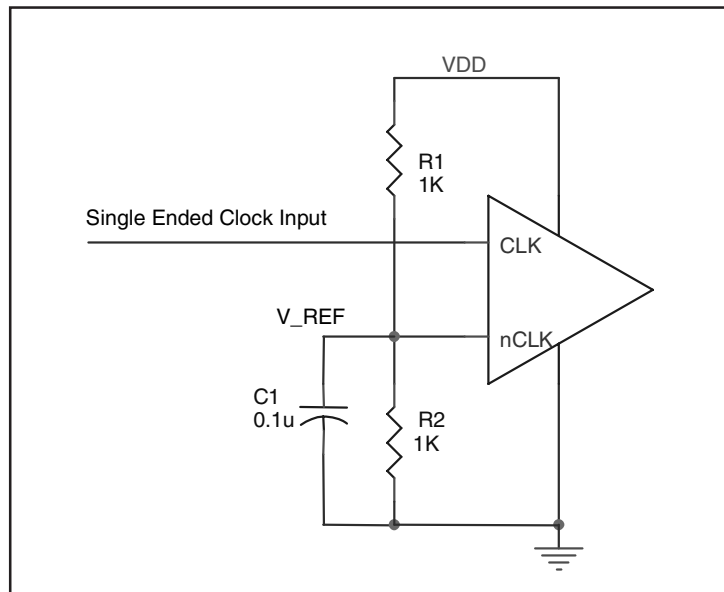


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVC MOS CONTROL PINS

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

LVC MOS OUTPUTS

All unused LVC MOS output can be left floating. There should be no trace attached.

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both signals must meet the V_{pp} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples

only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A*, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

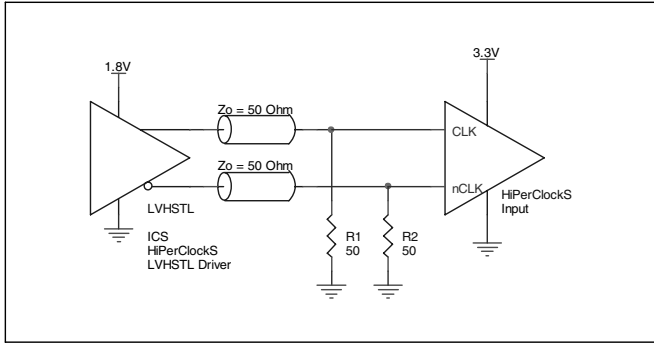


FIGURE 2A. HiPerClockS CLK/nCLK INPUT DRIVEN BY IDT HiPerClockS LVHSTL DRIVER

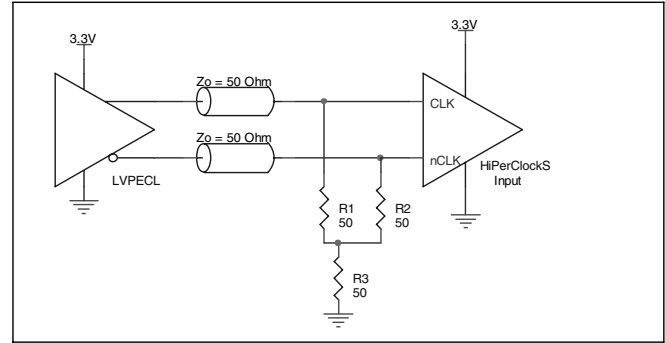


FIGURE 2B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

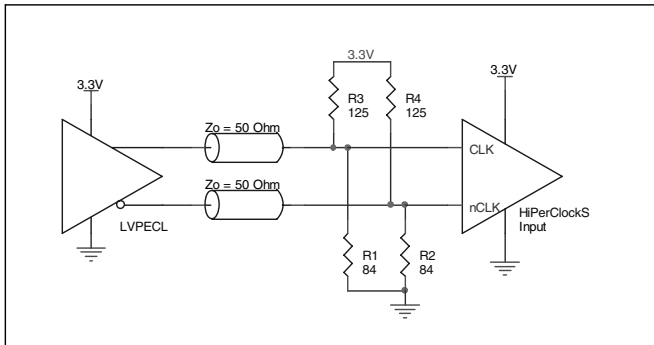


FIGURE 2C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

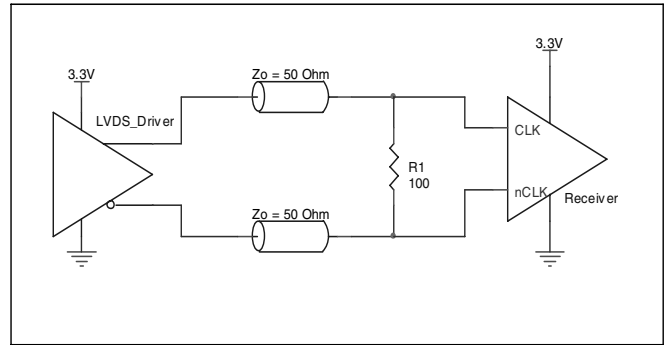


FIGURE 2D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

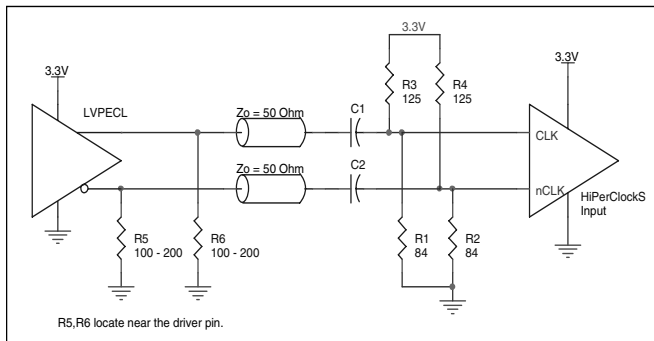


FIGURE 2E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} vs. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	123°C/W	110°C/W	99°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS870211 is: 414

PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

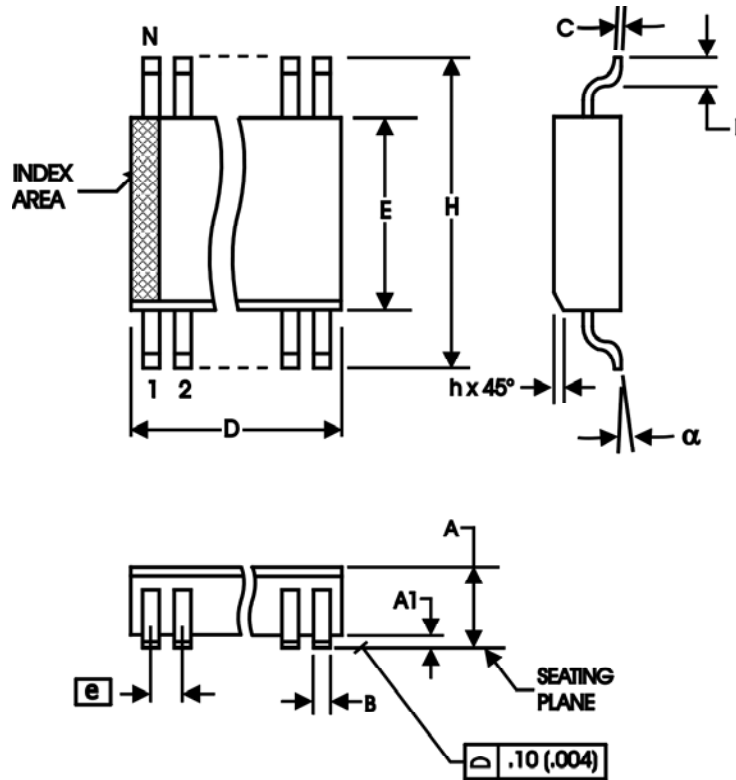


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87021AMI	87021AMI	8 lead SOIC	tube	-40°C to 85°C
87021AMIT	87021AMI	8 lead SOIC	2500 tape & reel	-40°C to 85°C
87021AMILF	87021AIL	8 lead "Lead-Free" SOIC	tube	-40°C to 85°C
87021AMILFT	87021AIL	8 lead "Lead-Free" SOIC	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology, Incorporated (IDT) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
B	T2	2	Pin Characteristics Table - added R _{OUT} row.	8/26/08

Innovate with IDT and accelerate your future networks. Contact:
www.IDT.com

For Sales

800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

For Tech Support

netcom@idt.com
+480-763-2056

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)

