

### General Description

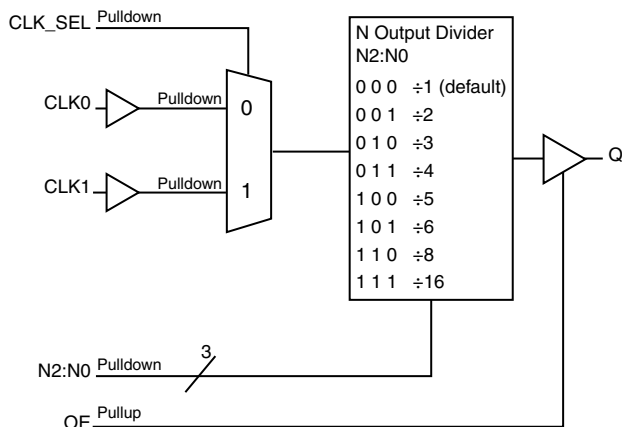
The ICS87001I-01 is a low skew,  $\div 1$ ,  $\div 2$ ,  $\div 3$ ,  $\div 4$ ,  $\div 5$ ,  $\div 6$ ,  $\div 8$ ,  $\div 16$  LVC MOS/LVTTL Clock Divider. The ICS87001I-01 has selectable clock inputs that accept single ended input levels. Output enable pin controls whether the output is in the active or high impedance state.

The ICS87001I-01 is characterized at 3.3V, 2.5V and mixed 3.3V/2.5V, 3.3V/1.8V, 2.5V/1.8V input/output supply operating modes. Guaranteed part-to-part skew characteristics make the ICS87001I-01 ideal for those applications demanding well defined performance and repeatability.

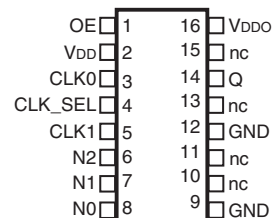
### Features

- One LVC MOS / LVTTL output
- Selectable LVC MOS / LVTTL clock inputs
- Maximum output frequency: 250MHz
- Part-to-part skew: 135ps (typical)
- Power supply modes:  
Core/Output  
3.3V/3.3V  
3.3V/2.5V  
3.3V/1.8V  
2.5V/2.5V  
2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### Block Diagram



### Pin Assignment



**ICS87001I-01**  
 16-Lead TSSOP  
 4.4mm x 5.0mm x 0.925mm  
 package body  
 G Package  
 Top View

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable. When LOW, output is in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.
2	V <sub>DD</sub>	Power		Power supply pin.
3, 5	CLK0, CLK1	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
4	CLK_SEL	Input	Pulldown	Input clock selection. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
6, 7, 8	N2, N1, N0	Input	Pulldown	Output divider select pins. LVCMOS/LVTTL interface levels. See Table 3.
9, 12	GND	Power		Power supply ground.
10, 11, 13, 15	nc	Unused		No connect.
14	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
16	V <sub>DDO</sub>	Power		Output supply pin.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>DDO</sub> = 3.465V		6		pF
		V <sub>DDO</sub> = 2.625V		5		pF
		V <sub>DDO</sub> = 1.95V		5		pF
R <sub>OUT</sub>	Output Impedance	V <sub>DDO</sub> = 3.3V±5%		17		Ω
		V <sub>DDO</sub> = 2.5V±5%		20		Ω
		V <sub>DDO</sub> = 1.8V±0.15V		28		Ω

## Function Table

**Table 3. Programmable Output Divider Function Table**

Inputs			N Divider Value	Maximum Output Frequency (MHz)
N2	N1	N0		
0	0	0	÷1 (default)	250
0	0	1	÷2	125
0	1	0	÷3	83.333
0	1	1	÷4	62.5
1	0	0	÷5	50
1	0	1	÷6	41.667
1	1	0	÷8	31.25
1	1	1	÷16	15.625

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	100.3°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				55	mA
$I_{DDO}$	Output Supply Current	No Load			5	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				55	mA
$I_{DDO}$	Output Supply Current	No Load			5	mA

**Table 4C. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.65	1.8	1.95	V
$I_{DD}$	Power Supply Current				55	mA
$I_{DDO}$	Output Supply Current	No Load			5	mA

**Table 4D. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				55	mA
$I_{DDO}$	Output Supply Current	No Load			5	mA

**Table 4E. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		1.65	1.8	1.95	V
$I_{DD}$	Power Supply Current				55	mA
$I_{DDO}$	Output Supply Current	No Load			5	mA

**Table 4F. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	CLK_SEL, CLK[0:1], N[2:0] $V_{DD} = 3.3V$	-0.3		0.8	V
		OE $V_{DD} = 3.3V$	-0.3		0.6	V
		CLK_SEL, CLK[0:1], N[2:0] $V_{DD} = 2.5V$	-0.3		0.7	V
		OE $V_{DD} = 2.5V$	-0.3		0.5	V
$I_{IH}$	Input High Current	CLK_SEL, CLK[0:1], N[2:0] $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu\text{A}$
		OE $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK_SEL, CLK[0:1], N[2:0] $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu\text{A}$
		OE $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1	$V_{DDO} = 3.3V$	2.6			V
		$V_{DDO} = 2.5V$	1.8			V
		$V_{DDO} = 1.8V$	1.25			V
$V_{OL}$	Output Low Voltage; NOTE 1	$V_{DDO} = 3.3V$			0.5	V
		$V_{DDO} = 2.5V$			0.5	V
		$V_{DDO} = 1.8V$			0.4	V
$I_{OZL}$	Output Hi-Z Current Low		-5			$\mu\text{A}$
$I_{OZH}$	Output Hi-Z Current High				5	$\mu\text{A}$

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information, *Output Load Test Circuit diagrams*.

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				250	MHz
$t_{PD}$	Propagation Delay, Low to High; NOTE 1	$N \leq 2$	3.6	4.6	5.7	ns
		$N > 2$	4.3	5.5	6.7	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				750	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	0.4	0.6	1.0	ns
odc	Output Duty Cycle		40		60	%
$t_{EN}$	Output Enable Time				10	ns
$t_{DIS}$	Output Disable Time				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f_{IN} \leq 250\text{MHz}$  unless noted otherwise.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5B. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				250	MHz
$t_{PD}$	Propagation Delay, Low to High; NOTE 1	$N \leq 2$	3.5	4.8	6.2	ns
		$N > 2$	4.5	5.7	6.9	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				590	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	0.4	0.7	1.1	ns
odc	Output Duty Cycle		40		60	%
$t_{EN}$	Output Enable Time				10	ns
$t_{DIS}$	Output Disable Time				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f_{IN} \leq 250\text{MHz}$  unless noted otherwise.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5C. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				250	MHz
$t_{PD}$	Propagation Delay, Low to High; NOTE 1	$N \leq 2$	3.6	5.2	7.0	ns
		$N > 2$	4.8	6.2	7.6	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				680	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	0.4	1.0	2.3	ns
odc	Output Duty Cycle		40		60	%
$t_{EN}$	Output Enable Time				10	ns
$t_{DIS}$	Output Disable Time				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f_{IN} \leq 250\text{MHz}$  unless noted otherwise.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5D. AC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				250	MHz
$t_{PD}$	Propagation Delay, Low to High; NOTE 1	$N \leq 2$	3.7	4.9	6.2	ns
		$N > 2$	4.5	5.8	7.1	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				570	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	0.4	0.7	1.2	ns
odc	Output Duty Cycle		40		60	%
$t_{EN}$	Output Enable Time				10	ns
$t_{DIS}$	Output Disable Time				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f_{IN} \leq 250\text{MHz}$  unless noted otherwise.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5E. AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				250	MHz
$t_{PD}$	Propagation Delay, Low to High; NOTE 1	$N \leq 2$	3.6	5.2	7.0	ns
		$N > 2$	4.8	6.2	7.7	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				550	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	0.5	1.1	2.5	ns
odc	Output Duty Cycle		40		60	%
$t_{EN}$	Output Enable Time				10	ns
$t_{DIS}$	Output Disable Time				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

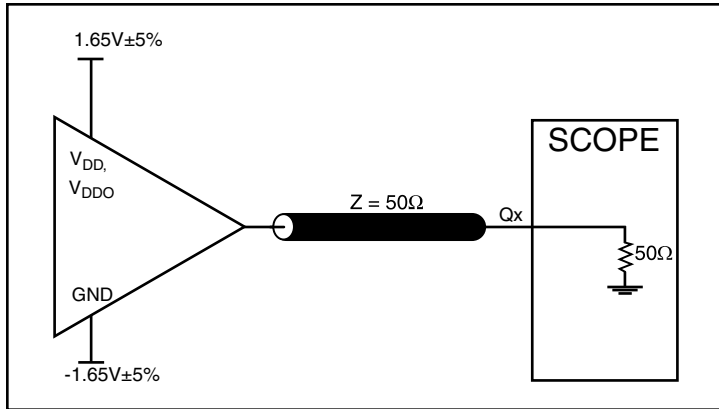
All parameters measured at  $f_{IN} \leq 250\text{MHz}$  unless noted otherwise.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

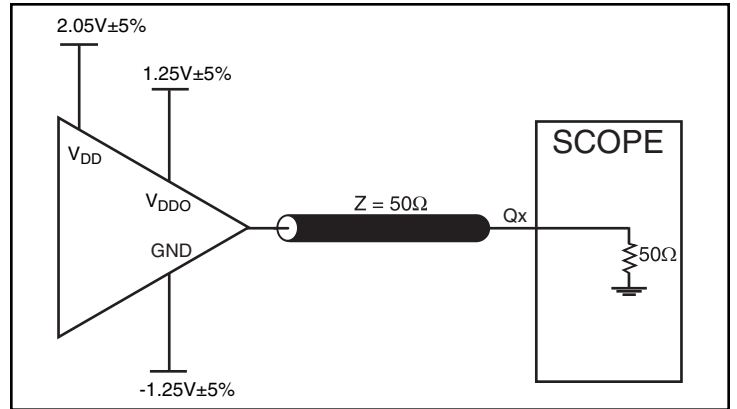
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

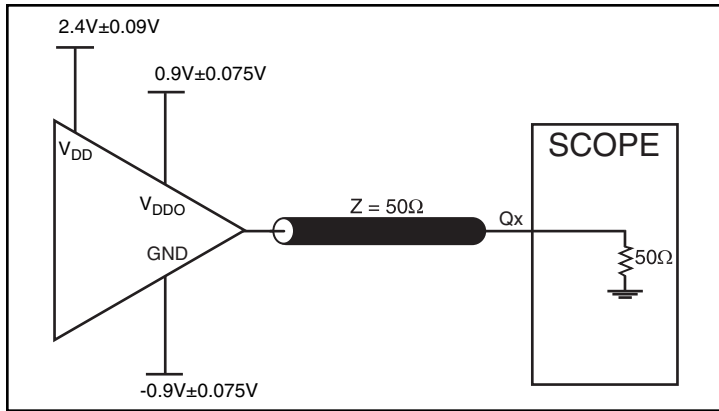
### Parameter Measurement Information



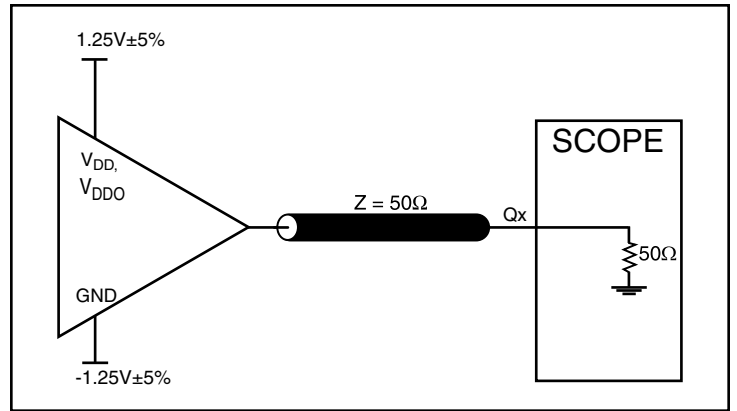
3.3V Core/3.3V LVC MOS Output Load AC Test Circuit



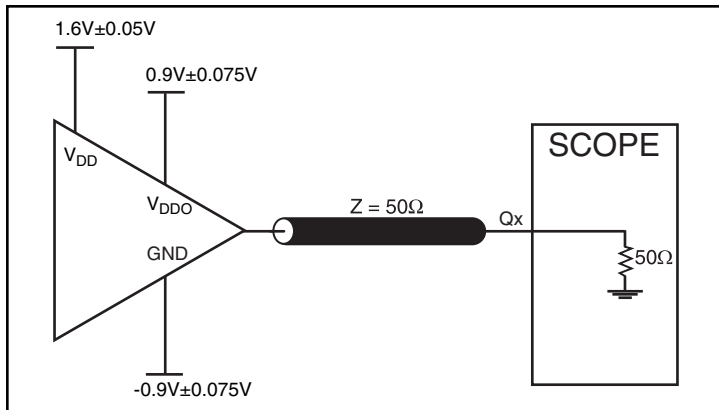
3.3V Core/2.5V LVC MOS Output Load AC Test Circuit



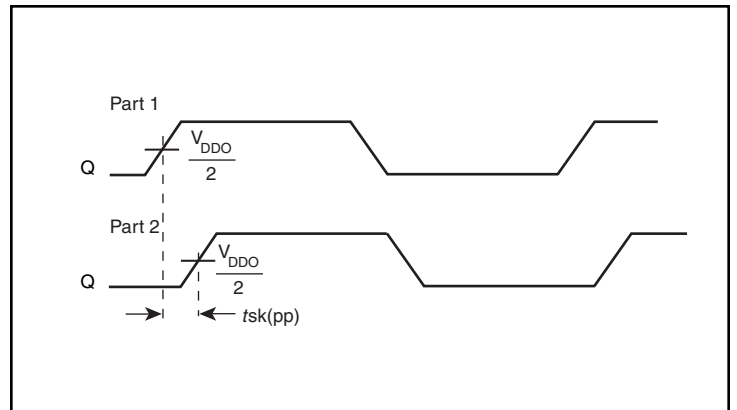
3.3V Core/1.8V LVC MOS Output Load AC Test Circuit



2.5V Core/2.5V LVC MOS Output Load AC Test Circuit

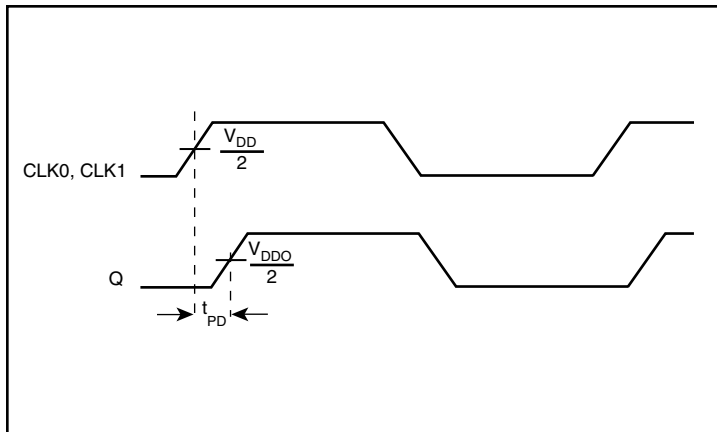


2.5V Core/1.8V LVC MOS Output Load AC Test Circuit

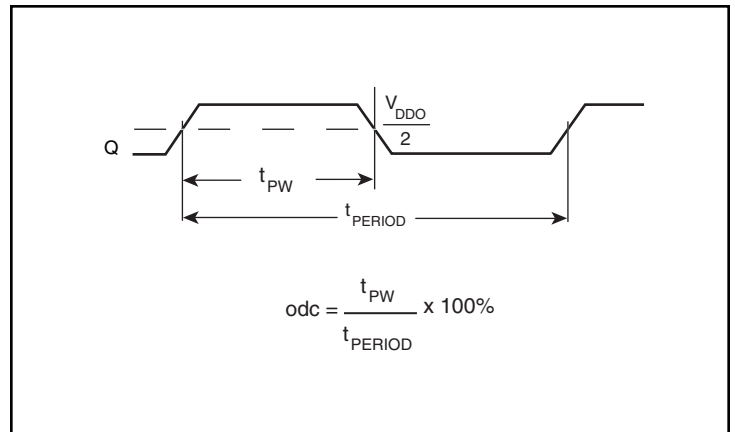


Part-to-Part Skew

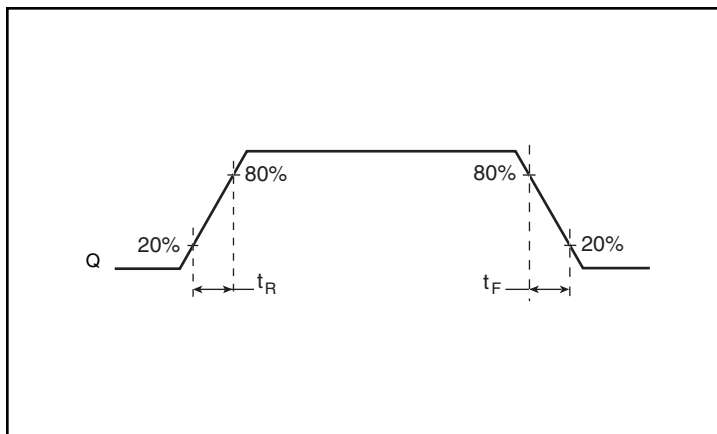
## Parameter Measurement Information, continued



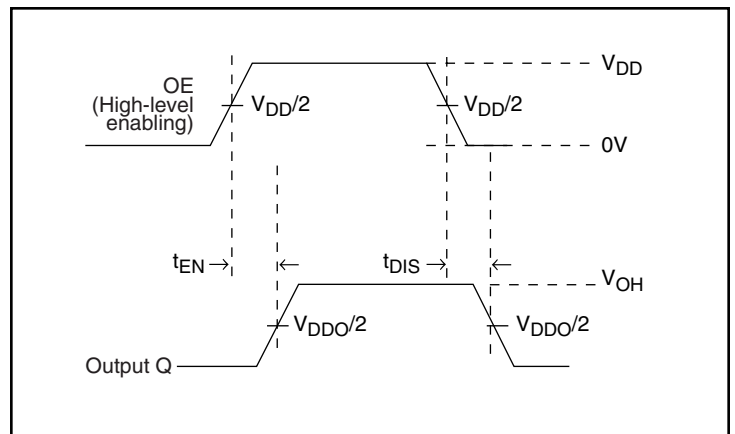
Propagation Delay



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



Output Enable/Disable Time

## Applications Information

### Recommendations for Unused Input Pins

#### Inputs:

##### CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the CLK input to ground.

##### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS87001I-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS87001I-01 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD} = 3.465V * 55mA = \mathbf{190.6mW}$
- Power (output)<sub>MAX</sub> =  $V_{DDO\_MAX} * I_{DDO} = 3.465V * 5mA = 17.3mW$

### LVCMOS Output Power Dissipation

- Output Impedance  $R_{OUT}$  Power Dissipation due to Loading  $50\Omega$  to  $V_{DD}/2$   
Output Current  $I_{OUT} = V_{DD\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 17\Omega)] = \mathbf{25.9mA}$
- Power Dissipation on the  $R_{OUT}$  per LVCMOS output  
Power ( $R_{OUT}$ ) =  $R_{OUT} * (I_{OUT})^2 = 17\Omega * (25.9mA)^2 = \mathbf{11.4mW}$
- Total Power ( $R_{OUT}$ ) =  $11.4mW * 1 = \mathbf{11.4mW}$

### Dynamic Power Dissipation at $f_{OUT\_MAX}$ (250MHz)

$$\text{Power (250MHz)} = C_{PD} * \text{Frequency} * (V_{DDO})^2 = 6pF * 250MHz * (3.465V)^2 = \mathbf{18mW \text{ per output}}$$

$$\text{Total Power (250MHz)} = 18mW * 1 = \mathbf{18mW}$$

### Total Power Dissipation

- **Total Power**  
= Power (core)<sub>MAX</sub> + Power (output)<sub>MAX</sub> + Total Power ( $R_{OUT}$ ) + Total Power (250MHz)  
=  $190.6mW + 17.3mW + 11.4mW + 18mW$   
=  $\mathbf{237.3mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is  $125^\circ\text{C}$ . Limiting the internal transistor junction temperature,  $T_j$ , to  $125^\circ\text{C}$  ensures that the bond wire and bond pad temperature remains below  $125^\circ\text{C}$ .

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is  $100.3^\circ\text{C/W}$  per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of  $85^\circ\text{C}$  with all outputs switching is:

$$85^\circ\text{C} + 0.237W * 100.3^\circ\text{C/W} = 109^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 16 Lead TSSOP, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

## Transistor Count

The transistor count for ICS87001I-01: 2769

## Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

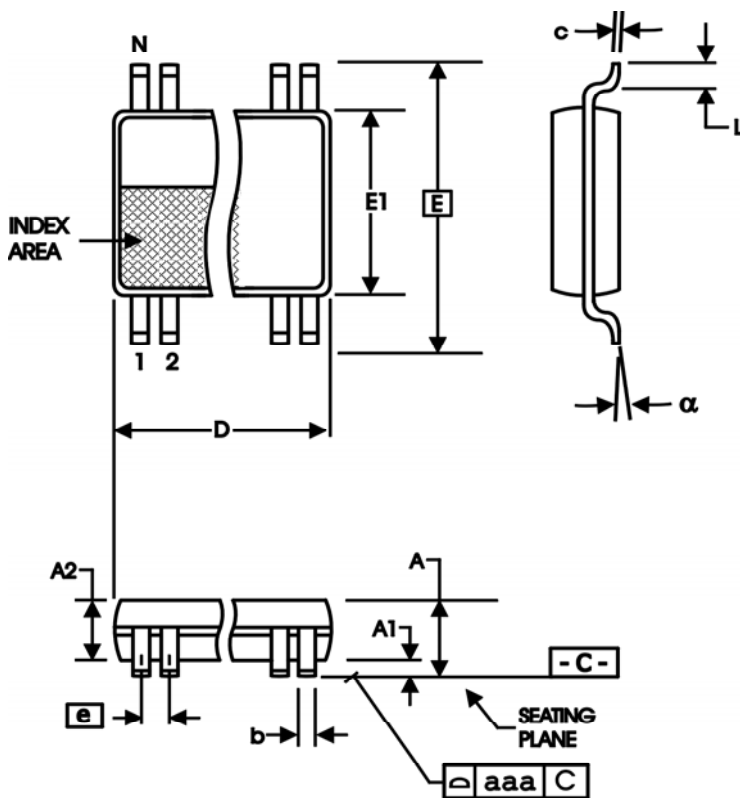


Table 8. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

**Table 9. Ordering Information**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
87001BGI-01LF	001BI01L	"Lead-Free" 16 Lead TSSOP	Tube	-40°C to 85°C
87001BGI-01LFT	001BI01L	"Lead-Free" 16 Lead TSSOP	Tape & Reel	-40°C to 85°C

## We've Got Your Timing Solution



6024 Silver Creek Valley Road  
San Jose, California 95138

**Sales**  
800-345-7015 (inside USA)  
+408-284-8200 (outside USA)  
Fax: 408-284-2775  
[www.IDT.com/go/contactIDT](http://www.IDT.com/go/contactIDT)

**Technical Support**  
[netcom@idt.com](mailto:netcom@idt.com)  
+480-763-2056

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright 2013. All rights reserved.