

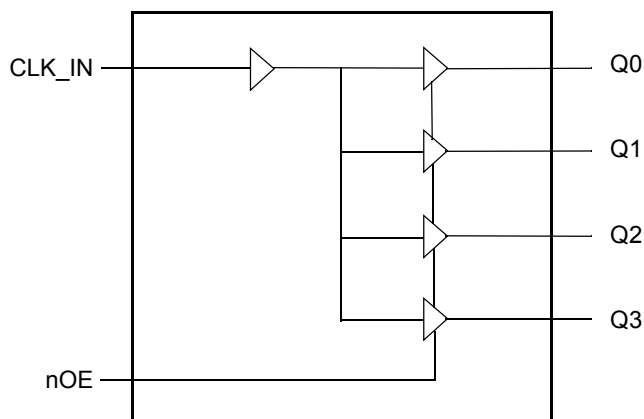
General Description

The ICS830154I-09 is an LVCMOS 1.5V supply, over-voltage tolerant clock fanout buffer targeted for clock generation in high-performance telecommunication, networking and computing applications. The device is optimized for low-skew clock distribution in low-voltage applications. The input over-voltage tolerance enables using this device in mixed-mode voltage applications. An output enable pin controls whether the outputs are in the active or high impedance state. Guaranteed output and part-to-part skew characteristics make the ICS830154I-09 ideal for those applications demanding well defined performance and repeatability. The ICS830154I-09 is packaged in a small 8-TSSOP and in an 8-SOIC package.

Features

- Low-skew 1:4 fanout buffer
- Supports 1.5V and 1.8V power supply
- LVCMOS input and output levels
- 3.6V Over-voltage tolerance at the clock and control input
- Support clock frequencies up to 150MHz
- LVCMOS compatible control input for output disable
- Output disabled to a high-impedance state
- Additive Phase Jitter, RMS: 0.24ps (typical), 1.5V output
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages (8-TSSOP, 8-SOIC)

Block Diagram



Pin Assignments

CLK_IN	1	8	Q0
VDD	2	7	Q1
nOE	3	6	Q2
GND	4	5	Q3

ICS830154I-09

8-SOIC, 150mil

3.9mm x 4.9mm x 1.375mm package body

M-Package

Top View

ICS830154I-09

8-TSSOP

4.4mm x 3.0mm x 0.925mm package body

G-Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK_IN	Input	Pulldown	Single-ended clock input. LVCMOS interface levels.
2	V _{DD}	Power		Power supply pin.
3	nOE	Input	Pulldown	Output enable pin. See Table 3. LVCMOS interface levels.
4	GND	Power		Power supply ground.
5	Q3	Output		Single-ended clock output. LVCMOS interface levels.
6	Q2	Output		Single-ended clock output. LVCMOS interface levels.
7	Q1	Output		Single-ended clock output. LVCMOS interface levels.
8	Q0	Output		Single-ended clock output. LVCMOS interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance	V _{DD} = 1.95V		13		pF
		V _{DD} = 1.6V		12		pF
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{OUT}	Output Impedance	V _{DD} = 1.8V ± 0.15V		12		Ω
		V _{DD} = 1.5 ± 0.1V		15		Ω

Function Table

Table 3. nOE Configuration Table

Input	Operation
nOE	
0 (default)	Q[3:0] are active.
1	Q[3:0] disabled in high-impedance state

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	3.6V
Outputs, V_O	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, θ_{JA} 8 Lead TSSOP 8 Lead SOIC	121.5°C/W (0 mps) 103.0°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 1.5V \pm 0.1V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.4	1.5	1.6	V
I_{DDQ}	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 1.8V \pm 0.15V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.65	1.8	1.95	V
I_{DDQ}	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

Table 4C. LVCMOS DC Characteristics, $V_{DD} = 1.5V \pm 0.1V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$0.65 * V_{DD}$		3.6V	V
V_{IL}	Input Low Voltage		-0.3		$0.35 * V_{DD}$	V
I_{IH}	Input High Current	CLK_IN, nOE $V_{DD} = V_{IN} = 1.6V$			150	μA
I_{IL}	Input Low Current	CLK_IN, nOE $V_{DD} = 1.6V$, $V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage	Q[3:0] $I_{OH} = -4mA$	$0.75 * V_{DD}$			V
V_{OL}	Output Low Voltage	Q[3:0] $I_{OL} = 4mA$			$0.25 * V_{DD}$	V

Table 4D. LVCMOS DC Characteristics, $V_{DD} = 1.8V \pm 0.15V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			$0.65 * V_{DD}$		3.6V	V
V_{IL}	Input Low Voltage			-0.3		$0.35 * V_{DD}$	V
I_{IH}	Input High Current	CLK_IN, nOE	$V_{DD} = V_{IN} = 1.95V$			150	μA
I_{IL}	Input Low Current	CLK_IN, nOE	$V_{DD} = 1.95V$, $V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage	Q[3:0]	$I_{OH} = -6mA$	$V_{DD} - 0.45$			V
V_{OL}	Output Low Voltage	Q[3:0]	$I_{OL} = 6mA$			0.45	V

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = 1.5V \pm 0.1V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Reference Frequency				150	MHz
t_{PLH}	Propagation Delay (low to high transition)		1.9		4.1	ns
t_{PHL}	Propagation Delay (high to low transition)		1.9		4.1	ns
t_{PLZ} , t_{PHZ}	Disable Time (active to high-impedance)				10	ns
t_{PZL} , t_{PZH}	Enable Time (high-impedance to disable)				10	ns
$tsk(o)$	Output Skew; NOTE 1, 2				40	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 3				1.25	ns
f_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	25MHz, Integration Range: 12kHz - 5MHz		0.241		ps
t_R / t_F	Output Rise/Fall Time; NOTE 4	0.525V to 0.975V	0.14		0.64	ns
odc	Output Duty Cycle		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.

NOTE 4: Characterized using a 33 Ω series terminated 5" transmission line to a 5pF capacitor to GND in parallel with 500 Ω (450 Ω resistor + 50 Ω scope) to GND.

Table 5B. AC Characteristics, $V_{DD} = 1.8V \pm 0.15V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Reference Frequency				150	MHz
t_{PLH}	Propagation Delay (low to high transition)		1.5		3.2	ns
t_{PHL}	Propagation Delay (high to low transition)		1.5		3.2	ns
t_{PLZ} , t_{PHZ}	Disable Time (active to high-impedance)				10	ns
t_{PZL} , t_{PZH}	Enable Time (high-impedance to disable)				10	ns
$tsk(o)$	Output Skew; NOTE 1, 2				40	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 3				1.25	ns
σ_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	25MHz, Integration Range: 12kHz - 5MHz		0.187		ps
t_R / t_F	Output Rise/Fall Time; NOTE 4	0.63V to 1.17V	0.15		0.6	ns
odc	Output Duty Cycle		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

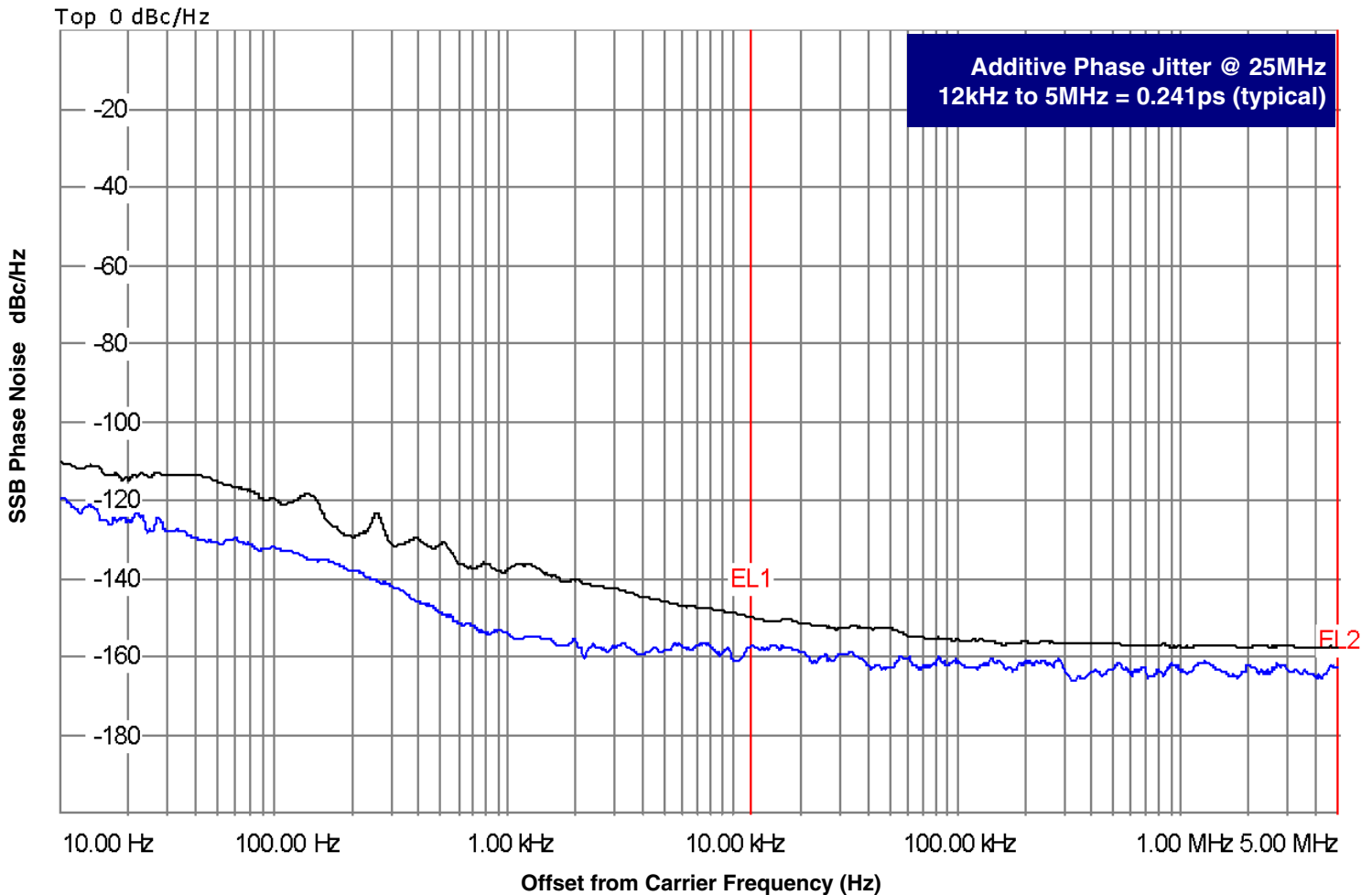
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.

NOTE 4: Characterized using a 33Ω series terminated 5" transmission line to a 5pF capacitor to GND in parallel with 500Ω (450Ω resistor + 50Ω scope) to GND.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

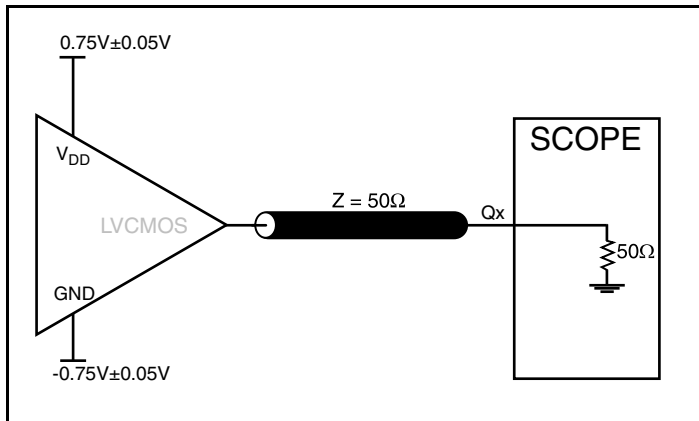
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



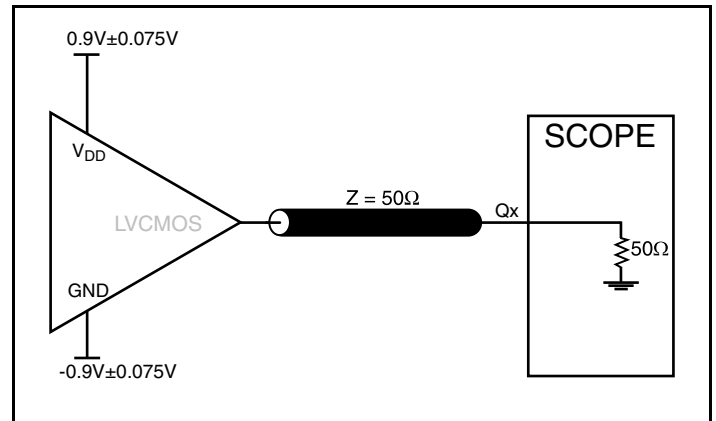
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator".

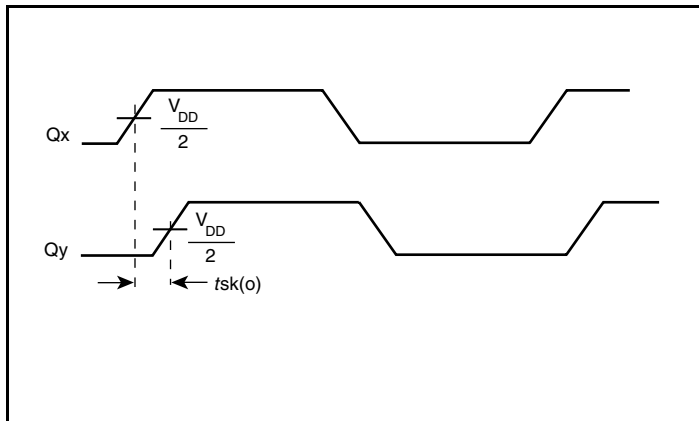
Parameter Measurement Information



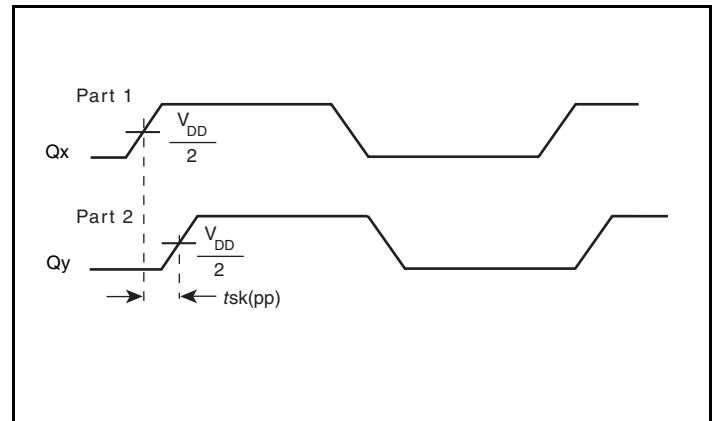
1.5V Output Load AC Test Circuit



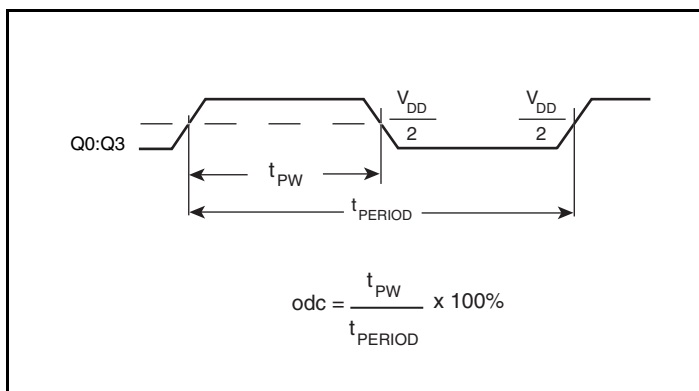
1.8V Output Load AC Test Circuit



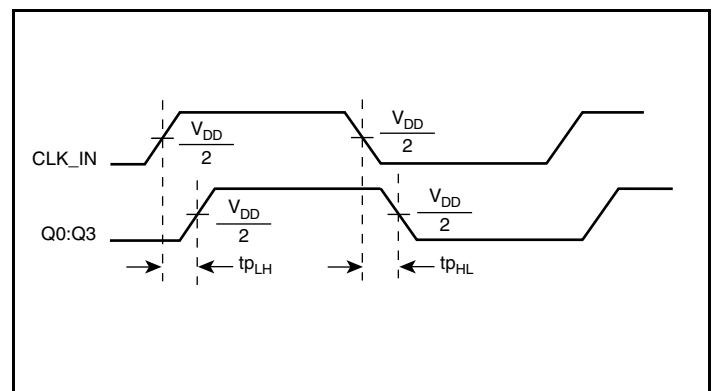
Output Skew



Part-to-Part Skew

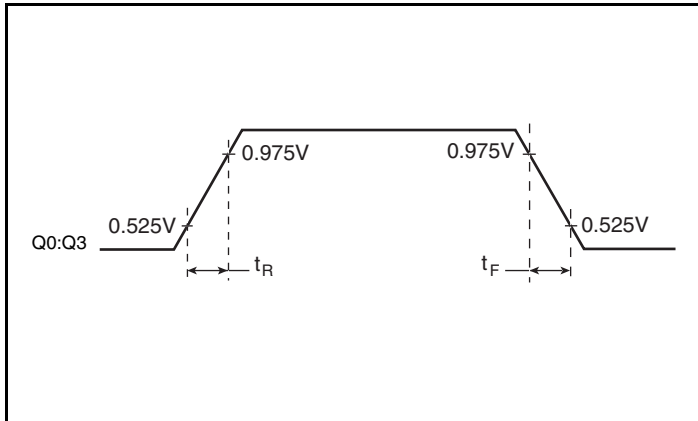


Output Duty Cycle/Pulse Width/Period

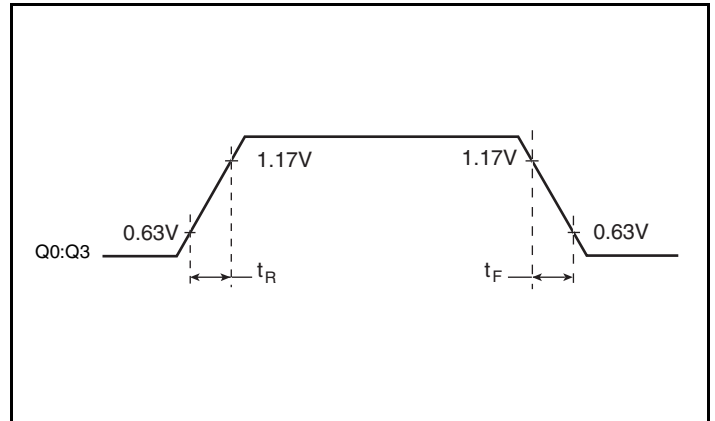


Propagation Delay

Parameter Measurement Information



1.5V Output Rise/Fall Time (Characterized using a 33Ω series terminated 5" transmission line to a 5pF capacitor to GND in parallel with 500Ω (450Ω resistor + 50Ω scope) to GND.)



1.8V Output Rise/Fall Time (Characterized using a 33Ω series terminated 5" transmission line to a 5pF capacitor to GND in parallel with 500Ω (450Ω resistor + 50Ω scope) to GND.)

Applications Information

Recommendations for Unused Output Pins

Outputs:

LVC MOS Outputs

All unused LVC MOS output can be left floating. There should be no trace attached.

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS830154I-09. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS830154I-09 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for $V_{DD} = 1.8V + 0.15V = 1.95V$, which gives worst case results.

$$\text{Power (core)}_{MAX} = V_{DD_MAX} * I_{DD_MAX} = 1.95V * 1mA = \mathbf{1.95mW}$$

Total Static Power:

$$= \text{Power (core)}_{MAX} = \mathbf{1.95mW}$$

Dynamic Power Dissipation at F_{OUT_MAX} (150MHz)

$$\text{Total Power (150MHz)} = [(C_{PD} * N) * \text{Frequency} * (V_{DDO})^2] = [(13pF * 4) * 150MHz * (1.95V)^2] = \mathbf{29.7mW}$$

N = number of outputs

Total Power

$$\begin{aligned} &= \text{Static Power} + \text{Dynamic Power Dissipation} \\ &= 1.95mW + 29.7mW \\ &= \mathbf{31.65mW} \end{aligned}$$

2. Junction Temperature.

Junction temperature, T_J , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_J , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

$$\text{The equation for } T_J \text{ is as follows: } T_J = \theta_{JA} * Pd_{total} + T_A$$

T_J = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 121.5°C/W per Table 6A below.

Therefore, T_J for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.032W * 121.5^\circ\text{C/W} = 88.9^\circ\text{C. This is below the limit of } 125^\circ\text{C.}$$

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	121.5°C/W	117.3°C/W	115.3°C/W

Table 6B. Thermal Resistance θ_{JA} for 8 Lead SOIC, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

Reliability Information

Table 7A. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	121.5°C/W	117.3°C/W	115.3°C/W

Table 7B. θ_{JA} vs. Air Flow Table for a 8 Lead SOIC

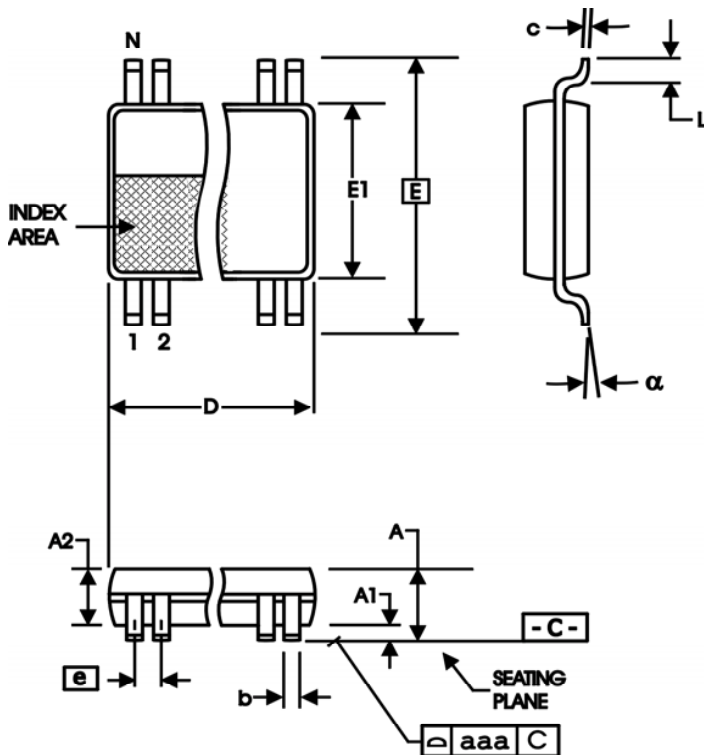
θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

Transistor Count

The transistor count for ICS830154I-09 is: 169

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP



Package Outline - M Suffix for 8 Lead SOIC

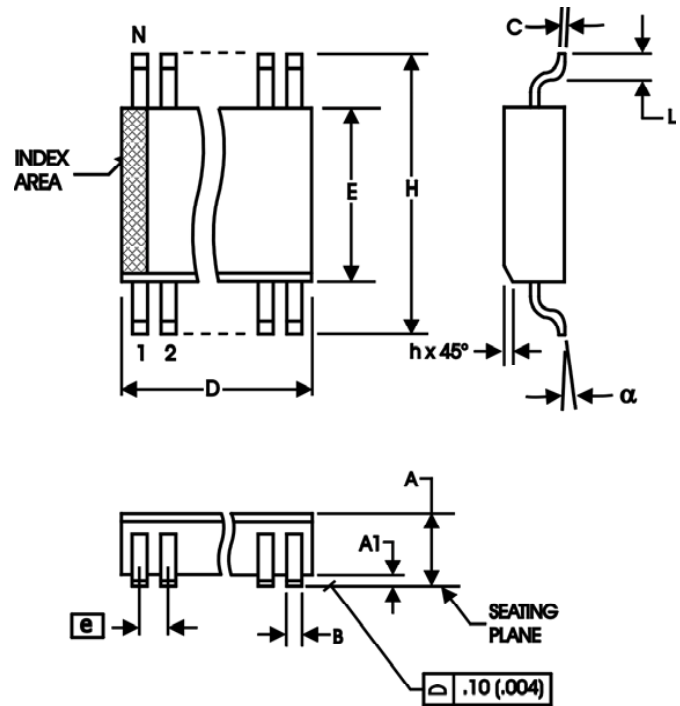


Table 8A. Package Dimensions for 8 Lead TSSOP

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 8B. Package Dimensions for 8 Lead SOIC

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
830154BGI-09	4BI09	8 Lead TSSOP	Tube	-40°C to 85°C
830154BGI-09T	4BI09	8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
830154BGI-09LF	BI09L	Lead-Free, 8 Lead TSSOP	Tube	-40°C to 85°C
830154BGI-09LFT	BI09L	Lead-Free, 8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
830154BMI-09	0154BI09	8 Lead SOIC	Tube	-40°C to 85°C
830154BMI-09T	0154BI09	8 Lead SOIC	2500 Tape & Reel	-40°C to 85°C
830154BMI-09LF	154BI09L	Lead-Free, 8 Lead SOIC	Tube	-40°C to 85°C
830154BMI-09LFT	154BI09L	Lead-Free, 8 Lead SOIC	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Pin Assignments - corrected part numbers.	6/9/10

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