



12-OUTPUT LOW POWER DIFFERENTIAL BUFFER FOR PCIE GEN1/2/3 AND QPI 9ZXL1231

General Description

The 9ZXL1231 is a low power 12-output differential buffer that meets all the performance requirements of the Intel DB1900Z specification. It is pin compatible to the 9ZX21201. The 9ZXL1231 is backwards compatible to PCIe Gen2 and QPI 6.4GT/s specifications. A fixed, internal feedback path maintains low drift for critical QPI applications.

Recommended Application

12-Output Low Power Differential Buffer for PCIe Gen1/2/3 & QPI

Output Features

- 12 - 0.7V low-power HCSL-compatible output pairs

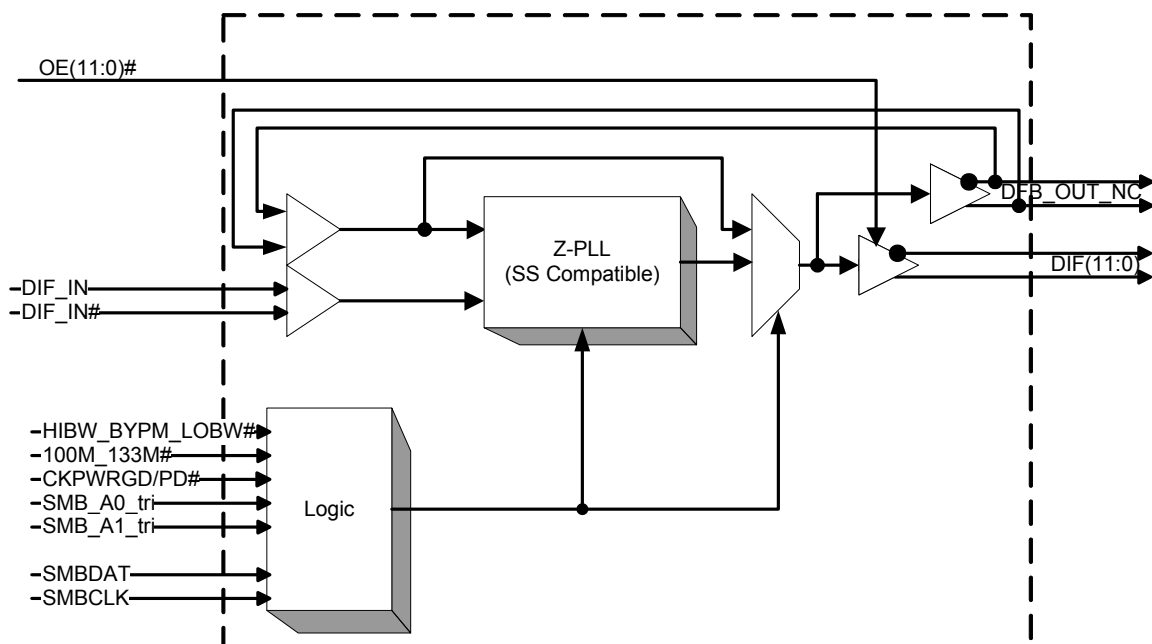
Features/Benefits

- Low-power push-pull outputs; Save power and board space - no Rp
- Pin compatible to 9ZX21201; easy path to >50% power savings
- Space-saving 64-pin QFN package
- Fixed feedback path for Ops input-to-output delay
- 9 Selectable SMBus Addresses; Multiple devices can share the same SMBus Segment
- 12 OE# pins; Hardware control of each output
- PLL or bypass mode; PLL can dejitter incoming clock
- 100MHz or 133MHz PLL mode operation; supports PCIe and QPI applications
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible; tracks spreading input clock for low EMI

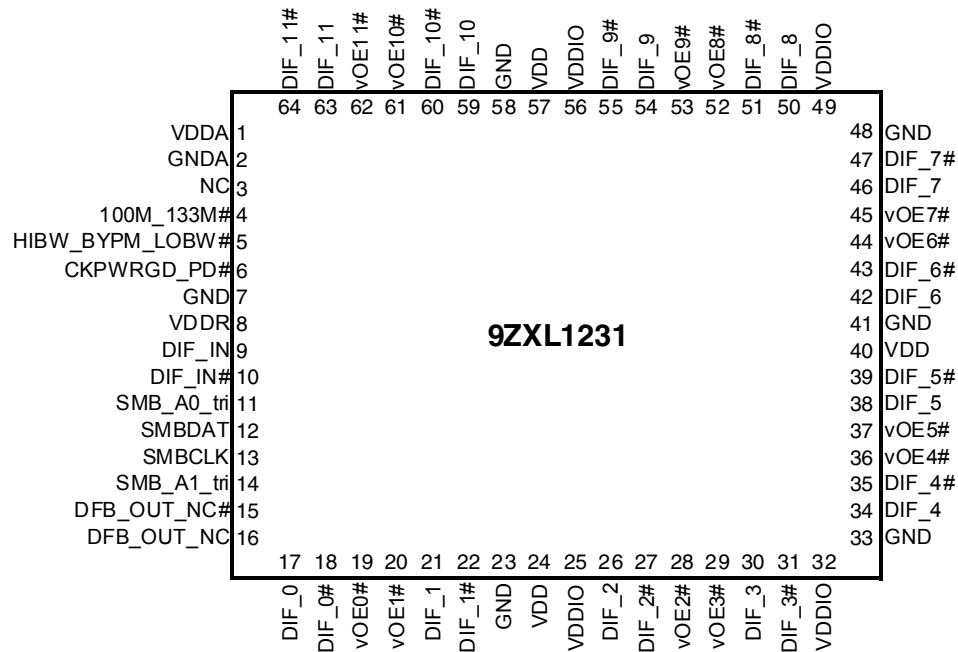
Key Specifications

- Cycle-to-cycle jitter <50ps
- Output-to-output skew <65 ps
- Input-to-output delay variation <50ps
- PCIe Gen3 phase jitter <1.0ps RMS
- QPI 9.6GT/s 12UI phase jitter <0.2ps RMS

Block Diagram



Pin Configuration



Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown

Power Management Table

| CKPWRGD_PD# | DIF_IN/ DIF_IN# | SMBus EN bit | DIF(11:0)/ DIF(1:0)# | PLL STATE IF NOT IN BYPASS MODE |
|-------------|--------------------|-----------------|-------------------------|--|
| 0 | X | X | Low/Low | OFF |
| 1 | Running | 0 | Low/Low | ON |
| | | 1 | Running | ON |

Functionality at Power-up (PLL mode)

| 100M_133M# | DIF_IN MHz | DIF(11:0) |
|------------|---------------|-----------|
| 1 | 100.00 | DIF_IN |
| 0 | 133.33 | DIF_IN |

Power Connections

| Pin Number | | | Description |
|------------|-------------|----------------|--------------|
| VDD | VDDIO | GND | |
| 1 | | 2 | Analog PLL |
| 8 | | 7 | Analog Input |
| 24,40,57 | 25,32,49,56 | 23,33,41,48,58 | DIF clocks |

PLL Operating Mode Readback Table

| HiBW_BypM_LoBW# | Byte0, bit 7 | Byte 0, bit 6 |
|-----------------|--------------|---------------|
| Low (Low BW) | 0 | 0 |
| Mid (Bypass) | 0 | 1 |
| High (High BW) | 1 | 1 |

Tri-Level Input Thresholds

| Level | Voltage |
|-------|--------------|
| Low | <0.8V |
| Mid | 1.2<Vin<1.8V |
| High | Vin > 2.2V |

PLL Operating Mode

| HiBW_BypM_LoBW# | MODE |
|-----------------|-----------|
| Low | PLL Lo BW |
| Mid | Bypass |
| High | PLL Hi BW |

NOTE: PLL is OFF in Bypass Mode

9ZXL1231 SMBus Addressing

| Pin | | SMBus Address |
|------------|------------|---------------|
| SMB_A1_tri | SMB_A0_tri | |
| 0 | 0 | D8 |
| 0 | M | DA |
| 0 | 1 | DE |
| M | 0 | C2 |
| M | M | C4 |
| M | 1 | C6 |
| 1 | 0 | CA |
| 1 | M | CC |
| 1 | 1 | CE |

Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------------|------|--|
| 1 | VDDA | PWR | 3.3V power for the PLL core. |
| 2 | GNDA | PWR | Ground pin for the PLL core. |
| 3 | NC | N/A | No Connection. |
| 4 | 100M_133M# | IN | 3.3V Input to select operating frequency. See Functionality Table for Definition |
| 5 | HIBW_BYPM_LOBW# | IN | Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details. |
| 6 | CKPWRGD_PD# | IN | 3.3V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. |
| 7 | GND | PWR | Ground pin. |
| 8 | VDDR | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| 9 | DIF_IN | IN | 0.7 V Differential TRUE input |
| 10 | DIF_IN# | IN | 0.7 V Differential Complementary Input |
| 11 | SMB_A0_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus Addresses. |
| 12 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 13 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 14 | SMB_A1_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus Addresses. |
| 15 | DFB_OUT_NC# | OUT | Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package. |
| 16 | DFB_OUT_NC | OUT | True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package. |
| 17 | DIF_0 | OUT | 0.7V differential true clock output |
| 18 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 19 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down resistor. 1 =disable outputs, 0 = enable outputs |
| 20 | vOE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 21 | DIF_1 | OUT | 0.7V differential true clock output |
| 22 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 23 | GND | PWR | Ground pin. |
| 24 | VDD | PWR | Power supply, nominal 3.3V |
| 25 | VDDIO | PWR | Power supply for differential outputs |
| 26 | DIF_2 | OUT | 0.7V differential true clock output |
| 27 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 28 | vOE2# | IN | Active low input for enabling DIF pair 2. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 29 | vOE3# | IN | Active low input for enabling DIF pair 3. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 30 | DIF_3 | OUT | 0.7V differential true clock output |
| 31 | DIF_3# | OUT | 0.7V differential Complementary clock output |
| 32 | VDDIO | PWR | Power supply for differential outputs |
| 33 | GND | PWR | Ground pin. |
| 34 | DIF_4 | OUT | 0.7V differential true clock output |
| 35 | DIF_4# | OUT | 0.7V differential Complementary clock output |
| 36 | vOE4# | IN | Active low input for enabling DIF pair 4. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 37 | vOE5# | IN | Active low input for enabling DIF pair 5. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |

Pin Descriptions (cont.)

| | | | |
|----|---------|-----|---|
| 38 | DIF_5 | OUT | 0.7V differential true clock output |
| 39 | DIF_5# | OUT | 0.7V differential Complementary clock output |
| 40 | VDD | PWR | Power supply, nominal 3.3V |
| 41 | GND | PWR | Ground pin. |
| 42 | DIF_6 | OUT | 0.7V differential true clock output |
| 43 | DIF_6# | OUT | 0.7V differential Complementary clock output |
| 44 | vOE6# | IN | Active low input for enabling DIF pair 6. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 45 | vOE7# | IN | Active low input for enabling DIF pair 7. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 46 | DIF_7 | OUT | 0.7V differential true clock output |
| 47 | DIF_7# | OUT | 0.7V differential Complementary clock output |
| 48 | GND | PWR | Ground pin. |
| 49 | VDDIO | PWR | Power supply for differential outputs |
| 50 | DIF_8 | OUT | 0.7V differential true clock output |
| 51 | DIF_8# | OUT | 0.7V differential Complementary clock output |
| 52 | vOE8# | IN | Active low input for enabling DIF pair 8. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 53 | vOE9# | IN | Active low input for enabling DIF pair 9. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 54 | DIF_9 | OUT | 0.7V differential true clock output |
| 55 | DIF_9# | OUT | 0.7V differential Complementary clock output |
| 56 | VDDIO | PWR | Power supply for differential outputs |
| 57 | VDD | PWR | Power supply, nominal 3.3V |
| 58 | GND | PWR | Ground pin. |
| 59 | DIF_10 | OUT | 0.7V differential true clock output |
| 60 | DIF_10# | OUT | 0.7V differential Complementary clock output |
| 61 | vOE10# | IN | Active low input for enabling DIF pair 10. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 62 | vOE11# | IN | Active low input for enabling DIF pair 11. This pin has an internal pull-down 1 =disable outputs, 0 = enable outputs |
| 63 | DIF_11 | OUT | 0.7V differential true clock output |
| 64 | DIF_11# | OUT | 0.7V differential Complementary clock output |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL1231. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDD, VDDA, VDDR | VDD for core logic and PLL | | | 4.6 | V | 1,2 |
| IO Supply Voltage | VDD_IO | VDD for differential IO | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics—Clock Input Parameters

T_A = T_{COM}; Supply Voltage V_{DD} = 3.3 V +/-5%, VDD_IO = 1.05 to 3.3V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|--------------------|---|-----------------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN | V _{IHDIF} | Differential inputs (single-ended measurement) | 600 | 800 | 1150 | mV | 1 |
| Input Low Voltage - DIF_IN | V _{ILDIF} | Differential inputs (single-ended measurement) | V _{SS} - 300 | 0 | 300 | mV | 1 |
| Input Common Mode Voltage - DIF_IN | V _{COM} | Common Mode Input Voltage | 300 | | 1000 | mV | 1 |
| Input Amplitude - DIF_IN | V _{SWING} | Peak to Peak value (single-ended measurement) | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | 1 |
| Input Duty Cycle | d _{tin} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFIn} | Differential Measurement | 0 | | 125 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Input/Supply/Common Output Parameters

$T_A = T_{COM}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DD_IO} = 1.05\text{ to }3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|-----------------|---|-------------|--------|----------------|--------|
| Ambient Operating Temperature | T_{COM} | Commercial range | 0 | | 70 | °C |
| Input High Voltage | V_{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | | $V_{DD} + 0.3$ | V |
| Input Low Voltage | V_{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | $GND - 0.3$ | | 0.8 | V |
| Input Current | I_{IN} | Single-ended inputs, $V_{IN} = GND$, $V_{IN} = V_{DD}$ | -5 | | 5 | µA |
| | I_{INP} | Single-ended inputs $V_{IN} = 0\text{ V}$; Inputs with internal pull-up resistors $V_{IN} = V_{DD}$; Inputs with internal pull-down resistors | -200 | | 200 | µA |
| Input Frequency | F_{ibyp} | $V_{DD} = 3.3\text{ V}$, Bypass mode | 33 | | 150 | MHz |
| | F_{ipll} | $V_{DD} = 3.3\text{ V}$, 100MHz PLL mode | 90 | 100.00 | 110 | MHz |
| | F_{ipll} | $V_{DD} = 3.3\text{ V}$, 133.33MHz PLL mode | 120 | 133.33 | 147 | MHz |
| Pin Inductance | L_{pin} | | | | 7 | nH |
| Capacitance | C_{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF |
| | C_{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF |
| | C_{OUT} | Output pin capacitance | | | 6 | pF |
| Clk Stabilization | T_{STAB} | From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.250 | 1 | ms |
| Input SS Modulation Frequency | f_{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | | 33 | kHz |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion DIF stop after OE# deassertion | 4 | | 12 | cycles |
| Tdrive_PD# | t_{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | µs |
| Tfall | t_F | Fall time of control inputs | | | 10 | ns |
| Trise | t_R | Rise time of control inputs | | | 10 | ns |
| SMBus Input Low Voltage | V_{ILSMB} | | | | 0.8 | V |
| SMBus Input High Voltage | V_{IHSMB} | | 2.1 | | V_{DDSMB} | V |
| SMBus Output Low Voltage | V_{OLSMB} | @ I_{PULLUP} | | | 0.4 | V |
| SMBus Sink Current | I_{PULLUP} | @ V_{OL} | 4 | | | mA |
| Nominal Bus Voltage | V_{DDSMB} | 3V to 5V +/- 10% | 2.7 | | 5.5 | V |
| SCLK/SDATA Rise Time | t_{RSMB} | (Max $V_{IL} - 0.15$) to (Min $V_{IH} + 0.15$) | | | 1000 | ns |
| SCLK/SDATA Fall Time | t_{FSMB} | (Min $V_{IH} + 0.15$) to (Max $V_{IL} - 0.15$) | | | 300 | ns |
| SMBus Operating Frequency | f_{MAXSMB} | Maximum SMBus operating frequency | | | 100 | kHz |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴DIF_IN input

⁵The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF 0.7V Low Power Differential Outputs

$T_A = T_{COM}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DD_IO} = 1.05\text{ to }3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------|---|------|------|------|-------|---------|
| Slew rate | Trf | Scope averaging on | 1 | 3.3 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | 7 | 20 | % | 1, 2, 4 |
| Voltage High | VHigh | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 778 | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | 0 | 150 | | 1 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 868 | 1150 | mV | 1 |
| Min Voltage | Vmin | | -300 | -64 | | | 1 |
| Vswing | Vswing | Scope averaging off | 300 | 1556 | | mV | 1, 2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 300 | 430 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | Δ -Vcross | Scope averaging off | | 17 | 140 | mV | 1, 6 |

¹Guaranteed by design and characterization, not 100% tested in production. $C_L = 2\text{pF}$ with $R_S = 27\Omega$ for $Z_0 = 85\Omega$ differential trace impedance).

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ -Vcross to be smaller than Vcross absolute.

Electrical Characteristics–Current Consumption

$T_A = T_{COM}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DD_IO} = 1.05\text{ to }3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------|-----------------|--|-----|------|-----|-------|-------|
| Operating Current | I_{DDVDD} | 133MHz, VDD rail | | 18 | 25 | mA | 1 |
| | I_{DDVDDA} | 133MHz, VDDA + VDDR rail, PLL Mode | | 16 | 20 | mA | 1 |
| | $I_{DDVDDIO}$ | 133MHz, $C_L = \text{Full load}$; VDD IO rail | | 101 | 110 | mA | 1 |
| Powerdown Current | $I_{DDVDDPD}$ | Power Down, VDD Rail | | 0.01 | 1 | mA | 1 |
| | $I_{DDVDDAPD}$ | Power Down, VDDA Rail | | 3 | 5 | mA | 1 |
| | $I_{DDVDDIOPD}$ | Power Down, VDD_IO Rail | | 0.01 | 0.2 | mA | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

² $C_L = 2\text{pF}$ with $R_S = 27\Omega$ for $Z_0 = 85\Omega$ differential trace impedance

Electrical Characteristics—Skew and Differential Jitter Parameters

$T_A = T_{COM}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DD_IO} = 1.05\text{ to }3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|-----------------|--|------|------|-----|----------|-----------|
| CLK_IN, DIF[x:0] | t_{SPO_PLL} | Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V | -100 | -60 | 100 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0] | t_{PD_BYP} | Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V | 2.5 | 3.2 | 4.5 | ns | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t_{DSPO_PLL} | Input-to-Output Skew Variation in PLL mode across voltage and temperature | -50 | 0 | 50 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t_{DSPO_BYP} | Input-to-Output Skew Variation in Bypass mode across voltage and temperature | -250 | | 250 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t_{DTE} | Random Differential Tracking error between two 9ZX devices in Hi BW Mode | | 3 | 5 | ps (rms) | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t_{DSSTE} | Random Differential Spread Spectrum Tracking error between two 9ZX devices in Hi BW Mode | | 10 | 75 | ps | 1,2,3,5,8 |
| DIF[x:0] | t_{SKEW_ALL} | Output-to-Output Skew across all outputs (Common to Bypass and PLL mode) | | 21 | 65 | ps | 1,2,3,8 |
| PLL Jitter Peaking | $j_{peak-hibw}$ | LOBW#_BYPASS_HIBW = 1 | 0 | 1.2 | 2.5 | dB | 7,8 |
| PLL Jitter Peaking | $j_{peak-lobw}$ | LOBW#_BYPASS_HIBW = 0 | 0 | 0.8 | 2 | dB | 7,8 |
| PLL Bandwidth | pl_{HIBW} | LOBW#_BYPASS_HIBW = 1 | 2 | 3 | 4 | MHz | 8,9 |
| PLL Bandwidth | pl_{LOBW} | LOBW#_BYPASS_HIBW = 0 | 0.7 | 1.1 | 1.4 | MHz | 8,9 |
| Duty Cycle | t_{DC} | Measured differentially, PLL Mode | 45 | 50.1 | 55 | % | 1 |
| Duty Cycle Distortion | t_{DCD} | Measured differentially, Bypass Mode @ 100MHz | -2 | -0.6 | 2 | % | 1,10 |
| Jitter, Cycle to cycle | $t_{cyc-cyc}$ | PLL mode | | 34 | 50 | ps | 1,11 |
| | | Additive Jitter in Bypass Mode | | 5 | 50 | ps | 1,11 |

Notes for preceding table:

- ¹ $C_L = 2\text{ pF}$ with $R_S = 27\Omega$ for $Z_o = 85\Omega$ differential trace impedance. Input to output skew is measured at the first output edge following the corresponding input.
- ² Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.
- ³ All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
- ⁴ This parameter is deterministic for a given device
- ⁵ Measured with scope averaging on to find mean value.
- ⁶ t is the period of the input clock
- ⁷ Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
- ⁸ Guaranteed by design and characterization, not 100% tested in production.
- ⁹ Measured at 3 db down or half power point.
- ¹⁰ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
- ¹¹ Measured from differential waveform

Electrical Characteristics–Phase Jitter Parameters

$T_A = T_{COM}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DD_IO} = 1.05\text{ to }3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------------------------|-------------------|--|-----|------|-----|----------|---------|
| Phase Jitter, PLL Mode | $t_{jphPCIEG1}$ | PCIe Gen 1 | | 34 | 86 | ps (p-p) | 1,2,3 |
| | $t_{jphPCIEG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 1.2 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 2.2 | 3.1 | ps (rms) | 1,2 |
| | $t_{jphPCIEG3}$ | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.5 | 1 | ps (rms) | 1,2,4 |
| | t_{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.24 | 0.5 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.14 | 0.3 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.12 | 0.2 | ps (rms) | 1,5 |
| Additive Phase Jitter, Bypass mode | $t_{jphPCIEG1}$ | PCIe Gen 1 | | 3.7 | 10 | ps (p-p) | 1,2,3 |
| | $t_{jphPCIEG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.1 | 0.3 | ps (rms) | 1,2,6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.4 | 0.6 | ps (rms) | 1,2,6 |
| | $t_{jphPCIEG3}$ | PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz) | | 0.09 | 0.2 | ps (rms) | 1,2,4,6 |
| | t_{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.14 | 0.2 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.01 | 0.1 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.01 | 0.1 | ps (rms) | 1,5,6 |

¹ Applies to all outputs.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final radification by PCI SIG.

⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.3

⁶ For RMS figures, additive jitter is calculated by solving the following equation: $(\text{Additive jitter})^2 = (\text{total jitter})^2 - (\text{input jitter})^2$

Clock Periods–Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|
| | | 1 Clock | 1 μ s | 0.1s | 0.1s | 0.1s | 1 μ s | 1 Clock | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | |
| DIF | 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns |
| | 133.33 | 7.44925 | | 7.49925 | 7.50000 | 7.50075 | | 7.55075 | ns |

Clock Periods–Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1 μ s | 0.1s | 0.1s | 0.1s | 1 μ s | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2,3 |
| | 133.00 | 7.44930 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.58830 | ns | 1,2,4 |

Notes:

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZXL1231 itself does not contribute to ppm error.

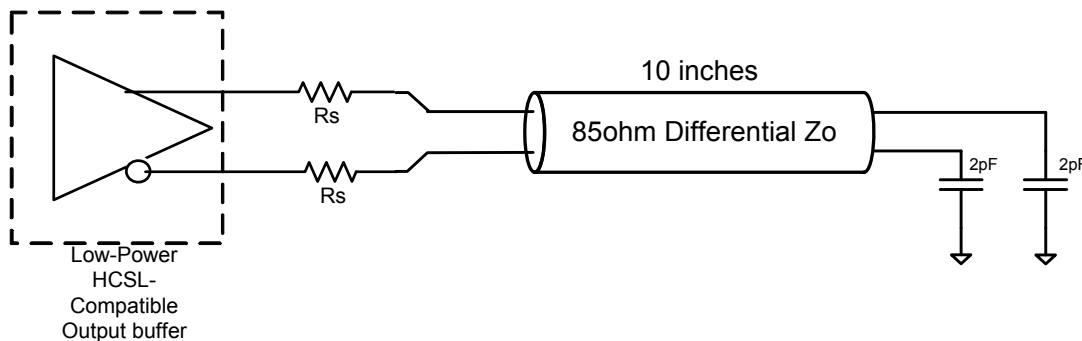
³ Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

⁴ Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

Differential Output Terminations

| DIF Zo (Ω) | Rs (Ω) |
|---------------------|-----------------|
| 100 | 33 |
| 85 | 27 |

9ZXL Differential Test Loads



General SMBus Serial Interface Information for 9ZXL1231

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Data Byte Count = X | | ACK |
| Beginning Byte N | | ACK |
| O | X Byte | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | ACK |
| P | stoP bit | |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Repeat starT | | ACK |
| Slave Address | | |
| RD | ReaD | |
| Data Byte Count=X | | ACK |
| Beginning Byte N | | ACK |
| ACK | | X Byte |
| ACK | | |
| O | | |
| O | | |
| O | | |
| O | | |
| Byte N + X - 1 | | |
| N | Not acknowledge | |
| P | stoP bit | |

SMBusTable: PLL Mode, and Frequency Select Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------------|------------------------------|------|------------------------|---------------|---------|
| Bit 7 | 5 | PLL Mode 1 | PLL Operating Mode Rd back 1 | R | See PLL Operating Mode | | Latch |
| Bit 6 | 5 | PLL Mode 0 | PLL Operating Mode Rd back 0 | R | Readback Table | | Latch |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | PLL_SW_EN | Enable SW control of PLL BW | RW | HW Latch | SMBus Control | 0 |
| Bit 2 | | PLL Mode 1 | PLL Operating Mode 1 | RW | See PLL Operating Mode | | 1 |
| Bit 1 | | PLL Mode 0 | PLL Operating Mode 1 | RW | Readback Table | | 1 |
| Bit 0 | 4 | 100M_133M# | Frequency Select Readback | R | 133MHz | 100MHz | Latch |

Note: Setting bit 3 to '1' allows the user to override the Latch value from pin 5 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Bits 7 and 6 will keep the value originally latched on pin 5. A warm reset of the system will have to be accomplished if the user changes these bits.

SMBusTable: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|--|------|---------|--------|---------|
| Bit 7 | 47/46 | DIF_7_En | Output Control - '0' overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 6 | 43/42 | DIF_6_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 5 | 39/38 | DIF_5_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 4 | 35/34 | DIF_4_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 3 | 30/31 | DIF_3_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 2 | 26/27 | DIF_2_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 1 | 21/22 | DIF_1_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 0 | 17/18 | DIF_0_En | Output Control - '0' overrides OE# pin | RW | | | 1 |

SMBusTable: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------|--|------|---------|--------|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | 64/63 | DIF_11_En | Output Control - '0' overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 2 | 59/60 | DIF_10_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 1 | 54/55 | DIF_9_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 0 | 50/51 | DIF_8_En | Output Control - '0' overrides OE# pin | RW | | | 1 |

SMBusTable: Reserved Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBusTable: Reserved Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBusTable: Vendor & Revision ID Register

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|--------------|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | A rev = 0000 | | X |
| Bit 6 | - | RID2 | | R | | | X |
| Bit 5 | - | RID1 | | R | | | X |
| Bit 4 | - | RID0 | | R | | | X |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBusTable: DEVICE ID

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|-------------------|------|----------------------------------|---|---------|
| Bit 7 | - | | Device ID 7 (MSB) | R | 1231 is 231 Decimal or E7 Hex | | 1 |
| Bit 6 | - | | Device ID 6 | R | | | 1 |
| Bit 5 | - | | Device ID 5 | R | | | 1 |
| Bit 4 | - | | Device ID 4 | R | | | 0 |
| Bit 3 | - | | Device ID 3 | R | | | 0 |
| Bit 2 | - | | Device ID 2 | R | | | 1 |
| Bit 1 | - | | Device ID 1 | R | | | 1 |
| Bit 0 | - | | Device ID 0 | R | | | 1 |

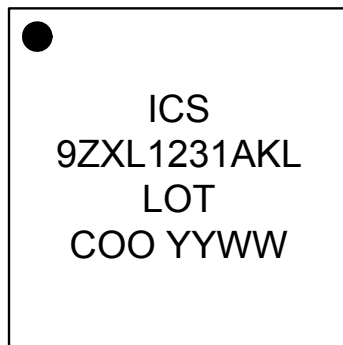
SMBusTable: Byte Count Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | - | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 0 |

SMBusTable: Reserved Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

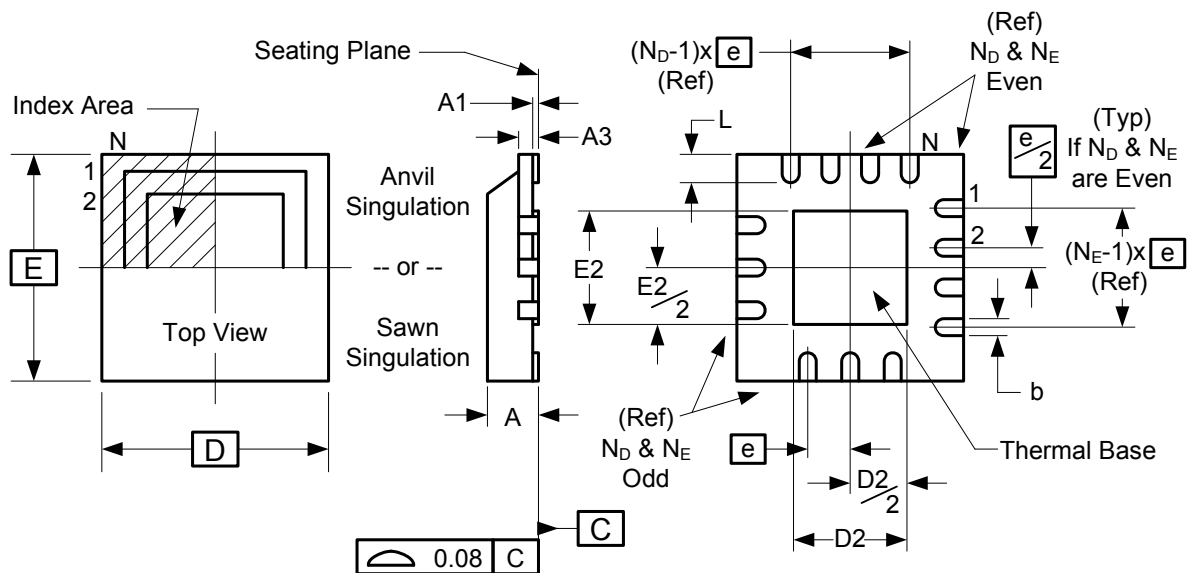
Marking Diagram



Notes:

1. "L" denotes RoHS compliant package.
2. 'LOT' denotes the lot number.
3. "COO": country of origin.
4. YYWW is the last two digits of the year and week that the part was assembled.

Package Outline and Package Dimensions (64-pin MLF)



| Symbol | Millimeters | |
|----------------|----------------|------|
| | Min | Max |
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |
| D x E BASIC | 9.00 x 9.00 | |
| D2 MIN./MAX. | 6.00 | 6.25 |
| E2 MIN./MAX. | 6.00 | 6.25 |
| L MIN./MAX. | 0.30 | 0.50 |
| N | 64 | |
| N _D | 16 | |
| N _E | 16 | |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|------------|-------------|
| 9ZXL1231AKLF | see page 15 | Trays | 64-pin MLF | 0 to +70° C |
| 9ZXL1231AKLFT | | Tape and Reel | 64-pin MLF | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History

| Rev. | Issuer | Issue Date | Description | Page # |
|------|--------|------------|--|---------------|
| A | RDW | 4/14/2011 | <ol style="list-style-type: none"> Updated Byte 0, PD# current and OE# Latency specs. Updated electrical tables with Characterization Data. Move to Final Corrected Pin Description, pin 37 was missing Corrected Pin 5 in pinout. Name was truncated. | |
| B | RDW | 8/3/2011 | <ol style="list-style-type: none"> Functionality added to Byte 0 [3:1]. Byte 0, bit 3 enables SW control of PLL BW and Bypass mode. Byte 0[2:1] is read write to mimic the readback status of Byte 0[7:6]. See SMBus table. | |
| C | RDW | 12/8/2011 | <ol style="list-style-type: none"> Changed Output Features description Fixed alignment issue in Power Connections Table - cosmetic fix, table information was and is correct. Updated tDSPO_BYP to +/-250ps Updated Differential Test Loads Figure to indicate impedance and trace length. Removed SMBus Address info on page 12, SMBus address is selectable as indicated on page 3. Added revised downward in Current Consumption Table | 1,2,8,9,11,12 |
| D | RDW | 4/9/2012 | <ol style="list-style-type: none"> Corrected Power Connections table, first column, last row. VDD for DIF clocks are pins 24, 40 and 57. | 2 |
| E | RDW | 5/11/2012 | <ol style="list-style-type: none"> Minor updates to some typical values in electrical tables, missing typical values added. DS title changed from "12-Output Low Power Differential Buffer for PCIe Gen3 and QPI" to "12-Output Low Power Differential Buffer for PCIe Gen1/2/3 and QPI" to emphasize backwards compatibility. Added comment to Vswing parameter on input clock to denote that the value is a single-ended value. Max IDDIO changed from 106mA to 110mA. | Various |

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

www.idt.com/go/clockhelp
pcclockhelp@idt.com

Corporate Headquarters

Integrated Device Technology, Inc.
www.idt.com

