ICS8702

LOW SKEW, ÷1, ÷2 DIFFERENTIAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS8702 is a low skew, ÷1, ÷2 Differential-to-LVCMOS Clock Generator. The ICS8702 is designed to translate any differential signal levels to LVCMOS/LVTTL levels. True or inverting, single-ended to LVCMOS translation can be achieved with a resistor bias on the nCLK or CLK inputs, respectively. The effective fan-out can be increased from 20 to 40 by utilizing the ability of the outputs to drive two series terminated lines.

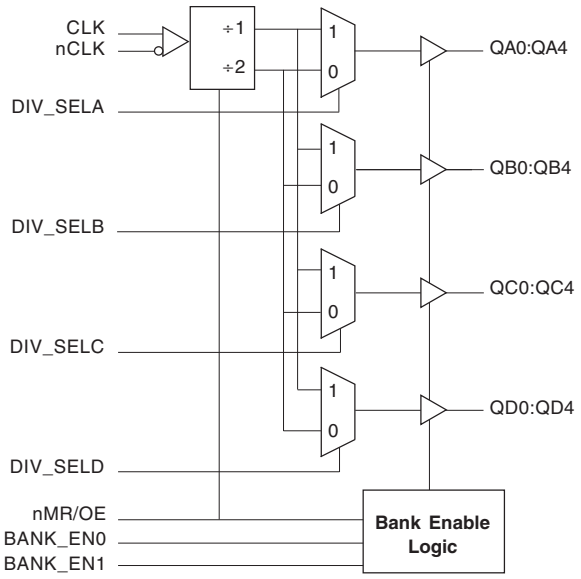
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The bank enable inputs, BANK_EN0:1, supports enabling and disabling each bank of outputs individually. The master reset input, nMR/OE, resets the internal frequency dividers and also controls the enabling and disabling of all outputs simultaneously.

The ICS8702 is characterized at 3.3V and mixed 3.3V input supply, and 2.5V output supply operating modes. Guaranteed bank, output, multiple frequency and part-to-part skew characteristics make the ICS8702 ideal for those clock dis-tribution applications demanding well defined performance and repeatability.

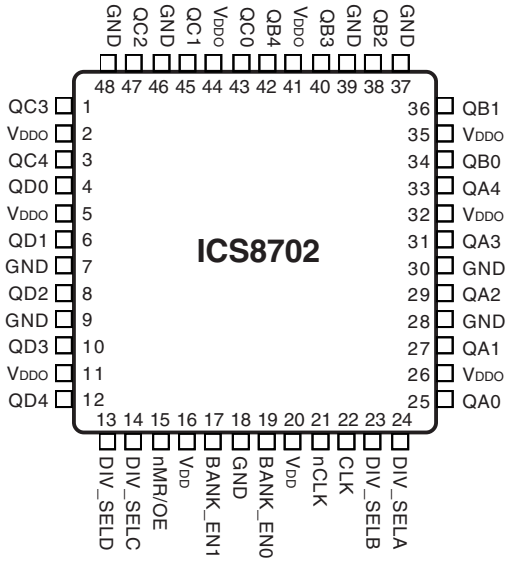
FEATURES

- Twenty LVCMOS outputs, 7Ω typical output impedance
- One differential clock input pair
- CLK, nCLK supports the following input types: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 250MHz
- Translates any differential input signal (LVPECL, LVHSTL, LVDS) to LVCMOS levels without external bias networks
- Translates any single-ended input signal to LVCMOS levels with a resistor bias on nCLK input
- Bank enable logic allows unused banks to be disabled in reduced fanout applications
- Output skew: 200ps (maximum)
- Bank skew: 150ps (maximum)
- Part-to-part skew: 650ps (maximum)
- Multiple frequency skew: 250ps (maximum)
- 3.3V or mixed 3.3V input, 2.5V output operating supply modes
- 0°C to 70°C ambient operating temperature
- Other divide values available on request
- Available in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
2, 5, 11, 26, 32, 35, 41, 44	V_{DDO}	Power		Output supply pins.
7, 9, 18, 28, 30, 37, 39, 46, 48	GND	Power		Output power supply.
16, 20	V_{DD}	Power		Positive supply pins.
25, 27, 29, 31, 33	QA0, QA1, QA2, QA3, QA4	Output		Bank A outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
34, 36, 38, 40, 42	QB0, QB1, QB2, QB3, QB4	Output		Bank B outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
43, 45, 47, 1, 3	QC0, QC1, QC2, QC3, QC4	Output		Bank C outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
4, 6, 8, 10, 12	QD0, QD1, QD2, QD3, QD4	Output		Bank D outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
22	CLK	Input	Pulldown	Non-inverting differential clock input.
21	nCLK	Input	Pullup	Inverting differential clock input.
13	DIV_SELD	Input	Pullup	Controls frequency division for Bank D outputs. LVCMOS/LVTTL interface levels.
14	DIV_SELC	Input	Pullup	Controls frequency division for Bank C outputs. LVCMOS/LVTTL interface levels.
23	DIV_SELB	Input	Pullup	Controls frequency division for Bank B outputs LVCMOS/LVTTL interface levels.
24	DIV_SELA	Input	Pullup	Controls frequency division for Bank A outputs. LVCMOS/LVTTL interface levels.
17, 19	BANK_EN1, BANK_EN0	Input	Pullup	Enables and disables outputs by banks. LVCMOS/LVTTL interface levels.
15	nMR/OE	Input	Pullup	Master Reset and output enable. When HIGH, output drivers are enabled. When LOW, output drivers are in HiZ and dividers are reset. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	$V_{DD} = V_{DDO} = 3.465V$			15	pF
R_{OUT}	Output Impedance			7		Ω

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs				
nMR/OE	BANK_EN1	BANK_EN0	DIV_SELx	QA0:QA4	QB0:QB4	QC0:QC4	QD0:QD4	Qx Frequency
0	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	zero
1	0	0	0	Enabled	Hi Z	Hi Z	Hi Z	fIN/2
1	1	0	0	Enabled	Enabled	Hi Z	Hi Z	fIN/2
1	0	1	0	Enabled	Enabled	Enabled	Hi Z	fIN/2
1	1	1	0	Enabled	Enabled	Enabled	Enabled	fIN/2
1	0	0	1	Enabled	Hi Z	Hi Z	Hi Z	fIN
1	1	0	1	Enabled	Enabled	Hi Z	Hi Z	fIN
1	0	1	1	Enabled	Enabled	Enabled	Hi Z	fIN
1	1	1	1	Enabled	Enabled	Enabled	Enabled	fIN

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs			Outputs	Input to Output Mode	Polarity
nMR/OE	CLK	nCLK	Qx0:Qx4		
1	0	1	LOW	Differential to Single Ended	Non Inverting
1	1	0	HIGH	Differential to Single Ended	Non Inverting
1	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
1	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
1	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
1	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting

NOTE 1: Please refer to the Application Information section, which discusses "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA =0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				95	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				95	mA

TABLE 4C. LVCMOS /LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA =0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE		-0.3		0.8	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		$V_{DD} = V_{DDO}$ = 3.135V I_{OH} = -36mA	2.6			V
V_{OL}	Output Low Voltage		$V_{DD} = V_{DDO}$ = 3.135V I_{OL} = 36mA			0.5	V

TABLE 4D. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE		-0.3		0.8	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		V_{DD} = 3.135V V_{DDO} = 2.375V I_{OL} = -27mA	1.9			V
V_{OL}	Output Low Voltage		V_{DD} = 3.135V V_{DDO} = 2.375V I_{OL} = 27mA			0.5	V

TABLE 4E. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5% OR 2.5V±5%, T_A =0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V			150	µA
		nCLK	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.8		2.4	V
			DCM, LVHSTL, LVDS, SSTL Levels	0.31		1.3	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK and nCLK is V_{DD} + 0.3V.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 200MHz	2.2		3.5	ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDO}/2$			150	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDO}/2$			200	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDO}/2$			250	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDO}/2$			650	ps
t_R	Output Rise Time; NOTE 6	30% to 70%	280		850	ps
t_F	Output Fall Time; NOTE 6	30% to 70%	280		850	ps
odc	Output Duty Cycle	f ≤ 200MHz	tCYCLE/2 - 0.5	tCYCLE/2	tCYCLE/2 + 0.5	ns
		f = 200MHz	2	2.5	3	ns
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz			6	ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz			6	ns

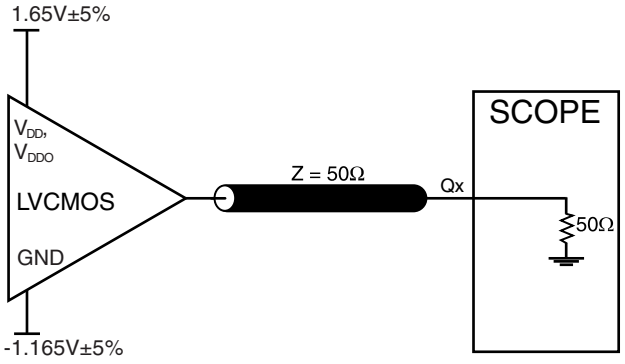
All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.
NOTE 5: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

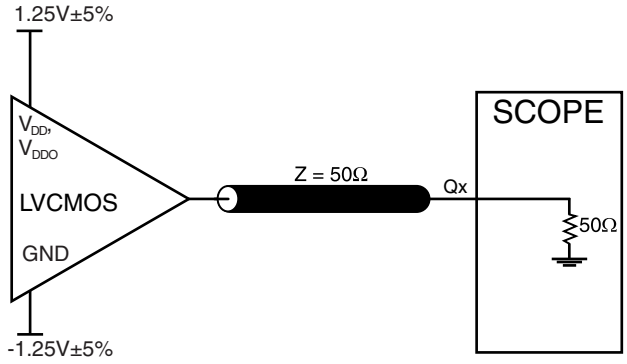
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 200MHz	2.3		3.6	ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on rising edge atV_{DDO}/2			150	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge atV_{DDO}/2			200	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge atV_{DDO}/2			250	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge atV_{DDO}/2			700	ps
t_R	Output Rise Time; NOTE 6	30% to 70%	280		850	ps
t_F	Output Fall Time; NOTE 6	30% to 70%	280		850	ps
odc	Output Duty Cycle	f ≤ 200MHz	tCYCLE/2 - 0.5	tCYCLE/2	tCYCLE/2 + 0.5	ns
		f = 200MHz	2	2.5	3	ns
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz			6	ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz			6	ns

All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at V_{DDO}/2.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.
NOTE 5: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

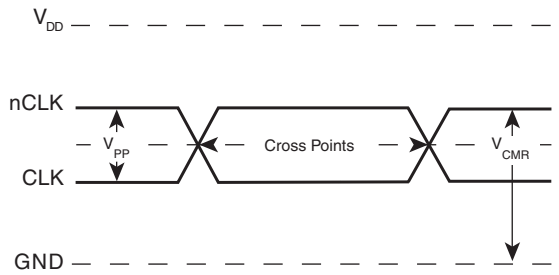
PARAMETER MEASUREMENT INFORMATION



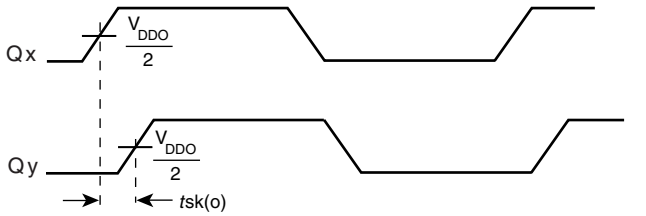
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



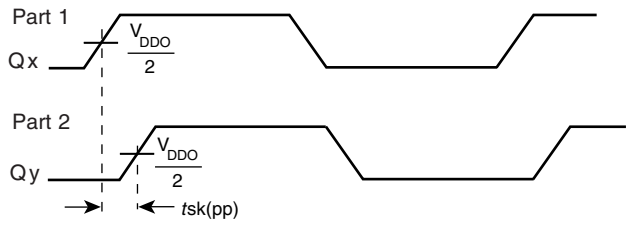
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



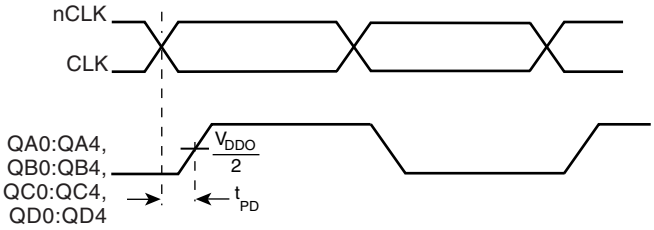
DIFFERENTIAL INPUT LEVEL



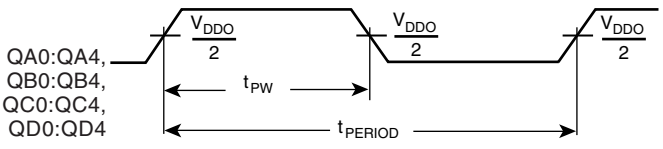
OUTPUT SKEW



PART-TO-PART SKEW

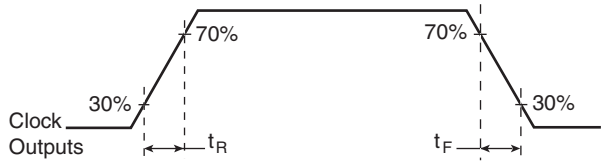


PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

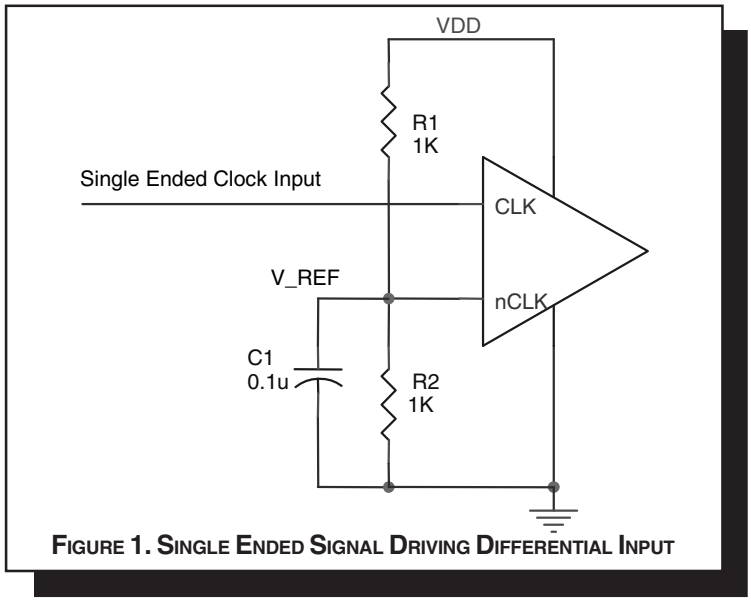


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUT:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

POWER CONSIDERATIONS

For Power Dissipation, please refer to a separate Application Note: *Power Dissipation for LVCMOS Buffer.*

DRIVER TERMINATION

For LVCMOS Output Termination, please refer to a separate Application Note: *LVCMOS Driver Termination.*

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 48 LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8702 is: 1746

PACKAGE OUTLINE - Y SUFFIX FOR 48 LQFP

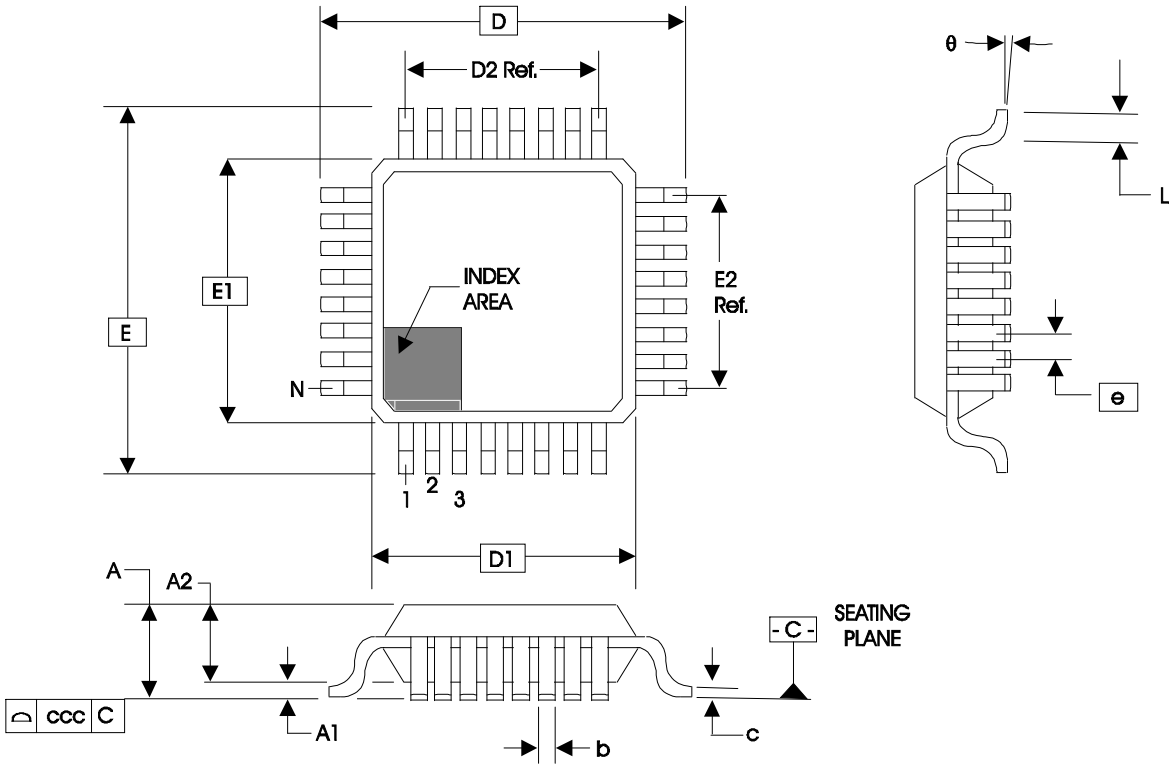


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8702BY	ICS8702BY	48 Lead LQFP	tray	0°C to 70°C
8702BYT	ICS8702BY	48 Lead LQFP	1000 tape & reel	0°C to 70°C
8702BYLF	ICS8702BYLF	48 Lead "Lead-Free" LQFP	tray	0°C to 70°C
8702BYLFT	ICS8702BYLF	48 Lead "Lead-Free" LQFP	1000 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	4A 4D	4 6	Revised IDD row from 70mA Maximum to 95mA Maximum. Revised IDD row from 70mA Maximum to 95mA Maximum.	8/2/01
C	4B 4E	4 6 11	Revised V_{IH} row from 3.8 Maximum to V_{DD} + 0.3 Maximum. Revised V_{IH} row from 3.8 Maximum to V_{DD} + 0.3 Maximum. Added Power Dissipation and Driver Termination notes.	11/28/01
C	1	2 10	Pin Description Table revised nMR/OE description. Updated Output Rise/Fall Time Diagram. Format changes.	8/21/02
D	T2	1 2 9 12	Features Section added Lead-Free bullet. Pin Characteristics Table - changed C_{IN} 4pF max to 4pF typical. Added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - added lead-free part number, marking, and note. Updated datasheet layout.	1/17/06
E	T9	12 12 14	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	7/25/10

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6024 Silver Creek Valley Road
San Jose, CA 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775

Tech Support
netcom@idt.com