DATASHEET

FOUR CHANNEL HD AUDIO CODEC

OPTIMIZED FOR LOW POWER/LOW COST

92HD95

DESCRIPTION

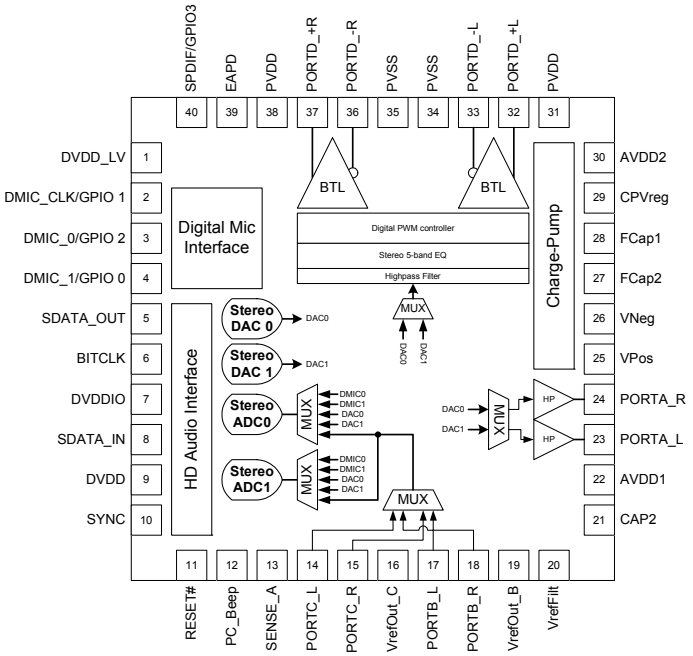
The 92HD95 is a low power optimized, high fidelity, 4-channel audio codec compatible with Intel's High Definition (HD) Audio Interface. The 92HD95 provides high quality, HD Audio capability to notebook and desktop PC applications.

FEATURES

- **4 Channel (2 stereo DACs, 2 stereo ADCs) with 24-bit resolution**
- **Microsoft WLP premium logo compliant**
- **2W(4ohm)/1W(8ohm) Class-D Stereo BTL Amplifier at <1% THD+N and 5V**
  - Selectable frequency hardware high-pass filter for speaker protection.
  - 10 band hardware parametric equalizer (5 bands per channel) for speaker optimization in ALL operating scenarios
  - Hardware compressor limiter allows higher average volume level without resonances or damage to speakers.
- **Integrated Class-G true capless stereo headphone amplifier with charge pump/LDO**
- **4 analog ports with port presence detect (3 single ended, 1 BTL)**
- **Combo Jack Support allowing for dual-function headphone and headset detection**
- **2 Voltage adjustable VREF_Out pins for microphone bias**
- **2 Digital microphone inputs (4 mic support)**
- **Microphone Mute Input**
- **Selectable 1.5V and 3.3V HDA signaling**
- **Internal DVDD LDO voltage regulator**
- **Supports Runtime D3 (RTD3) low power mode**
- **Capable of MSLync Compliance**
- **Full HDA015-B and EuP low power support**
  - Audio inactivity transitions codec from D0 to D3 low power mode
  - Resume from D3 to D0 with audio activity in < 10 msec
  - D3 to D0 transition with < -65dB pop/click
  - Port presence detect in D3 with or without bit clock
  - PC beep wake up in D3
  - Additional vendor specific modes for even lower power
- **3.3 V analog power supply**
- **Digital and Analog PC Beep to all outputs**
- **40-pin 5mm x 5mm QFN RoHS package**

SOFTWARE SUPPORT

- **Intuitive IDT HD Sound graphical user interface that allows configurability and preference settings**
- **Output Path Processing**
  - 12 band fully parametric equalizer
  - Compressor/limiter allows higher average volume level without resonances or damage to speakers.
    - Enables improved voice articulation
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode "presets" tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- **Input Path Processing**
  - 2 band fully parametric equalizer to allow for shaping of microphone response
  - Compressor/limiter allows higher average volume level
  - Available near-field and far-field voice capture algorithms to support conference room/lecture hall applications
  - Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- **IDT APO wrapper**
  - Enables multiple APOs to be used with the IDT Driver
- **Dynamic Stream Switching**
  - Improved multi-streaming (Real Time Communication) user experience with less support calls
- **Broad 3rd party branded software including Creative, Dolby, DTS, Waves, Sonic Focus & SRS**



©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

TABLE OF CONTENTS

1. DESCRIPTION 9
1.1. Overview 9
1.2. Orderable Part Numbers 9
2. DETAILED DESCRIPTION 10
2.1. Port Functionality 10
2.1.1. Port Characteristics 10
2.1.2. Vref_Out 11
2.1.3. Jack Detect 12
2.1.4. SPDIF Output 12
2.2. ADC Multiplexers 13
2.3. Power Management 13
2.4. AFG D0 14
2.5. AFG D1 14
2.6. AFG D2 15
2.7. AFG D3 15
2.7.1. AFG D3cold / RTD3 15
2.8. Vendor Specific Function Group Power States D4/D5 15
2.9. 4.12 Vendor Specific Function Group Power State “D5 Kill” 16
2.10. Low-voltage HDA Signaling 16
2.11. Multi-channel capture 16
2.12. EAPD 18
2.13. Digital Microphone Support 21
2.14. Analog PC-Beep 25
2.15. Digital PC-Beep 27
2.16. Headphone Drivers 28
2.17. Class-D BTL Amplifier 28
2.18. BTL Amplifier High-Pass Filter 28
2.18.1. Filter Description 29
2.19. EQ 29
2.20. Combo Jack Detection 29
2.21. GPIO 30
2.21.1. GPIO Pin mapping and shared functions 30
2.21.2. SPDIF/GPIO Selection 30
2.21.3. Digital Microphone/GPIO Selection 30
2.22. HD Audio HDA015-B support 30
2.23. Digital Core Voltage Regulator 31
2.24. Microphone Mute Input 31
3. CHARACTERISTICS 32
3.1. Electrical Specifications 32
3.1.1. Absolute Maximum Ratings 32
3.1.2. Recommended Operating Conditions 32
3.2. 92HD95 Analog Performance Characteristics 33
3.3. Class-D BTL Amplifier Performance 36
3.4. Capless Headphone Supply Characteristics 37
3.5. AC Timing Specs 37
3.5.1. HD Audio Bus Timing 37
3.5.2. SPDIF Timing 38
3.5.3. Digital Microphone Timing 38
3.5.4. GPIO Characteristics 38
4. FUNCTIONAL BLOCK DIAGRAM 39
5. WIDGET DIAGRAM 40
6. PORT AND PIN CONFIGURATIONS 41
6.1. Port Configurations 41
6.2. Pin Configuration Default Register Settings 42
7. WIDGET INFORMATION 43
7.1. Widget List 44
7.2. Reset Key 45

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.3. Root (NID = 00h): VendorID 45
7.3.1. Root (NID = 00h): VendorID 46
7.3.2. Root (NID = 00h): RevID 46
7.3.3. Root (NID = 00h): NodeInfo 47
7.4. AFG (NID = 01h): NodeInfo 47
7.4.1. AFG (NID = 01h): FGType 48
7.4.2. AFG (NID = 01h): AFGCap 48
7.4.3. AFG (NID = 01h): PCMCap 49
7.4.4. AFG (NID = 01h): StreamCap 51
7.4.5. AFG (NID = 01h): InAmpCap 51
7.4.6. AFG (NID = 01h): PwrStateCap 52
7.4.7. AFG (NID = 01h): GPIOCnt 53
7.4.8. AFG (NID = 01h): OutAmpCap 54
7.4.9. AFG (NID = 01h): PwrState 54
7.4.10. AFG (NID = 01h): UnsolResp 55
7.4.11. AFG (NID = 01h): GPIO 56
7.4.12. AFG (NID = 01h): GPIOEn 57
7.4.13. AFG (NID = 01h): GPIODir 57
7.4.14. AFG (NID = 01h): GPIOWakeEn 58
7.4.15. AFG (NID = 01h): GPIOUnsol 59
7.4.16. AFG (NID = 01h): GPIOSticky 59
7.4.17. AFG (NID = 01h): SubID 60
7.4.18. AFG (NID = 01h): GPIOPlrty 61
7.4.19. AFG (NID = 01h): GPIODrive 62
7.4.20. AFG (NID = 01h): DMic 62
7.4.21. AFG (NID = 01h): DACMode 63
7.4.22. AFG (NID = 01h): ADCMode 64
7.4.23. AFG (NID = 01h): EAPD 65
7.4.24. AFG (NID = 01h): PortUse 66
7.4.25. AFG (NID = 01h): ComJack 67
7.4.26. AFG (NID = 01h): ComboJackTime 68
7.4.27. AFG (NID = 01h): VSPwrState 70
7.4.28. AFG (NID = 01h): AnaPort 70
7.4.29. AFG (NID = 01h): AnaBeep 71
7.4.30. AFG (NID = 01h): AnaBTL 72
7.4.31. AFG (NID = 01h): AnaBTLStatus 74
7.4.32. AFG (NID = 01h): AnaCapless 75
7.4.33. AFG (NID = 01h): Reset 78
7.5. PortA (NID = 0Ah): WCap 79
7.5.1. PortA (NID = 0Ah): PinCap 80
7.5.2. PortA (NID = 0Ah): ConLst 81
7.5.3. PortA (NID = 0Ah): ConLstEntry0 82
7.5.4. PortA (NID = 0Ah): ConSelectCtrl 82
7.5.5. PortA (NID = 0Ah): PwrState 83
7.5.6. PortA (NID = 0Ah): PinWCntrl 84
7.5.7. PortA (NID = 0Ah): UnsolResp 84
7.5.8. PortA (NID = 0Ah): ChSense 85
7.5.9. PortA (NID = 0Ah): EAPDBTLLR 85
7.5.10. PortA (NID = 0Ah): ConfigDefault 86
7.6. PortB (NID = 0Bh): WCap 89
7.6.1. PortB (NID = 0Bh): PinCap 90
7.6.2. PortB (NID = 0Bh): InAmpLeft 91
7.6.3. PortB (NID = 0Bh): InAmpRight 92
7.6.4. PortB (NID = 0Bh): PwrState 92
7.6.5. PortB (NID = 0Bh): PinWCntrl 93
7.6.6. PortB (NID = 0Bh): UnsolResp 94
7.6.7. PortB (NID = 0Bh): ChSense 94
7.6.8. PortB (NID = 0Bh): EAPDBTLLR 95
7.6.9. PortB (NID = 0Bh): ConfigDefault 95

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.7. PortC (NID = 0Ch): WCap 98
7.7.1. PortC (NID = 0Ch): PinCap 99
7.7.2. PortC (NID = 0Ch): InAmpLeft 100
7.7.3. PortC (NID = 0Ch): InAmpRight 101
7.7.4. PortC (NID = 0Ch): PwrState 101
7.7.5. PortC (NID = 0Ch): PinWCntrl 102
7.7.6. PortC (NID = 0Ch): UnsolResp 103
7.7.7. PortC (NID = 0Ch): ChSense 103
7.7.8. PortC (NID = 0Ch): EAPDBTLLR 104
7.7.9. PortC (NID = 0Ch): ConfigDefault 104
7.8. PortD (NID = 0Dh): WCap 107
7.8.1. PortD (NID = 0Dh): PinCap 108
7.8.2. PortD (NID = 0Dh): ConLst 109
7.8.3. PortD (NID = 0Dh): ConLstEntry0 110
7.8.4. PortD (NID = 0Dh): ConSelectCtrl 110
7.8.5. PortD (NID = 0Dh): PwrState 111
7.8.6. PortD (NID = 0Dh): PinWCntrl 112
7.8.7. PortD (NID = 0Dh): EAPDBTLLR 112
7.8.8. PortD (NID = 0Dh): EsdRest 113
7.8.9. PortD (NID = 0Dh): ConfigDefault 113
7.9. DMic0 (NID = 0Eh): WCap 116
7.9.1. DMic0 (NID = 0Eh): PinCap 117
7.9.2. DMic0 (NID = 0Eh): InAmpLeft 118
7.9.3. DMic0 (NID = 0Eh): InAmpRight 119
7.9.4. DMic0 (NID = 0Eh): PwrState 119
7.9.5. DMic0 (NID = 0Eh): PinWCntrl 120
7.9.6. DMic0 (NID = 0Eh): ConfigDefault 121
7.10. DMic1 (NID = 0Fh): WCap 123
7.10.1. DMic1 (NID = 0Fh): PinCap 125
7.10.2. DMic1 (NID = 0Fh): InAmpLeft 126
7.10.3. DMic1 (NID = 0Fh): InAmpRight 127
7.10.4. DMic1 (NID = 0Fh): PwrState 127
7.10.5. DMic1 (NID = 0Fh): PinWCntrl 128
7.10.6. DMic1 (NID = 0Fh): ConfigDefault 128
7.11. DAC0 (NID = 10h): WCap 131
7.11.1. DAC0 (NID = 10h): Cnvtr 132
7.11.2. DAC0 (NID = 10h): OutAmpLeft 133
7.11.3. DAC0 (NID = 10h): OutAmpRight 134
7.11.4. DAC0 (NID = 10h): PwrState 134
7.11.5. DAC0 (NID = 10h): CnvtrID 135
7.11.6. DAC0 (NID = 10h): EAPDBTLLR 136
7.12. DAC1 (NID = 11h): WCap 136
7.12.1. DAC1 (NID = 11h): Cnvtr 138
7.12.2. DAC1 (NID = 11h): OutAmpLeft 139
7.12.3. DAC1 (NID = 11h): OutAmpRight 139
7.12.4. DAC1 (NID = 11h): PwrState 140
7.12.5. DAC1 (NID = 11h): CnvtrID 141
7.12.6. DAC1 (NID = 11h): EAPDBTLLR 141
7.13. ADC0 (NID = 12h): WCap 142
7.13.1. ADC0 (NID = 12h): ConLst 143
7.13.2. ADC0 (NID = 15h): ConLstEntry0 144
7.13.3. ADC0 (NID = 15h): Cnvtr 144
7.13.4. ADC0 (NID = 12h): ProcState 145
7.13.5. ADC0 (NID = 12h): PwrState 146
7.13.6. ADC0 (NID = 12h): CnvtrID 147
7.14. ADC1 (NID = 13h): WCap 147
7.14.1. ADC1 (NID = 13h): ConLst 149
7.14.2. ADC1 (NID = 13h): ConLstEntry0 149
7.14.3. ADC1 (NID = 13h): Cnvtr 150

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.14.4. ADC1 (NID = 13h): ProcState 151
7.14.5. ADC1 (NID = 13h): PwrState 152
7.14.6. ADC1 (NID = 1Bh): CnvtrID 153
7.15. ADC0Mux (NID = 14h): WCap 153
7.15.1. ADC0Mux (NID = 14h): ConLst 155
7.15.2. ADC0Mux (NID = 14h): ConLstEntry4 155
7.15.3. ADC0Mux (NID = 14h): ConLstEntry0 156
7.15.4. ADC0Mux (NID = 14h): OutAmpCap 156
7.15.5. ADC0Mux (NID = 14h): OutAmpLeft 157
7.15.6. ADC0Mux (NID = 14h): OutAmpRight 157
7.15.7. ADC0Mux (NID = 14h): ConSelectCtrl 158
7.15.8. ADC0Mux (NID = 14h): PwrState 158
7.15.9. ADC0Mux (NID = 14h): EAPDBTLLR 159
7.16. ADC1Mux (NID = 15h): WCap 160
7.16.1. ADC1Mux (NID = 15h): ConLst 161
7.16.2. ADC1Mux (NID = 15h): ConLstEntry4 162
7.16.3. ADC1Mux (NID = 15h): ConLstEntry0 162
7.16.4. ADC1Mux (NID = 15h): OutAmpCap 163
7.16.5. ADC1Mux (NID = 15h): OutAmpLeft 163
7.16.6. ADC1Mux (NID = 15h): OutAmpRight 164
7.16.7. ADC1Mux (NID = 15h): ConSelectCtrl 164
7.16.8. ADC1Mux (NID = 15h): PwrState 165
7.16.9. ADC1Mux (NID = 15h): EAPDBTLLR 166
7.17. PortMux (NID = 16h): WCap 166
7.17.1. PortMux (NID = 16h): ConLst 168
7.17.2. PortMux (NID = 16h): ConLstEntry0 168
7.17.3. PortMux (NID = 16h): ConSelectCtrl 169
7.17.4. PortMux (NID = 16h): PwrState 169
7.18. SPDIFOut0 (NID = 17h): WCap 170
7.18.1. SPDIFOut0 (NID = 17h): PCMCap 171
7.18.2. SPDIFOut0 (NID = 17h): StreamCap 173
7.18.3. SPDIFOut0 (NID = 17h): OutAmpCap 173
7.18.4. SPDIFOut0 (NID = 17h): Cnvtr 174
7.18.5. SPDIFOut0 (NID = 17h): OutAmpLeft 175
7.18.6. SPDIFOut0 (NID = 17h): OutAmpRight 176
7.18.7. SPDIFOut0 (NID = 1Dh): PwrState 176
7.18.8. SPDIFOut0 (NID = 17h): CnvtrID 177
7.18.9. SPDIFOut0 (NID = 17h): DigCnvtr 178
7.19. Dig0Pin (NID = 18h): WCap 179
7.19.1. Dig0Pin (NID = 18h): PinCap 180
7.19.2. Dig0Pin (NID = 18h): ConLst 181
7.19.3. Dig0Pin (NID = 18h): ConLstEntry0 182
7.19.4. Dig0Pin (NID = 18h): PwrState 182
7.19.5. Dig0Pin (NID = 18h): PinWCntrl 183
7.19.6. Dig0Pin (NID = 18h): UnsolResp 184
7.19.7. Dig0Pin (NID = 18h): ChSense 184
7.19.8. Dig0Pin (NID = 18h): ConfigDefault 185
7.20. DigBeep (NID = 19h): WCap 187
7.20.1. DigBeep (NID = 19h): OutAmpCap 188
7.20.2. DigBeep (NID = 19h): OutAmpLeft 189
7.20.3. DigBeep (NID = 19h): PwrState 190
7.20.4. DigBeep (NID = 19h): Gen 190
7.20.5. DigBeep (NID = 19h): Gain 191
7.21. AdvancedFunctions (NID = 1Ah): WCap 191
7.21.1. AdvancedFunctions (NID = 1Ah): Cntrl0 193
7.21.2. AdvancedFunctions (NID = 1Ah): Cntrl1 193
7.21.3. AdvancedFunctions (NID = 1Ah): Cntrl2 194
7.21.4. AdvancedFunctions (NID = 1Ah): Cntrl3 194
8. PINOUT AND PACKAGING 208

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

8.0.1. 40-QFN Pin Table 209
8.0.2. 40-QFN Package Outline and Package Dimensions 210
8.1. Standard Reflow Profile Data 211
9. DISCLAIMER 212
10. DOCUMENT REVISION HISTORY 212

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

LIST OF FIGURES

Figure 1. Multi-channel capture 17
Figure 2. Multi-channel timing diagram 17
Figure 3. HP EAPD Example to be replaced by single pin for internal amp 21
Figure 4. EAPD implementation 21
Figure 5. Single Digital Microphone (data is ported to both left and right channels 23
Figure 6. Stereo Digital Microphone Configuration 24
Figure 7. Quad Digital Microphone Configuration 25
Figure 8. Analog PC Beep Active 26
Figure 9. Analog PC Beep Flow chart 27
Figure 10. Combo Jack 29
Figure 11. HD Audio Bus Timing 37
Figure 12. Functional Block Diagram 39
Figure 13. Widget Diagram 40
Figure 14. Port Configurations 41
Figure 15. 40-QFN Pin Assignment 208
Figure 16. 40-QFN Package Diagram 210

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

LIST OF TABLES

Table 1. Port Functionality 10
Table 2. Analog Output Port Behavior 11
Table 3. Jack Detect 12
Table 4. SPDIF OUT 0 Behavior 12
Table 5. Power Management 14
Table 6. Example channel mapping 17
Table 8. EAPD Pin Mode Select 19
Table 9. Control bit descriptions for BTL amplifier and Headphone amplifier enable configurations 19
Table 10. BTL Amp Enable Configuration 19
Table 11. Headphone Amp Enable Configuration 19
Table 12. EAPD Analog PC_Beep behavior 20
Table 13. EAPD Behavior 20
Table 14. Valid Digital Mic Configurations 22
Table 15. DMIC_CLK and DMIC_0,1 Operation During Power States 22
Table 16. Electrical Specification: Maximum Ratings 32
Table 17. Recommended Operating Conditions 32
Table 18. 92HD95 Analog Performance Characteristics 33
Table 19. Class-D BTL Amplifier Performance 36
Table 20. Capless Headphone Supply 37
Table 21. HD Audio Bus Timing 37
Table 22. SPDIF Timing 38
Table 23. Digital Mic timing 38
Table 24. GPIO Characteristics 38
Table 25. Pin Configuration Default Settings 42
Table 26. Command Format for Verb with 4-bit Identifier 43
Table 27. Command Format for Verb with 12-bit Identifier 43
Table 28. Solicited Response Format 43
Table 29. Unsolicited Response Format 43
Table 30. Widget List 44
Table 31. 40QFN Pin Description 209
Table 32. Standard Reflow Profile 211

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

1. DESCRIPTION

1.1. Overview

The 92HD95 audio CODEC provides stereo 24- bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. SPDIF output supports sample rates of 192kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz. Additional sample rates are supported by the driver software.

An integrated BTL stereo amplifier is ideal for driving 4ohm or 8ohm integrated speakers in mobile and ultra-mobile computers. For desktop computers or mobile computers using only one speaker, the BTL output stage may be configured to support a single mono speaker.

The 92HD95 includes an Integrated **Class-G** true capless stereo headphone amplifier with charge pump and LDO.

The 92HD95 supports a wide range of desktop and laptop configurations. The SPDIF output interfaces provide connectivity to consumer electronic equipment or to a home entertainment system. All inputs can be programmed with 0-30 dB gain in 10 dB steps allowing for line or microphone use of any input.

Port presence detect capabilities allow the CODEC to detect when audio devices are connected to the CODEC. The fully parametric Internal EQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD95 also supports the Intel Runtime D3 (RTD3) low power state for Always On, Always Connected.

The 92HD95 audio CODEC operates with a 3.3V digital supply and a 3.3V analog supply. It allows for 1.5V and 3.3V HDA signaling; the correct signalling level is selected dynamically based on the power supply voltage on the DVDD-IO pin.

The 92HD95 audio CODEC is offered in a 40-pin QFN Environmental (ROHS) package.

1.2. Orderable Part Numbers

92HD95B2X3NDGXyyX	4ch, 40QFN, switchable 1.5V or 3.3V HDA Signaling, 3.3V AVDD

yy = silicon stepping/revision, contact sales for current data.
Add an “8” to the end for tape and reel delivery.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

2. DETAILED DESCRIPTION

2.1. Port Functionality

Multi-function (Input/Output) ports allow for the highest possible flexibility and supporting a wide variety of consumer desktop and mobile system use models.

- Port A supports
  - Cap-less Headphone Out
  - Cap-less Line Out
- Port B supports
  - Line Input
  - Mic with 0/10/20/30 dB Boost and Vref_Out
- Port C supports
  - Line Input
  - Mic with 0/10/20/30 dB Boost and Vref_Out
- Port D supports
  - BTL stereo output
  - BTL (L+/L-) mono out

Pins 40-QFN	Port	Input	Output	Headphone	BTL	Mic Bias (Vref pin)	Input boost amp
22/23	A		Yes	Yes			
17/18	B	Yes				Yes	Yes
14/15	C	Yes				Yes	Yes
32/33/36/37	D		Yes		Yes		
3 (CLK=2)	E (DMIC0)	Yes				NA	Yes
4 (CLK=2)	F (DMIC1)	Yes				NA	Yes
40	SPDIF_OUT		Yes				

Table 1. Port Functionality

2.1.1. Port Characteristics

Port A is designed to drive 32 ohm (nominal) headphones or a 10K (nominal) load. Input ports are 50K (nominal) at the pin.

DAC full scale outputs and intended full scale input levels are 1V rms at 3.3V. Line output ports and Headphone output ports on the codec may be configured for +3dBV full scale output levels (0.707Vrms) by using a vendor specific verb.

Unused ports should be left unconnected. When updating existing designs to use the codec, ensure that there are no conflicts between the output ports on the codec and existing circuitry.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

AFG Power State	Input Enable	Output Enable	Used as output for DAC/Mixer	Used as output for analog PC_Beep	Used as input for ADC, mixer	Port Behavior
D0-D2	1	1	Don't care	Don't care	Yes	Not allowed. Port is active as input.
					No	Not allowed. Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
	1	0	NA	NA	Yes	Active - Port enabled as input
	1	0	NA	NA	No	Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
	0	1	currently used by DAC, mixer, beep, or is traditional line or headphone output		NA	Active - Port enabled as output
	0	1	not currently used by DAC, mixer, beep and is capless HP/BTL port			Inactive (Power Down)
	0	0	NA	NA	NA	Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
D3	1	1	NA	NA	Don't care	Not allowed. Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
	1	0	NA	NA	Don't care	Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
	0	1	currently used by DAC, mixer, beep, or is traditional line or headphone output		Don't care	Low power state. If enabled, Beep will output from the port
	0	1	not currently used by DAC, mixer, beep and is capless HP/BTL port		Don't care	Inactive (Power Down)
	0	0	NA	NA	Don't care	Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
D3cold	-	-				Inactive (lower power) - Port keeps output coupling caps charged if port uses caps.
D4	-	-				Inactive (lower power) - Port keeps output coupling caps charged if port uses caps.
D5	-	-				Off - Charge on coupling caps (if used) will not be maintained.

Table 2. Analog Output Port Behavior

2.1.2. Vref_Out

Ports B & C support Vref_Out pins for biasing electret cartridge microphones. Settings of 80% AVDD, 50% AVDD, GND, and Hi-Z are supported. Attempting to program a pin widget control with a reserved or unsupported value will cause the associated Vref_Out pin to assume a Hi-Z state and the pin widget control Vref_En field will return a value of '000' (Hi-Z) when read.

To ensure that the BIAS voltage reaches a level of ~2.6V, please add the following widgets to the codec initialization routine at system power-on: 0x0017E442, 0x0017DC02, 0x0017EA0D. Testing has shown that the microphone in some headsets may not function properly unless these widgets are properly configured.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

2.1.3. Jack Detect

Plugs inserted to a jack on Ports A, B, C & SPDIFOUT are detected using SENSE_A. Per HDA015-B, the detection circuit operates when the CODEC is in D0 - D3 and can also operate if both the CODEC and Controller are in D3 (no bus clock.) Jack detection requires that all supplies (analog and digital) are active and stable. When AVDD is not present, the value reported in the pin widget is invalid.

When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in port connectivity is sensed and then generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per HDA015-B, this will take less than 10mS.

The following table summarizes the proper resistor tolerances for different analog supply voltages.

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance Pull-Up	Resistor Tolerance SENSE_A
3.3V	1%	1%

Resistor	SENSE_A
39.2K	PORT A
20.0K	PORT B
10.0K	Port C
5.11K	SPDIFOUT
2.49K	Pull-up to AVDD

Table 3. Jack Detect

See reference design for more information on Jack Detect implementation.

2.1.4. SPDIF Output

The SPDIF Output can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

Per the HDA015-B, the SPDIF outputs support the ability to provide clocking information even when no stream is selected for the converter, or when in a low power state. Also, the SPDIF output port supports port presence detect.

SPDIF Output is outlined in table below.

AFG Power State	RESET#	Output Enable	Converter Dig Enable	Stream ID	Keep Alive Enable	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained.

Table 4. SPDIF OUT 0 Behavior

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

AFG Power State	RESET#	Output Enable	Converter Dig Enable	Stream ID	Keep Alive Enable	Pin Behavior
D0	De-Asserted (High)	Disabled	-	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	Disabled	-	-	Active - Pin drives 0 (internal pull-down NA)
	De-Asserted (High)	Enabled	Enabled	0	-	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA)
	De-Asserted (High)	Enabled	Enabled	1-15	-	Active - Pin drives SPDIFOut0 data (internal pull-down NA)
D1-D2	De-Asserted (High)	Disabled	-	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	-	-	0	Active - Pin drives 0 (internal pull-down NA)
			Enabled	-	1	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA)
D3	De-Asserted (High)	-	-	-	0	Hi-Z (internal pull-down enabled)
		Disabled	-	-	1	Hi-Z (internal pull-down enabled)
		Enabled	Enabled	-	1	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA)
D3cold / RTD3	-	-	-	-	-	Hi-Z (internal pull-down enabled)
D4	-	-	-	-	-	Hi-Z (port off)
D5	-	-	-	-	-	Hi-Z (port off)

Table 4. SPDIF OUT 0 Behavior

2.2. ADC Multiplexers

The codec implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function:(-16 to +30dB gain in 1dB steps) as an output amp and allow a preselection of one of below possible inputs:

- Port Mux (selects between Port B and Port C)
- DMIC 0
- DMIC 1
- DAC0
- DAC1

2.3. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG) , all converter widgets, and all pin complexes support the power state verb F05/705. Converter widgets are active in D0 and inactive in D1-D3.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

The following table describes what functionality is active in each power state.

Function	D0	D1[1]	D2	D3	D3cold / RTD3	Vendor Specific D4	Vendor SpecificD5
SPDIF Output	On	On	On (idle)	On (idle)[5]	Off	Off	Off
Digital Microphone inputs	On	Off	Off	Off	Off	Off	Off
DAC	On	Off	Off	Off	Off	Off	Off
ADC	On	Off	Off	Off	Off	Off	Off
ADC Volume Control	On	Off	Off	Off	Off	Off	Off
Ref ADC	On	Off	Off	Off	Off	Off	Off
Analog Clocks	On	Off	Off	Off	Off	Off	Off
GPIO pins	On	On	On	On[5]	On	On	Off
VrefOut Pins	On	On	Off	Off	Off	Off	Off
Input Boost	On	On	Off	Off	Off	Off	Off
Analog PC_Beep	On	On	On	On	Off	Off	Off
Digital PC_Beep	On	On	On	On[5]	Off	Off	Off
Capless LO/HP Amps	On	On	On	Low Drive[2]	Low Drive[2]	Low Drive[2]	Off
BTL Amp	On	On	On	Low Drive[2]	Off	Off	Off
VAG amp	On	On	On	Low Drive[3]	Low Drive	Low Drive	Off
Port Sense	On	On	On	On[4]	Off	Off	Off
Reference Bias generator	On	On	On	On	On	On	Off
Reference Bandgap core	On	On	On	On	On	On	Off
HD Audio-Link	On	On	On	On[5]	Limited	Off	Off

Table 5. Power Management

1. No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2. VAG is kept active when ports are disabled or in D3/D3cold/D4. PC_Beep is supported in D3 but may be attenuated and distorted depending on load impedance. Hendrix and Kaveri will shut down the capless headphone amplifiers and BTL amplifier in D3 and below. In D3, the codec will turn on the BTL and Capless amplifiers if activity is detected on the PC_BEEP input and analog PC_Beep is enabled.
3. VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
4. Both AVDD and DVDD must be available for Port Sense to operate.
5. Not active if BITCLK is not running (Controller in D3), but can signal power state change request (PME)

The D3-default state is available for HD Audio compliance. The programmable values, exposed via vendor-specific settings, are under IDT Device Driver control for further power reduction. The analog mixer, line and headphone amps, port presence detect, and internal references may be disabled using vendor specific verbs. Use of these vendor specific verbs will cause pops.

The default power state for the Audio Function Group after reset is D3.

2.4. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

2.5. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active. The part will resume from theD1 to theD0 state within 1 mS.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

2.6. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state. The part will resume from the D2 state to the D0 state within 2mS.

2.7. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still less than 10mS to meet Intel low power goals. The default power state for the Audio Function Group after power is applied is D3.

While in AFG D3, the HD Audio controller may be in a D0 state (HD Audio bus active) or in a D3 state (HD Audio bus held in reset with no Bit_Clk, SData_Out, or Sync activity.) The expected behavior is as follows (see the HDA015-B section for more information):

Function	HDA Bus active	HDA Bus stopped
Port Presence Detect state change	Unsolicited Response	Wake Event followed by an unsolicited response
GPIO state change	Unsolicited Response	Wake Event followed by an unsolicited response

2.7.1. AFG D3cold / RTD3

The D3cold/RTD3 power state is the lowest power state available that does not use vendor specific verbs. While in D3cold/RTD3, the CODEC will still respond to bus requests to revert to a higher power state (double AFG reset, link reset). However, audio processing, port presence detect, and other functions are disabled. Per the HD Audio bus HDA015-B, the D3cold state is intended to be used just prior to removing power to the CODEC. Typically, power will be removed within 200mS. However, the codec may exit from the D3cold/RTD3 state by generating 2, back-to-back, AFG reset events. Resume time from D3cold/RTD3 is less than 200mS.

The codec also supports Intel's Runtime D3 (RTD3) state for Always On, Always Connected support.

2.8. Vendor Specific Function Group Power States D4/D5

The codec introduces vendor specific power states. A vendor defined verb is added to the Audio Function Group that combines multiple vendor specific power control bits into logical power states for use by the audio driver. The 2 states defined offer lower power than the 5 existing states defined in the HD Audio specification and HDA015-B. The Vendor Specific D4 state provides lower digital power consumption relative to D3cold by disabling HD Audio link responses. Vendor specific D5 further reduces power consumption on the digital supply by turning off GPIO drivers, and reduces analog power consumption by turning off all analog circuitry except for reset circuits.

States D4/D5 are not entered until D3cold has been requested so are actually D3cold options rather than true, independent, power states. Software can pre-program the D4 or D5 state as a re-definition of how the part will behave when the D3cold power state is requested or software may enter D3cold, then set the D4 or D5 before performing the power state get command. The preferred method is to request D3cold, then select D4 or D5 as desired.This will reduce the severity of pops encountered when entering D4 or D5.

Both power states require a link reset or removal of DVDD to exit.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

The CODEC may pop when using these verbs and transition times to an active state (D1 or D0 for example) may take several seconds.

2.9. 4.12 Vendor Specific Function Group Power State "D5 Kill"

Vendor specific "D5 Kill" places the device in a low power, non responsive, state that is intended to disable the CODEC when, for security reasons, it is desired that no audio playback or recording take place.

State "D5 Kill" is not entered until D3cold has been requested. Software pre-programs both the D4 and D5 state request bits (D4 and D5 = 1) then request D3cold. After responding to the Function Group Power State Get verb (needed to enter D3cold), the CODEC will no longer respond to any link activity. The only way to exit this state is to remove power (Power on reset will set the power state to D3.)

"D5 Kill" is identical to vendor specific D5 with the exception that the CODEC will only exit this state when power is removed.

2.10. Low-voltage HDA Signaling

The codec is compatible with either 1.5V or 3.3V HDA bus signaling; in the 48-QFN package the voltage selection is done dynamically based on the input voltage of DVDD_IO.

DVDD_IO is currently not a logic configuration pin, but rather provides the digital power supply to be used for the HDA bus signals.

When in 1.5V mode, the codec can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

2.11. Multi-channel capture

The capability to assign multiple ADC Converters to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported this is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones.

The ADC Converters can be associated with a single stream as long the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the "CnvtrID" widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the "Multi-Converter Stream Critical Entries." table.

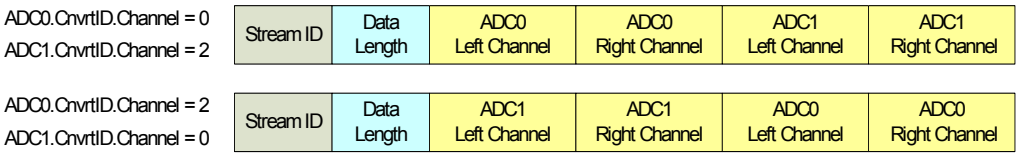
An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2 & 3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id "Strm= N" to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels "NmbrChan = 0011".

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

ADC1 CnvtrID	**(NID = 0x08)**	
	[3:0]	Ch = 2
ADC0 CnvtrID	**(NID = 0x07)**	
	[3:0]	Ch=0

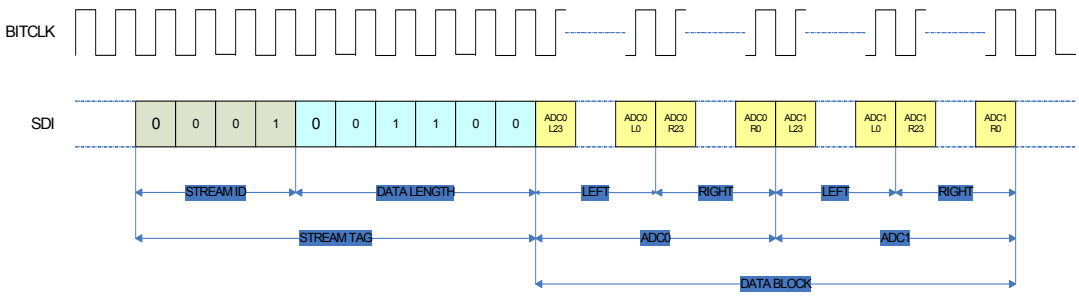
Table 6. Example channel mapping

Figure 1. Multi-channel capture



The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

Figure 2. Multi-channel timing diagram



ADC[1:0] Cnvtr	Bit Number	Sub Field Name	Description
	[15]	StrmType	Stream Type (TYPE): 0: PCM 1: Non-PCM (not supported)
	[14]	FrmtSmplRate	Sample Base Rate 0= 48kHz 1=44.1KHz
	[13:11]	SmplRateMultp	Sample Base Rate Multiple 000=48kHz/44.1kHz or less 001= x2 010= x3 (not supported) 011= x4 192kHz only, 176.4 not supported 100-111= Reserved

Table 7: Mult-channel

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

	[10:8]	SmplRateDiv	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 (not supported) 010= Divide by 3 (not supported) 011= Divide by 4 (not supported) 100= Divide by 5 (not supported) 101= Divide by 6 (not supported) 110= Divide by 7 (not supported) 111= Divide by 8 (not supported)
	[6:4]	BitsPerSmpl	Bits per Sample 000= 8 bits (not supported) 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
	[3:0]	NmbrChan	Number of Channels Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000=1 channel (not supported) 0001 = 2 channels … 1111= 16 channels.
	[7:4]	Strm	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
	[3:0]	Ch	Integer representing lowest channel used by converter. 0 and 2 are valid Entries If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2.

Table 7: Mult-channel

2.12. EAPD

The EAPD pin is a dedicated, bi-directional control pin. Although named External Amplifier Power Down (EAPD) by the HD Audio specification, this pin operates as an external amplifier power up signal. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up (equivalent to D0), and a 0 causes it to power down (equivalent to D3.) When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value (in the register) may remain 1. The default state of this pin is 0 (driving low.) The pin defaults to an open-drain configuration (an external pull-up is recommended.)

Per the HD Audio specification and HDA015-B, multiple ports may control EAPD. The EAPD pin assumes the highest power state of all the EAPD bits in all of the pin complexes. The default value of EAPD is 1 (powered on), but the FG power state will override and the pin will be low. A port will request External Amp Power Up when its power state is active (FG and pin widget power state is D1 or D0) or (Analog PC_Beep is enabled and port is enabled as an output) and the port’s EAPD bit is set to 1. The state of the EAPD pin (unless configured as an input or held low by an external circuit when configured as an open drain output) will be the logical OR of the external amp power up requests from all ports.

By default, the EAPD pin also functions as the Mute#/ShutDown# input for the internal BTL amplifier. In this mode, a low value at the pin (either due to internal EAPD being 0, or to an external entity forc-

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

ing the pin low) will cause the internal BTL amplifier to mute or enter a low power state depending on the amplifier configuration. (See below)

Vendor specific verbs are available to configure this pin. These verbs retain their values across link and single function group resets but are set to their default values by a power on reset:

MODE1	MODE0	EAPD Pin Function	Description
0	0	Open Drain I/O	Value at pin is wired-AND of EAPD bit and external signal.(default)
0	1	CMOS Output	Value of EAPD bit in pin widget is forced at pin
1	0	CMOS Input	External signal controls internal amps. EAPD bit in pin widget ignored
1	1	CMOS Input	External signal controls internal amps. EAPD bit in pin widget ignored

Table 8. EAPD Pin Mode Select

Control Flag	Description
EAPD PIN MODE 1:0	Defines if EAPD pin is used as input, output, or bi-directional port (Open Drain)
BTL/HP SD	0 = Amp controlled by EAPD pin only (default) / 1 = Amp controlled by power state (pin and FG) only
BTL/HP SD MODE	0 = Amp will mute when disabled. (default for ZA and ZB only) / 1 = Amp will shut down (enter a low power state) when disabled (default for YA forward)
BTL/HP SD INV	0 = AMP will power down (or mute) when EAPD pin is low (default) / 1 = Amp will power down (or mute) when EAPD pin is high.

Table 9. Control bit descriptions for BTL amplifier and Headphone amplifier enable configurations

BTL SD	BTL SD MODE	BTL SD INV	EAPD Pin State	BTL Amp State
0	0	0	0	Amplifier is mute
0	0	0	1	Amplifier is active
0	0	1	0	Amplifier is active
0	0	1	1	Amplifier is mute
0	1	0	0	Amplifier is in a low power state (default[1])
0	1	0	1	Amplifier is active
0	1	1	0	Amplifier is active
0	1	1	1	Amplifier is in a low power state
1	0	NA	NA	Amplifier follows pin/function group power state and will mute when disabled
1	1	NA	NA	Amplifier follows pin/function group power state and will enter a low power state when disabled

Table 10. BTL Amp Enable Configuration

1. EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with HDA015-B.

HP SD	HP SD MODE	HP SD INV	EAPD Pin State	Headphone Amp State
0	0	0	0	Amplifier is mute
0	0	0	1	Amplifier is active
0	0	1	0	Amplifier is active
0	0	1	1	Amplifier is mute
0	1	0	0	Amplifier is in a low power state (default[1])
0	1	0	1	Amplifier is active

Table 11. Headphone Amp Enable Configuration

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

HP SD	HP SD MODE	HP SD INV	EAPD Pin State	Headphone Amp State
0	1	1	0	Amplifier is active
0	1	1	1	Amplifier is in a low power state
1	0	NA	NA	Amplifier follows pin/function group power state and will mute when disabled
1	1	NA	NA	Amplifier follows pin/function group power state and will enter a low power state when disabled

Table 11. Headphone Amp Enable Configuration

1. EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with HDA015-B.

Analog BEEP enabled	EAPD Pin value[1]	Description
0	Forced to low when in D2 or D3	Follows description in HD Audio spec. External amplifier is shut down when pin or function group power state is D2 or D3 independent of value in EAPD bit.
1	Forced low in D2 or D3 unless port is enabled as output	Power state is ignored if port is enabled as output and port EAPD=1 to allow PC_Beep support in D2 and D3

Table 12. EAPD Analog PC_Beep behavior

1. When pin is enabled as Open Drain or CMOS output.

AFG Power State	RESET#	Analog PC_BEEP	Port Power State	Pin Behavior
D0-D3	Asserted (Low)	-	-	Active low immediately after power on, otherwise the previous state is retained across FG and link reset events
D0	De-Asserted (High)	-	-	Active - Pin reflects EAPD bit unless held low by external source.
D1	De-Asserted (High)	-	D0-D1	Active - Pin reflects EAPD bit unless held low by external source.
D2	De-Asserted (High)	Disabled	D0-D2	Pin forced low to disable external amp
D2	De-Asserted (High)	Enabled	D0-D2	Active - EAPD Pin high if any port EAPD bit =1 and that port also enabled as output.
D3	De-Asserted (High)	Disabled	D0-D3	Pin forced low to disable external amp
D3	De-Asserted (High)	Enabled	D0-D3	Active - EAPD Pin high if any port EAPD bit=1 and that port also enabled as output.
D3cold/ RTD3	De-Asserted (High)	-	-	Pin forced low to disable external amp
D4	De-Asserted (High)	-	-	Pin forced low to disable external amp
D5	De-Asserted (High)	-	-	Pin Hi-Z (off)

Table 13. EAPD Behavior

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Figure 3. HP EAPD Example to be replaced by single pin for internal amp

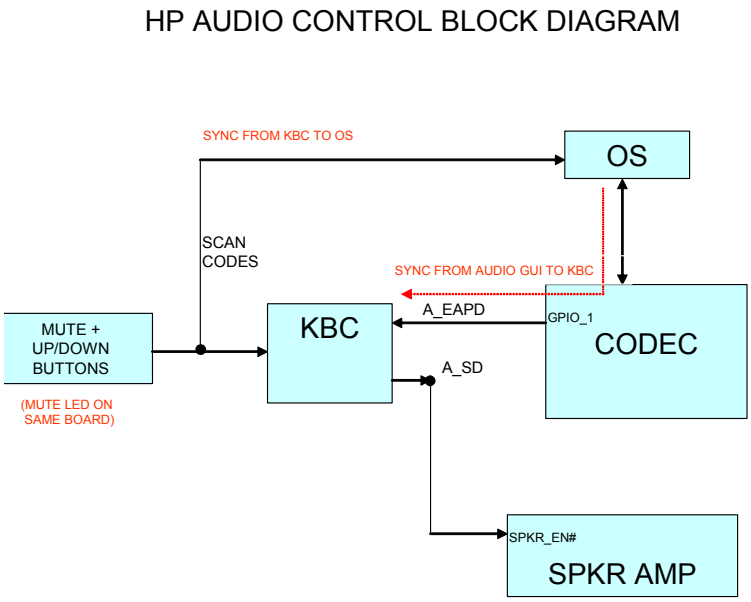
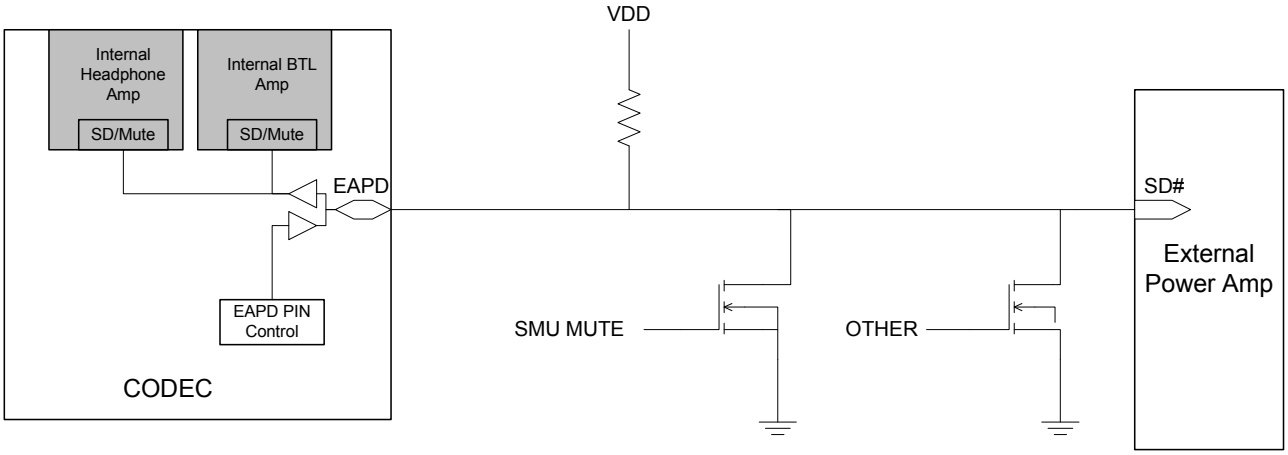


Figure 4. EAPD implementation



2.13. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0, DMIC1, and DMIC_CLK 3-pin interface. The DMIC0 and DMIC1 signals are inputs that carry individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a vendor specific verb and the left time slot is copied to the ADC left and right inputs.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the internal master clock. The default frequency is 2.352Mhz.

The two DMIC data inputs are reported as two stereo input pin widgets that incorporate a boost amplifier. The pin widgets are shown connected to the ADCs through the same multiplexors as the

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

analog ports. Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

To conserve power, the analog portion of the ADC will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input. This should take less than 10mS.

DMIC pin widgets support port presence detect directly using SENSE-B input.

The codec supports the following digital microphone configurations:

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones
1	Single Edge	0, or 1	Available on either DMIC_0 or DMIC_1 When using a microphone that supports multiplexed operation (2-mics can share a common data line), configure the microphone for “Left” and select mono operation using the vendor specific verb. “Left” D-mic data is used for ADC left and right channels.
2	Double Edge on either DMIC_0 or 1	0, or 1	Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge (multiplexed output) capability.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0, or 1	Requires both DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge (multiplexed output) capability. Two ADC units are required to support this configuration
4	Double Edge	0, or 1	Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge capability. Two ADC units are required to support this configuration

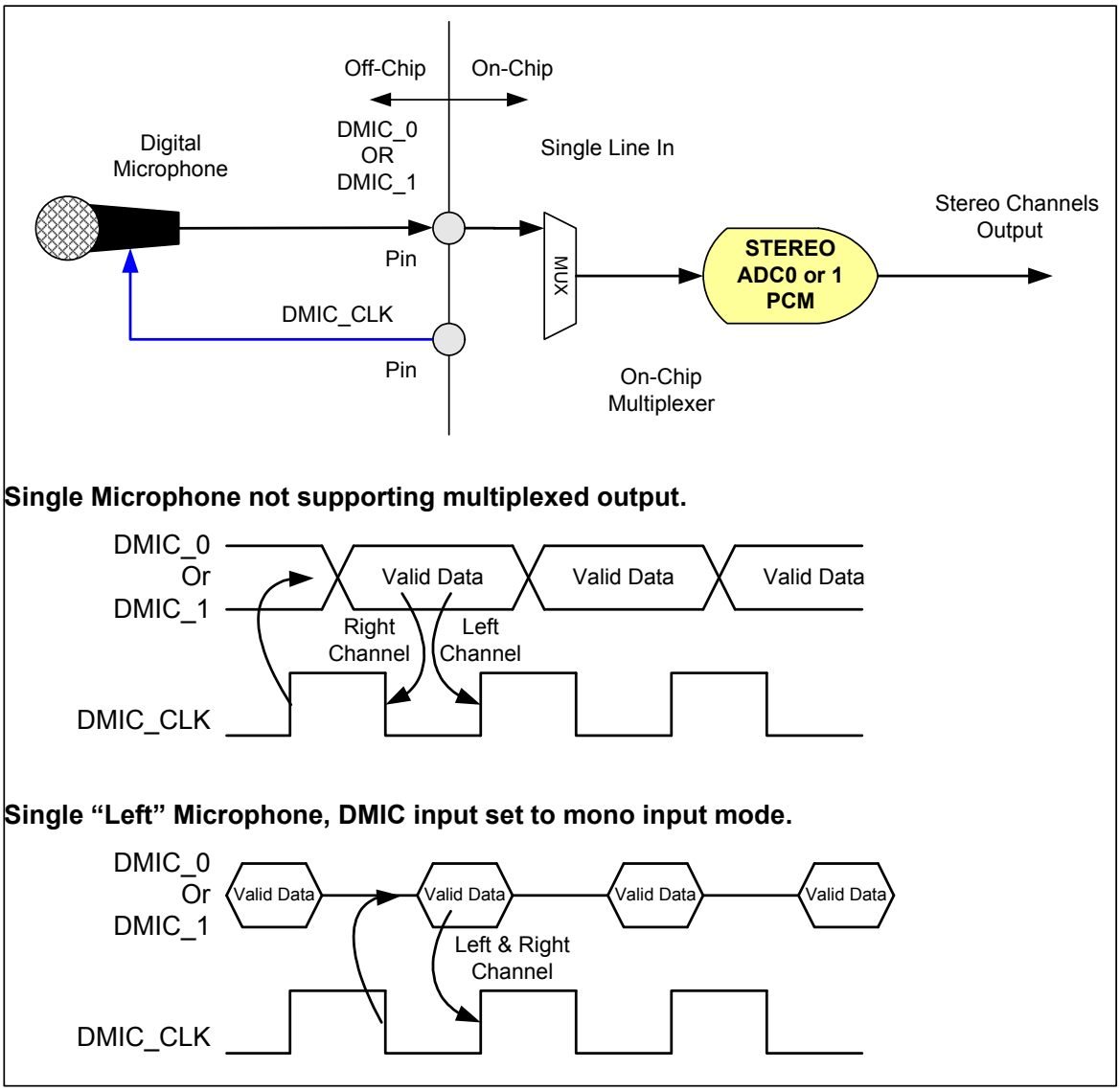
Table 14. Valid Digital Mic Configurations

Power State	DMIC Widget Enabled?	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D1-D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D4	-	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D5	-	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down

Table 15. DMIC_CLK and DMIC_0,1 Operation During Power States

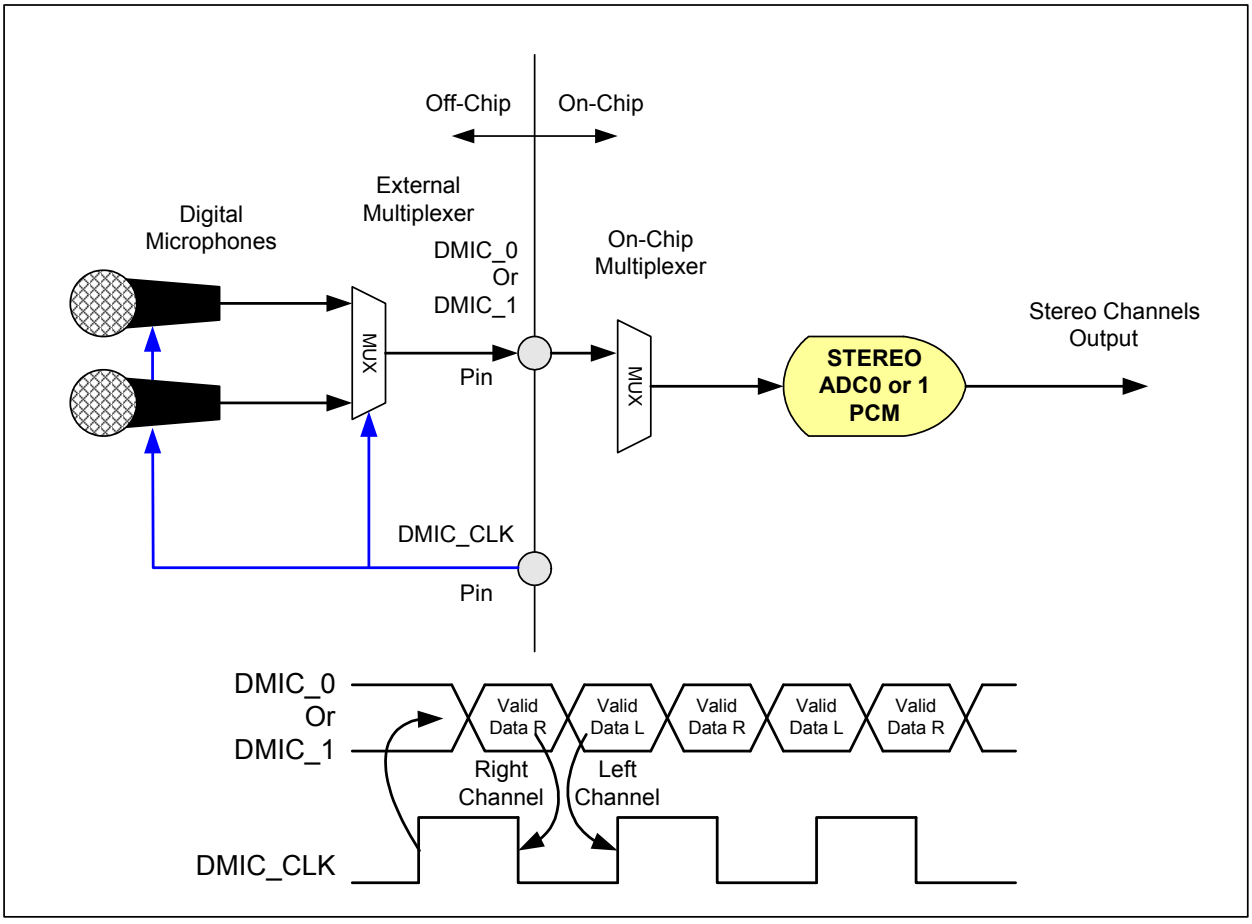
©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Figure 5. Single Digital Microphone (data is ported to both left and right channels



©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

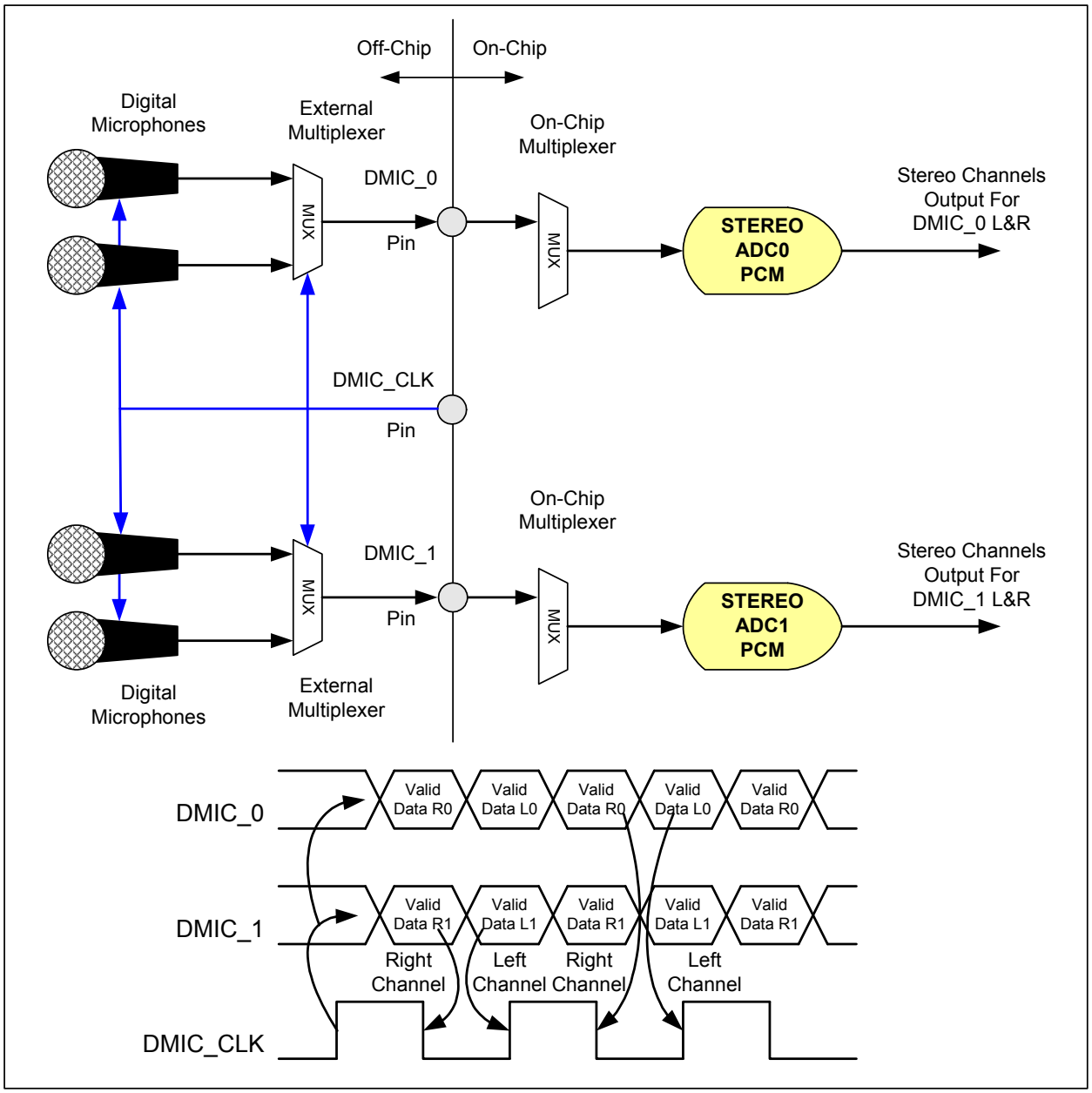
Figure 6. Stereo Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Figure 7. Quad Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, in this case the external multiplexer is not required.

2.14. Analog PC-Beep

The codec supports automatic routing of the PC_Beep pin to Port A and Port D outputs when the HD-Link is in reset.

When the link is active (not held in reset) Analog PC-Beep may be enabled manually. Analog PC_Beep is mixed at the port and only ports enabled as outputs will pass PC_Beep.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Beep activity monitoring is provided when the analog beep path is enabled and the CODEC or amplifier is in a low power state (D3).

The Analog PC Beep input is sampled for 500us every 1ms. If the beep input is high or low (>200mVpp) for at least 37% of that time, it is considered active. If it is active for less than 7.5% of that time, it is possibly inactive. If no activity is detected for 64ms (128ms, 256ms and 512ms also selectable for the idle threshold), then beep is considered inactive.

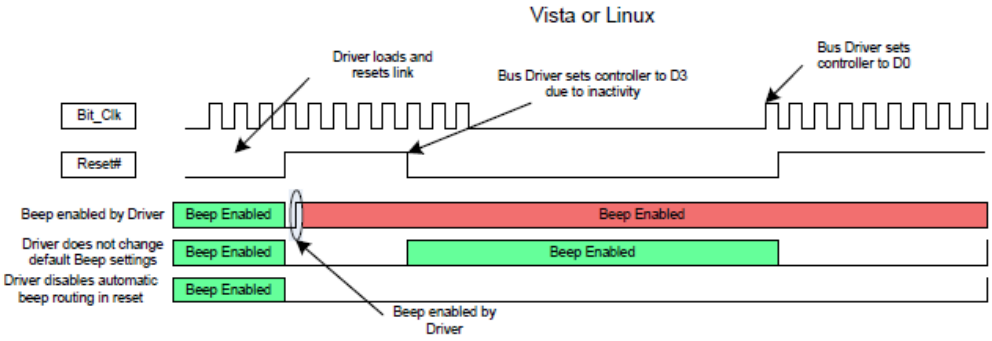


Figure 8. Analog PC Beep Active

Phase 1: analog beep auto-routing phase in the period after application of DVDD, before the first rising edge of link reset.

Once Analog PCbeep is detected(BEEP_PRESENCE=1) after 64ms delays (after POR (power on reset)), the Amplifier will be turned on(port_pwd=0, port_output_en=1, there is a timing between these two signals) and analog_beep_en=1. If BEEP_PRESENCE=0 for longer than the threshold time, the amplifiers will be turned off to save power and prevent unwanted system noise from being heard.

Phase 2: When not in phase 1

A. If analog beep function is disabled by driver.

Analog beep auto-detect will also be disabled.

B. If analog beep function is enabled by driver.

Once analog PCbeep is detected(BEEP_PRESENCE=1), analog pc_beep will be enabled

If in D0-D2, enabled simply means muting or un-muting beep to avoid hearing system noise on the beep input pin but it is acceptable to turn off port amplifiers if not currently used by DACs, mixer, or beep to save power.

If in D3, enabled means that the necessary amplifiers are turned on so that the beep signal may be heard on all ports configured as outputs (see analog pc-beep description section above)

All needed amplifiers are enabled until BEEP_PRESENCE=0 for longer than the idle threshold

A flow chart of Analog PC Beep is below.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

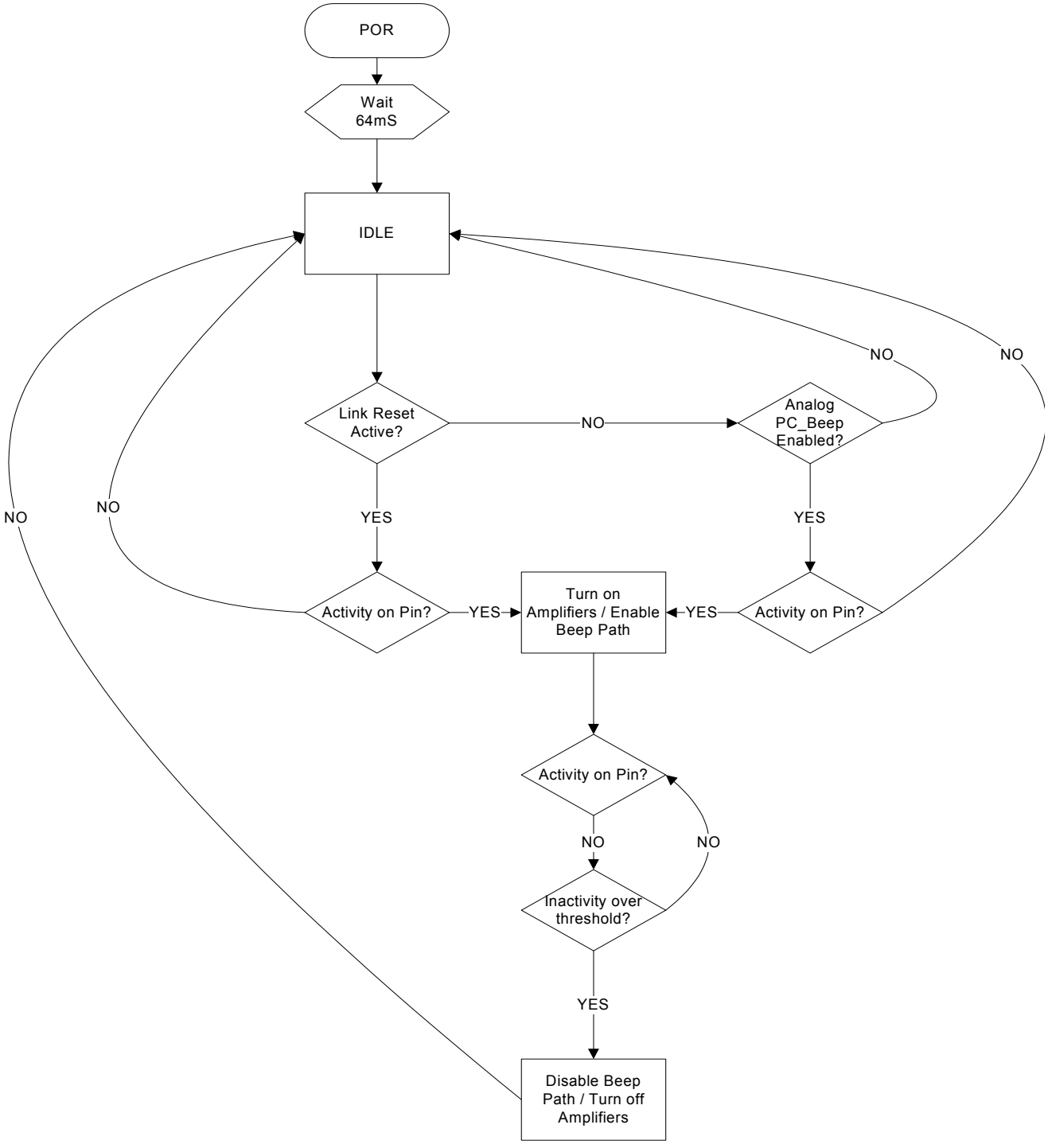


Figure 9. Analog PC Beep Flow chart

2.15. Digital PC-Beep

This block uses an 8-bit divider value to generate the PC beep from the 48kHz HD Audio Sync pulse. The digital PC_Beep block generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). Other audio sources are disabled when digital PC_Beep is active.

It should be noted that digital PC Beep is disabled if the divider = 00h.

PC-Beep may be attenuated and distorted when the CODEC is in D3 depending on the load impedance seen by the output amplifier since all ports are in a low power state while in D3. Load impedances of 10K or larger can support full scale outputs but lower impedance loads will distort unless the output amplitude is reduced. Digital PC_Beep requires a clock to operate and the CODEC will prevent the system from stopping the bus clock while in D3 by setting the Clock_Stop_OK bit to 0 to indicate that the part requires a clock.

2.16. Headphone Drivers

The codec implements class-G cap-less headphone outputs. The Microsoft Windows Logo Program allows up to the equivalent of 100ohms in series. However, an output level of +3dBV at the pin is required to support 300mV at the jack with a 32ohm load and 1V with a 320 ohm load. Microsoft allows device and system manufactures to limit output voltages to address EU safety requirements. (WLP 3.09 - please refer to the latest Windows Logo Program requirements from Microsoft.) The codec does not support power limiting.

The cap-less headphone drivers are supplied with +/-2.5V derived from AVDD. Therefore, it is possible to run the headphone supply from 3.3V to 5V and maintain ~60mW peak output power into 32 ohm headphones.

2.17. Class-D BTL Amplifier

An integrated class-D stereo BTL amplifier is provided to directly drive 4 ohm speakers (2W @ 4.75V) or 8 ohm speakers (1W @ 4.75V). No external filter is needed for cable runs of 18” or less. An internal DC blocking filter prevents distortion when the audio source has DC content, and prevents unintentional power consumption when pausing audio playback. The amplifier may be controlled using the EAPD pin (see EAPD section.)

Using a vendor specific verb, the BTL amplifier may be configured to support a mono speaker connected to the L +/- pins. In this mode, the Left and Right audio is mixed and sent to the left output only. The right channel is turned off to conserve power.

Maximum gain for the BTL amplifier is programmable. The following 4 gain settings relative to a nominal line output are desired: +6.5dB, +9.5dB, +14.5dB, +16.5dB. Absolute gain may vary and the suggested accuracy is +/-1.5dB.

This gain is exposed in a vendor specific widget and is intended to mimic the pin programmable gain implemented in discrete BTL amplifiers commonly used in notebook computers.

The BTL amplifier includes thermal management circuitry. When the CODEC reaches a temperature of about 140 degrees, the output amplitude of the BTL amp is gradually lowered until the temperature falls below 140. All other functions will remain active if the BTL amplifier is shut down due to die temperature.

2.18. BTL Amplifier High-Pass Filter

For mobile applications, speakers are often incapable of reproducing low frequency audio and unable to handle the maximum output power of the BTL amplifier. A high-pass filter is implemented

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

in the BTL output path to reduce the amount of low frequency energy reaching speakers attached to the BTL amplifier. This can prevent speaker failure.

2.18.1. Filter Description

The high-pass filter is derived from the common biquadratic filter and provides a 12dB/octave roll-off. The filter may be programmed for a -3dB response at: 100Hz, 200Hz, 300Hz, 400Hz, 500Hz, 750Hz, 1KHz, or 2KHz. The high pass filter is enabled by default with a cut-off frequency of 300Hz. The filter may be bypassed using the associated verb (processing state verb).

The analog PC_Beep input is not affected by the digital high-pass filter. To ensure that the speakers attached to the BTL amplifier are not harmed by low frequency audio entering the PC_Beep input, an external filter must be implemented. Fortunately, it is common practice to implement an attenuation circuit and DC blocking capacitor at the PC_Beep input. This attenuator/filter is easily adjusted to restrict low frequency audio. The easiest approach is to reduce the value of the DC blocking capacitor but other approaches are equally effective.

2.19. EQ

There are 5 bands of parametric EQ (bi-quad) per channel. Due to the flexibility of the bi-quad implementation, each filter band may be configured as a high-pass, low-pass, band-pass, high shelving, low shelving, or other function.

Each band has an independent set of coefficients. A bi-quad filter has 6 coefficients. One coefficient is normalized to 1 and 5 are programmed into the core. Each band supports up to +15dB boost or up to -36dB cut.

2.20. Combo Jack Detection

4 conductor (combo) jacks are becoming popular. In the most common implementation the 4 conductor plug has the same mechanical dimensions as a 3 conductor 3.5mm plug but the sleeve portion has been split into two segments:S1 and S2. When a 4-conductor plug (headset) is inserted into the jack T (Tip) = Left headphone audio, R (Ring) = Right headphone audio, S1 (First half of sleeve) = microphone input, and S2 (Second half of sleeve) = return (GND). When a 3-conductor plug (headphones) is inserted into the jack; T=Left audio, R=Right audio, S1=GND, S2=GND. By monitoring the S1 connection to see if it is shorted to ground, we can distinguish between headsets and headphones. Please note that analog microphone plugs (3-conductor-Lmic/Rmic/GND) and optical SPDIF plugs can not be supported using this implementation.

Figure 10. Combo Jack

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Plug insertion is reported on the headphone port using the switch integrated into the jack.

The internal circuit monitors the voltage at the jack to determine if a low impedance load is present.

Detection of a microphone is not reported unless plug insertion is also detected.

2.21. GPIO

2.21.1. GPIO Pin mapping and shared functions

GPIO #	Pin	Supply	SPDIF In	SPDIF Out	GPI/O	GPI	GPO	VrefOut	DMIC	VOL	Pull Up	Pull Down
0	4	DVDD			YES				IN			50K
1	2	DVDD			YES				CLK			50K
2	3	DVDD			YES				IN			50K
3	40	DVDD		YES	YES							50K

2.21.2. SPDIF/GPIO Selection

2 functions are available on the GPIO3/SPDIFOUT (pin 40). To determine which function is enabled, the order of precedence is followed:

1. If the GPIOs are enabled, they override both SPDIF_OUT
2. If the GPIOs are not enabled through the AFG, then at reset, the pin is pulled low by an internal pull-down resistor.
3. If the port is enabled as an output, the SPDIF output will be used.

2.21.3. Digital Microphone/GPIO Selection

2 functions are available on the DMIC_CLK/GPIO1 (pin 2) and the DMIC_0/GPIO2 (pin 3) pins. To determine which function is enabled, the order of precedence is followed:

1. If GPIOs are not enabled through the AFG, then at reset, pins 2,3 and 4 are pulled low by an internal pull-down resistor.
2. If the GPIO 1 is enabled, the 2 DMIC pins become mute (unless programmed for GPIO or SPDIF use) and pin 3 becomes GPIO with an internal pull-down.
3. If GPIO2 is enabled through the AFG, pin 4 becomes a GPIO and is pulled low by an internal pull-down resistor.
4. If the port is enabled as an input, the digital microphones will be used.
5. If the port is not enabled as an input or if the pin is configured as a GPIO, the digital microphone path will be mute.

2.22. HD Audio HDA015-B support

The codec provides complete support for the HDA015-B specification (now DCN) building on the support already present in previous products. HDA015-B features supported are:

1. Persistence of many configuration options through bus and function group reset.
2. The ability to support port presence detect in D3 even when the HD Audio bus is in a low power state (no clock.)
3. Fast resume times from low power states: 1ms D1 to D0, 2ms D2 to D0, 10mS D3 to D0.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

4. Notification if persistent register settings have been unexpectedly reset.
5. SPDIF active in D3 (required)

2.23. Digital Core Voltage Regulator

The digital core operates from a 1.8V (10%) supply voltage. Many systems require that the CODEC use a single 3.3V digital supply, so an integrated regulator is included on die. The regulator uses pin 9, DVDD, as its voltage source. The output of the LDO is connected to pin 1 and the digital core. A 10uF capacitor must be placed on pin 1 for proper load regulation and regulator stability.

The digital core voltage regulator is only dependent on DVDD. DVDDIO may be either 3.3 or 1.5V and may precede or follow DVDD in sequence. The CODEC digital logic and I/O (unless referenced to AVDD) will operate in the absence of AVDD. DVDD and AVDD supply sequencing for the application of power and the removal of power is neither defined nor guaranteed. It is common for desktop systems to supply AVDD from the system standby supply and the CODEC will tolerate, indefinitely, the condition where AVDD is active but DVDD and DVDDIO are inactive.

2.24. Microphone Mute Input

The 92HD95 supports a microphone mute input. An external switch or other circuit may directly mute the CODEC without relying on software control. This is a most helpful feature for allowing the end user to conveniently enforce privacy since it bypasses the record gain/mute functions typically controlled by software. While recording is muted, any active stream will receive digital silence.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

3. CHARACTERISTICS

3.1. Electrical Specifications

3.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 92HD95. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	3.6 Volts
Digital maximum supply voltage	DVdd	3.6 Volts
BTL maximum supply voltage	PVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0 ^{O}C to +70 ^{O}C
Storage temperature		-55 ^{O}C to +125 ^{O}C
Soldering temperature		Soldering temperature information is available in the package section of this datasheet.

Table 16. Electrical Specification: Maximum Ratings

3.1.2. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supplies	DVDD_Core	1.62	1.8	1.98	V
	DVDD_IO (3.3V signaling)	3.135	3.3	3.465	V
	DVDD_IO (1.5V signaling)	1.418	1.5	1.583	V
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (40-QFN)			+90	°C

Table 17. Recommended Operating Conditions

ESD: The 92HD95 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the 92HD95 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

3.2. 92HD95 Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 3.3V +/-5%, DVdd = 3.3V ± 5% or 1.8V± 10%, AVss=DVss=0V; 20Hz to 20KHz swept sinusoidal input; Sample Frequency = 48 kHz; 0dB FS = 1Vrms for AVdd = 4.75V and 0.71Vrms for AVdd = 3.3V, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Conditions	Min	Typ	Max	Unit
Digital to Analog Converters					
Resolution			24		Bits
Dynamic Range[1]: PCM to All Analog Outputs	-60dB FS signal level, Analog Mixer disabled	93			dB
SNR[2] - DAC to All Line-Out Ports	Analog Mixer Disabled, PCM data	95			dB
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Disabled,-3dB FS Signal, PCM data	82			dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 10KΩ load, PCM data	95			dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled,-3dB FS Signal, 10KΩ load, PCM data	65			dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 32Ω load, PCM data	95			dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, -3dB FS Signal, 32Ω load, PCM data	68			dBr
Any Analog Input (ADC) to DAC Crosstalk	10KHz Signal Frequency. 0dBV signal applied to ADC, DACs idle, ports enabled as output.	-65	-	-	dB
Any Analog Input (ADC) to DAC Crosstalk	1KHz Signal Frequency. see above	-65	-	-	dB
DAC L/R crosstalk	DAC to LO or HP 20-15KHz into 10KΩ load	70	73		dB
DAC L/R crosstalk	DAC to HP 20-15KHz into 32Ω load	65	68		dB
Gain Error	Analog Mixer Disabled			0.5	dB
Interchannel Gain Mismatch	Analog Mixer Disabled			0.5	dB
D/A Digital Filter Pass Band[4]		20	-	21,000	Hz
D/A Digital Filter Pass Band Ripple[5]				0.125	+/- dB
D/A Digital Filter Transition Band		21,000	-	31,000	Hz
D/A Digital Filter Stop Band		31,000	-	-	Hz
D/A Digital Filter Stop Band Rejection[6]		-100	-	-	dB
D/A Out-of-Band Rejection[7]		-55	-	-	dB
Group Delay (48KHz sample rate)		-	-	1	ms
Attenuation, Gain Step Size DIGITAL		-	0.75	-	dB
DAC Offset Voltage		-	10	20	mV
Deviation from Linear Phase		-	1	10	deg.
Analog Outputs					
Full Scale All Outputs	DAC PCM Data	1.00	-	-	Vrms
Full Scale All Outputs	DAC PCM Data	2.83	-	-	Vp-p

Table 18. 92HD95 Analog Performance Characteristics

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Parameter	Conditions	Min	Typ	Max	Unit
All Headphone Capable Outputs	32Ω load	40	60	-	mW (peak)
Amplifier output impedance	Headphone Outputs	150 0.1			Ohms
External load Capacitance	Headphone Outputs		220		pF
Analog inputs					
Full Scale Input Voltage	0dB Boost (input voltage required for 0dB FS output)	1.05	-	-	Vrms
All Analog Inputs with boost	10dB Boost	0.320	-	-	Vrms
All Analog Inputs with boost	20dB Boost	0.105	-	-	Vrms
All Analog Inputs with boost	30dB Boost	0.032	-	-	Vrms
Boost Gain Accuracy		-2		2	dB
Input Impedance		-	50	-	KΩ
Input Capacitance		-	15	-	pF
Analog to Digital Converter					
Resolution			24		Bits
Full Scale Input Voltage	0dB Boost (input voltage required to generate 0dBFS per AES 17)	1.05			
Dynamic Range[1], All Analog Inputs to A/D	High Pass Filer Enabled, -60dB FS, No boost	86			dB
Full Scale Input Voltage	20dB Boost (input voltage required to generate 0dBFS per AES 17)	0.105			
Dynamic Range[1], All Analog Inputs to A/D	20dB Boost High Pass Filter Enabled, -60dB FS	80			dB
THD+N[3] All Analog Inputs to A/D	High Pass Filter enabled, -1/-3dB FS signal level	77			dB
THD+N[3] All Analog Inputs to A/D	20dB Boost, High Pass Filter enabled, -1/-3dB FS signal level	72			dB
Analog Frequency Response[8]		10	-	30,000	Hz
A/D Digital Filter Pass Band[4]		20	-	21,000	Hz
A/D Digital Filter Pass Band Ripple[5]				0.1	+/- dB
A/D Digital Filter Transition Band		21,000	-	31,000	Hz
A/D Digital Filter Stop Band		31,000	-	-	Hz
A/D Digital Filter Stop Band Rejection[6]		-100	-	-	dB
Group Delay	48 KHz sample rate	-	-	1	ms
Any unselected analog Input to ADC Crosstalk	10KHz Signal Frequency	-65	-	-	dB
Any unselected analog Input to ADC Crosstalk	1KHz Signal Frequency	-65	-	-	dB
ADC L/R crosstalk	Any selected input to ADC 20-15Khz	-65			dB
DAC to ADC crosstalk	DAC output 0dBFS. All outputs loaded. Input to ADC open. 20-15Khz	-65			dB

Table 18. 92HD95 Analog Performance Characteristics

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Parameter	Conditions	Min	Typ	Max	Unit
Spurious Tone Rejection[9]		-	-100	-	dB
Attenuation, Gain Step Size (analog)		-	1.5	-	dB
Interchannel Gain Mismatch ADC		-	-	0.5	dB
Power Supply					
Power Supply Rejection Ratio	10kHz	-	-65	-	dB
Power Supply Rejection Ratio	1kHz	-	-65	-	dB
D0 Didd[10]	DVDD =3.3V		1.3		mA
D0 Didd_Core[10]	DVDD_CORE =1.8V		11.7		mA
D0 Aidd[10]	AVDD=3.3V		10		mA
D3hot Didd[11]	DVDD =3.3V		130		uA
D3hot Didd_Core[11]	DVDD_CORE =1.8V		150		uA
D3hot Aidd[11]	AVDD=3.3V		1.95		mA
D3cold Didd[12]	DVDD =3.3V		126		uA
D3cold Didd_Core[12]	DVDD_CORE =1.8V		110		uA
D3cold Aidd[12]	AVDD=3.3V		150		uA
Voltage Reference Outputs					
VREFOut[13]	80% setting with default widget values	2.25	2.4	-	V
	80% setting with widget writes[14]	2.5	2.6	-	
VREFOut Drive			1.6		mA
VREFILT (VAG)			0.45 X AVdd		V
Phased Locked Loop					
PLL lock time			96	200	usec
PLL (or HD Audio Bit CLK) 24MHz clock jitter			150	500	psec
ESD / Latchup					
IEC1000-4-2		1			Level
JESD22-A114-B		2			Class
JESD22-C101		4			Class

Table 18. 92HD95 Analog Performance Characteristics

1.Dynamic Range is the ratio of the full scale signal to the noise output with a -60dBFS signal as defined in AES17 as SNR in the presence of signal and outlined in AES6id, measured “A weighted” over 20 Hz to 20 kHz bandwidth

2.Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).

3.THD+N ratio as defined in AES17 and outlined in AES6id,non-weighted, over 20 Hz to 20 kHz bandwidth.Results at the jack are dependent on external components and will likely be 1 - 2dB worse.

4.Peak-to-Peak Ripple over Passband meets ± 0.125dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.

5.Peak-to-Peak Ripple over Passband meets ± 0.125dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.

6.Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.

7.The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

8.± 1dB limits for Line Output & 0 dB gain, at -20dBV

9.Spurious tone rejection is tested with ADC dither enabled and compared to ADC performance without dither.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

10.One stereo DAC playing 1mW sine wave into 32Ohm load, with power optimizations applied.
11.ICodec in D3 with BUS stopped and power optimizations applied.
12.Codec in D3cold with BUS stopped and power optimizations applied.
13.VREFOut may be set to Hi-Z, GND, 50% or 80%.
14.See section 2.1.2 for initialization information.

3.3. Class-D BTL Amplifier Performance

Parameter	Min	Typ	Max	Unit
Output Power (BTL 4 ohm, 5V, <1% THD+N)	2			W
Output Power (BTL 4 ohm, 5V, <10% THD+N)		3		W
Amplifier Efficiency η (4Ω, 5V, 2W)		80		%
THD+N (BTL 4Ω, 5V, FS)			1	%
THD+N (BTL 4Ω, 5V, -3dBFS)			0.3	%
Frequency Response	20	-	20K	Hz
PWM frequency		352.8		KHz
Output voltage noise (4Ω, 5V)		90		uV
Idle current		15		mA
Shutdown current		0.1		mA

Table 19. Class-D BTL Amplifier Performance

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

3.4. Capless Headphone Supply Characteristics

Parameter	Min	Typ	Max	Unit
LDO idle current		1	2	mA
Capless Headphone Amp idle current		2	3	mA
Charge Pump idle current		4	6	mA
Charge Pump shutdown time		1		mS
Charge Pump start-up time		10		mS
Frequency		384		KHz
C1/C2 cap value		2.2		uF

Table 20. Capless Headphone Supply

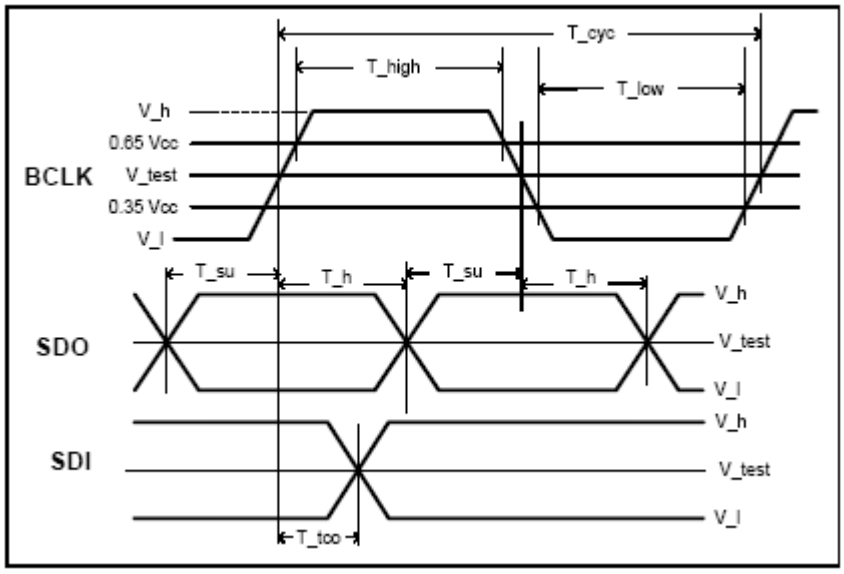
3.5. AC Timing Specs

3.5.1. HD Audio Bus Timing

Parameter	Definition	Symbol	Min	Typ	Max	Units
BCLK Frequency	Average BCLK frequency		23.9976	24.0	24.0024	Mhz
BCLK Period	Period of BCLK including jitter	Tcyc	41.163	41.67	42.171	ns
BCLK High Phase	High phase of BCLK	T_high	17.5		24.16	ns
BCLK Low Phase	Low phase of BCLK	T_low	17.5		24.16	ns
BCLK jitter	BCLK jitter			150	500	ps
SDI delay	Time after rising edge of BCLK that SDI becomes valid	T_tco	3		11	ns
SDO setup	Setup for SDO at both rising and falling edges of BCLK	T_su	5			ns
SDO hold	Hold for SDO at both rising and falling edges of BCLK	T_h	5			ns

Table 21. HD Audio Bus Timing

Figure 11. HD Audio Bus Timing



©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

3.5.2. SPDIF Timing

Parameter	Definition	Symbol	Min	Typ	Max	Units
SPDIF_OUT Frequency	highest rate of encoded signal 64 times the sample rate		2.8224	3.072	12.288	MHz
SPDIF_OUT unit interval	1/(128 times the sample rate)	UI	177.15	162.76	40.69	ns
SPDIF_OUT jitter	SPDIF_OUT jitter				4.43	ns
SPDIF_OUT rise time		T_rise			15	ns
SPDIF_OUT fall time		T_fall			15	ns

Table 22. SPDIF Timing

3.5.3. Digital Microphone Timing

Parameter	Definition	Symbol	Min	Typ	Max	Units
DMIC_CLK Frequency	Average DMIC_CLK frequency		1.176	2.352	4.704	MHz
DMIC_CLK Period	Period of DMIC_CLK	Tdmic_cyc	850.34	425.17	212.59	ns
DMIC_CLK jitter	DMIC_CLK jitter				5000	ps
DMIC Data setup	Setup for the microphone data at both rising and falling edges of DMIC_CLK	Tdmic_su	5			ns
DMIC Data hold	Hold for the microphone data at both rising and falling edges of DMIC_CLK	Tdmic_h	5			ns

Table 23. Digital Mic timing

3.5.4. GPIO Characteristics

Parameter	Definition	Symbol	Min	Typ	Max	Units
Input High Voltage[1]	input level at or above which a 1 is reliably recorded	Vih	0.6 x VDD			V
Input Low Voltage[1]	input level at or below which a 0 is reliably recorded. VDD may be DVDD or AVDD	Vil			0.35 x VDD	V
Output High Voltage	iout = 4mA VDD may be DVDD or AVDD depending on pin	Voh	0.9 x VDD			V
Output Low Voltage	iout = -4mA VDD may be DVDD or AVDD depending on pin	Vol			0.1 x VDD	V
Input rise/fall time	transition time between 10% and 90% of supply	T_rise/T_fall			10	ns
Input/Tristate High Leakage Current	Vin = VDD VDD may be DVDD or AVDD depending on pin (does not include pull-up or pull-down resistor if present)			0.5		uA
Input/Tristate Low Leakage Current	Vin = 0 VDD may be DVDD or AVDD depending on pin (does not include pull-up or pull-down resistor if present)			-50		uA

Table 24. GPIO Characteristics

1.High peak currents during dynamic switching of the Class-D PWM Outputs can result in Ground Rail Bounce. The amount of Ground Bounce should be kept below 0.35 x VDD for all Inputs, including internal logic which is tied to DVDD_CORE.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

4. FUNCTIONAL BLOCK DIAGRAM

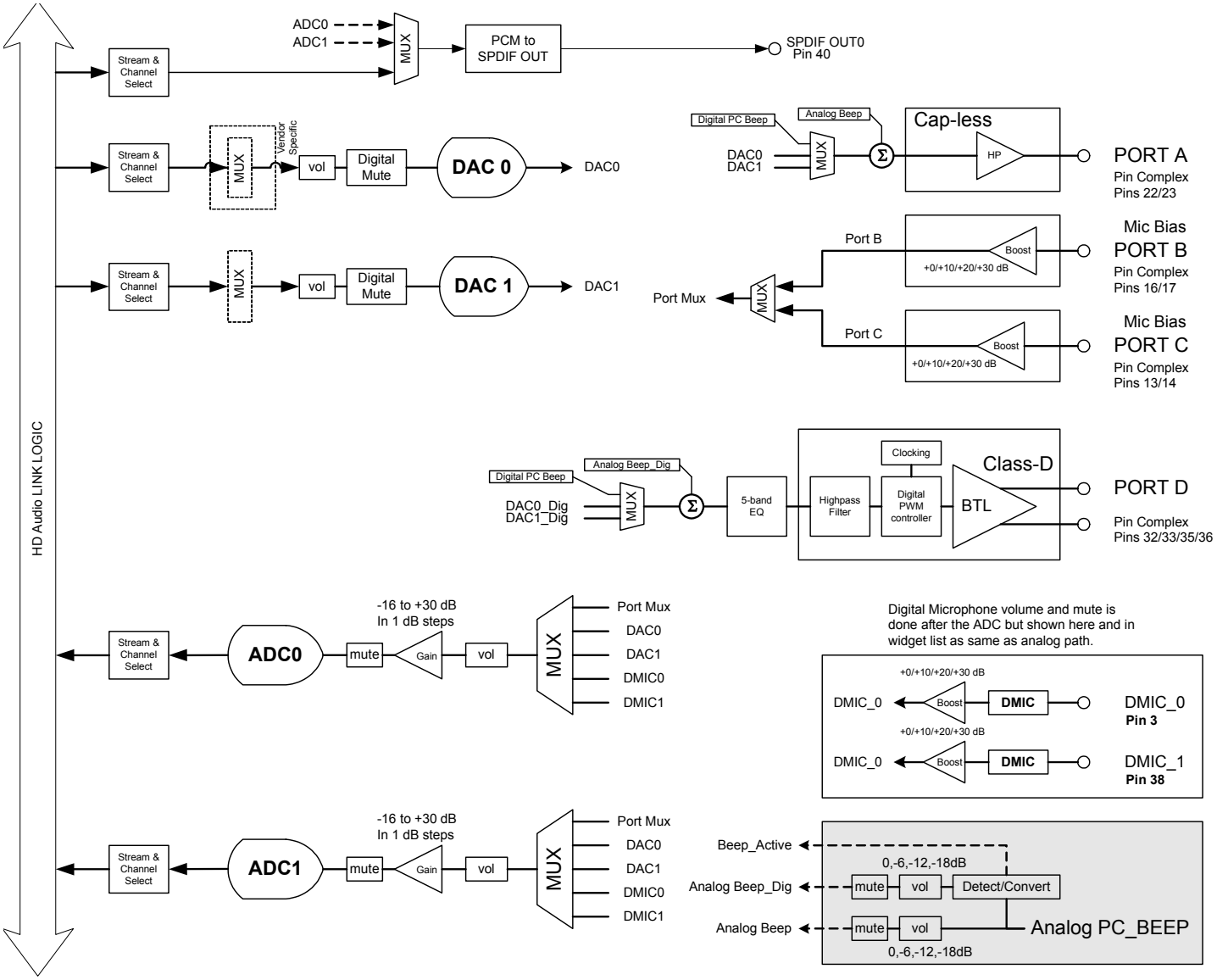


Figure 12. Functional Block Diagram

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

5. WIDGET DIAGRAM

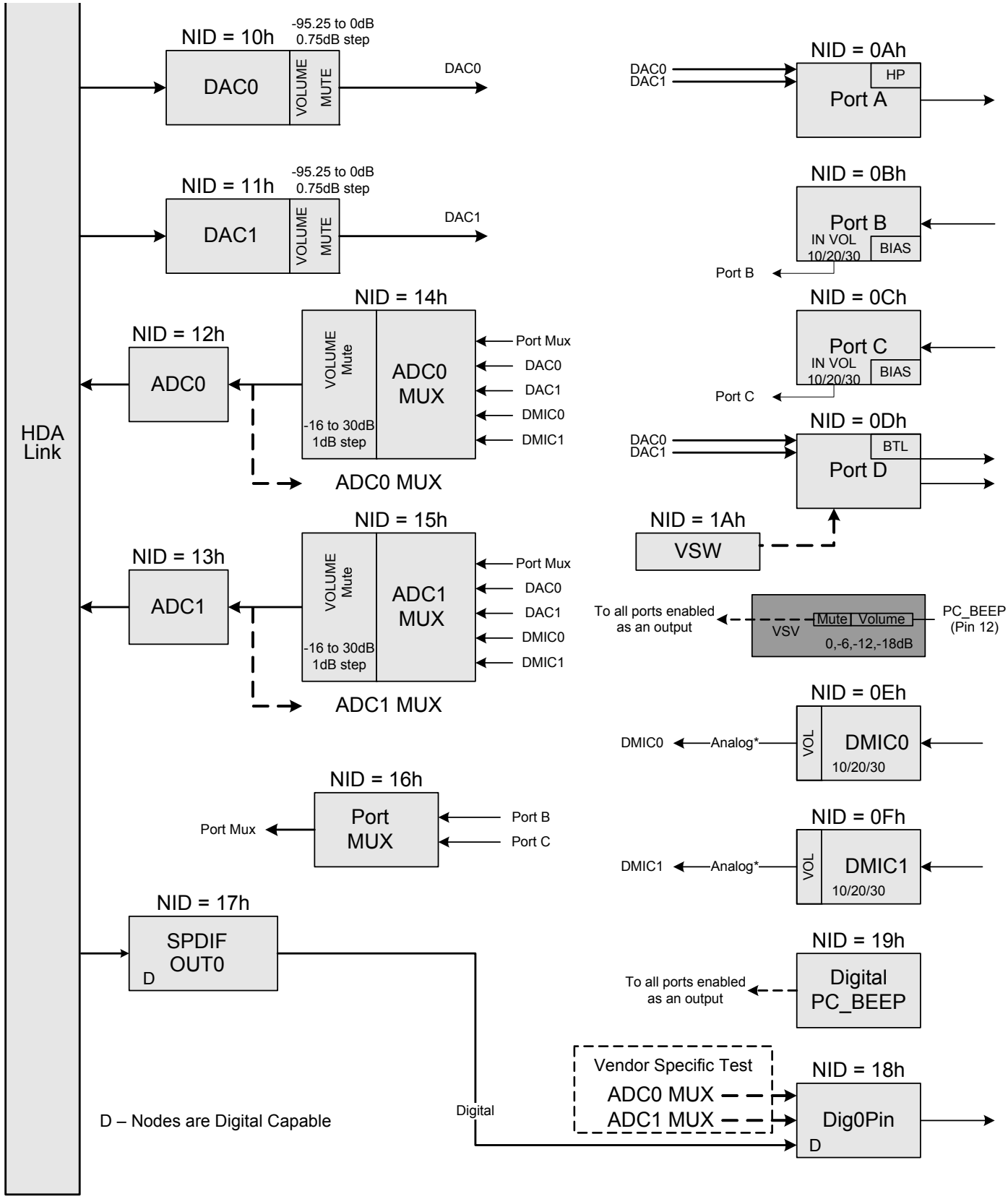


Figure 13. Widget Diagram

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

6. PORT AND PIN CONFIGURATIONS

6.1. Port Configurations

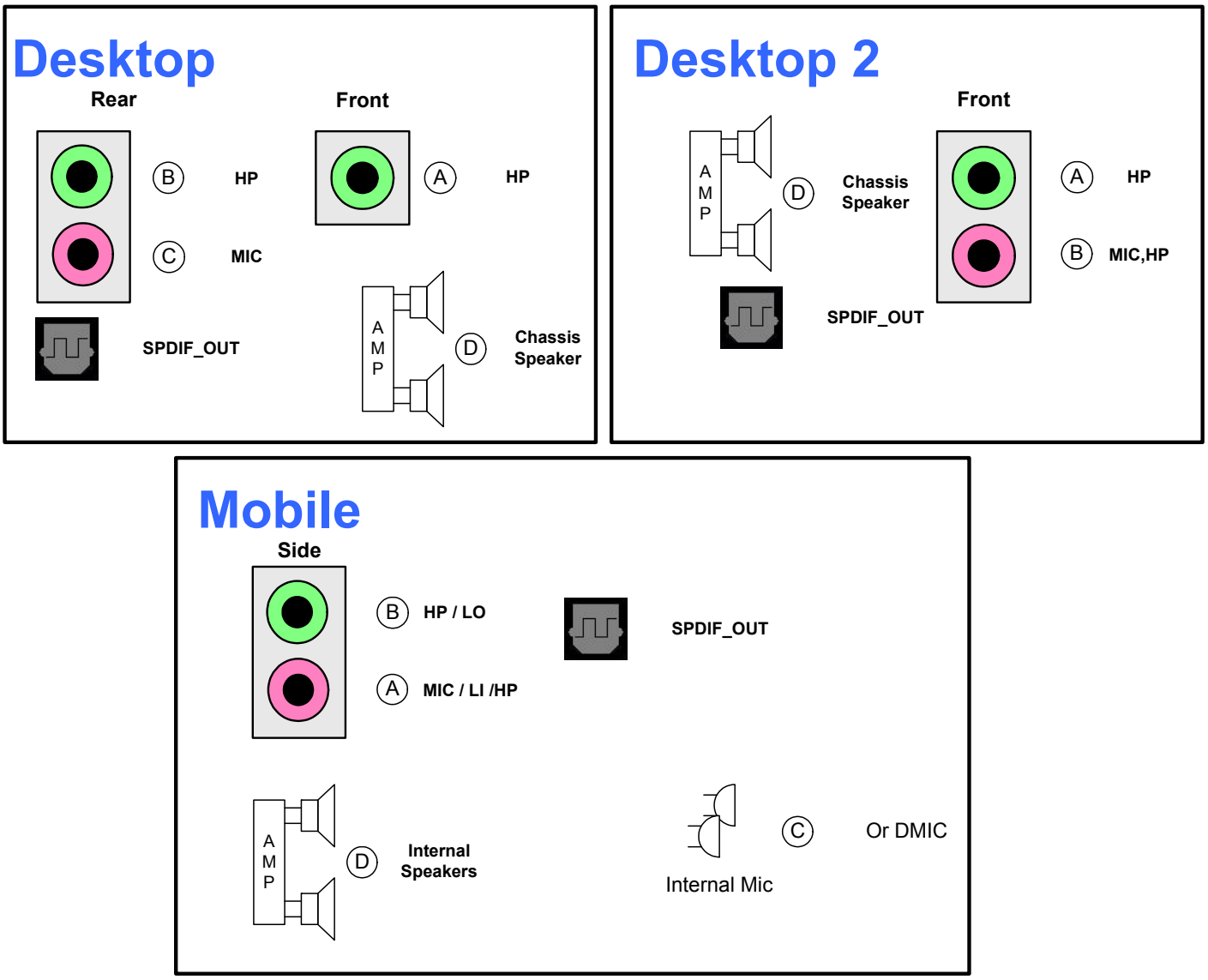


Figure 14. Port Configurations

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

6.2. Pin Configuration Default Register Settings

The following table shows the Pin Widget Configuration Default settings. Desktop implementation with 2 jacks in front and 1 jack in rear. The internal speaker is redirected from the front (green) headphone jack. An internal microphone is present.

Pin Name	Port	Location	Device	Connection	Color	Misc	Assoc.	Seq
PortAPin	Connect to Jack 00b	Mainboard Right 4h	HP Out 2h	1/8 inch Jack 1h	Green 4h	Jack Detect Override=0	1h	0h
PortBPin	Connect to Jack 00b	Mainboard Right 4h	Mic In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override=0	2h	0h
PortCPin	No Connect 01b	NA Rear 0h	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
PortDPin	Internal 10b	NA 010000b	Speaker 1h	Other Analog 7h	Unknown 0h	Jack Detect Override=1	3h	0h
DigOutPin0	No Connect 01b	NA 0h	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
DigMic0Pin	Internal 10b	Internal 010000b	Mic In Ah	ATAPI 3h	Unknown 0h	Jack Detect Override=1	4h	0h
DigMic1Pin	No Connect 01b	NA 0h	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h

Table 25. Pin Configuration Default Settings

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7. WIDGET INFORMATION

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:16]	BITS [15:0]
Reserved	CODEC Address	NID	Verb ID (4-bit)	Payload Data (16-bit)

Table 26. Command Format for Verb with 4-bit Identifier

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:8]	BITS [7:0]
Reserved	CODEC Address	NID	Verb ID (12-bit)	Payload Data (8-bit)

Table 27. Command Format for Verb with 12-bit Identifier

There are two types of responses: Solicited and Unsolicited. Solicited responses are provided as a direct response to an issued command and will be provided in the frame immediately following the command. Unsolicited responses are provided by the CODEC independent of any command. Unsolicited responses are the result of CODEC events such as a jack insertion detection. The formats for Solicited Responses and Unsolicited Responses are shown in the tables below. The “Tag” field in bits [31:28] of the Unsolicited Response identify the event.

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:0]
Valid (Valid = 1)	UnSol = 0	Reserved	Response

Table 28. Solicited Response Format

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:28]	BITS [27:0]
Valid (Valid = 1)	UnSol = 1	Reserved	Tag	Response

Table 29. Unsolicited Response Format

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.1. Widget List

ID	Widget Name	Description
00h	Root	Root Node
01h	AFG	Audio Function Group
0Ah	Port A	Port A Pin Widget (Cap-less Headphone, Line OUT)
0Bh	Port B	Port B Pin Widget (Line IN, MIC+ VrefOut)
0Ch	Port C	Port C Pin Widget (Line IN, MIC+ VrefOut)
0Dh	Port D	Port D Pin Widget (Class-D BTL output)
0Eh	DigMic0	Digital Microphone 0 Pin Widget
0Fh	DigMic1	Digital Microphone 1 Pin Widget
10h	DAC0	Stereo Output Converter to DAC
11h	DAC1	Stereo Output Converter to DAC
12h	ADC0	Stereo Input Converter to ADC
13h	ADC1	Stereo Input Converter to ADC
14h	ADC0Mux	ADC0 Mux with volume and mute
15h	ADC1Mux	ADC1 Mux with volume and mute
16h	Port Mux	Port B/C selector
17h	SPDIFOut0	Stereo Output for SPDIF_Out
18h	Dig0Pin	Digital Output Pin (pin40)
19h	PCBeep	Digital PC Beep
1Ah	VSW	BTL register access

Table 30. Widget List

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.2. Reset Key

Abbreviation	Description
POR	Power On Reset.
SAFG	Single AFG Reset - One single write to the Reset Verb in the AFG Node.
DAFG	Double AFG Reset - Two consecutive Single AFG Resets with only idle frames (if any) and no Link Resets between.
S&DAFG	Single And Double AFG Reset - Either one will cause reset.
LR	Link Reset - Level sensitive reset anytime the HDA Reset is set low.
ELR	Exiting Link Reset - Edge sensitive reset any time the HDA Reset transitions from low to high.
ULR	Unexpected Link Reset - Level sensitive reset anytime the HDA Reset is set low when the ClkStopOK indicator is currently set to 0.
PS	Power State Change - Reset anytime the Actual Power State changes for the Widget in question.

7.3. Root (NID = 00h): VendorID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0000h			

Field Name	Bits	R/W	Default	Reset
Vendor	31:16	R	111Dh	N/A
	Vendor ID.			
DeviceFix	15:8	R	see below	N/A
	Device ID.			
DeviceProg	7:0	R	see below	N/A
	Device ID.			

Device	92HD95
Device ID	7695h

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.3.1. Root (NID = 00h): VendorID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0000h			

Field Name	Bits	R/W	Default	Reset
Vendor	31:16	R	111Dh	N/A (Hard-coded)
	Vendor ID.			
DeviceFix	15:8	R	76h	N/A (Hard-coded)
	Fixed portion of Device ID.			
DeviceProg	7:0	R	95h	N/A (Hard-coded)
	Programmable portion of Device ID (top 4 bits in metal, bottom 4 bits by bond option.			

7.3.2. Root (NID = 00h): RevID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0002h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Major	23:20	R	1h	N/A (Hard-coded)
	Major rev number of compliant HD Audio spec.			
Minor	19:16	R	0h	N/A (Hard-coded)
	Minor rev number of compliant HD Audio spec.			
RevisionFix	15:12	R	xh	N/A (Hard-coded)
	Vendor's rev number for this device.			
RevisionProg	11:8	R	xh	N/A (Hard-coded)
	Vendor's rev number for this device.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
SteppingFix	7:4	R	xh	N/A (Hard-coded)
	Vendor stepping number within the Vendor RevID.			
SteppingProg	3:0	R	xh	N/A (Hard-coded)
	Vendor stepping number within the Vendor RevID.			

7.3.3. Root (NID = 00h): NodeInfo

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0004h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
StartNID	23:16	R	01h	N/A (Hard-coded)
	Starting node number (NID) of first function group			
Rsvd1	15:8	R	00h	N/A (Hard-coded)
	Reserved.			
TotalNodes	7:0	R	01h	N/A (Hard-coded)
	Total number of nodes			

7.4. AFG (NID = 01h): NodeInfo

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0004h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
StartNID	23:16	R	0Ah	N/A (Hard-coded)
	Starting node number for function group subordinate nodes.			
Rsvd1	15:8	R	00h	N/A (Hard-coded)
	Reserved.			
TotalNodes	7:0	R	11h	N/A (Hard-coded)
	Total number of nodes.			

7.4.1. AFG (NID = 01h): FGType

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0005h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:9	R	000000h	N/A (Hard-coded)
	Reserved.			
UnSol	8	R	1h	N/A (Hard-coded)
	Unsolicited response supported: 1 = yes, 0 = no.			
NodeType	7:0	R	1h	N/A (Hard-coded)
	Function group type: 00h = Reserved 01h = Audio Function Group 02h = Vendor Defined Modem Function Group 03h-7Fh = Reserved 80h-FFh = Vendor Defined Function Group			

7.4.2. AFG (NID = 01h): AFGCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0008h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd3	31:17	R	00h	N/A (Hard-coded)
	Reserved.			
BeepGen	16	R	1h	N/A (Hard-coded)
	Beep generator present: 1 = yes, 0 = no.			
Rsvd2	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
InputDelay	11:8	R	Dh	N/A (Hard-coded)
	Typical latency in frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link.			
Rsvd1	7:4	R	0h	N/A (Hard-coded)
	Reserved.			
OutputDelay	3:0	R	Dh	N/A (Hard-coded)
	Typical latency in frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin.			

7.4.3. AFG (NID = 01h): PCMCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ah			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:21	R	000h	N/A (Hard-coded)
	Reserved.			
B32	20	R	0h	N/A (Hard-coded)
	32 bit audio format support: 1 = yes, 0 = no.			
B24	19	R	1h	N/A (Hard-coded)
	24 bit audio format support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
B20	18	R	1h	N/A (Hard-coded)
	20 bit audio format support: 1 = yes, 0 = no.			
B16	17	R	1h	N/A (Hard-coded)
	16 bit audio format support: 1 = yes, 0 = no.			
B8	16	R	0h	N/A (Hard-coded)
	8 bit audio format support: 1 = yes, 0 = no.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
R12	11	R	0h	N/A (Hard-coded)
	384kHz rate support: 1 = yes, 0 = no.			
R11	10	R	1h	N/A (Hard-coded)
	192kHz rate support: 1 = yes, 0 = no.			
R10	9	R	0h	N/A (Hard-coded)
	176.4kHz rate support: 1 = yes, 0 = no.			
R9	8	R	1h	N/A (Hard-coded)
	96kHz rate support: 1 = yes, 0 = no.			
R8	7	R	1h	N/A (Hard-coded)
	88.2kHz rate support: 1 = yes, 0 = no.			
R7	6	R	1h	N/A (Hard-coded)
	48kHz rate support: 1 = yes, 0 = no.			
R6	5	R	1h	N/A (Hard-coded)
	44.1kHz rate support: 1 = yes, 0 = no.			
R5	4	R	0h	N/A (Hard-coded)
	32kHz rate support: 1 = yes, 0 = no.			
R4	3	R	0h	N/A (Hard-coded)
	22.05kHz rate support: 1 = yes, 0 = no.			
R3	2	R	0h	N/A (Hard-coded)
	16kHz rate support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
R2	1	R	0h	N/A (Hard-coded)
	11.025kHz rate support: 1 = yes, 0 = no.			
R1	0	R	0h	N/A (Hard-coded)
	8kHz rate support: 1 = yes, 0 = no.			

7.4.4. AFG (NID = 01h): StreamCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Bh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
AC3	2	R	0h	N/A (Hard-coded)
	AC-3 formatted data support: 1 = yes, 0 = no.			
Float32	1	R	0h	N/A (Hard-coded)
	Float32 formatted data support: 1 = yes, 0 = no.			
PCM	0	R	1h	N/A (Hard-coded)
	PCM-formatted data support: 1 = yes, 0 = no.			

7.4.5. AFG (NID = 01h): InAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Dh			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	0h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	27h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	03h	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	00h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.4.6. AFG (NID = 01h): PwrStateCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Fh			

Field Name	Bits	R/W	Default	Reset
EPSS	31	R	1h	N/A (Hard-coded)
	Extended power states support: 1 = yes, 0 = no.			
ClkStop	30	R	1h	N/A (Hard-coded)
	D3 clock stop support: 1 = yes, 0 = no.			
S3D3ColdSup	29	R	1h	N/A (Hard-coded)
	Codec state intended during system S3 state: 1 = D3Hot, 0 = D3Cold.			
Rsvd	28:5	R	000000h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
D3ColdSup	4	R	1h	N/A (Hard-coded)
	D3Cold power state support: 1 = yes, 0 = no.			
D3Sup	3	R	1h	N/A (Hard-coded)
	D3 power state support: 1 = yes, 0 = no.			
D2Sup	2	R	1h	N/A (Hard-coded)
	D2 power state support: 1 = yes, 0 = no.			
D1Sup	1	R	1h	N/A (Hard-coded)
	D1 power state support: 1 = yes, 0 = no.			
D0Sup	0	R	1h	N/A (Hard-coded)
	D0 power state support: 1 = yes, 0 = no.			

7.4.7. AFG (NID = 01h): GPIOCnt

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0011h			

Field Name	Bits	R/W	Default	Reset
GPIWake	31	R	1h	N/A (Hard-coded)
	Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIO's configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin.			
GPIUnsol	30	R	1h	N/A (Hard-coded)
	GPIO unsolicited response support: 1 = yes, 0 = no.			
Rsvd	29:24	R	00h	N/A (Hard-coded)
	Reserved.			
NumGPIs	23:16	R	00h	N/A (Hard-coded)
	Number of GPI pins supported by function group.			
NumGPOs	15:8	R	00h	N/A (Hard-coded)
	Number of GPO pins supported by function group.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
NumGPIOs	7:0	R	04h	N/A (Hard-coded)
	Number of GPIO pins supported by function group.			

7.4.8. AFG (NID = 01h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	02h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	7Fh	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	7Fh	N/A (Hard-coded)
	Indicates which step is 0dB			

7.4.9. AFG (NID = 01h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd3	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Function Group have been reset. Cleared by PwrState 'Get' to this Widget.			
ClkStopOK	9	R	1h	POR - DAFG - ULR
	Bit clock can currently be removed: 1 = yes, 0 = no.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7	R	0h	N/A (Hard-coded)
	Reserved.			
Act	6:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3	R	0h	N/A (Hard-coded)
	Reserved.			
Set	2:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.4.10. AFG (NID = 01h): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable: 1 = enabled, 0 = disabled.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.4.11. AFG (NID = 01h): GPIO

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				715h
Get	F1500h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
Data3	3	RW	0h	POR - DAFG - ULR
	Data for GPIO3. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22			
Data2	2	RW	0h	POR - DAFG - ULR
	Data for GPIO2. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22			
Data1	1	RW	0h	POR - DAFG - ULR
	Data for GPIO1. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22			
Data0	0	RW	0h	POR - DAFG - ULR
	Data for GPIO0. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.4.12. AFG (NID = 01h): GPIOEn

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				716h
Get	F1600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
Mask3	3	RW	0h	POR - DAFG - ULR
	Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control			
Mask2	2	RW	0h	POR - DAFG - ULR
	Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control			
Mask1	1	RW	0h	POR - DAFG - ULR
	Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control			
Mask0	0	RW	0h	POR - DAFG - ULR
	Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control			

7.4.13. AFG (NID = 01h): GPIODir

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				717h
Get	F1700h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Control3	3	RW	0h	POR - DAFG - ULR
	Direction control for GPIO3: 0 = GPIO is configured as input; 1 = GPIO is configured as output			
Control2	2	RW	0h	POR - DAFG - ULR
	Direction control for GPIO2: 0 = GPIO is configured as input; 1 = GPIO is configured as output			
Control1	1	RW	0h	POR - DAFG - ULR
	Direction control for GPIO1: 0 = GPIO is configured as input; 1 = GPIO is configured as output			
Control0	0	RW	0h	POR - DAFG - ULR
	Direction control for GPIO0: 0 = GPIO is configured as input; 1 = GPIO is configured as output			

7.4.14. AFG (NID = 01h): GPIOWakeEn

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				718h
Get	F1800h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
W3	3	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			
W2	2	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			
W1	1	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
W0	0	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			

7.4.15. AFG (NID = 01h): GPIOUnsol

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				719h
Get	F1900h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
EnMask3	3	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO3. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.			
EnMask2	2	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.			
EnMask1	1	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO1 is configured as input and changes state.			
EnMask0	0	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.			

7.4.16. AFG (NID = 01h): GPIOSticky

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				71Ah

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.4.16. AFG (NID = 01h): GPIOSticky

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F1A00h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
Mask3	3	RW	0h	POR - DAFG - ULR
	GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			
Mask2	2	RW	0h	POR - DAFG - ULR
	GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			
Mask1	1	RW	0h	POR - DAFG - ULR
	GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			
Mask0	0	RW	0h	POR - DAFG - ULR
	GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			

7.4.17. AFG (NID = 01h): SubID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	723h	722h	721h	720h
Get	F2300h / F2200h / F2100h / F2000h			

Field Name	Bits	R/W	Default	Reset
Subsys3	31:24	RW	00h	POR
	Subsystem ID (byte 3)			
Subsys2	23:16	RW	00h	POR
	Subsystem ID (byte 2)			
Subsys1	15:8	RW	01h	POR
	Subsystem ID (byte 1)			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Assembly	7:0	RW	00h	POR
	Assembly ID (Not applicable to codec vendors).			

7.4.18. AFG (NID = 01h): GPIOPIrty

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				770h
Get	F7000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
GP3	3	RW	1h	POR
	GPIO3 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			
GP2	2	RW	1h	POR
	GPIO2 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			
GP1	1	RW	1h	POR
	GPIO1 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
GP0	0	RW	1h	POR
	GPIO0 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			

7.4.19. AFG (NID = 01h): GPIODrive

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				771h
Get	F7100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
OD3	3	RW	0h	POR
	GPIO3 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1).			
OD2	2	RW	0h	POR
	GPIO2 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1).			
OD1	1	RW	0h	POR
	GPIO1 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1).			
OD0	0	RW	0h	POR
	GPIO0 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open-drain (drive 0, float for 1).			

7.4.20. AFG (NID = 01h): DMic

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				778h

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.4.20. AFG (NID = 01h): DMic

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F7800h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:6	R	0000000h	N/A (Hard-coded)
	Reserved.			
Mono1	5	RW	0h	POR
	DMic1 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel).			
Mono0	4	RW	0h	POR
	DMic0 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel).			
PhAdj	3:2	RW	0h	POR
	Selects what phase of the DMic clock the data should be latched: 0h = left data rising edge/right data falling edge 1h = left data center of high/right data center of low 2h = left data falling edge/right data rising edge 3h = left data center of low/right data center of high			
Rate	1:0	RW	2h	POR
	Selects the DMic clock rate: 0h = 4.704MHz 1h = 3.528MHz 2h = 2.352MHz 3h = 1.176MHz.			

7.4.21. AFG (NID = 01h): DACMode

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			781h	780h
Get	F8100h / F8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:9	R	000000h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
SwapEn	8	RW	0h	POR
	Internal DAC left channel and right channel swap. 0h = not swap, 1h = swap.			
SDMSettleDisable	7	RW	0h	POR
	SDM wait-to-settle disable: 1 = at mute, the SDM switches to the mute pattern immediately 0 = at mute, the SDM switches to the mute pattern after settling (can take up to ~45ms)			
SDMCoeffSel	6	RW	0h	POR
	DAC SDM coefficient select (stages 1, 2, 3): 1 = 1/16, 1/2, 1/4 0 = 1/16, 1/4, 1/2			
SDMLFHalf	5	RW	0h	POR
	DAC SDM local feedback coefficient select: 1 = 1/4096, 0 = 1/2048.			
SDMLFDisable	4	RW	0h	POR
	DAC SDM local feedback disable: 1 = local feedback disabled, 0 = local feedback enabled.			
InvertValid	3	RW	0h	POR
	DAC Valid Invert: 1 = 7.056MHz valid strobe is inverted, 0 = 7.056MHz valid strobe is not inverted.			
InvertData	2	RW	0h	POR
	DAC Data Invert: 1 = 1-bit outputs are inverted, 0 = 1-bit outputs are not inverted.			
Atten6dBDisable	1	RW	1h	POR
	Disable built-in -6dB digital attenuation: 1 = -6dB disabled, 0 = -6dB enabled.			
Fade	0	RW	1h	POR
	DAC Gain Fade Enable: 1 = gain will be slowly faded from old value to new value (~10ms) 0 = gain will jump immediately to new value.			

7.4.22. AFG (NID = 01h): ADCMode

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				784h
Get	F8400h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:5	R	0000000h	N/A (Hard-coded)
	Reserved.			
ADCGainSel	4	RW	0h	POR
	ADC boost gain selection: 1 = 1dB, 0 = 3dB.			
InvertValid	3	RW	0h	POR
	ADC Valid Invert: 1 = 14.112MHz valid strobe is inverted, 0 = 14.112MHz valid strobe is not inverted.			
InvertData	2	RW	0h	POR
	ADC Data Invert: 1 = 1-bit inputs are inverted, 0 = 1-bit inputs are not inverted.			
ADCClkDelay	1	RW	0h	POR
	Delay ADC clock.			
DACClkDelay	0	RW	0h	POR
	Delay DAC clock.			

7.4.23. AFG (NID = 01h): EAPD

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set		78Ah	789h	788h
Get	F8A00h / F8900h / F8800h			

Field Name	Bits	R/W	Default	Reset
Rsvd3	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
HPASDInv	10	RW	0h	POR
	Port A HP Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high			
HPASDMode	9	RW	1h	POR
	Port A HP Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
HPASD	8	RW	0h	POR
	Port A HP Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only			
Rsvd2	7	R	0h	N/A (Hard-coded)
	Reserved.			
BTLSDInv	6	RW	0h	POR
	BTL Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high			
BTLSDMode	5	RW	1h	POR
	BTL Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled			
BTLSD	4	RW	0h	POR
	BTL Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
PinMode	1:0	RW	0h	POR
	EAPD Pin Mode: 00b = Open Drain I/O (Value at pin is wired-AND of EAPD bit & external signal) 01b = CMOS Output (Value of EAPD bit is forced at pin) 1xb = CMOS Input (External signal controls internal amps, EAPD bit ignored)			

7.4.24. AFG (NID = 01h): PortUse

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7C0h
Get	FC000h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
PortD	3	RW	1h	POR
	1=power down port if not input or output enabled, 0=do not force power down based on input or output enable.			
PortC	2	RW	1h	POR
	1=power down port if not input or output enabled, 0=do not force power down based on input or output enable			
PortB	1	RW	1h	POR
	1=power down port if not input or output enabled, 0=do not force power down based on input or output enable			
PortA	0	RW	1h	POR
	1=power down port if not input or output enabled, 0=do not force power down based on input or output enable.			

7.4.25. AFG (NID = 01h): ComJack

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			7C7h	7C6h
Get	FC700h/FC600h			

Field Name	Bits	R/W	Default	Reset
Rsvd3	31:11	R	00000000h	N/A (Hard-coded)
	Reserved.			
RbCon	10:8	RW	4h	POR
	Combo jack detection reference voltage 000 = 0.18*AVDD 001 = 0.16*AVDD 010 = 0.14*AVDD 011 = 0.12*AVDD 100 = 0.10*AVDD 101 = 0.08*AVDD 110 = 0.06*AVDD 111 = 0.04*AVDD			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
MasterPort	7:5	RW	0h	POR
	Port tied to the jack presence detection switch 000 = Port A 001 = Port B 010 = Port C 011 = Port D 100 = Port E 101 = Port F			
Rsvd1	4	R	0h	N/A (Hard-coded)
	Reserved.			
SlavePort	3:1	RW	0h	POR
	Port used as microphone input When combo jack detection is enabled, Port presence detection as shown in the pin complex is not sensed directly by the sense input but is inferred by the load placed on the Vref_Output associated with the port 000 = Port A 001 = Port B 010 = Port C 011 = Port D;100 = Port E 101 = Port F			
Det-en	0	R	0h	POR
	0h = disable combo jact detection 1h = enable combo jact detection			

7.4.26. AFG (NID = 01h): ComboJackTime

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			7CAh	7C9h
Get	FCA00h/FC900h			

Field Name	Bits	R/W	Default	Reset
Rsvd3	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
bouncertimer_bypass	15	RW	0h	POR
	0 = all the combjack debounce time in normal; 1= all the comjack debounce time in simulation mode(debounce time is short).			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
t_delay_slave_port_usr	14:12	RW	3h	POR
	000 = 2frame 001 =4frame 010 =8frame 011 =16frame 100 = 32frame 101 =64frame 110 = 128frame 111 = 256frame			
t_stable	11:8	RW	6h	POR
	0000 = 0.1ms 0001 =0.5ms 0010 =1ms 0011 =2ms 0100 = 4ms 0101 =8ms 0110 = 16ms 0111 = 32ms 1000 = 64ms 1001 =128ms;1010 =256ms;1011 =512ms 1100 = 1024ms 1101 =1024ms 1110 = 1024ms 1111 = 1024ms			
RSVD2	7	R	0h	N/A (Hard-coded)
	Reserved			
t_long_realtime_detect	6:4	RW	5h	POR
	000 = 2s 001 =4s 010 =8s 011 =16s 100 = 32s 101 =64s 110 = 128s 111 = infinite			
RSVD1	3	R	0h	N/A (Hard-coded)
	Reserved			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
t_delay_verfout	2:0	RW	3h	POR
	000 = 0.1ms 001 =50ms 010 = 125ms 011 =250ms 100 = 500ms 101 = 1s 110 = 2s 111 = 4s			

7.4.27. AFG (NID = 01h): VSPwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7D8h
Get	FD800h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
D5	1	RW	0h	POR - ELR
	Vendor specific D5 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If set, this bit overrides the D4 bit (bit 0). Includes the power savings of D4, but additionally powers down GPIO pins, the VAG amp, and the HP amps. Exits this power state via POR or rising edge of Link Reset.			
D4	0	RW	0h	POR - ELR
	Vendor specific D4 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If the D5 bit (bit 1) is set, this bit is overridden. Includes the power savings of D3cold, but additionally powers down the HDA interface (no responses). Exit this power state via POR or rising edge of Link Reset.			

7.4.28. AFG (NID = 01h): AnaPort

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7ECh
Get	FEC00h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
DPwd	3	RW	0h	POR
	Power down Port D.			
CPwd	2	RW	0h	POR
	Power down Port C.			
BPwd	1	RW	0h	POR
	Power down Port B.			
APwd	0	RW	0h	POR
	Power down Port A.			

7.4.29. AFG (NID = 01h): AnaBeep

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			7EFh	7EEh
Get	FEE00h / FEE00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:14	R	00000h	N/A (Hard-coded)
	Reserved.			
Detect	13	R	0h	POR - DAFG - ULR
	0: no beep present; 1: beep present.			
GainAdj	12:10	RW	3h	POR
	Analog PC Beep Gain in digital side 7h = -6dB, 6h = -12dB, 5h = -18dB, 4h = -24dB, 3h = -30dB, 2h = -36dB, 1h = -42dB, 0h = -48dB.			
ConvertEn	9	RW	1h	POR
	Analog pc beep quantization enable (enabled only when both ""d2a_ana_pc_beep_det_en"" and ""d2a_ana_pc_beep_convert_en"" are 1).			
DetectEn	8	RW	1h	POR
	Analog pc beep detection enable 0h = disable 1h = enable.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd1	7:6	R	0h	N/A (Hard-coded)
Gain	5:4	RW	3h	POR
	Analog PC Beep Gain: 0h = -24dB, 1h = -18dB, 2h = -12dB, 3h = -6dB.			
CntSel	3:2	RW	0h	POR
	Select counter delay.0h=64ms,1h = 128ms, 2h = 256ms, 3h = 512ms.			
Mode	1:0	RW	2h	POR
	Analog PC Beep Mode: 00b = Always disabled 01b = Always enabled 1Xb = Enabled during HDA Link Reset only			

7.4.30. AFG (NID = 01h): AnaBTL

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set		7F6h	7F5h	7F4h
Get	FF600h / FF500h / FF400h			

Field Name	Bits	R/W	Default	Reset
Rsvd6	31:22	R	000h	N/A (Hard-coded)
	Reserved.			
SCStableTimeSel	21:20	RW	0h	POR
	The programmed time window for short circuit detect.			
TSOverrideHiz	19	RW	0h	POR
	Override Hiz for the BTL amplifier power stage circuit: set to 1 to Hiz, set back to 0 to normal mode			
TSTestMode	18	RW	0h	POR
	Temp sense test mode select, 0=normal operation, 1=sensor will trip at ambient temperature.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
TSForcePwd	17	RW	1h	POR
	Temp sense force powerdown select 0=BTL will not be muted and powered down even if it is still overheating when the volume is 0h 1=BTL will be muted and powered down even if it is still overheating when the volume is 0h			
TSInstantCutMode	16	RW	0h	POR
	Temp sense instant cut mode 0=Two trip points used to smoothly adjust the volume 1=One single trip point used to set volume to wither 0 or max value (TI mode)			
TSWait	15:12	RW	3h	POR
	Temperature sensing wait time between volume increments 0h = 2ms (polling at 2ms) 1h = 4ms (polling at 4ms) 2h = 8ms (polling at 8ms) 3h = 16ms (polling at 16ms) 4h = 32ms (polling at 16ms) 5h = 64ms (polling at 16ms) 6h = 128ms (polling at 16ms) 7h = 256ms (polling at 16ms) 8h = 512ms (polling at 16ms) 9h = 1.024s (polling at 16ms) Ah = 2.048s (polling at 16ms) Bh = 4.096s (polling at 16ms) Ch = 8.192s (polling at 16ms) Dh = 16.384s (polling at 16ms) Eh = 32.768s (polling at 16ms) Fh = 65.536s (polling at 16ms).			
TSTripHish	11:9	RW	3h	POR
	Temp sense high trip point setting: 0h = 125 Degrees C 1h =140 Degrees C 2h = 155 Degrees C 3h = 170 Degrees C 4h = 185 C 5h = 200 C 6h = 215 C 7h = Reserved			
TSOverrideRest	8	RW	0h	POR
	Override reset for the BTL amplifier Temp sense circuit: set to 1 to recalculate, set back to 0 to latch the value			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
TSTripLow	7:5	RW	2h	POR
	Temp sense low trip point setting: 0h = 110 Degrees C 1h = 125 Degrees C 2h = 140 Degrees C 3h = 155 Degrees C 4h = 170 C 5h = 185 C 6h = 200 C 7h = 215 C			
ClassDMono	4	RW	0h	POR
	Config BTL to mono mode. 0:stereo 1:Mono			
MonoSpkvolSelEn	3	RW	0h	POR
	BTL right channel spkvol selection enable under mono mode. 0:keep right channel spkvol; 1:select left channel spkvol.			
DCBypass	2	RW	0h	POR
	1 = Bypass BTL DC filter			
Rsvd1	1:0	R	0h	NA
	Reserved			

7.4.31. AFG (NID = 01h): AnaBTLStatus

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	FF700h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:20	R	000h	N/A (Hard-coded)
	Reserved.			
TSTripHigh	19	R	0h	POR
	Temp sense high trip point status			
TSTripLow	18	R	0h	POR
	Temp sense low trip point status			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
TSMute	17	R	0h	POR
	Temp sense forced mute status for BTL amplifier			
TSPwd	16	R	0h	POR
	Temp sense forced powerdown status for BTL amplifier			
TSLeftVol	15:8	R	FFh	POR
	Temp sense volume status for the BTL amplifier: 00000000b..11111111b = Range specified for SPKVol field.			
TSRightVol	7:0	R	FFh	POR
	Temp sense volume status for the BTL amplifier: 00000000b..11111111b = Range specified for SPKVol field.			

7.4.32. AFG (NID = 01h): AnaCapless

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	7FBh	7FAh	7F9h	7F8h
Get	FFB00h / FFA00h / FF900h / FF800h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31	R	0h	N/A (Hard-coded)
	Reserved.			
PwdAnaMd	30	RW	1h	POR
	Power down analog select block.			
AnaSelEn	29	RW	0h	POR
	1=enable analog select mode, 0=enable digital select mode.			
MdLevSel	28	RW	0h	POR
	1=selct high threshold level of analog mode, 0=select low threshold level of analog mode			
ClasGBypass	27	RW	0h	POR
	0=clasg enable, 1=bypass clasg, only class ab work			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd3	26	R	0h	N/A (Hard-coded)
	Reserved.			
VRegSCDet	25	R	0h	POR
	Capless regulator short circuit detect indicator.			
ChargePumpSCDet	24	R	0h	POR
	Capless charge pump short circuit detect indicator.			
VRegSel	23:20	RW	5h	POR
	Capless regulator output voltage multiply ratio Bits [3..2] Reserved Bits [1..0]: 00b = 2*Vbg 01b = 2.1*Vbg 10b = 2.2*Vbg 11b = 2.3*Vbg			
VRegSCRstB	19	RW	0h	POR
	Capless regulator short circuit detect reset: 0 = short circuit detect disabled, 1 = short circuit detect enabled.			
VRegGndShort	18	RW	0h	POR
	Ground the capless regulator output.			
VRegPwd	17	RW	0h	POR
	Capless regulator powerdown.			
ChargePumpSCRstB	16	RW	0h	POR
	Capless charge pump short circuit detect reset: 0 = short circuit detect disabled, 1 = short circuit detect enabled.			
ChargePumpHiZ	15	RW	0h	POR
	Hi-Z the capless charge pump outputs.			
ChargePumpPwd	14	RW	0h	POR
	Capless charge pump powerdown.			
ChargePumpSplyDetOverride	13	RW	0h	POR
	Capless charge pump supply detect override.			
Rsvd2	12	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ChargePumpClkRate	11:8	RW	8h	POR
	Capless charge pump clock rate: 0000b = 800.0kHz (24MHz/30) 0001b = 750.0kHz (24MHz/32) 0010b = 706.9kHz (24MHz/34) 0011b = 666.7kHz (24MHz/36) 0100b = 631.6kHz (24MHz/38) 0101b = 600.0kHz (24MHz/40) 0110b = 571.4kHz (24MHz/42) 0111b = 545.5kHz (24MHz/44) 1000b = 800.0kHz (24MHz/30) 1001b = 857.1kHz (24MHz/28) 1010b = 923.1kHz (24MHz/26) 1011b = 1.000MHz (24MHz/24) 1100b = 1.091MHz (24MHz/22) 1101b = 1.200MHz (24MHz/20) 1110b = 1.333MHz (24MHz/18) 1111b = 1.500MHz (24MHz/16)			
ChargePumpClkDiv	7:5	RW	4h	POR
	Capless charge pump analog clock divider: 001b = No divide 010b = Divide by 2, 50% duty cycle 100b = Divide by 4, 50% duty cycle 110b = Divide by 2, 75% duty cycle 011b = Divide by 4, 75% duty cycle 111b = Divide by 4, 87.5% duty cycle Other values undefined			
ChargePumpClkSel	4	RW	0h	POR
	Capless charge pump clock select: 0 = ring oscillator, 1 = charge pump clock defined by AFGCaplessChargePumpClkRate[3:0] field below.			
PadGnd	3	RW	0h	POR
	Ground the output pad of the capless amplifiers.			
InputGnd	2	RW	0h	POR
	Ground the input to the capless output amplifiers.			
Rsvd1	1	R	0h	NA
	Reserved			
AntiPopBypass	0	RW	0h	POR
	0 = Enable anti-pop on the capless headphone; 1 = bypass anti-pop on the capless headphone.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.4.33. AFG (NID = 01h): Reset

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7FFh
Get	FFF00h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Execute	7:0	W	00h	N/A (Hard-coded)
	Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The codec should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.5. PortA (NID = 0Ah): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.5.1. PortA (NID = 0Ah): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	0h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	1h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

7.5.2. PortA (NID = 0Ah): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	02h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.5.3. PortA (NID = 0Ah): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Reserved.			
ConL1	15:8	R	11h	N/A (Hard-coded)
	DAC1 Converter widget (0x11)			
ConL0	7:0	R	10h	N/A (Hard-coded)
	DAC0 Converter widget (0x10)			

7.5.4. PortA (NID = 0Ah): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:1	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.5.5. PortA (NID = 0Ah): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.5.6. PortA (NID = 0Ah): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
HPhnEn	7	RW	0h	POR - DAFG - ULR
	Headphone amp enable: 1 = enabled, 0 = disabled.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	R	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:3	R	0h	N/A (Hard-coded)
	Reserved.			
VRefEn	2:0	R	0h	POR - DAFG - ULR
	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved			

7.5.7. PortA (NID = 0Ah): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.5.8. PortA (NID = 0Ah): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.5.9. PortA (NID = 0Ah): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.5.10. PortA (NID = 0Ah): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Location	29:24	RW	04h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	2h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	4h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	1h	POR
	Default association.			
Sequence	3:0	RW	0h	POR
	Sequence.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.6. PortB (NID = 0Bh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.6.1. PortB (NID = 0Bh): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
VrefCntrl	15:8	R	17h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	0h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

7.6.2. PortB (NID = 0Bh): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.6.3. PortB (NID = 0Bh): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.6.4. PortB (NID = 0Bh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.6.5. PortB (NID = 0Bh): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	5:0	RW	00h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
VRefEn	2:0	RW	0h	POR - DAFG - ULR
	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved			

7.6.6. PortB (NID = 0Bh): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.6.7. PortB (NID = 0Bh): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.6.8. PortB (NID = 0Bh): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.6.9. PortB (NID = 0Bh): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	04h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	Ah	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	9h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	2h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.7. PortC (NID = 0Ch): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.7.1. PortC (NID = 0Ch): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
VrefCntrl	15:8	R	17h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	0h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

7.7.2. PortC (NID = 0Ch): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.7.3. PortC (NID = 0Ch): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.7.4. PortC (NID = 0Ch): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.7.5. PortC (NID = 0Ch): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	0000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	R	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:3	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
VRefEn	2:0	RW	0h	POR - DAFG - ULR
	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved			

7.7.6. PortC (NID = 0Ch): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.7.7. PortC (NID = 0Ch): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.7.8. PortC (NID = 0Ch): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.7.9. PortC (NID = 0Ch): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	1h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	00h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	Fh	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	0h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	0h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	Fh	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.8. PortD (NID = 0Dh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.8.1. PortD (NID = 0Dh): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	1h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	0h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	0h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

7.8.2. PortD (NID = 0Dh): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	02h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.8.3. PortD (NID = 0Dh): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Reserved			
ConL2	23:16	R	00h	N/A (Hard-coded)
	MixerOutVol Selector widget (0x1C)			
ConL1	15:8	R	11h	N/A (Hard-coded)
	DAC1 Converter widget (0x11)			
ConL0	7:0	R	10h	N/A (Hard-coded)
	DAC0 Converter widget (0x10)			

7.8.4. PortD (NID = 0Dh): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.8.5. PortD (NID = 0Dh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.8.6. PortD (NID = 0Dh): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	000000h	N/A (Hard-coded)
	Reserved.			
HPhnEn	7	R	0h	POR - DAFG - ULR
	Headphone amp enable: 1 = enabled, 0 = disabled.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	R	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	0h	N/A (Hard-coded)
	Reserved.			

7.8.7. PortD (NID = 0Dh): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.8.8. PortD (NID = 0Dh): EsdRest

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				780h
Get	F8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:1	R	00000000h	N/A (Hard-coded)
	Reserved.			
Execute	0	W	0h	N/A (Hard-coded)
	Reset_b the esd trigger block. Low active.			

7.8.9. PortD (NID = 0Dh): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	2h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Location	29:24	RW	10h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	1h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	7h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	0h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	1h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	3h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.9. DMic0 (NID = 0Eh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.9.1. DMic0 (NID = 0Eh): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			
EapdCap	16	R	0h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
VRefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	0h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HPhnDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	0h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

7.9.2. DMic0 (NID = 0Eh): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.9.3. DMic0 (NID = 0Eh): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.9.4. DMic0 (NID = 0Eh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.9.5. DMic0 (NID = 0Eh): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:6	R	0000000h	N/A (Hard-coded)
	Reserved.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	00h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.9.6. DMic0 (NID = 0Eh): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	2h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	10h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Device	23:20	RW	Ah	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			
ConnectionType	19:16	RW	3h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Color	15:12	RW	0h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	1h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	4h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

7.10. DMic1 (NID = 0Fh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.10.1. DMic1 (NID = 0Fh): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			
EapdCap	16	R	0h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VRefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	0h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HPhnDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	0h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

7.10.2. DMic1 (NID = 0Fh): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.10.3. DMic1 (NID = 0Fh): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.10.4. DMic1 (NID = 0Fh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.10.5. DMic1 (NID = 0Fh): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:6	R	0000000h	N/A (Hard-coded)
	Reserved.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.10.6. DMic1 (NID = 0Fh): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	1h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	00h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	Fh	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	0h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	0h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	Fh	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.11. DAC0 (NID = 10h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.11.1. DAC0 (NID = 10h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.11.2. DAC0 (NID = 10h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.11.3. DAC0 (NID = 10h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.11.4. DAC0 (NID = 10h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.11.5. DAC0 (NID = 10h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.11.6. DAC0 (NID = 10h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

7.12. DAC1 (NID = 11h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.12.1. DAC1 (NID = 11h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.12.2. DAC1 (NID = 11h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.12.3. DAC1 (NID = 11h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.12.4. DAC1 (NID = 11h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.12.5. DAC1 (NID = 11h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.12.6. DAC1 (NID = 11h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.13. ADC0 (NID = 12h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	1h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ProcWidget	6	R	1h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.13.1. ADC0 (NID = 12h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.13.2. ADC0 (NID = 15h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL0	7:0	R	14h	N/A (Hard-coded)
	ADC0Mux Selector widget (0x14)			

7.13.3. ADC0 (NID = 15h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.13.4. ADC0 (NID = 12h): ProcState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				703h
Get	F0300h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
HPFOCDIS	7	RW	0h	POR - DAFG - ULR
	HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled.			
Rsvd1	6:2	R	00h	N/A (Hard-coded)
	Reserved.			
ADCHPFByp	1:0	RW	1h	POR - DAFG - ULR
	Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign").			

7.13.5. ADC0 (NID = 12h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.13.6. ADC0 (NID = 12h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.14. ADC1 (NID = 13h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	1h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	1h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.14.1. ADC1 (NID = 13h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.14.2. ADC1 (NID = 13h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL0	7:0	R	15h	N/A (Hard-coded)
	ADC1Mux widget (0x18)			

7.14.3. ADC1 (NID = 13h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.14.4. ADC1 (NID = 13h): ProcState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				703h
Get	F0300h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
HPFOCDIS	7	RW	0h	POR - DAFG - ULR
	HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd1	6:2	R	00h	N/A (Hard-coded)
	Reserved.			
ADCHPFByp	1:0	RW	1h	POR - DAFG - ULR
	Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign").			

7.14.5. ADC1 (NID = 13h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.14.6. ADC1 (NID = 1Bh): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.15. ADC0Mux (NID = 14h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParamOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.15.1. ADC0Mux (NID = 14h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	05h	N/A (Hard-coded)
	Number of NID entries in connection list			

7.15.2. ADC0Mux (NID = 14h): ConLstEntry4

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0204h			

Field Name	Bits	R/W	Default	Reset
ConL7	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL6	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL5	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL4	7:0	R	0Fh	N/A (Hard-coded)
	DMIC 1 widget (0x0F)			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.15.3. ADC0Mux (NID = 14h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	0Eh	N/A (Hard-coded)
	DMIC 0 widget (0x0E)			
ConL2	23:16	R	11h	N/A (Hard-coded)
	DAC1 widget (0x11)			
ConL1	15:8	R	10h	N/A (Hard-coded)
	DAC0 widget (0x10)			
ConL0	7:0	R	16h	N/A (Hard-coded)
	PortMux widget (0x16)			

7.15.4. ADC0Mux (NID = 14h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	03h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
NumSteps	14:8	R	2Eh	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	10h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.15.5. ADC0Mux (NID = 14h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	5:0	RW	10h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.15.6. ADC0Mux (NID = 14h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	5:0	RW	10h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.15.7. ADC0Mux (NID = 14h): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	2:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.15.8. ADC0Mux (NID = 14h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.15.9. ADC0Mux (NID = 14h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.16. ADC1Mux (NID = 15h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParamOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.16.1. ADC1Mux (NID = 15h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	05h	N/A (Hard-coded)
	Number of NID entries in connection list.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.16.2. ADC1Mux (NID = 15h): ConLstEntry4

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0204h			

Field Name	Bits	R/W	Default	Reset
ConL7	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL6	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL5	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL4	7:0	R	0Fh	N/A (Hard-coded)
	DMIC 1 widget (0x0F)			

7.16.3. ADC1Mux (NID = 15h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	0Eh	N/A (Hard-coded)
	DMIC 0 widget (0x0E)			
ConL2	23:16	R	11h	N/A (Hard-coded)
	DAC1 widget (0x11)			
ConL1	15:8	R	10h	N/A (Hard-coded)
	DAC0 widget (0x10)			
ConL0	7:0	R	16h	N/A (Hard-coded)
	PortMux widget (0x16)			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.16.4. ADC1Mux (NID = 15h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	03h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	2Eh	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	10h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.16.5. ADC1Mux (NID = 15h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	5:0	RW	10h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.16.6. ADC1Mux (NID = 15h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	5:0	RW	10h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.16.7. ADC1Mux (NID = 15h): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	2:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.16.8. ADC1Mux (NID = 15h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.16.9. ADC1Mux (NID = 15h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

7.17. PortMux (NID = 16h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.17.1. PortMux (NID = 16h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	02h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.17.2. PortMux (NID = 16h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Reserved.			
ConL1	15:8	R	0Bh	N/A (Hard-coded)
	PortB pin widget (0x0B)			
ConL0	7:0	R	0Ch	N/A (Hard-coded)
	PortC pin widget (0x0C)			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.17.3. PortMux (NID = 16h): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	0000000h	N/A (Hard-coded)
	Reserved.			
Index	1:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.17.4. PortMux (NID = 16h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.18. SPDIFOut0 (NID = 17h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	4h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	1h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	1h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.18.1. SPDIFOut0 (NID = 17h): PCMCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ah			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:21	R	000h	N/A (Hard-coded)
	Reserved.			
B32	20	R	0h	N/A (Hard-coded)
	32 bit audio format support: 1 = yes, 0 = no.			
B24	19	R	1h	N/A (Hard-coded)
	24 bit audio format support: 1 = yes, 0 = no.			
B20	18	R	1h	N/A (Hard-coded)
	20 bit audio format support: 1 = yes, 0 = no.			
B16	17	R	1h	N/A (Hard-coded)
	16 bit audio format support: 1 = yes, 0 = no.			
B8	16	R	0h	N/A (Hard-coded)
	8 bit audio format support: 1 = yes, 0 = no.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
R12	11	R	0h	N/A (Hard-coded)
	384kHz rate support: 1 = yes, 0 = no.			
R11	10	R	1h	N/A (Hard-coded)
	192kHz rate support: 1 = yes, 0 = no.			
R10	9	R	0h	N/A (Hard-coded)
	176.4kHz rate support: 1 = yes, 0 = no.			
R9	8	R	1h	N/A (Hard-coded)
	96kHz rate support: 1 = yes, 0 = no.			
R8	7	R	1h	N/A (Hard-coded)
	88.2kHz rate support: 1 = yes, 0 = no.			
R7	6	R	1h	N/A (Hard-coded)
	48kHz rate support: 1 = yes, 0 = no.			
R6	5	R	1h	N/A (Hard-coded)
	44.1kHz rate support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
R5	4	R	0h	N/A (Hard-coded)
	32kHz rate support: 1 = yes, 0 = no.			
R4	3	R	0h	N/A (Hard-coded)
	22.05kHz rate support: 1 = yes, 0 = no.			
R3	2	R	0h	N/A (Hard-coded)
	16kHz rate support: 1 = yes, 0 = no.			
R2	1	R	0h	N/A (Hard-coded)
	11.025kHz rate support: 1 = yes, 0 = no.			
R1	0	R	0h	N/A (Hard-coded)
	8kHz rate support: 1 = yes, 0 = no.			

7.18.2. SPDIFOut0 (NID = 17h): StreamCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Bh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
AC3	2	R	1h	N/A (Hard-coded)
	AC-3 formatted data support: 1 = yes, 0 = no.			
Float32	1	R	0h	N/A (Hard-coded)
	Float32 formatted data support: 1 = yes, 0 = no.			
PCM	0	R	1h	N/A (Hard-coded)
	PCM-formatted data support: 1 = yes, 0 = no.			

7.18.3. SPDIFOut0 (NID = 17h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.18.3. SPDIFOut0 (NID = 17h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	00h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	00h	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	00h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.18.4. SPDIFOut0 (NID = 17h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
FrmtNonPCM	15	RW	0h	POR - DAFG - ULR
	Stream type: 1 = Non-PCM, 0 = PCM.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.18.5. SPDIFOut0 (NID = 17h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.18.6. SPDIFOut0 (NID = 17h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.18.7. SPDIFOut0 (NID = 1Dh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.18.8. SPDIFOut0 (NID = 17h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.18.9. SPDIFOut0 (NID = 17h): DigCnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	73Fh	73Eh	70Eh	70Dh
Get	F0E00h / F0D00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
KeepAlive	23	RW	0h	POR - DAFG - ULR
	Keep Alive Enable: 1 = clocking information maintained during D3, 0 = clock information not required during D3.			
Rsvd1	22:15	R	00h	N/A (Hard-coded)
	Reserved.			
CC	14:8	RW	00h	POR - DAFG - ULR
	CC: Category Code.			
L	7	RW	0h	POR - DAFG - ULR
	L: Generation Level.			
PRO	6	RW	0h	POR - DAFG - ULR
	PRO: Professional.			
AUDIO	5	RW	0h	POR - DAFG - ULR
	/AUDIO: Non-Audio.			
COPY	4	RW	0h	POR - DAFG - ULR
	COPY: Copyright.			
PRE	3	RW	0h	POR - DAFG - ULR
	PRE: Preemphasis.			
VCFG	2	RW	0h	POR - DAFG - ULR
	VCFG: Validity Config.			
V	1	RW	0h	POR - DAFG - ULR
	V: Validity.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
DigEn	0	RW	0h	POR - DAFG - ULR
	Digital enable: 1 = converter enabled, 0 = converter disable.			

7.19. Dig0Pin (NID = 18h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	1h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.19.1. Dig0Pin (NID = 18h): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	0h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	0h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

7.19.2. Dig0Pin (NID = 18h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.19.3. Dig0Pin (NID = 18h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL0	7:0	R	17h	N/A (Hard-coded)
	SPDIFOut0 Converter widget (0x17)			

7.19.4. Dig0Pin (NID = 18h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.19.5. Dig0Pin (NID = 18h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	0000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd1	5:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.19.6. Dig0Pin (NID = 18h): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.19.7. Dig0Pin (NID = 18h): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.19.8. Dig0Pin (NID = 18h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	1h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	00h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Device	23:20	RW	Fh	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			
ConnectionType	19:16	RW	0h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Color	15:12	RW	0h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	Fh	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

7.20. DigBeep (NID = 19h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:24	R	00h	N/A (Hard-coded)
	Reserved.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Type	23:20	R	7h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Rsvd3	19:11	R	000h	N/A (Hard-coded)
	Reserved.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no."			
Rsvd2	9:4	R	00h	N/A (Hard-coded)
	Reserved			
AmpParOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

7.20.1. DigBeep (NID = 19h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	17h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	03h	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	03h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.20.2. DigBeep (NID = 19h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:2	R	00h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	1h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.20.3. DigBeep (NID = 19h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.20.4. DigBeep (NID = 19h): Gen

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ah
Get	F0A00h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Divider	7:0	RW	00h	POR - DAFG - LR
	Enable internal PC-Beep generation. Divider == 00h disables internal PC Beep generation and enables normal operation of the codec. Divider != 00h generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale).			

7.20.5. DigBeep (NID = 19h): Gain

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				77Ah
Get	F7A00h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	000000h	N/A (Hard-coded)
	Reserved.			
Divider	2:0	RW	05h	POR - DAFG - LR
	Digital PC Beep Gain adjust in digital side 0h = -9dB, 1h = -6dB, 2h = -3dB, 3h = 0dB, 4h = +3db, 5h = +6db			

7.21. AdvancedFunctions (NID = 1Ah): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

This register is reset by POR

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	Fh	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	0h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Field Name	Bits	R/W	Default	Reset
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

All registers are available when in normal mode through the HD Audio interface. Most are implemented using vendor defined verbs but some (volume controls specifically) are supported through standard verbs at the pin widgets

7.21.1. AdvancedFunctions (NID = 1Ah): Cntrl0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				77?h
Get	F7?00h			

This register is reset by POR

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	F7?0077?,, Please refer to the class-D register description.			
Value	7:0	RW	00h	POR - DAFG - ULR
	Control register value of I2C module.			

7.21.2. AdvancedFunctions (NID = 1Ah): Cntrl1

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				78?h
Get	F8?00h			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

This register is reset by POR

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	F8?0078?,, Please refer to the class-D register description.			
Value	7:0	RW	00h	POR - DAFG - ULR
	Control register value of I2C module.			

7.21.3. AdvancedFunctions (NID = 1Ah): Cntrl2

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				79?h
Get	F9?00h			

This register is reset by POR

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	F9?0079?,, Please refer to the class-D register description.			
Value	7:0	RW	00h	POR - DAFG - ULR
	Control register value of I2C module.			

7.21.4. AdvancedFunctions (NID = 1Ah): Cntrl3

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7A?h
Get	FA?00h			

This register is reset by POR

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	FA?007A?,, Please refer to the class-D register description.			
Value	7:0	RW	00h	POR - DAFG - ULR
	Control register value of I2C module.			

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.21.4.1. SPKVOL L/R Registers.

Register Address	Bit	Label	Type	Default	Description
verb F71/771 (Left) verb F72/772 (Right) verb 773 (Left and Right - write only)	7:0	VOL[7:0]	RW	30	+36 to -91.5dB in 0.75dB steps 0x00 = +36dB 0x01 = +35.25dB ... 0x2F = +0.75dB 0x30 = 0dB 0x31 = -0.75dB ... 0xA9 = -90.75 0xAA to 0xFE = -91.5dB 0xFF = mute

Note: Register values reset by POR or by writing to the reset register.

7.21.4.2. PWRM Register

Register Address	Bit	Label	Type	Default	Description
verb F79/779	7	RSVD	RO	0	Reserved
	6	RSVD	RO	0	Reserved
	5	RSVD	RO	0	Reserved
	4	HPPWD	RW	0	Reserved
	3	SPKRON	RW	0	Reserved
	2	DMICPWD	RW	0	Reserved
	1	RSVD	RO	1	Reserved
	0	AUXEn	RO	0	Reserved

Note: Register values reset by POR or by writing to the reset register.

7.21.4.3. RESET Register

Register Address	Bit	Label	Type	Default	Description
verb F7F/77F	7:0	RESET	RW	0	Writing causes registers to revert to their default values (similar to a function group reset). EQRAM contents (EQ coefficients and EQ prescale) are not affected.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.21.4.4. STATUS Register

Register Address	Bit	Label	Type	Default	Description
verb F80/780	7	limit1latch	RO	0	Latched version of limit1, clear via GAINCTRL_LO[7]
	6	limit0latch	RO	0	Latched version of limit0, clear via GAINCTRL_LO[7]
	5:3	Reserved	RO	0x0	RESERVED
	2	limit1	RO	0	Set (1) if regz saturation after gain multiply for CH1. may change on a sample by sample basis.
	1	limit0	RO	0	Set (1) if regz saturation after gain multiply for CH0. may change on a sample by sample basis.
	0	zerodet_flag	RO	0	Set when input zero detect of long string of zeroes.

Note: Register values reset by POR or by writing to the reset register.

7.21.4.5. INIT Register

Register Address	Bit	Label	Type	Default	Description
verb F81/781	7:4	Reserved	RO	0	RESERVED
	3	anabeep_dcbyp	RW	0	1 = bypass analog Beep DC filter
	2:1	anabeep_dc_coef f	RW	0x2	0: dc_coef = 24'h004000; 1: dc_coef = 24'h001000; 2: dc_coef = 24'h000400; 3: dc_coef = 24'h000100;
	0	Initialize	RW	0	1= Initialize/soft reset data path. Must be set when changing the config0 or config1 registers.

Note: Register values reset by POR or by writing to the reset register.

7.21.4.6. CONFIG Register

Register Address	Bit	Label	Type	Default	Description
verb F82/782	7	RSVD	RW	0	Reserved
	6	PREBYP	RW	1	1= Bypass BTL EQ filter prescale
	5	EQBYP	RW	1	1= Bypass BTL EQ filter
	4:1	Reserved	RW	0	Reserved
	0	HPFBYP	RO	0	1= Bypass BTL high-pass filter (not DC removal filter)

Note: Register values reset by POR or by writing to the reset register.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.21.4.7. PWM4 Register.

Register Address	Bit	Label	Type	Default	Description
verb F83/783	7	sc_status_clear_right	RWC	0	Write once operation will clear sc_fault_status_right
	6	sc_status_clear_left	RWC	0	Write once operation will clear sc_fault_status_left
	5	Reserved	RO	0	RESERVED
	4	sc_Fault_status_right	RO	0	1 = Fault occurs on right channel
	3	sc_Fault_status_left	RO	0	1 = Fault occurs on left channel
	2:1	scdly_set	RW	00	Used for short circuit detection; designer will set the value
	0	evenbit	RW	0	1=Noise Shaper output data are even

Note: Register values reset by POR or by writing to the reset register.

7.21.4.8. PWM3 Register

Register Address	Bit	Label	Type	Default	Description
verb F84/784	7:6	outctrl	RW	0	pwm output muxing 0 = normal 1 = swap 0/1 2 = ch0 on both 3 = ch1 on both
	5:0	cvalue	RW	0x2	Tristate constant value filed, must be even and not 0

Note: Register values reset by POR or by writing to the reset register.

7.21.4.9. PWM2 Register

Register Address	Bit	Label	Type	Default	Description
verb F85/785	7:2	dvalue	RW	0x10	dvalue constant field.
	1	pwm_outflip	RW	0	1= swap pwm a/b output pair for all channels
	0	pwm_outmode	RW	1	1= tristate, 0 = binary

Note: Register values reset by POR or by writing to the reset register.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.21.4.10. PWM1Register

Register Address	Bit	Label	Type	Default	Description
verb F86/786	7	Reserved	RO	0	RESERVED
	6:2	dithpos	RW	0	Dither position, where dither inserted after NS 0,1,2 = dither bits 2:0 4 = dither bits 3:1 5 = dither bits 4:1 ... 19 = dither bits 19:17
	1	dither_range	RW	0	1= dither -1 to +1, 0 = dither -3 to +3
	0	dithclr	RW	0	1 = disable dither

Note: Register values reset by POR or by writing to the reset register.

7.21.4.11. PWM0 Register

Register Address	Bit	Label	Type	Default	Description
verb F87/787	7:6	PhaseOffset	RW	01	PWM ch1 offset from ch0 at 8x sample rate by: 00 = 0 degrees 01 = 90 degrees 10 = 180 degrees 11 = NA
	5	clk320mode	R	1	1 = PCA clock 320 mode 0 = PCA clock 294 mode
	4	roundup	RW	1	1= roundup, 0 = truncate for quantizer
	3	bfclr	RW	0	1 = disable binomial filter
	2	fourthorder	RW	0	1 = fourth order binomial filter, 0 = 3rd order binomial filter
	1	add3_sel	RW	0	1 = 24-bit Noise Shaper output (pre-quantizer), 0 = 8/9/10-bit quantizer output
	0	Btl_test_mode	RW	0	1 = power stage test mode

Note: Register values reset by POR or by writing to the reset register.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.21.4.12. LMTCTRL Register

Control operation of the volume Limiter (Compressor).

Register Address	Bit	Label	Type	Default	Description
verb F88/788	7:4	–	RO	0	Reserved for future use.
	3	zerocross	RW	0	1 = only change limiter gain value on zero cross.
	2:1	stepsize	RW	0	Gain stepsize when incrementing or decrementing: 0 - 0.75 dB, 1 - 1.5 dB, 2 - 3.0 dB, 3 - 6.0 dB
	0	limiter_en	RW	0	1 = enable limiter (compressor)

Note: Register values reset by POR or by writing to the reset register.

7.21.4.13. LMTATKTIME (0x19), LMTHOLDTIME (0x1A), LMTRELTIME (0x1B) Registers

These 8-bit registers set the timer values between incrementing/decrementing the Compressor attenuation values. There is one register each for Attack, Hold, and Release times, the configuration parameters are the same for all three and are shown in the table below..

Register Address	Bit	Label	Type	Default	Description
verb F89/789	7	ATK10ms	RW	0	1 = value in bits 6:0 is in 10ms units, otherwise 1ms units.
	6:0	LMTAT[6:0]	RW	0	Timer value in units of 1 or 10ms.

Register Address	Bit	Label	Type	Default	Description
verb F8A/78A	7	HOLD10ms	RW	0	1 = value in bits 6:0 is in 10ms units, otherwise 1ms units.
	6:0	LMTHT[6:0]	RW	0	Timer value in units of 1 or 10ms.

Register Address	Bit	Label	Type	Default	Description
verb F8B/78B	7	REL10ms	RW	0	1 = value in bits 6:0 is in 10ms units, otherwise 1ms units.
	6:0	LMTRT[6:0]	RW	0	Timer value in units of 1 or 10ms.

Note: Register values reset by POR or by writing to the reset register.

7.21.4.14. LMTATKTH (0x1D–LO, 0x1C–HI), LMTRELTH (0x1F–LO, 0x1E–HI) Registers

These 16-bit registers set the threshold values. When in attack phase and the Attack Threshold is exceeded the Compressor attenuation is incremented by stepsize (see LMTCTRL). When in release phase and the Release Threshold is not exceeded the Compressor attenuation is incremented by stepsize (but not above 0)..

Register Address	Bit	Label	Type	Default	Description
verb F8C/78C	7:0	LATKTH[15:8]	RW	7F	8'hFF would equal threshold level of +2.0dB. Each step below this 8-bit full scale value reduces threshold level by 0.0078 dB.

Register Address	Bit	Label	Type	Default	Description
verb F8D/78D	7:0	LATKTH[7:0]	RW	FF	Always 0. It isn't necessary to provide threshold resolution to the point where these lower 8 bits would be used.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Register Address	Bit	Label	Type	Default	Description
verb F8E/78E	7:0	LRELTH[15:8]	RW	0	8'hFF would equal threshold level of +2.0dB. Each step below this 8-bit full scale value reduces threshold level by 0.0078 dB.

Register Address	Bit	Label	Type	Default	Description
verb F8F/78F	7:0	LRELTH[7:0]	RW	0	Always 0. It isn't necessary to provide threshold resolution to the point where these lower 8 bits would be used.

7.21.4.15. GAINCTRL_HI Register.

Register Address	Bit	Label	Type	Default	Description
verb F90/790	7:5	Reserved	RO	0	RESERVED
	4:3	zerodetlen	RW	0x2	enable mute if input consecutive zeros exceeds this length: 00 = 32 01 = 1000 10 = 2000 11 = 4000
	2:0	step_time	RW	0x5	step time units = 1<<step_time, units in GAINCTRL_LO bit 5

Note: Register values reset by POR or by writing to the reset register.

7.21.4.16. GAINCTRL_LO Register.

Register Address	Bit	Label	Type	Default	Description
verb F91/791	7	clr_latch	RW	0	1 = clear limit 0/1 latches, see STATUS register
	6	RSVD	RO	0	Reserved
	5	step_10ms	RW	0	1 = units for step_time are 10ms 0 = units for step_time are 1ms
	4	stepped_change	RW	0	1 = step volume progressively to new setting
	3	disable_gain	RW	0	1 = disable all gain functions (bypass gain multiply)
	2	auto_mute	RW	1	1 = auto mute if detect long strings of zeros on input
	1	change_mode	RW	0	1 = change gain immediately 0 = change on zero cross
	0	mute_mode	RW	1	1 = hard mute after reset, 0 = soft mute

Note: Register values reset by POR or by writing to the reset register.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.21.4.17. MUTE Register.

Register Address	Bit	Label	Type	Default	Description
verb F92/792	7:3	Reserved	RO	0x0	RESERVED
	2	Mute	RW	0	1 = mute all channels
	1	mute1	RW	0	1 = mute ch1
	0	mute0	RW	0	1 = mute ch0

Note: Register values reset by POR or by writing to the reset register.

7.21.4.18. ATTEN Register.

Register Address	Bit	Label	Type	Default	Description
verb F93/793	7:0	atten	RW	0x0	Attenuation. Each bit represents 0.5dB of attenuation to be applied to the channel. The range will be -125dB to 2dB as follows: 0x00: +2dB 0x01: +1.5dB 0x02: +1.0dB ... 0x47: -33.5dB 0x48: -34.0dB 0x49: -34.5dB ... 0xFE: -125dB 0xFF: Hard Master Mute

Note: Register values reset by POR or by writing to the reset register.

7.21.4.19. DC_COEF_SEL Register

Register Address	Bit	Label	Type	Default	Description
verb F94/794	7:3	Reserved	RO	0	RESERVED
	2:0	dc_coef_sel	RW	0x5	0:dc_coef = 24'h100000; //2^^-3 = 0.125 1:dc_coef = 24'h040000; 2:dc_coef = 24'h010000; 3:dc_coef = 24'h004000; 4:dc_coef = 24'h001000; 5:dc_coef = 24'h000400; 6:dc_coef = 24'h000100; //2^^-15 = 0.000330517 7:dc_coef = 24'h000040; //2^^-17

Note: Register values reset by POR or by writing to the reset register.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.21.4.20. BTL High-Pass Filter COEF_SEL Register.

Register Address	Bit	Label	Type	Default	Description
verb F95/795	7:3	Reserved	RO	0	RESERVED
	2:0	hp_coef_sel	RW	0x2	Select IIR coefficients for BTL amplifier high pass filter corner frequency 000 = 100Hz 001 = 200Hz **010 = 300Hz** 011 = 400Hz 100 = 500Hz 101 = 750Hz 110 = 1000Hz 111 = 2000Hz

Note: Register values reset by POR or by writing to the reset register.

7.21.4.21. BTL Class-D Power Stage Register Settings

Register Address	Bit	Label	Type	Default	Description
verb F97/797	7	ENABLE	RW	1	1 = Enable BTL Power stage
	6	TRC_ESD	RO	0	1 = ESD trigger detected 0 = No trigger
	5	STRENDRV	RW	0	1 = Strengthen pre-drive 0 = Normal
	4:3	SCTHR	RW	01	Short circuit threshold current 00 = 10% of PVDD 01 = 14% of PVDD 10 = 16% of PVDD 11 = 20% of PVDD
	2:0	DEADTIME	RW	001	Dead time for output FETs 000 = 0.5ns 001 = 1.0ns 010 = 1.5ns 011 = 2ns 100 = 4ns 101 = 8ns 110 = 8ns 111 = 8ns

.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Register Address	Bit	Label	Type	Default	Description
verb F98/798	7	TEST_EN	RW	0	1 = Enable short circuit test
	6	SC_DIS	RW	0	1 = disable short circuit protection
	5	RSVD	RW	0	Reserved
	4	FAULT_SC	RO	0	1 = Fault
	3	RSVD	RW	0	Reserved
	2	PNSEL	RW	0	1=PFET tested, 0=NFET tested
	1	FORCE_SC	RW	0	1 = force short circuit
	0	TEST	RW	0	1 = Pos PFET / Neg NFET on, 0 = Pos NFET / Neg PFET on

Register Address	Bit	Label	Type	Default	Description
verb F99/799	7	ENABLE	RW	1	1 = Enable BTL Power stage
	6	TRC_ESD	RO	0	1 = ESD trigger detected 0 = No trigger
	5	STRENDRV	RW	0	1 = Strengthen pre-drive 0 = Normal
	4:3	SCTHR	RW	01	Short circuit threshold current 00 = 10% of PVDD 01 = 14% of PVDD 10 = 16% of PVDD 11 = 20% of PVDD
	2:0	DEADTIME	RW	001	Dead time for output FETs 000 = 0.5ns 001 = 1.0ns 010 = 1.5ns 011 = 2ns 100 = 4ns 101 = 8ns 110 = 8ns 111 = 8ns

Register Address	Bit	Label	Type	Default	Description
verb F9A/79A	7	TEST_EN	RW	0	1 = Enable short circuit test
	6	SC_DIS	RW	0	1 = disable short circuit protection
	5	RSVD	RW	0	Reserved
	4	FAULT_SC	RO	0	1 = Fault
	3	RSVD	RW	0	Reserved
	2	PNSEL	RW	0	1=PFET tested, 0=NFET tested
	1	FORCE_SC	RW	0	1 = force short circuit
	0	TEST	RW	0	1 = Pos PFET / Neg NFET on, 0 = Pos NFET / Neg PFET on

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Note: Register values reset by POR or by writing to the reset register.

7.21.4.22. LDO LEVEL CONTROL Register.

Register Address	Bit	Label	Type	Default	Description
verb F9B/79B	7:3	Reserved	RO	0x0	RESERVED
	2	Lv_QUAD_BIAS	RO	0	RESERVED
	1:0	Lv_reg_cntrl_bit	RW	0x0	Two bits are defined to program the output of the 1.8V LDO 00 = normal operation (3.3V in to 1.8V out) 01 = 1.8V*1.1 = 1.98V 10 = 1.8V*0.9 = 1.62V 11 = power down LDO/bypass. When disabled, the DVDD_Core pin must be supplied with a nominal 1.8V from an external source.

Note: Register values reset by POR only.

7.21.4.23. EQRAM

The EQ RAM is a 52 x 48-bit SRAM that contains the EQ coefficients..

Address	Channel RIGHT Coefficients (24bit)	Channel LEFT Coefficients (24bit)
EQRAM Bits	[47:24]	[23:00]
	based on 44.1Khz sample rate	
0x00	EQ_COEF_F0_B0	EQ_COEF_F0_B0
0x01	EQ_COEF_F0_B1	EQ_COEF_F0_B1
0x02	EQ_COEF_F0_B2	EQ_COEF_F0_B2
0x03	EQ_COEF_F0_A1	EQ_COEF_F0_A1
0x04	EQ_COEF_F0_A2	EQ_COEF_F0_A2
0x05	EQ_COEF_F1_B0	EQ_COEF_F1_B0
0x06	EQ_COEF_F1_B1	EQ_COEF_F1_B1
0x07	EQ_COEF_F1_B2	EQ_COEF_F1_B2
0x08	EQ_COEF_F1_A1	EQ_COEF_F1_A1
0x09	EQ_COEF_F1_A2	EQ_COEF_F1_A2
0x0A	EQ_COEF_F2_B0	EQ_COEF_F2_B0
0x0B	EQ_COEF_F2_B1	EQ_COEF_F2_B1
0x0C	EQ_COEF_F2_B2	EQ_COEF_F2_B2
0x0D	EQ_COEF_F2_A1	EQ_COEF_F2_A1
0x0E	EQ_COEF_F2_A2	EQ_COEF_F2_A2
0x0F	EQ_COEF_F3_B0	EQ_COEF_F3_B0
0x10	EQ_COEF_F3_B1	EQ_COEF_F3_B1
0x11	EQ_COEF_F3_B2	EQ_COEF_F3_B2
0x12	EQ_COEF_F3_A1	EQ_COEF_F3_A1
0x13	EQ_COEF_F3_A2	EQ_COEF_F3_A2
0x14	EQ_COEF_F4_B0	EQ_COEF_F4_B0
0x15	EQ_COEF_F4_B1	EQ_COEF_F4_B1
0x16	EQ_COEF_F4_B2	EQ_COEF_F4_B2

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Address	Channel RIGHT Coefficients (24bit)	Channel LEFT Coefficients (24bit)
EQRAM Bits	[47:24]	[23:00]
0x17	EQ_COEF_F4_A1	EQ_COEF_F4_A1
0x18	EQ_COEF_F4_A2	EQ_COEF_F4_A2
0x19	EQ_PRESCALE	EQ_PRESCALE
	based on 48Khz sample rate	
0x1A	EQ_COEF_F0_B0	EQ_COEF_F0_B0
0x1B	EQ_COEF_F0_B1	EQ_COEF_F0_B1
0x1C	EQ_COEF_F0_B2	EQ_COEF_F0_B2
0x1D	EQ_COEF_F0_A1	EQ_COEF_F0_A1
0x1E	EQ_COEF_F0_A2	EQ_COEF_F0_A2
0x1F	EQ_COEF_F1_B0	EQ_COEF_F1_B0
0x20	EQ_COEF_F1_B1	EQ_COEF_F1_B1
0x21	EQ_COEF_F1_B2	EQ_COEF_F1_B2
0x22	EQ_COEF_F1_A1	EQ_COEF_F1_A1
0x23	EQ_COEF_F1_A2	EQ_COEF_F1_A2
0x24	EQ_COEF_F2_B0	EQ_COEF_F2_B0
0x25	EQ_COEF_F2_B1	EQ_COEF_F2_B1
0x26	EQ_COEF_F2_B2	EQ_COEF_F2_B2
0x27	EQ_COEF_F2_A1	EQ_COEF_F2_A1
0x28	EQ_COEF_F2_A2	EQ_COEF_F2_A2
0x29	EQ_COEF_F3_B0	EQ_COEF_F3_B0
0x2A	EQ_COEF_F3_B1	EQ_COEF_F3_B1
0x2B	EQ_COEF_F3_B2	EQ_COEF_F3_B2
0x2C	EQ_COEF_F3_A1	EQ_COEF_F3_A1
0x2D	EQ_COEF_F3_A2	EQ_COEF_F3_A2
0x2E	EQ_COEF_F4_B0	EQ_COEF_F4_B0
0x2F	EQ_COEF_F4_B1	EQ_COEF_F4_B1
0x30	EQ_COEF_F4_B2	EQ_COEF_F4_B2
0x31	EQ_COEF_F4_A1	EQ_COEF_F4_A1
0x32	EQ_COEF_F4_A2	EQ_COEF_F4_A2
0x33	EQ_PRESCALE	EQ_PRESCALE

The EQRAM is programmed indirectly through the Control Bus in the following manner:
1) Write the 48-bit write data to the EQRAM_WRITE register
2) Write the target address to the EQ_ADDRESS register
3) Set bit 7 of the EQRAM_CTRL register
The write will occur when the EQRAM is not being accessed by the DSP audio processing routines. When complete the hardware will automatically clear this bit.

Reading back from the EQRAM is done in the following manner:
1) Write target address to EQ_ADDR register
2) Set bit 6 of the EQRAM_CTRL register
When the hardware completes the read it will automatically clear this bit.
3) When bit 6 of the EQRAM_CTRL register has been cleared, read the 48bit data from the EQRAM_READ register.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

7.21.4.24. EQRAM Read Data (0x30–0x35), EQRAM Write Data (0x36–3B) Registers

These two 48-bit registers (addressed as 12 8-bit registers) are 48-bit data holding registers used-when doing indirect writes/reads to the EQRAM..]]

Register Address	Bit	Label	Type	Default	Description
EQRAM_READ[47:40] verb FA0/7A0	7:0	EQRD[47:40]	RW	0x00	48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_READ[39:32] verb FA1/7A1	7:0	EQRD[39:32]	RW	0x00	48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_READ[31:24] verb FA2/7A2	7:0	EQRD[31:24]	RW	0x00	48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_READ[23:16] verb FA3/7A3	7:0	EQRD[23:16]	RW	0x00	48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_READ[15:8] verb FA4/7A4	7:0	EQRD[15:8]	RW	0x00	48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_READ[7:0] verb FA5/7A5	7:0	EQRD[7:0]	RW	0x00	48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_WRITE[47:40] verb FA6/7A6	7:0	EQWD[47:40]	RW	0x00	48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_WRITE[39:32] verb FA7/7A7	7:0	EQWD[39:32]	RW	0x00	48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Register Address	Bit	Label	Type	Default	Description
EQRAM_WRITE[31:24] verb FA8/7A8	7:0	EQWD[31:24]	RW	0x00	48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_WRITE[23:16] verb FA9/7A9	7:0	EQWD[23:16]	RW	0x00	48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_WRITE[15:8] verb FAA/7AA	7:0	EQWD[15:8]	RW	0x00	48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields.

Register Address	Bit	Label	Type	Default	Description
EQRAM_WRITE[7:0] verb FAB/7AB	7:0	EQWD[7:0]	RW	0x00	48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields.

Note: Register values reset by POR or by writing to the reset register.

7.21.4.25. EQRAM Address Register

This 8-bit register provides the address to the internal RAM when doing indirect writes/reads to the EQRAM..

Register Address	Bit	Label	Type	Default	Description
verb FAC/7AC	7:6	RSVD	RO	0x00	Reserved
	5:0	EQADD[5:0]	RW	0x00	Contains the address (between 0x00 and 0x33) of the EQRAM to be accessed by a read or write. This is not a byte address--it is the address of the 48-bit data item to be accessed from the EQRAM.

Note: Register values reset by POR or by writing to the reset register.

7.21.4.26. EQRAM Control Register

This control register provides the write/read enable when doing indirect writes/reads to the EQRAM.

Register Address	Bit	Label	Type	Default	Description
verb FAD/7AD	7	EQRAM_wr	RW	0	1 = write to EQRAM, cleared by HW when done
	6	EQRAM_rd	RW	0	1 = read from EQRAM, cleared by HW when done
	5:0	RSVD	RO	0	Reserved

Note: Register values reset by POR or by writing to the reset register.

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

8. PINOUT AND PACKAGING

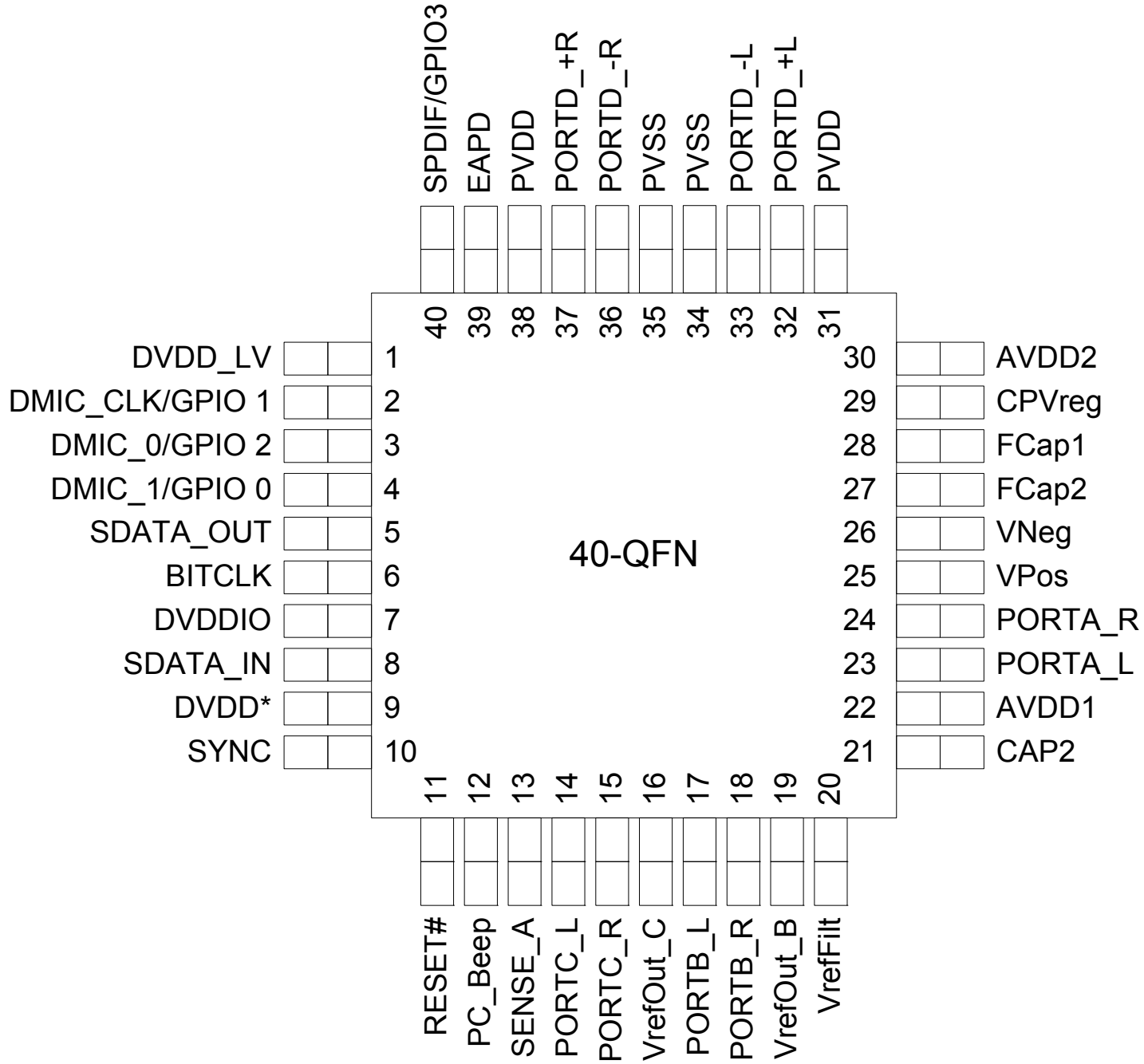


Figure 15. 40-QFN Pin Assignment

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

8.0.1. 40-QFN Pin Table

Pin Name	Pin Function	I/O	Internal Pull-up/Pull-down	40 pin location
DVDD_LV	1.8V Digital Core Regulator Filter Cap	O(Digital)	None	1
DMIC_CLK/GPIO1	Digital Mic Clock Output/GPIO1	I/O(Digital)	60K Pull-down	2
DMIC0/GPIO2	Digital Mic 01 Input/GPIO2	I/O(Digital)	60K Pull-down	3
DMIC1/GPIO0	Digital Mic 23 Input/GPIO0	I/O(Digital)	60K Pull-down	4
SDATA_OUT	HD Audio Serial Data output from controller	I/O(Digital)	None	5
BITCLK	HD Audio Bit Clock	I(Digital)	None	6
DVDD_IO	HD Audio bus signal level 3.3V or 1.5V	I(Digital)	None	7
SDATA_IN	HD Audio Serial Data Input to controller	O(Digital)	None	8
DVDD	Digital Vdd= 3.3V	I(Digital)	None	9
SYNC	HD Audio Frame Sync	I(Digital)	None	10
RESET#	HD Audio Reset	I(Digital)	None	11
PCBEEP	PC Beep	I(Analog)	None	12
SENSE_A	Jack insertion detection Ports A,B,C	I(Analog)	None	13
PORTC_L	Port C Left	I(Analog)	None	14
PORTC_R	Port C Right	I(Analog)	None	15
VREFOUT-C	Port C Microphone Bias	O(Analog)	None	16
PORTB_L	Port B Left	I(Analog)	None	17
PORTB_R	Port B Right	I(Analog)	None	18
VREFOUT-B	Port B Microphone Bias	O(Analog)	None	19
VREFFILT	Analog Virtual Ground	O(Analog)	None	20
CAP2	Reference filter Cap	O(Analog)	None	21
AVDD1	Analog Vdd= 3.3V	I(Analog)	None	22
PORTA_L	Port A Output Left	O(Analog)	None	23
PORTA_R	Port A Output Right	O(Analog)	None	24
VPos	Positive headphone supply	O(Analog)	None	25
VNeg	Negative headphone supply	O(Analog)	None	26
FCap2	Charge pump flying cap	O(Analog)	None	27
FCap1	Charge pump flying cap	O(Analog)	None	28
CPVreg	Linear Regulator Output filter cap	O(Analog)	None	29
AVDD2	Analog Supply for VREG	I(Analog)	None	30
PVDD	Analog Supply for Class-D amp	I(Analog)	None	31
PORTD_+L	BTL amp Left +	O(Analog)	None	32
PORTD_-L	BTL amp Left -	O(Analog)	None	33
PVSS	Analog Ground	I(Analog)	None	34
PVSS	Analog Ground	I(Analog)	None	35
PORTD_-R	BTL amp Right -	O(Analog)	None	36
PORTD_+R	BTL amp Right +	O(Analog)	None	37

Table 31. 40QFN Pin Description

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

Pin Name	Pin Function	I/O	Internal Pull-up/Pull-down	40 pin location
PVDD	Analog Supply for Class-D amp	I(Analog)	None	38
EAPD	EAPD	I/O (Digital)	60K Pull-up	39
SPDIFOUT/GPIO3	SPDIF Output or GPIO3	I/O (Digital)	60K Pull-down	40

Table 31. 40QFN Pin Description

8.0.2. 40-QFN Package Outline and Package Dimensions

Package dimensions are kept current with JEDEC Publication No. 95

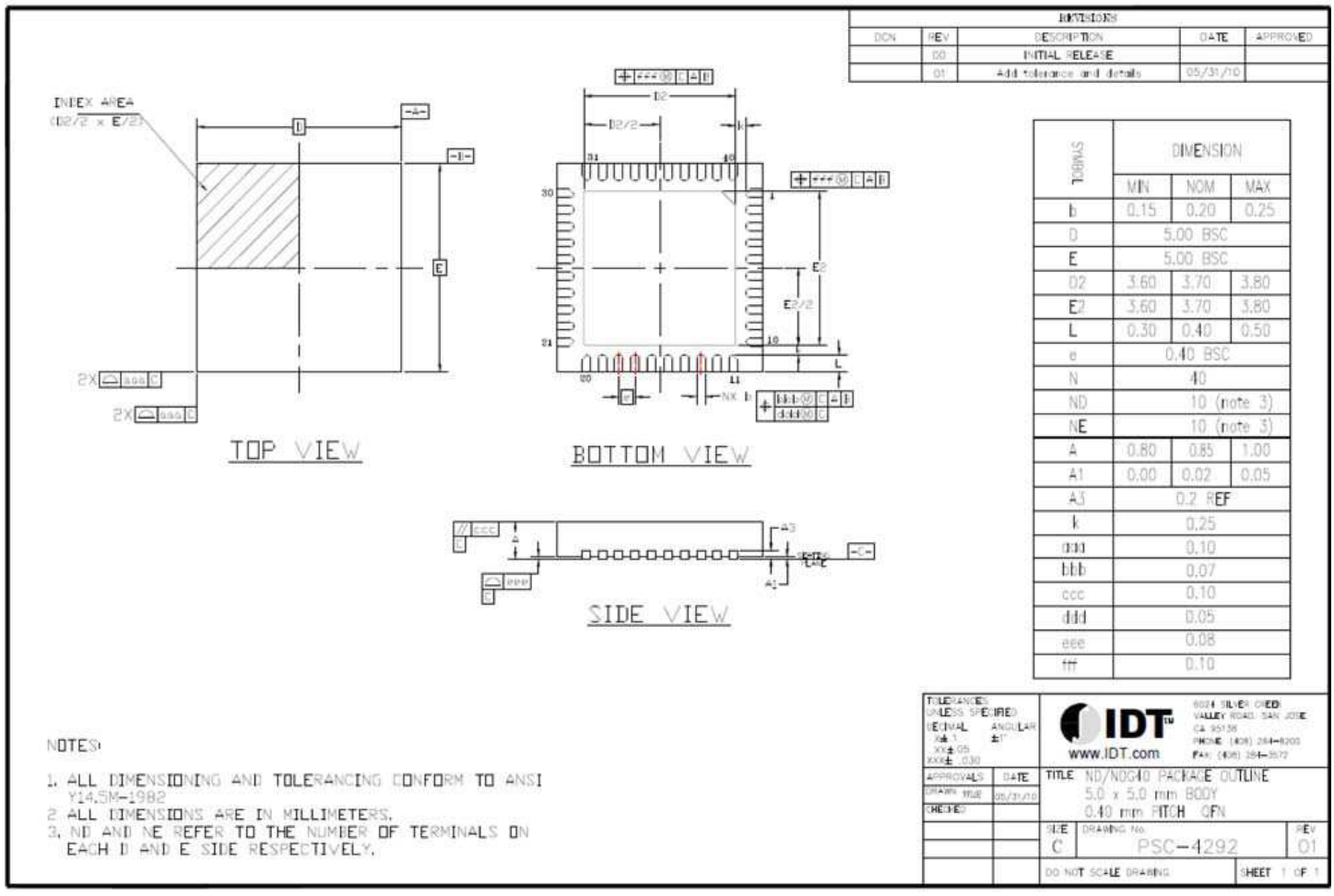


Figure 16. 40-QFN Package Diagram

©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

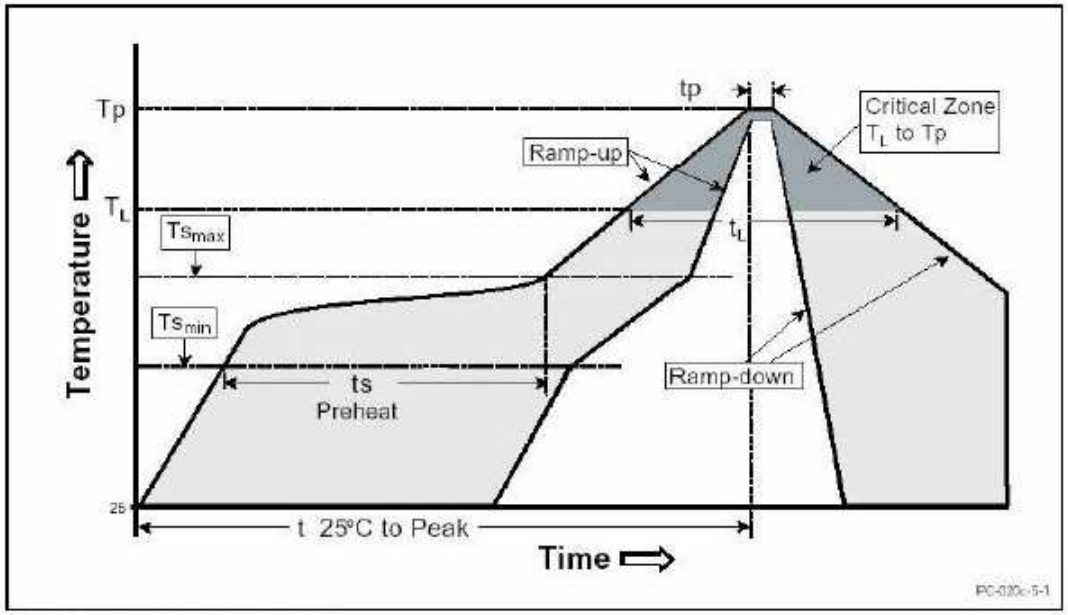
8.1. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices" (www.jedec.org/download).

Profile Feature		Pb Free Assembly
Average Ramp-Up Rate (Ts_{max} - Tp)		3 °C / second max
Preheat:	Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (ts_{min} - ts_{max})	150 °C 200 °C 60 - 180 seconds
Time maintained above:	Temperature (T_L) Time (t_L)	217 °C 60 - 150 seconds
Peak / Classification Temperature (Tp)		See "Package Classification Reflow Temperatures"
Time within 5 °C of actual Peak Temperature (tp)		20 - 40 seconds
Ramp-Down rate		6 °C / second max
Time 25 °C to Peak Temperature		8 minutes max
Note: All temperatures refer to topside of the package, measured on the package body surface.		

Table 32. Standard Reflow Profile



©2012 INTEGRATED DEVICE TECHNOLOGY, INC.

9. DISCLAIMER

While the information presented herein has been checked for both accuracy and reliability, manufacturer assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements, are not recommended without additional processing by manufacturer. Manufacturer reserves the right to change any circuitry or specifications without notice. Manufacturer does not authorize or warrant any product for use in life support devices or critical medical instruments.

10. DOCUMENT REVISION HISTORY

Revision	Date	Description of Change
0.5	January 2012	Initial release
0.6	April 2012	Updated Config defaults, Added RTD3 support
0.9	April 2012	Widget details added.
0.91	June 2012	Added THD+N setting to Class D Output power and 3W typical line.
1.0	October 2012	Updated PSRR and power consumption numbers in electrical section.
1.0	January 2013	Added comment to VREF_Out section. Updated VREF_Out section in electrical characteristics table.

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.