3.3 VOLT TIME SLOT INTERCHANGE DIGITAL SWITCH WITH RATE MATCHING 2,048 x 2,048

IDT72V71623

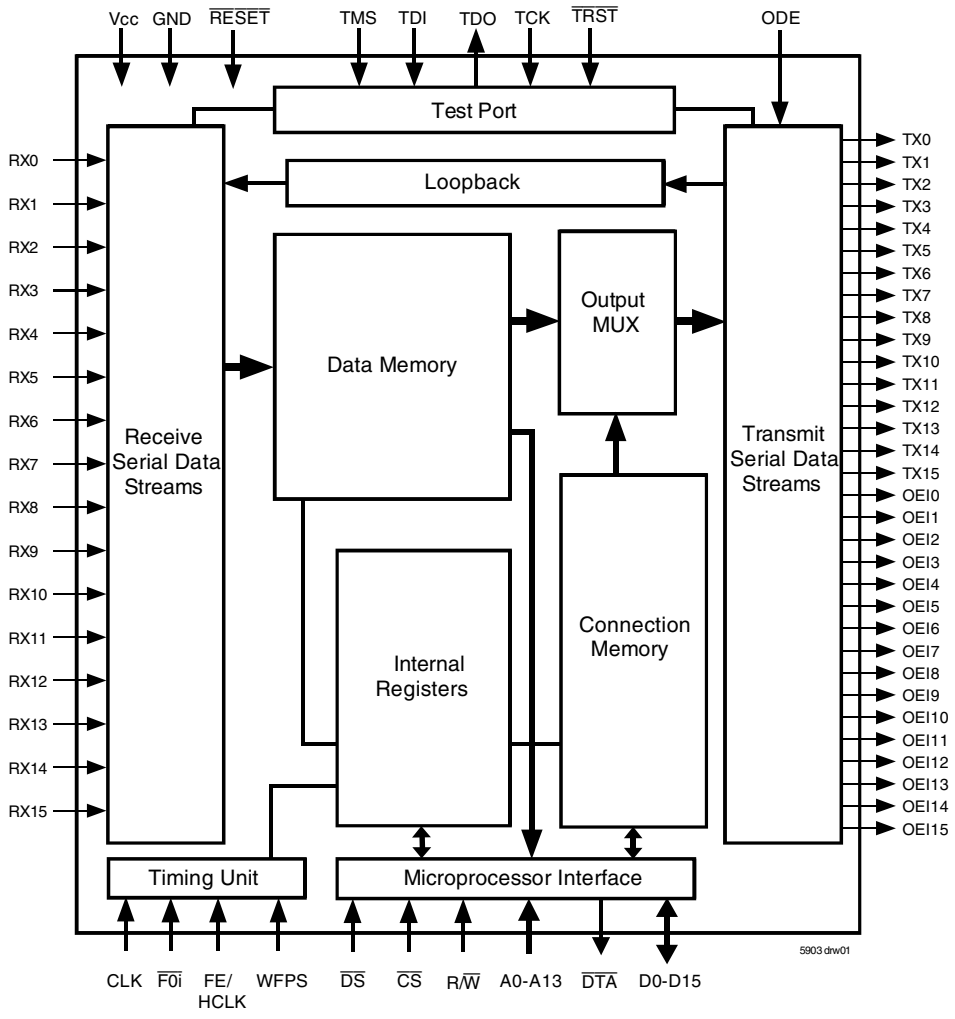
FEATURES:

- Up to 16 serial input and output streams
- Maximum 2,048 x 2,048 channel non-blocking switching
- Accepts data streams at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s
- Rate matching capability: Mux/Demux mode
- Output Enable Indication pins provided by dedicated pins
- Per-channel Variable Delay mode for low-latency applications
- Per-channel Constant Delay mode for frame integrity applications
- Automatic identification of ST-BUS® and GCI serial streams
- Automatic frame offset delay measurement
- Per-stream frame delay offset programming
- Per-channel high-impedance output control
- Per-channel Processor mode to allow microprocessor writes to TX streams
- Direct microprocessor access to all internal memories
- Memory block programming for quick setup
- IEEE-1149.1 (JTAG) Test Port
- Internal Loopback for testing
- Available in 144-pin Thin Quad Flatpack (TQFP) and 144-pin Ball Grid Array (BGA) packages
- Operating Temperature Range -40°C to +85°C
- 3.3V I/O with 5V tolerant inputs and TTL compatible outputs

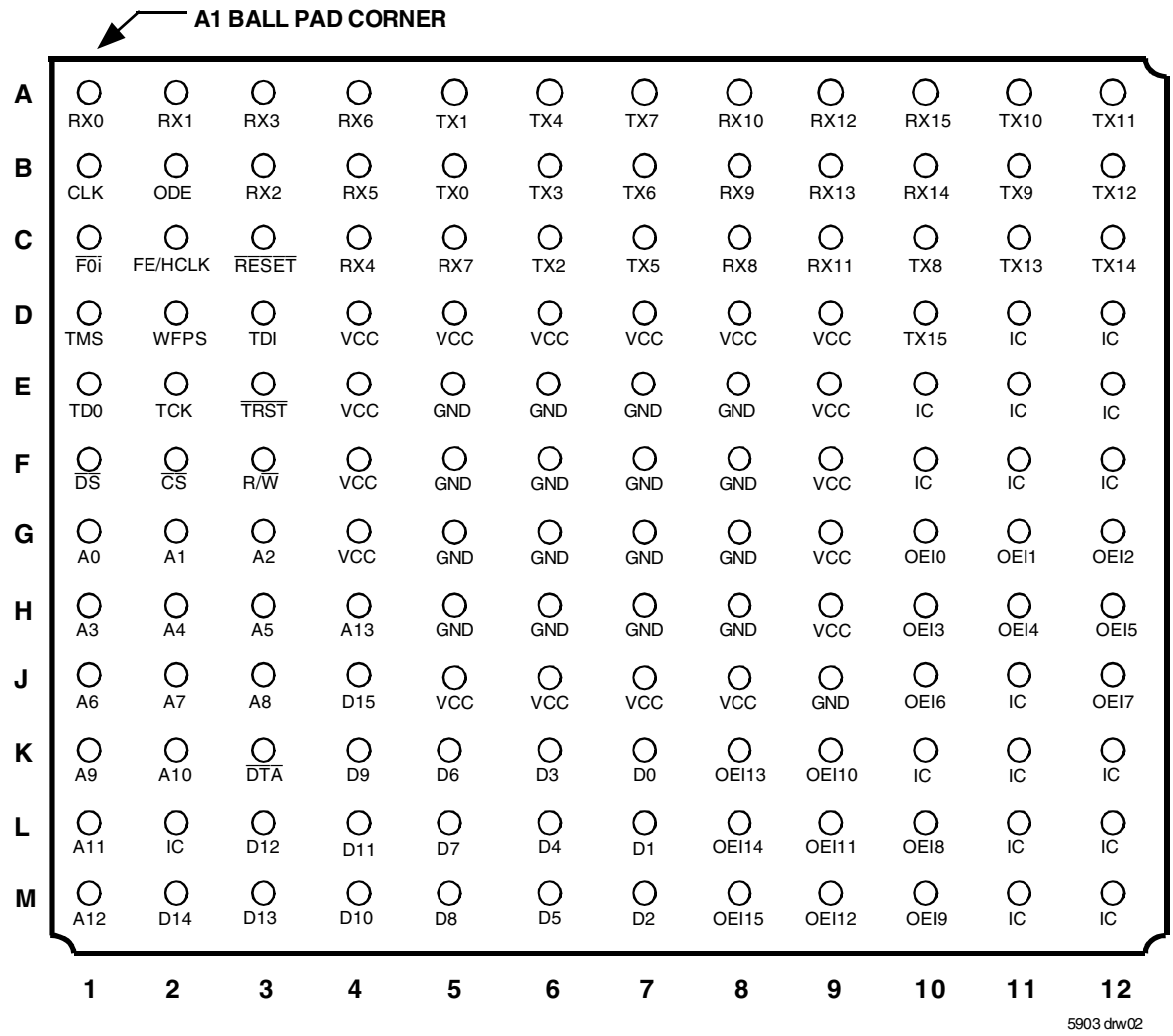
DESCRIPTION:

The IDT72V71623 has a maximum non-blocking switch capacity of 2,048 x 2,048 channels with data rates at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s. With 16 inputs and 16 outputs, a variety of rate combinations is supported under Mux/Demux mode, to allow for switching between streams of different data rates.

FUNCTIONAL BLOCK DIAGRAM



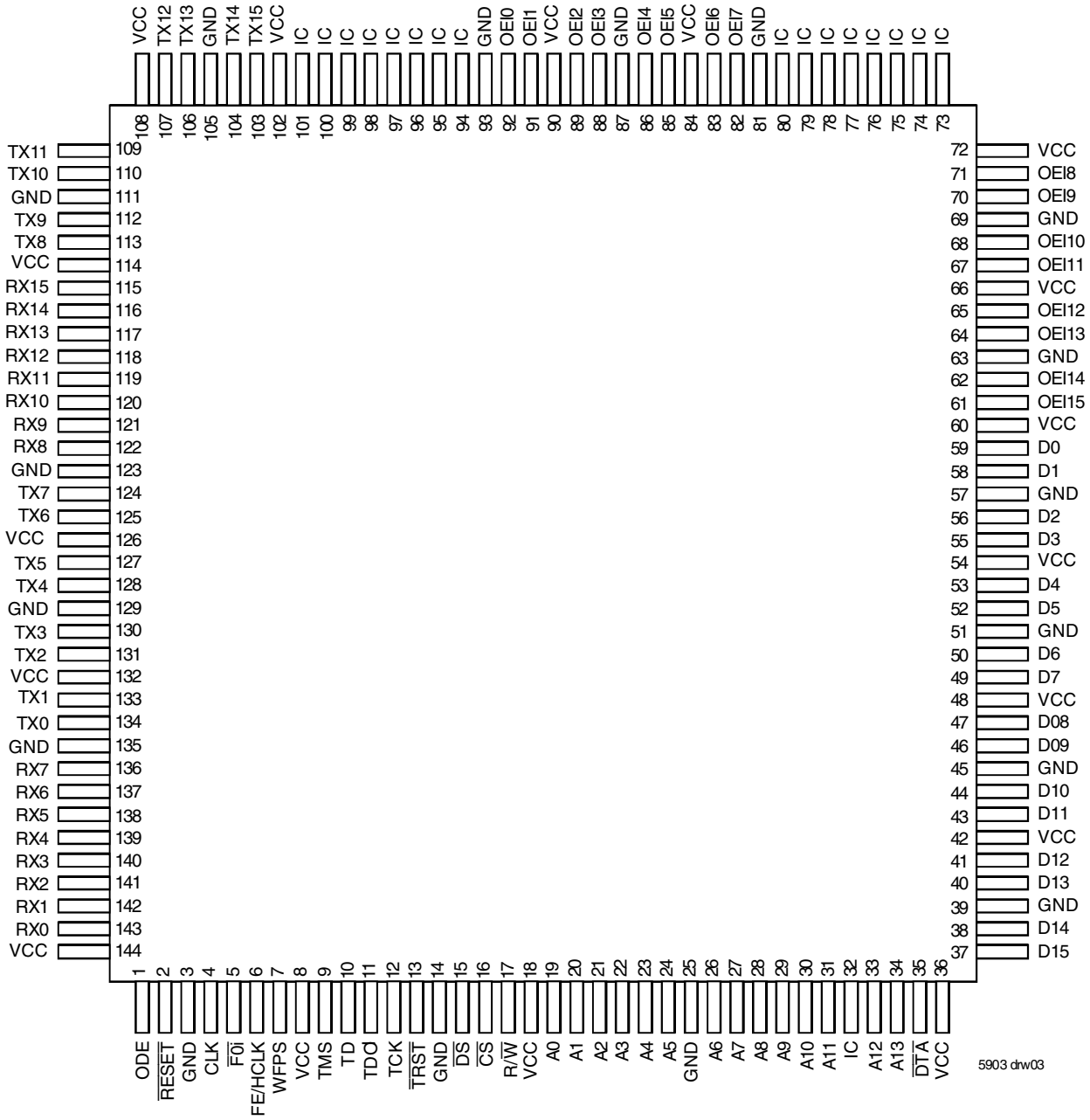
PIN CONFIGURATIONS



BGA: 1mm pitch, 13mm x 13mm (Order Code: BC, BCG)
TOP VIEW

NOTES:
1. IC - Internal Connection, tie to Ground for normal operation.
2. All I/O pins are 5V tolerant except for TMS, TDI and $\overline{\text{TRST}}$.

PIN CONFIGURATIONS (CONTINUED)



TQFP: 0.50mm pitch, 20mm x 20mm (Order Code: DA, DAG)
TOP VIEW

NOTES:
1. IC - Internal Connection, tie to Ground for normal operation.
2. All I/O pins are 5V tolerant except for TMS, TDI and $\overline{TRST}$.

PIN DESCRIPTION

SYMBOL	NAME	I/O	DESCRIPTION
GND	Ground.		Ground Rail.
Vcc	Vcc		+3.3 Volt Power Supply.
TX0-15	TX Output 0 to 15 (Three-state Outputs)	O	Serial data output stream. These streams may have a data rate of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s, or 16.384 Mb/s.
OEI0-15	Output Enable Indication 0 to 15 (Three-state Outputs)	O	These pins reflect the active or three-state status for the corresponding, (TX0-15) output streams.
RX0-15	RX Input 0 to 15	I	Serial data input stream. These streams may have a data rate of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s, or 16.384 Mb/s.
$\overline{F0i}$	Frame Pulse	I	This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS® and GCI specifications.
FE/HCLK	Frame Evaluation/ HCLK Clock	I	When the WFPS pin is LOW, this pin is the frame measurement input. When the WFPS pin is HIGH, the HCLK (4.096 MHZ clock) is required for frame alignment in the wide frame pulse (WFP) mode.
CLK	Clock	I	Serial clock for shifting data in/out on the serial streams (RX/TX 0-15).
TMS	Test Mode Select	I	JTAG signal that controls the state transitions of the TAP controller. This pin is pulled HIGH by an internal pull-up when not driven.
TDI	Test Serial Data In	I	JTAG serial test instructions and data are shifted in on this pin. This pin is pulled HIGH by an internal pull-up when not driven.
TDO	Test Serial Data Out	O	JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high-impedance state when JTAG scan is not enabled.
TCK	Test Clock	I	Provides the clock to the JTAG test logic.
$\overline{TRST}$	Test Reset	I	Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-reset state. This pin is pulled by an internal pull-up when not driven. This pin should be pulsed LOW on power-up, or held LOW, to ensure that the IDT72V71623 is in the normal functional mode.
$\overline{RESET}$	Device Reset	I	This input (active LOW) puts the IDT72V71623 in its reset state that clears the device internal counters, registers and brings TX0-15 and microport data outputs to a high-impedance state. In normal operation, the $\overline{RESET}$ pin must be held LOW for a minimum of 100ns to reset the device. After reset state, $\overline{RESET}$ must be held HIGH for minimum 100ns before beginning operation.
WFPS	Wide Frame Pulse Select	I	When 1, enables the wide frame pulse (WFP) Frame Alignment interface. When 0, the device operates in ST-BUS® /GCI mode.
$\overline{DS}$	Data Strobe	I	This active LOW input works in conjunction with $\overline{CS}$ to enable the read and write operations.
R/$\overline{W}$	Read/Write	I	This input controls the direction of the data bus lines during a microprocessor access.
$\overline{CS}$	Chip Select	I	Active LOW input used by a microprocessor to activate the microprocessor port of IDT72V71623.
A0-13	Address Bus 0 to 13	I	These pins allow direct access to Connection Memory, Data Memory and internal control registers.
D0-15	Data Bus 0-15	I/O	These pins are the data bits of the microprocessor port.
$\overline{DTA}$	Data Transfer Acknowledgment	O	This active LOW signal indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then goes high-impedance, allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is in high-impedance.
ODE	Output Drive Enable	I	This is the output enable control for the TX0-15 serial outputs. When ODE input is LOW and the OSB bit of the IMS register is LOW, TX0-15 are in a high-impedance state. If this input is HIGH, the TX0-15 output drivers are enabled. However, each channel may still be put into a high-impedance state by using the per channel control bit in the Connection Memory.

DESCRIPTION (CONTINUED)

Output enable indications are provided through dedicated pins (one pin per output stream) to facilitate external data bus control.

The IDT72V71623 is capable of switching up to 2,048 x 2,048 channels without blocking. Designed to switch 64 Kbit/s PCM or N x 64 Kbit/s data, the device maintains frame integrity in data applications and minimizes throughput delay for voice applications on a per channel basis.

The serial input streams (RX) and serial output streams (TX) of the IDT72V71623 can be run up to 16.384 Mb/s allowing 256 channels per 125µs frame. Depending on the input and output data rates the device can support up to 16 serial streams.

With two main operating modes, Processor mode and Connection Mode, the IDT72V71623 can easily switch data from incoming serial streams (Data Memory) or from the controlling microprocessor (Connection Memory). As control and status information is critical in data transmission, the Processor mode is especially useful when there are multiple devices sharing the input and output streams.

With two main configuration modes, Regular and Mux/Demux mode the IDT72V71623 is designed to work in a mixed data-rate environment. In Mux/Demux mode, all of the input streams work at one data rate and the output streams at another. Depending on the configuration, more or less serial streams will be available on the inputs or outputs to maintain a non-blocking switch.

With data coming from multiple sources and through different paths, data entering the device is often delayed. To handle this problem, the IDT72V71623 has a frame evaluation feature to allow individual streams to be offset from the frame pulse in half clock-cycle intervals up to +4.5 clock cycles for speeds up to 8 Mb/s or +2.5 clock cycles for 16 Mb/s. (See Table 8 for maximum allowable skew).

The IDT72V71623 also provides a JTAG test access port, an internal loopback feature, memory block programming, a simple microprocessor interface and automatic ST-BUS®/GCI sensing to shorten setup time, aid in debugging and ease use of the device without sacrificing capabilities.

FUNCTIONAL DESCRIPTION

DATA AND CONNECTION MEMORY

All data that comes in through the RX inputs go through a serial-to-parallel conversion before being stored into internal Data Memory. The 8 KHz frame pulse (F0i) is used to mark the 125µs frame boundaries and to sequentially address the input channels in Data Memory. The Data Memory is only written by the device from the RX streams and can be read from either the TX streams or the microprocessor.

Data output on the TX streams may come from either the Serial Input Streams (Data Memory) or from the microprocessor (Connection Memory). In the case that RX input data is to be output, the addresses in Connection Memory are used to specify a stream and channel of the input. The Connection Memory is setup in such a way that each location corresponds to an output channel for each particular stream. In that way, more than one channel can output the same data. In Processor mode, the microprocessor writes data to the Connection Memory locations corresponding to the stream and channel that is to be output. The lower byte (8 least significant bits) of the Connection Memory is output every frame until the microprocessor changes the data or mode of the channel. By using this Processor mode capability, the microprocessor can access input and output time-slots on a per channel basis.

The most significant bits of the Connection Memory are used to control per channel functions such as Processor mode, Constant or Variable Delay mode, three-state of output drivers, and the Loopback function.

OPERATING MODES

In addition to Regular mode where input and output streams are operating at the same rate, the IDT72V71623 incorporates a rate matching function, Mux/Demux mode. In Mux/Demux mode, all input streams are operating at the same rate, while output streams are operating at a different rate. All configurations are non-blocking. These modes can be entered by setting the DR3-0 bits in the Control Register, see Table 5.

OUTPUT IMPEDANCE CONTROL

In order to put all streams in three-state, all per-channel three-state control bits in the Connection Memory are set (MOD0 and MOD1 = 1) or both the ODE pin and the OSB bit of the Control Register must be zero. If any combination other than 0-0, for the ODE pin and the OSB bit, is used, the three-state control of the streams will be left to the state of the MOD1 and MOD0 bits of the Connection Memory. The IDT72V71623 incorporates a memory block programming feature to facilitate three-state control after reset. See Table 1 for Output High-Impedance Control.

SERIAL DATA INTERFACE TIMING

When a 16Mb/s serial data rate is required, the master clock frequency will be running at 16.384MHz resulting in a single-bit per clock. For all other cases, 2Mb/s, 4Mb/s, and 8Mb/s, the master clock frequency will be twice the fastest data rate on the serial streams. Use Table 5 to determine clock speed and DR3-0 bits in the Control Register to setup the device. The IDT72V71623 provides two different interface timing modes, ST-BUS® or GCI. The IDT72V71623 automatically detects the presence of an input frame pulse and identifies it as either ST-BUS® or GCI.

In ST-BUS®, when running at 16.384MHz, data is clocked out on the falling edge and is clocked in on the subsquent rising-edge. At all other data rates, there are two clock cycles per bit and every second falling edge of the master clock marks a bit boundary and the data is clocked in on the rising edge of CLK, three quarters of the way into the bit cell. See Figure 15 for timing.

In GCI format, when running at 16.384MHz, data is clocked out on the rising edge and is clocked in on the subsquent falling edge. At all other data rates, there are two clock cycles per bit and every second rising edge of the master clock marks the bit boundary and data is clocked in on the falling edge of CLK at three quarters of the way into the bit cell. See Figure 16 for timing.

INPUT FRAME OFFSET SELECTION

Input frame offset selection allows the channel alignment of individual input streams to be offset with respect to the output stream channel alignment (i.e. F0i). Although input data is synchronous, delays can be caused by variable path serial backplanes and variable path lengths, which may be implemented in large centralized and distributed switching systems. Because data is often delayed this feature is useful in compensating for the skew between clocks.

Each input stream can have its own delay offset value by programming the frame input offset registers (FOR, Table 7). The frame offset shown is a function of the data rate, and can be as large as +4.5 master clock (CLK) periods forward with a resolution of ½ clock period. To determine the maximum offset allowed see Table 8.

SERIAL INPUT FRAME ALIGNMENT EVALUATION

The IDT72V71623 provides the frame evaluation (FE) input to determine different data input delays with respect to the frame pulse F0i. Setting the start frame evaluation (SFE) bit low for at least one frame starts a measurement cycle. When the SFE bit in the Control Register is changed from low to high, the

evaluation starts. Two frames later, the complete frame evaluation (CFE) bit of the frame alignment register (FAR) changes from low to high to signal that a valid offset measurement is ready to be read from bits 0 to 11 of the FAR register. The SFE bit must be set to zero before a new measurement cycle is started.

In ST-BUS® mode, the falling edge of the frame measurement signal (FE) is evaluated against the falling edge of the ST-BUS® frame pulse. In GCI mode, the rising edge of FE is evaluated against the rising edge of the GCI frame pulse. See Table 6 and Figure 5 for the description of the frame alignment register.

MEMORY BLOCK PROGRAMMING

The IDT72V71623 provides users with the capability of initializing the entire Connection Memory block in two frames. To set bits 15 to 13 of every Connection Memory location, first program the desired pattern in bits 9 to 7 of the Control Register.

Setting the memory block program (MBP) bit of the control register high enables the block programming mode. When the block programming enable (BPE) bit of the Control Register is set to high, the block programming data will be loaded into the bits 15 to 13 of every Connection Memory location. The other Connection Memory bits (bit 12 to bit 0) are loaded with zeros. When the memory block programming is complete, the device resets the BPE bit to zero.

LOOPBACK CONTROL

The loopback control (LPBK) bit of each Connection Memory location allows the TX output data to be looped backed internally to the RX input for diagnostic purposes.

If the LPBK bit is high, the associated TX output channel data is internally looped back to the RX input channel (i.e., data from TXn channel m routes to the RXn channel m internally); if the LPBK bit is low, the loopback feature is disabled. For proper per-channel loopback operation, the contents of frame delay offset registers must be set to zero and the device must be in regular switch mode (DR3-0 = 0x0, 0x1 or 0x2).

DELAY THROUGH THE IDT72V71623

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time-slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, Variable throughput delay is best as it ensures minimum delay between input and output data. In wideband data applications, Constant throughput delay is best as the frame integrity of the information is maintained through the switch.

The delay through the device varies according to the type of throughput delay selected in the MOD1 and MOD0 bits of the Connection Memory.

VARIABLE DELAY MODE (MOD1-0 = 0x0)

In this mode, the delay is dependent only on the combination of source and destination serial stream speed. Although the minimum delay achievable is dependent on the input and output serial stream speed, if data is switched out +3 channels of the slowest data rate, the data will be switched out in the same frame except if the input and output data rates are both 16 Mb/s (DR3-0 = 0x3). (See Figure 2 for example).

For example, given the input data rate is 2 Mb/s and the output data rate is 8 Mb/s, input channel CH0 can be switch out by output channel CH12. In the above example the input streams are slower than the output streams. Also, for every 2 Mb/s time slot there are four 8 Mb/s time slots, thus a three 2 Mb/s channel delay equates to 12 output channel time slots. See Figure 2 for this example and other examples of minimum delay to guarantee transmission in the same frame.

CONSTANT DELAY MODE (MOD1-0 = 0x1)

In this mode, frame integrity is maintained in all switching configurations by making use of a multiple Data Memory buffer. Input channel data is written into the Data Memory buffers during frame n will be read out during frame n+2. Figure 1 shows examples of Constant Delay mode.

MICROPROCESSOR INTERFACE

The IDT72V71623's microprocessor interface looks like a standard RAM interface to improve integration into a system. With a 14-bit address bus and a 16-bit data bus, read and writes are mapped directly into Data and Connection memories and require only one Master Clock cycle to access. By allowing the internal memories to be randomly accessed in one cycle, the controlling microprocessor has more time to manage other peripheral devices and can more easily and quickly gather information and setup the switch paths.

Table 2 shows the mapping of the addresses into internal memory blocks, Table 3 shows the Control Register information and Figure 11 and Figure 12 shows asynchronous and synchronous microprocessor accesses.

MEMORY MAPPING

The address bus on the microprocessor interface selects the internal registers and memories of the IDT72V71623. The two most significant bits of the address select between the registers, Data Memory, and Connection Memory. If A13 and A12 are HIGH, A11-A0 are used to address the Data Memory (Read Only) where data output is read from the 8 least significant bits on the data bus. If A13 is HIGH and A12 is LOW, A11-A0 are used to address Connection Memory (Read/Write). If A13 is LOW and A12 is HIGH A11-A9 are used to select the Control Register, Frame Alignment Register, and Frame Offset Registers. See Table 2 for mappings..

CONTROL REGISTER

As explained in the Serial Data Interface Timing and Switching Configurations sections, after system power-up, the Control Register should be programmed immediately to establish the desired switching configuration.

The data in the Control Register consists of the Memory Block Programming bit (MBP), the Block Programming Data (BPD) bits, the Begin Block Programming Enable (BPE), the Output Stand By (OSB), Start Frame Evaluation (SFE), and Data Rate Select bits (DR 3-0). As explained in the Memory Block Programming section, the BPE begins the programming if the MBP bit is enabled. This allows the entire Connection Memory block to be programmed with the Block Programming Data bits.

CONNECTION MEMORY CONTROL

If the ODE pin or the OSB bit is high, the MOD1-0 bits of each Connection Memory location controls the output drivers. See Table 1 for detail. The Processor Channel (PC) mode is entered by a 1-0 of the MOD1-0 of the Connection Memory. In Processor Channel Mode, this allows the microprocessor to access TX output channels. Once the MOD1-0 bits are set the lower 8 bits of the Connection Memory will be output on the TX serial streams. Also controlled in the Connection Memory is the Variable Delay mode or Constant Delay mode. Each Connection Memory location allows the per-channel selection between Variable and Constant throughput Delay modes and Processor mode.

If the LPBK bit is high, the associated TX output channel data is internally looped back to the RX input channel (i.e., RXn channel m data comes from the TXn channel m). If the LPBK bit is low, the loopback feature is disabled. For proper per-channel loopback operation, the contents of the frame delay offset registers must be set to zero and the device must be in regular switch mode (DR3-0 = 0x0, 0x1 or 0x2).

OUTPUT ENABLE INDICATION

The IDT72V71623 has dedicated pins to indicate the state of the outputs (active or three-state). See Figure 13 for timing.

INITIALIZATION OF THE IDT72V71623

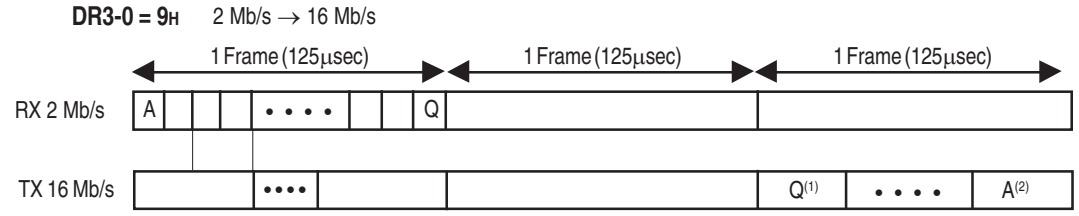
After power up, the IDT72V71623 should be reset. During reset, the internal registers are put into their default state and all TX outputs are put into three-state. After reset however, the state of Connection Memory is unknown. As such, the outputs should be put in high-impedance by holding the ODE low. While the ODE is low, the microprocessor can initialize the device, program the active paths, and disable unused outputs by programming the OE bit in Connection Memory. Once the device is configured, the ODE pin (or OSB bit depending on initialization) can be switched. See Figure 8.

TABLE 1 — OUTPUT HIGH-IMPEDANCE CONTROL

MOD1-0 BITS IN CONNECTION MEMORY	ODE PIN	OSB BIT IN CONTROL REGISTER	OUTPUT DRIVER STATUS
1 and 1	Don't Care	Don't Care	Per Channel High-Impedance
Don't Care	0	0	High-Impedance
Any, other than 1 and 1	0	1	Enable
Any, other than 1 and 1	1	0	Enable
Any, other than 1 and 1	1	1	Enable

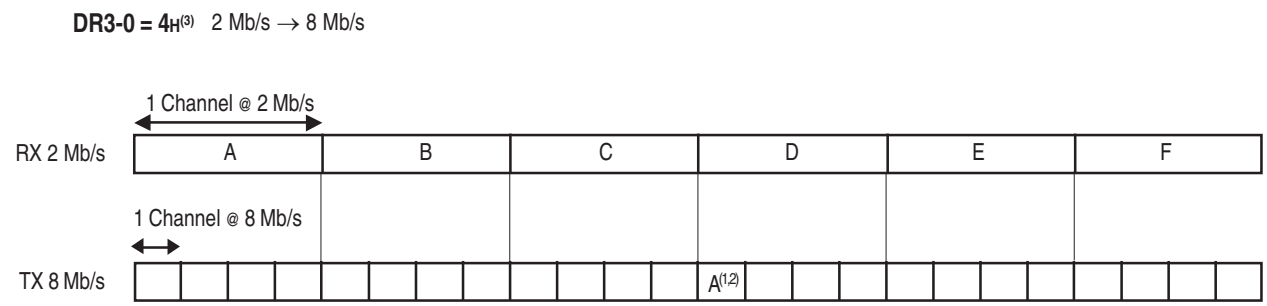
TABLE 2 — INTERNAL REGISTER AND ADDRESS MEMORY MAPPING

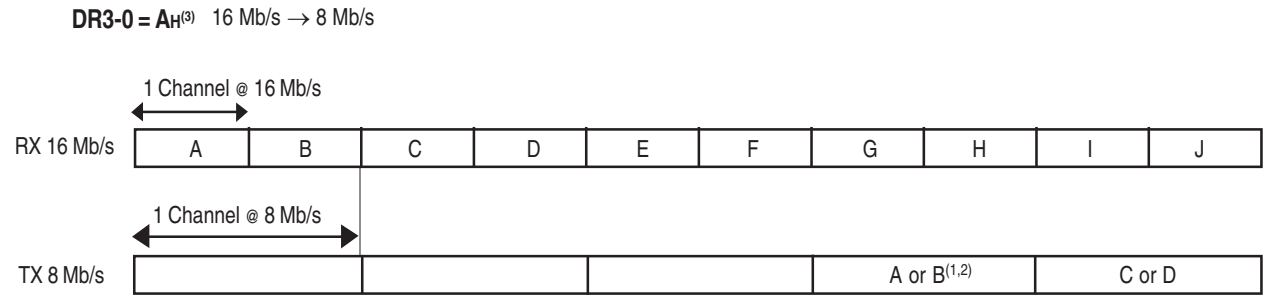
A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	Location
1	1	STA3	STA2	STA1	STA0	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	R	Data Memory
1	0	STA3	STA2	STA1	STA0	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	R/W	Connection Memory
0	1	0	0	0	x	x	x	x	x	x	x	x	x	R/W	Control Register
0	1	0	0	1	x	x	x	x	x	x	x	x	x	R	Frame Align Register
0	1	0	1	0	x	x	x	x	x	x	x	x	x	R/W	FOR0
0	1	0	1	1	x	x	x	x	x	x	x	x	x	R/W	FOR1
0	1	1	0	0	x	x	x	x	x	x	x	x	x	R/W	FOR2
0	1	1	0	1	x	x	x	x	x	x	x	x	x	R/W	FOR3

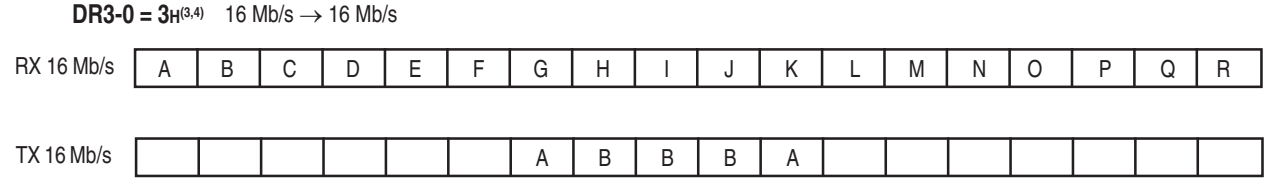


NOTES:
1. Timeslot Q — 2 Frames — minimum delay.
2. Timeslot A — 3 Frames - 1 output channel period — maximum delay.

Figure 1. Constant Delay Mode Examples







NOTES:
1. If data is switched at least +3 channel periods of the slower data rate, the data will transmit out in the same frames except if the input and output data rates are both 16 Mb/s (DR3-0 = 0x3).
2. Delay is a function of input channel and output channel combinations, and input and output stream data rate.
3. See switching mode table for input and output speed combinations.
4. When the input and output data rates are both 16 Mb/s, the minimum delay achievable is 6 time slots.

Figure 2. Variable Delay Mode Examples

TABLE 3 — CONTROL REGISTER (CR) BITS

Reset Value: 4000H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRS	1	OEP	0	MBP	0	BPD2	BPD1	BPD0	BPE	OSB	SFE	DR3	DR2	DR1	DR0

Bit	Name	Description
15	Reset (Software Reset)	A one will reset the device and have the same effect as of the RESET pin. Must be zero for normal operation. Before beginning operation, this bit must be held zero for minimum 100ns.
14	Unused	Must be one for proper operation.
13	OEPOL (Output Enable Polarity)	When 1, a one on OEI pin denotes an active state on the output data stream; zero on OEI pin denotes high-impedance state. When 0, a one denotes high-impedance and a zero denotes an active state.
12	Unused	Must be zero for normal operation.
11	MBP (Memory Block Program)	When 1, the Connection Memory block programming feature is ready for the programming of Connection Memory high bits, bit 13 to bit 15. When 0, this feature is disabled.
10	Unused	Must be zero for normal operation.
9-7	BPD2-0 (Block Programming Data)	These bits carry the value to be loaded into the Connection Memory block whenever the memory block programming feature is activated. After the MBP bit in the control register is set to 1 and the BPE bit is set to 1, the contents of the bits BPD2-0 are loaded into bit 15 and 13 of the Connection Memory. Bit 12 to bit 0 of the Connection Memory are set to 0.
6	BPE (Begin Block Programming Enable)	A zero to one transition of this bit enables the memory block programming function. The BPE and BPD2-0 bits in the CR register have to be defined in the same write operation. Once the BPE bit is set HIGH, the device requires two frames to complete the block programming. After the programming function has finished, the BPE bit returns to zero to indicate the operation is completed. When the BPE=1, the other bit in the control register must not be changed for two frames to ensure proper operation.
5	OSB (Output Stand By)	When ODE=0 and OSB=0, the output drivers of transmit serial streams are in high-impedance mode. When ODE=1 or OSB=1, Connection Memory Mod 1 - 0 ≠ 1 and 1, the output serial stream drivers function normally. When both Connection Memory Mod 1 - 0 = 1 and 1, the output drivers of the transmit serial streams are in high impedance mode. Please refer to Table 1.
4	SFE (Start Frame Evaluation)	A zero to one transition in this bit starts the frame evaluation procedure. When the CFE bit in the FAR register changes from zero to one, the evaluation procedure stops. To start another frame evaluation cycle, set this bit to zero for at least one frame.
3-0	DR3-0	Input/Output data rate selection. See Table 5 for detailed programming.

TABLE 4 — CONNECTION MEMORY BITS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPBK	MOD1	MOD0	0	SAB3	SAB2	SAB1	SAB0	CAB7	CAB6	CAB5	CAB4	CAB3	CAB2	CAB1	CAB0

Bit	Name	Description
15	LPBK (Per Channel Loopback)	When 1, the RX n channel m data comes from the TX n channel m. For proper per channel loopback operations, set the delay offset register bits OFn[2:0] to zero for the streams which are in the loopback mode. This feature is offered only when DR3-0 = 0000, 0001 or 0010 is selected via the control register.
14,13	MOD1-0 (Switching Mode Selection)	MOD1 MOD0 MODE 0 0 Variable Delay mode 0 1 Constant Delay mode 1 0 Processor mode 1 1 Output High-Impedance
12	Unused	Must be zero for normal operation.
11-8	SAB3-0 (Source Stream Address Bits)	The binary value is the number of the data stream for the source of the connection. Unused SAB bits must be zero for proper operation.
7-0	CAB7-0 (Source Channel Address Bits)	The binary value is the number of the channel for the source of the connection. Unused CAB bits must be zero for proper operation.

TABLE 5 — SWITCH MODES

Switching Mode	Control Bits				Data Rate bits/s		Clock Rate MHz
	DR3	DR2	DR1	DR0	Receive Streams	Transmit Streams	
Regular	0	0	0	0	2 M on RX0-15	2 M on TX0-15	4
	0	0	0	1	4 M on RX0-15	4 M on TX0-15	8
	0	0	1	0	8 M on RX0-15	8 M on TX0-15	16
	0	0	1	1	16 M on RX0-7	16 M on TX0-7	16
Mux/Demux	0	1	0	0	2 M on RX0-15	8 M on TX0-3	16
	0	1	0	1	8 M on RX0-3	2 M on TX0-15	16
	0	1	1	0	4 M on RX0-15	8 M on TX0-7	16
	0	1	1	1	8 M on RX0-7	4 M on TX0-15	16
	1	0	0	0	16 M on RX0-1	2 M on TX0-15	16
	1	0	0	1	2 M on RX0-15	16 M on TX0-3	16
	1	0	1	0	16 M on RX0-7	8 M on TX0-15	16
	1	0	1	1	8 M on RX0-15	16 M on TX0-7	16

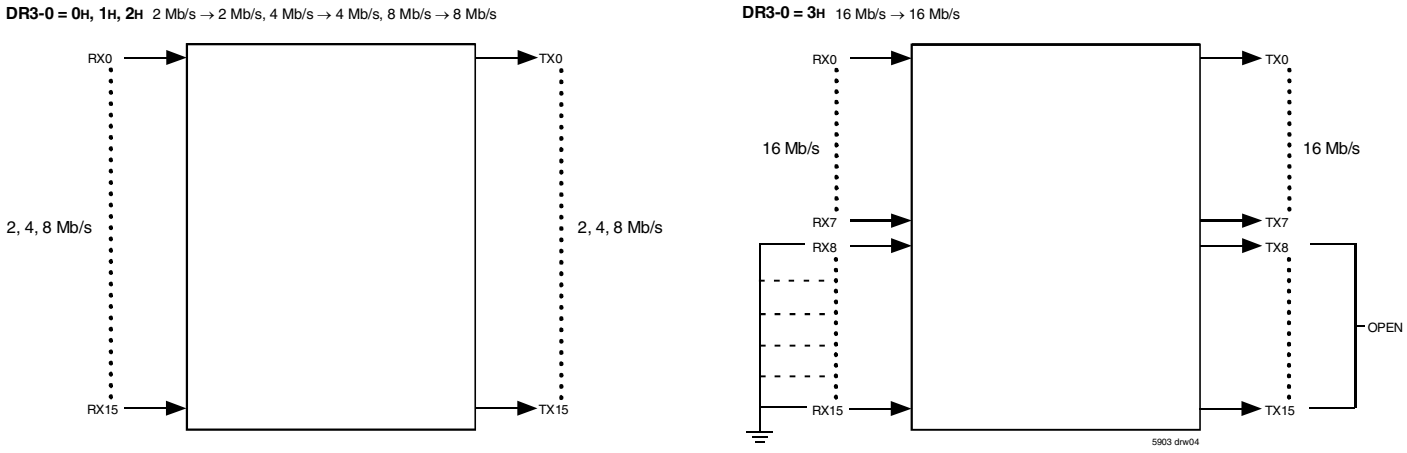


Figure 3. Regular Switch Mode

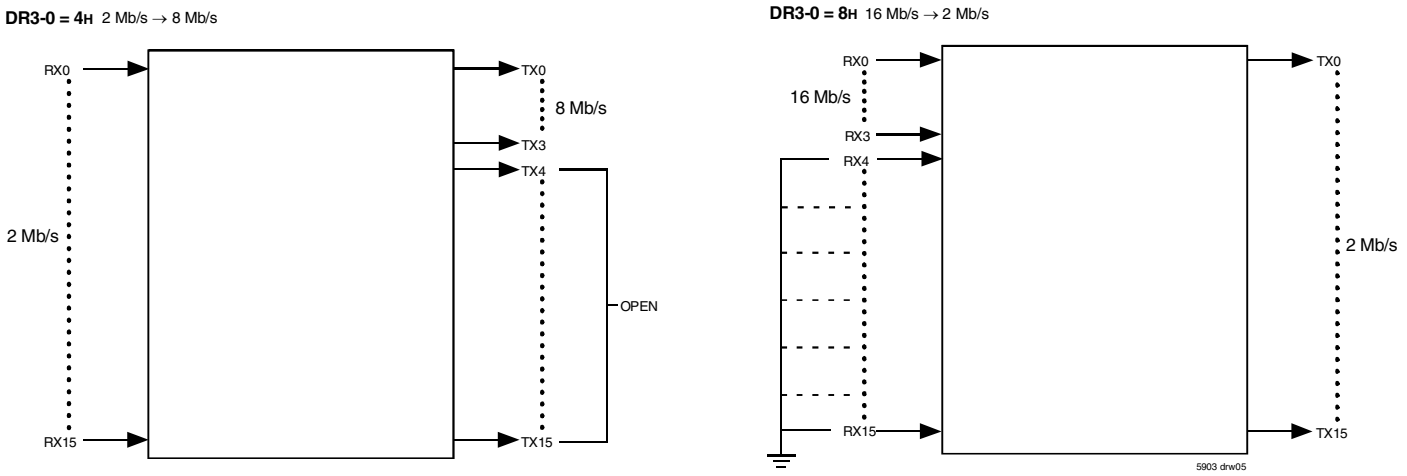


Figure 4. Mux/Demux Mode

TABLE 6 — FRAME ALIGNMENT REGISTER (FAR) BITS

Reset Value: 0000H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	CFE	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Bit	Name	Description
15-13	Unused	Must be zero for normal operation
12	CFE (Complete Frame Evaluation)	When CFE = 1, the frame evaluation is completed and bits FD10 to FD0 bits contains a valid frame alignment offset. This bit is reset to zero, when SFE bit in the CR register is changed from 1 to 0.
11	FD11 (Frame Delay Bit 11)	The falling edge of FE (or rising edge for GCI mode) is sampled during the CLK-high phase (FD11 = 1) or during the CLK-low phase (FD11 = 0). This bit allows the measurement resolution to ½ CLK cycle.
10-0	FD10-0 (Frame Delay Bits)	The binary value expressed in these bits refers to the measured input offset value. These bits are rest to zero when the SFE bit of the CR register changes from 1 to 0. (FD10 – MSB, FD0 – LSB)

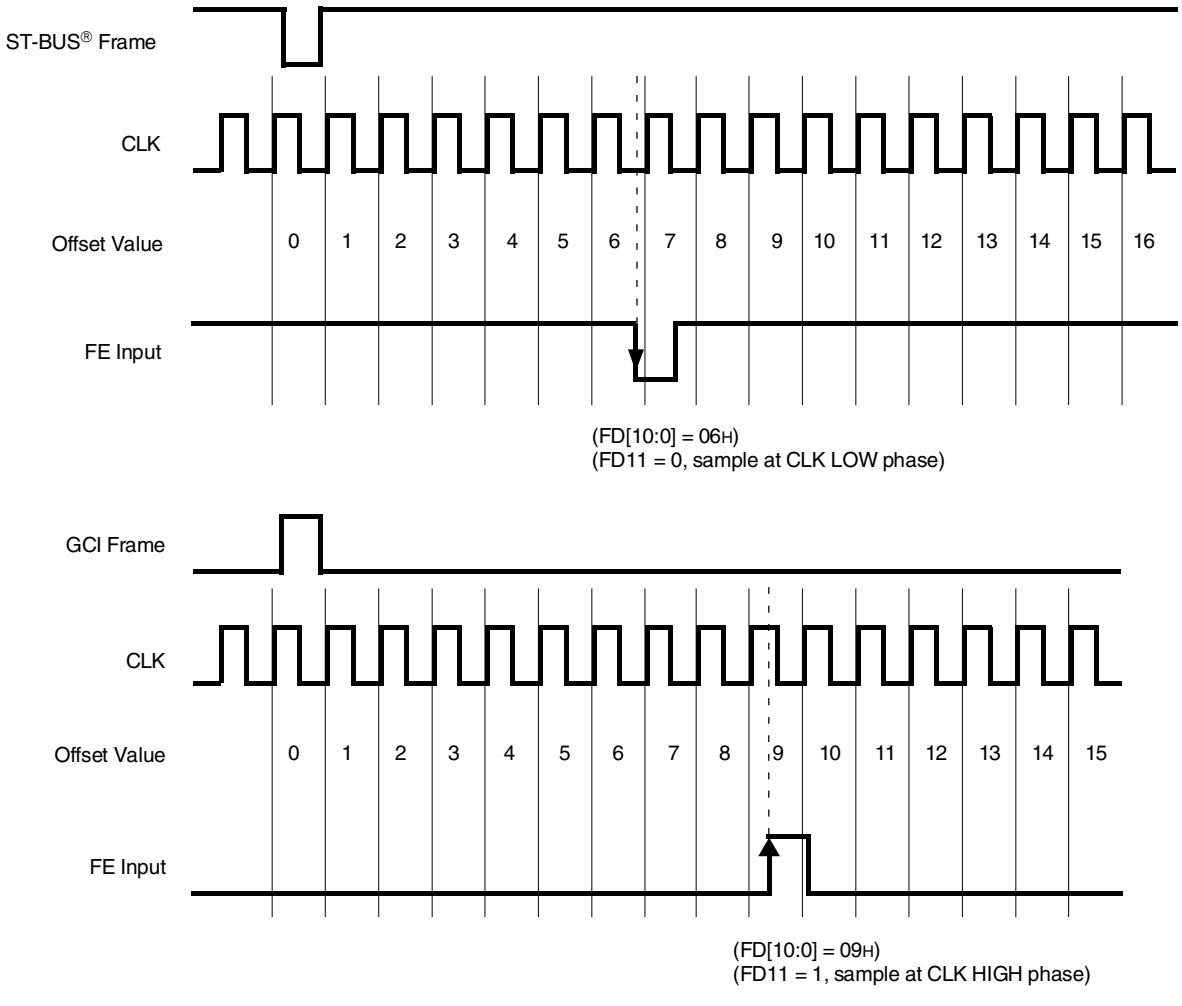
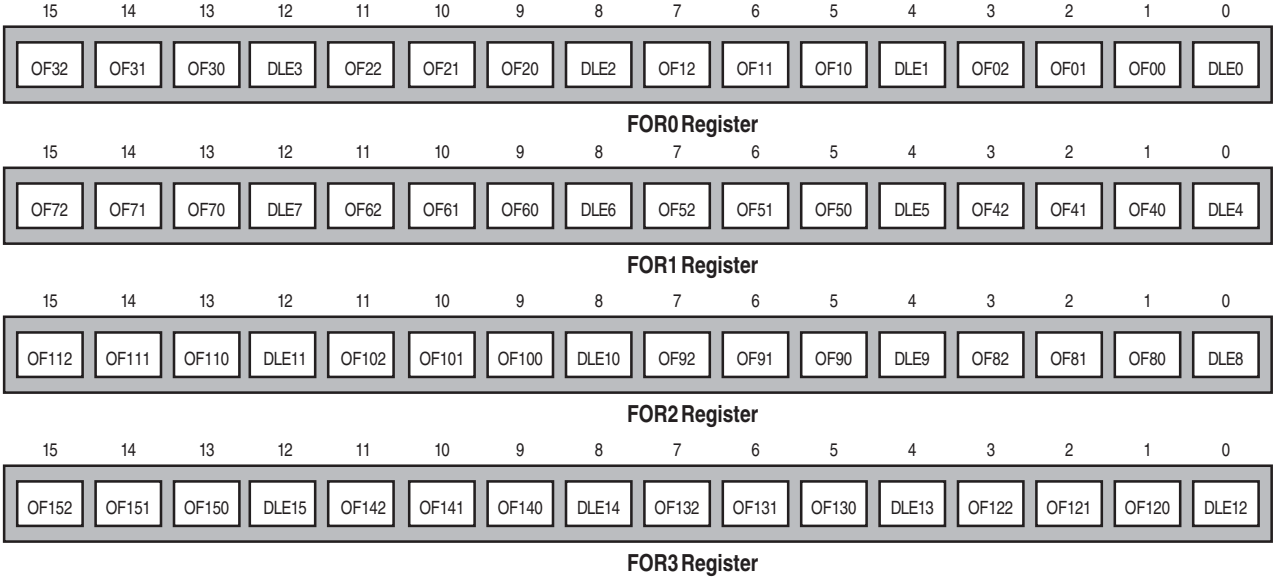


Figure 5. Example for Frame Alignment Measurement

TABLE 7 — FRAME INPUT OFFSET REGISTER (FOR) BITS

Reset Value: 0000H for all FOR registers.



Name(1)	Description
OFn2, OFn1, OFn0 (Offset Bits 2, 1 & 0)	These three bits define how long the serial interface receiver takes to recognize and store bit 0 from the RX input pin: i.e., to start a new frame. The input frame offset can be selected to +4.5 clock periods from the point where the external frame pulse input signal is applied to the $\overline{F0i}$ input of the device. See Figure 6.
DLEn	ST-BUS® mode: DLEn = 0, if clock rising edge is at the ¾ point of the bit cell. (Data Latch Edge) DLEn = 1, if when clock falling edge is at the ¾ of the bit cell. GCI mode: DLEn = 0, if clock falling edge is at the ¾ point of the bit cell. DLEn = 1, if when clock rising edge is at the ¾ of the bit cell.

NOTE:
1. n denotes an input stream number from 0 to 31.

TABLE 8 — MAXIMUM ALLOWABLE SKEW

Switching Mode	Control Bits				Data Rate bits/s		Maximum allowable skew
	DR3	DR2	DR1	DR0	Receive Streams	Transmit Streams	
Regular	0	0	0	0	2 M on RX0-15	2 M on TX0-15	+4.5
	0	0	0	1	4 M on RX0-15	4 M on TX0-15	+4.5
	0	0	1	0	8 M on RX0-15	8 M on TX0-15	+4.5
	0	0	1	1	16 M on RX0-7	16 M on TX0-7	+2.5
Mux/Demux	0	1	0	0	2 M on RX0-15	8 M on TX0-3	+1.5
	0	1	0	1	8 M on RX0-3	2 M on TX0-15	+4.5
	0	1	1	0	4 M on RX0-15	8 M on TX0-7	+1.5
	0	1	1	1	8 M on RX0-7	4 M on TX0-15	+4.5
	1	0	0	0	16 M on RX0-3	2 M on TX0-15	+2.5
	1	0	0	1	2 M on RX0-15	16 M on TX0-3	+1.5
	1	0	1	0	16 M on RX0-7	8 M on TX0-15	+4.5
	1	0	1	1	8 M on RX0-15	16 M on TX0-7	+4.5

TABLE 9 — OFFSET BITS (OFN2, OFN1, OFN0, DLEN) & FRAME DELAY BITS (FD11, FD2-0)

Input Stream Offset	Measurement Result from Frame Delay Bits				Corresponding Offset Bits			
	FD11	FD2	FD1	FD0	OFn2	OFn1	OFn0	DLEn
No clock period shift (Default)	1	0	0	0	0	0	0	0
+ 0.5 clock period shift	0	0	0	0	0	0	0	1
+ 1.0 clock period shift	1	0	0	1	0	0	1	0
+ 1.5 clock period shift	0	0	0	1	0	0	1	1
+ 2.0 clock period shift	1	0	1	0	0	1	0	0
+ 2.5 clock period shift	0	0	1	0	0	1	0	1
+ 3.0 clock period shift	1	0	1	1	0	1	1	0
+ 3.5 clock period shift	0	0	1	1	0	1	1	1
+ 4.0 clock period shift	1	1	0	0	1	0	0	0
+ 4.5 clock period shift	0	1	0	0	1	0	0	1

NOTE:
1. See Table 8 for maximum allowable offsets.

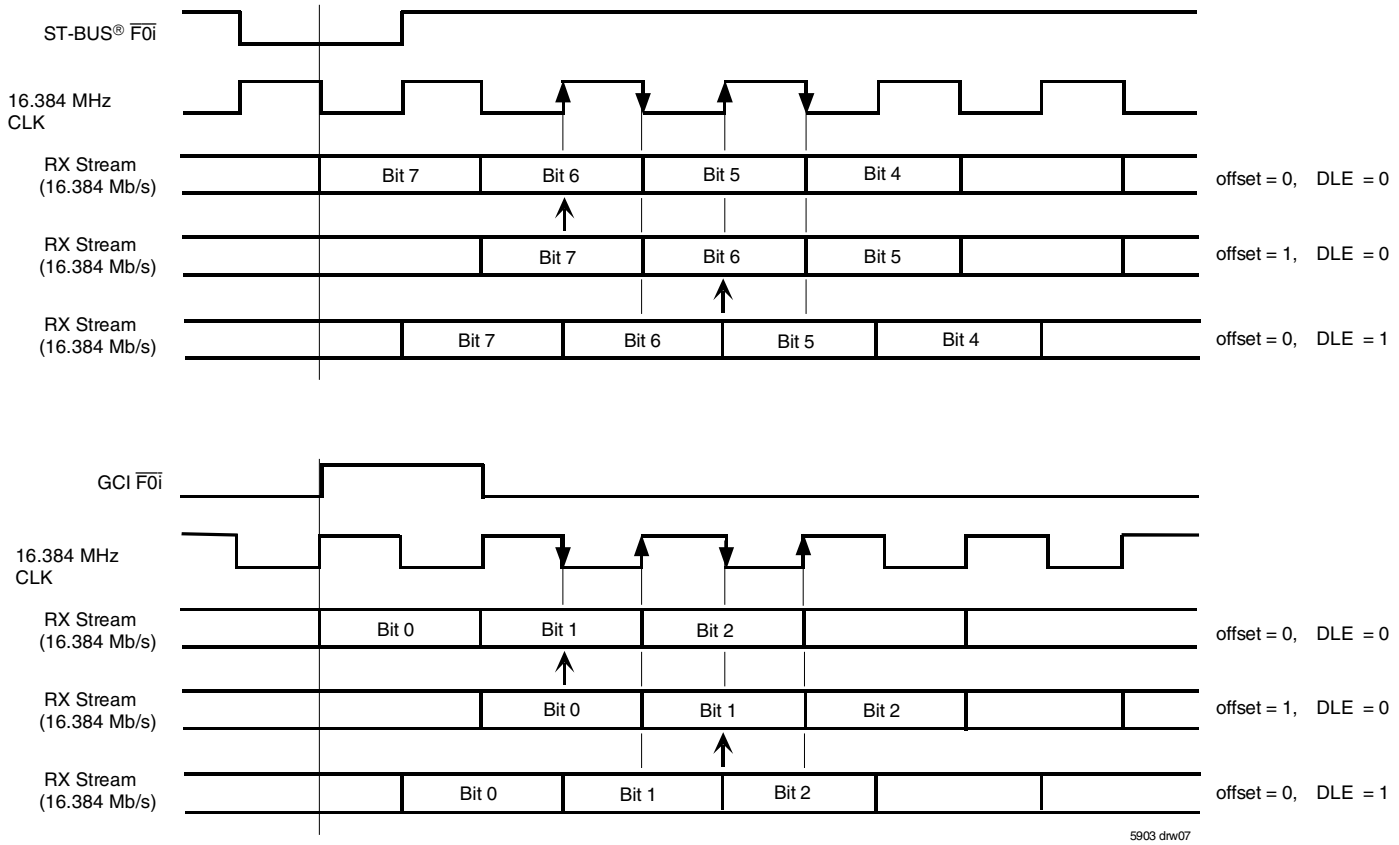


Figure 6. Examples for Input Offset Delay Timing in 16 Mb/s mode

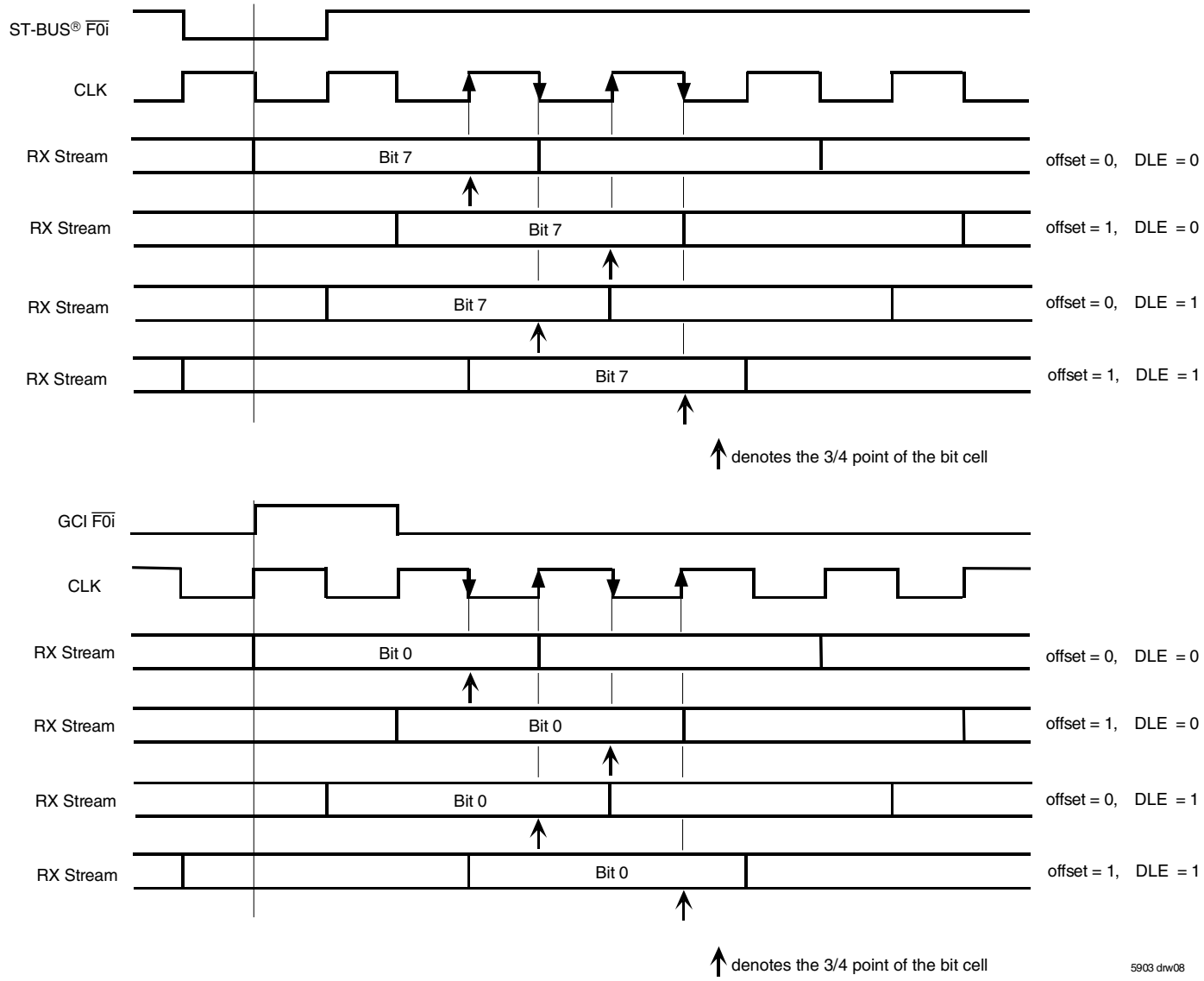


Figure 6. Examples for Input Offset Delay Timing in 8 Mb/s, 4 Mb/s and 2 Mb/s mode (Continued)

JTAG SUPPORT

The IDT72V71623 JTAG interface conforms to the Boundary-Scan standard IEEE-1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the boundary-scan circuitry is controlled by an external test access port (TAP) Controller.

TEST ACCESS PORT (TAP)

The Test Access Port (TAP) provides access to the test functions of the IDT72V71623. It consists of three input pins and one output pin.

•Test Clock Input (TCK)

TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remain independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.

•Test Mode Select Input (TMS)

The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to VCC when it is not driven from an external source.

•Test Data Input (TDI)

Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to VCC when it is not driven from an external source.

•Test Data Output (TDO)

Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high-impedance state.

•Test Reset ($\overline{TRST}$)

Reset the JTAG scan structure. This pin is internally pulled to VCC.

INSTRUCTION REGISTER

In accordance with the IEEE-1149.1 standard, the IDT72V71623 uses public instructions. The IDT72V71623 JTAG Interface contains a two-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning.

Value	Instruction
00	EXTEST
11	BYPASS
01 or 10	SAMPLE/PRELOAD

JTAG Instruction Register Decoding

TEST DATA REGISTER

As specified in IEEE-1149.1, the IDT72V71623 JTAG Interface contains two test data registers:

•The Boundary-Scan register

The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the IDT72V71623 core logic.

•The Bypass Register

The Bypass register is a single stage shift register that provides a one-bit path from TDI to its TDO. The IDT72V71623 boundary scan register bits are shown in Table 10. Bit 0 is the first bit clocked out. All three-state enable bits are active high.

TABLE 10 — BOUNDARY SCAN REGISTER BITS

Device Pin	Boundary Scan Bit 0 to bit 168		
	Three-State Control	Output Scan Cell	Input Scan Cell
ODE			0
$\overline{\text{RESET}}$			1
CLK			2
$\overline{\text{F0i}}$			3
FE/HCLK			4
WFPS			5
$\overline{\text{DS}}$			6
$\overline{\text{CS}}$			7
R/$\overline{\text{W}}$			8
A0			9
A1			10
A2			11
A3			12
A4			13
A5			14
A6			15
A7			16
A8			17
A9			18
A10			19
A11			20
IC			21
A12			22
A13			23
$\overline{\text{DTA}}$		24	
D15	25	26	27
D14	28	29	30
D13	31	32	33
D12	34	35	36
D11	37	38	39
D10	40	41	42
D9	43	44	45
D8	46	47	48
D7	49	50	51
D6	52	53	54
D5	55	56	57
D4	58	59	60
D3	61	62	63
D2	64	65	66
D1	67	68	69
D0	70	71	72
OEI15	73	74	
OEI14	75	76	
OEI13	77	78	
OEI12	79	80	
OEI11	81	82	
OEI10	83	84	
OEI9	85	86	
OEI8	87	88	
IC			89
IC			90
IC			91
IC			92

Device Pin	Boundry Scan Bit 0 to bit 168		
	Three-State Control	Output Scan Cell	Input Scan Cell
IC			93
IC			94
IC			95
IC			96
OEI7	97	98	
OEI6	99	100	
OEI5	101	102	
OEI4	103	104	
OEI3	105	106	
OEI2	107	108	
OEI1	109	110	
OEI0	111	112	
IC			113
IC			114
IC			115
IC			116
IC			117
IC			118
IC			119
IC			120
TX15	121	122	
TX14	123	124	
TX13	125	126	
TX12	127	128	
TX11	129	130	
TX10	131	132	
TX9	133	134	
TX8	135	136	
RX15			137
RX14			138
RX13			139
RX12			140
RX11			141
RX10			142
RX9			143
RX8			144
TX7	145	146	
TX6	147	148	
TX5	149	150	
TX4	151	152	
TX3	153	154	
TX2	155	156	
TX1	157	158	
TX0	159	160	
RX7			161
RX6			162
RX5			163
RX4			164
RX3			165
RX2			166
RX1			167
RX0			168

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
Vi	Voltage on Digital Inputs	GND -0.3	5.3	V
Io	Current at Digital Outputs	-50	50	mA
Ts	Storage Temperature	-55	+125	° C
P_D	Package Power Dissapation	—	2	W

NOTE:
1. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Positive Supply	3.0	3.3	3.6	V
V_{IH}	Input HIGH Voltage	2.0	—	5.3	V
V_{IL}	Input LOW Voltage	—	—	0.8	V
T_{OP}	Operating Temperature Commercial	-40	25	+85	°C

NOTE:
1. Voltages are with respect to Ground unless otherwise stated.

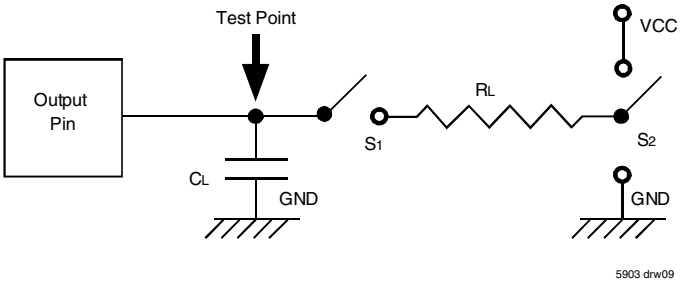
DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units
I_{CC} (2)	Supply Current	-	-	75	mA
I_{IL}(3,4)	Input Leakage (input pins)	-	-	60	µA
I_{OZ}(3,4)	High-impedance Leakage	-	-	60	µA
V_{OH}(5)	Output HIGH Voltage	2.4	-	-	V
V_{OL}(6)	Output LOW Voltage	-	-	0.4	V

NOTES:
1. Voltages are with respect to ground (GND) unless otherwise stated.
2. Outputs unloaded.
3. $0 \leq V \leq V_{CC}$.
4. Maximum leakage on pins (output or I/O pins in high-impedance state) is over an applied voltage (V).
5. IOH = 10 mA.
6. IOL = 10 mA.

AC ELECTRICAL CHARACTERISTICS - TIMING PARAMETER MEASUREMENT VOLTAGE LEVELS

Symbol	Rating	Level	Unit
V_{TT}	TTL Threshold	1.5	V
V_{HM}	TTL Rise/Fall Threshold Voltage HIGH	2.0	V
V_{LM}	TTL Rise/Fall Threshold Voltage LOW	0.8	V



S1 is open circuit except when testing output levels or high-impedance states.

S2 is switched to V_{CC} or GND when testing output levels or high-impedance states.

Figure 7. Output Load

AC ELECTRICAL CHARACTERISTICS - FRAME PULSE AND CLK

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{FPW}[1]	Frame Pulse Width (ST-BUS®, GCI)				
	Bit rate = 2.048 Mb/s	26	—	295	ns
	Bit rate = 4.096 Mb/s	26	—	145	ns
	Bit rate = 8.192 Mb/s or 16.384 Mb/s	26	—	65	ns
t_{FPS}[1]	Frame Pulse Setup time before CLK falling (ST-BUS® or GCI)	5	—	—	ns
t_{FPH}[1]	Frame Pulse Hold Time from CLK falling (ST-BUS® or GCI)	10	—	—	ns
t_{CP}[1]	CLK Period				
	Bit rate = 2.048 Mb/s	190	—	300	ns
	Bit rate = 4.096 Mb/s	110	—	150	ns
	Bit rate = 8.192 Mb/s or 16.384 Mb/s	58	—	70	ns
t_{CH}[1]	CLK Pulse Width HIGH				
	Bit rate = 2.048 Mb/s	85	—	150	ns
	Bit rate = 4.096 Mb/s	50	—	75	ns
	Bit rate = 8.192 Mb/s or 16.384 Mb/s	20	—	40	ns
t_{CL}[1]	CLK Pulse Width LOW				
	Bit rate = 2.048 Mb/s	85	—	150	ns
	Bit rate = 4.096 Mb/s	50	—	75	ns
	Bit rate = 8.192 Mb/s or 16.384 Mb/s	20	—	40	ns
t_r, t_f	Clock Rise/Fall Time	—	—	10	ns
t_{HFPW}[2]	Wide Frame Pulse Width				
	HCLK = 4.096 MHz		244		ns
	HCLK = 8.192 MHz		122		ns
t_{HFPS}[2]	Frame Pulse Setup Time before HCLK 4 MHz falling	50	—	150	ns
t_{HFPH}[2]	Frame Pulse Hold Time from HCLK 4 MHz falling	50	—	150	ns
t_{HFPS}[2]	Frame Pulse Setup Time before HCLK 8 MHz rising	45	—	90	ns
t_{HFPH}[2]	Frame Pulse Hold Time from HCLK 8 MHz rising	45	—	90	ns
t_{HCP}[2]	HCLK Period				
	@ 4.096 MHz		244		ns
	@ 8.192 MHz		122		ns
t_{Hr}, t_{Hf}	HCLK Rise/Fall Time	—	—	10	ns
t_{DIF}[3]	Delay between falling edge of HCLK and falling edge of CLK	-10	—	10	ns

NOTES:
1. WFPS Pin = 0.
2. WFPS Pin = 1.
3. WFPS Pin = 0 or 1.

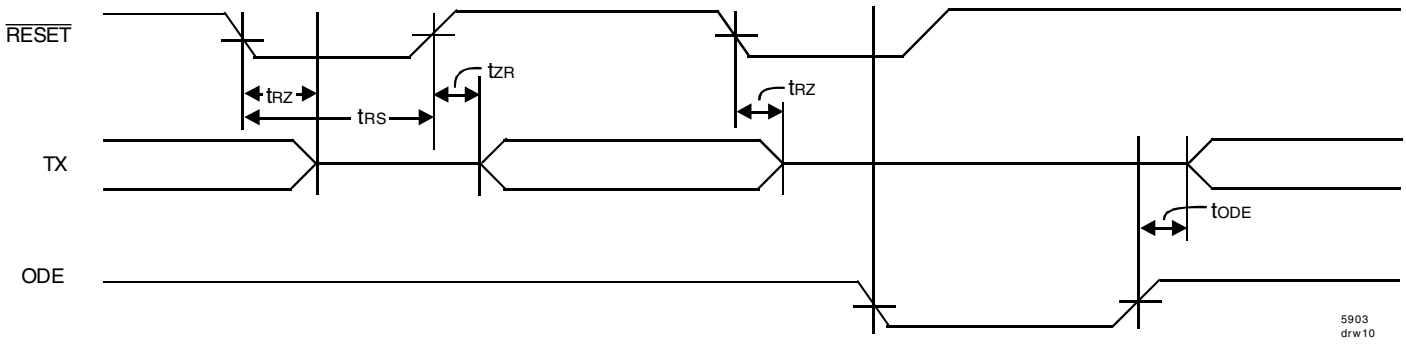


Figure 8. Reset and ODE Timing

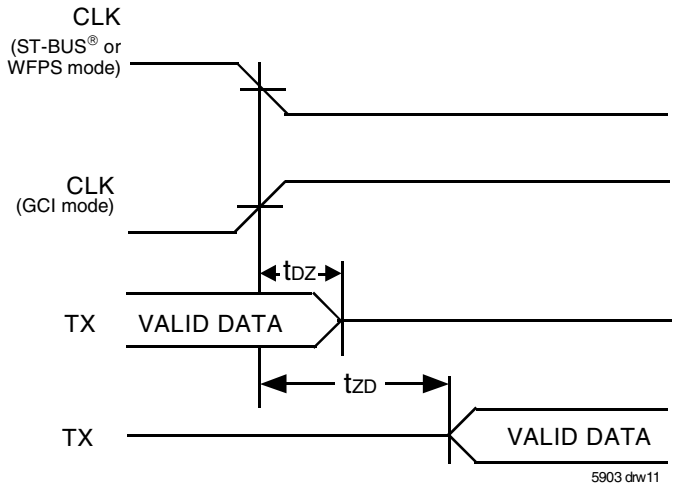


Figure 9. Serial Output and External Control

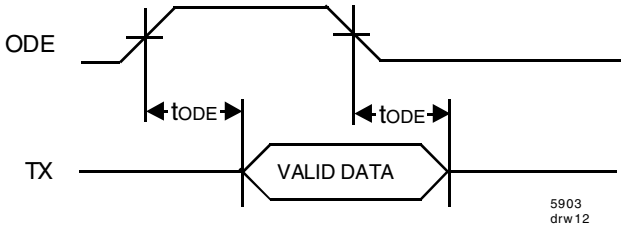


Figure 10. Output Driver Enable (ODE)

AC ELECTRICAL CHARACTERISTICS - MICROPROCESSOR INTERFACE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CSS}	CS Setup from DS falling	0	—	—	ns
t_{RWS}	R/W Setup from DS falling	3	—	—	ns
t_{ADS}	Address Setup from DS falling	2	—	—	ns
t_{CSH}	CS Hold after DS rising	0	—	—	ns
t_{RWH}	R/W Hold after DS Rising	3	—	—	ns
t_{ADH}	Address Hold after DS Rising	2	—	—	ns
t_{DDR} (1)	Data Setup from $\overline{DTA}$ LOW on Read	2	—	—	ns
t_{DHR} (1,2,3)	Data Hold on Read	10	15	25	ns
t_{DSW}	Data Setup on Write (Register Write)	10	—	—	ns
t_{SWD}	Valid Data Delay on Write (Connection Memory Write)	-	—	0	ns
t_{DHW}	Data Hold on Write	5	—	—	ns
t_{DSPW}	DS Pulse Width	5	—	—	ns
t_{CKAK}	Clock to ACK	—	—	35	ns
t_{AKD} (1)	Acknowledgment Delay:				
	Reading/Writing Registers			30	ns
	Reading/Writing Memory @ 2.048 Mb/s			345	ns
	@ 4.096 Mb/s			200	ns
	@ 8.192 Mb/s or 16.384 Mb/s			120	ns
t_{AKH} (1,2,3)	Acknowledgment Hold Time	—	—	15	ns
t_{DSS} (4)	Data Strobe Setup Time	2	—	—	ns

NOTES:
1. C_L= 150pF
2. R_L = 1K
3. High-Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.
4. To achieve one clock cycle fast memory access, this setup time, t_{DSS} should be met. Otherwise, worst case memory access operation is determined by t_{AKD}.

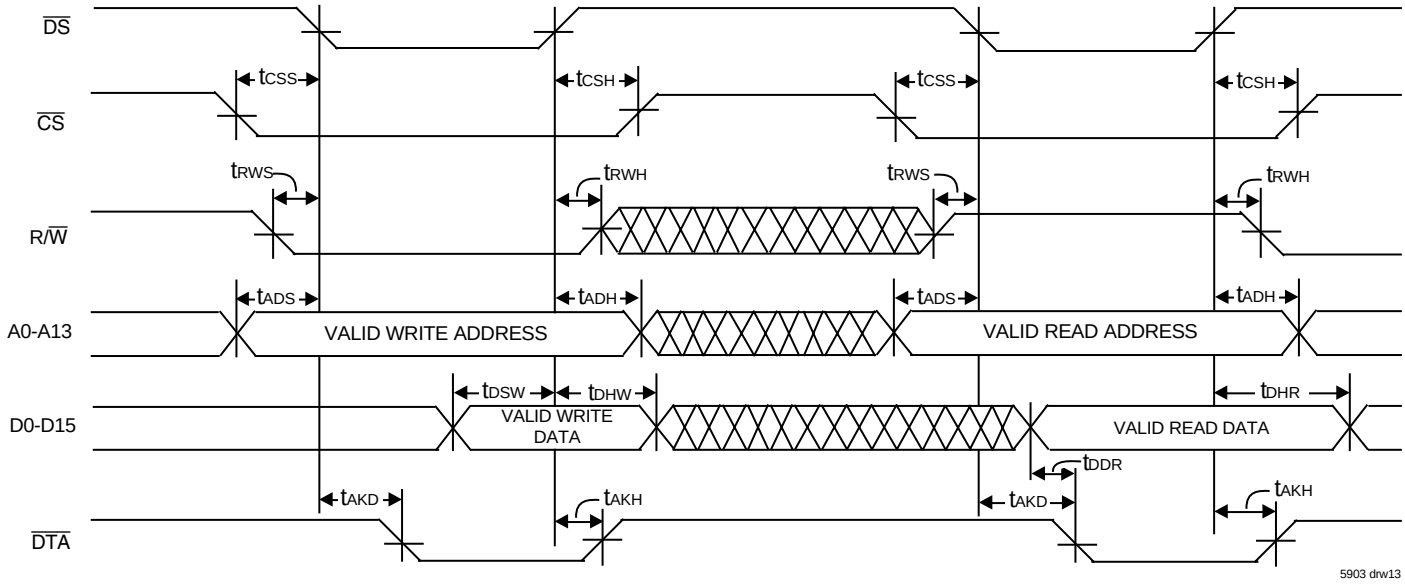


Figure 11. Asyncronous Bus Timing

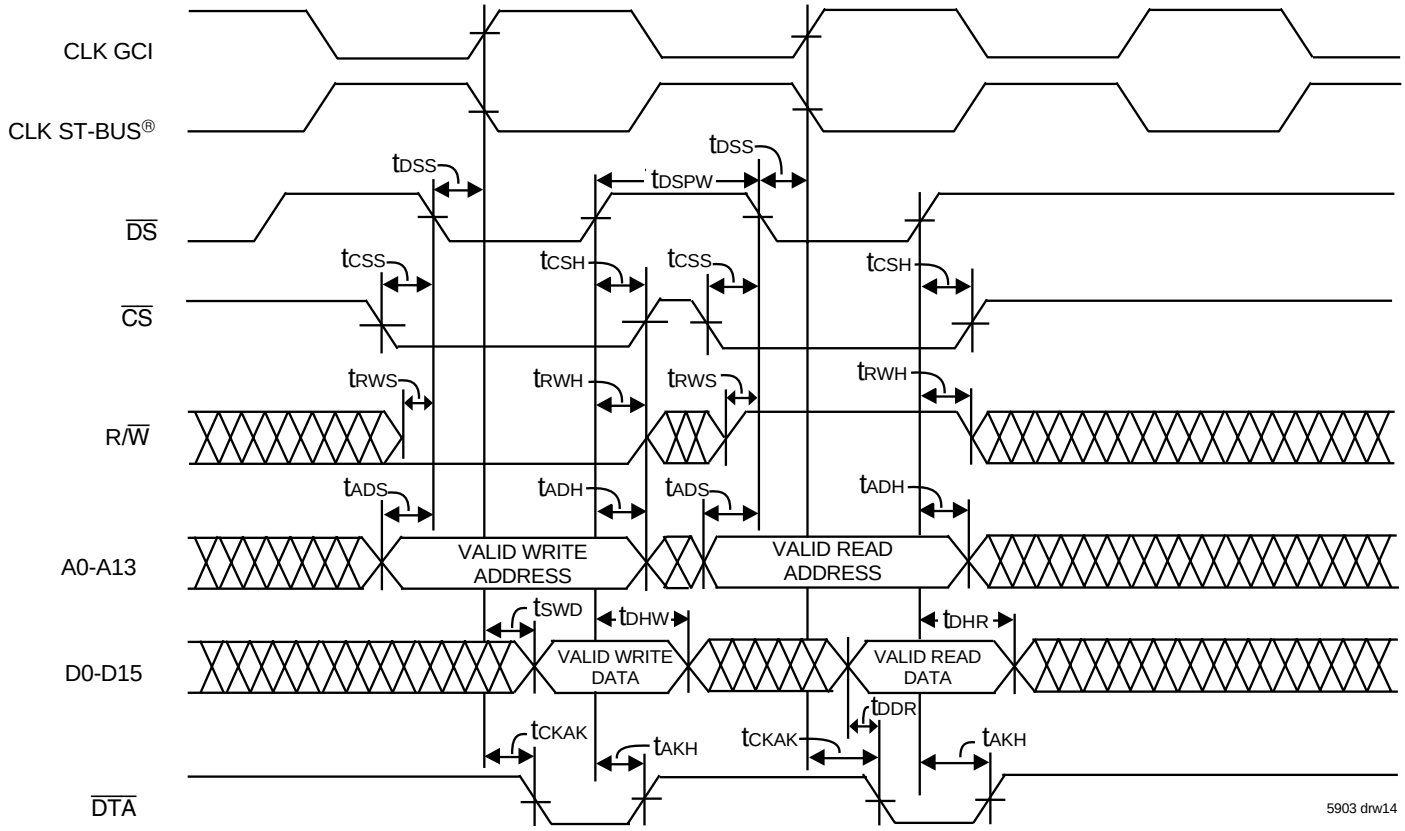
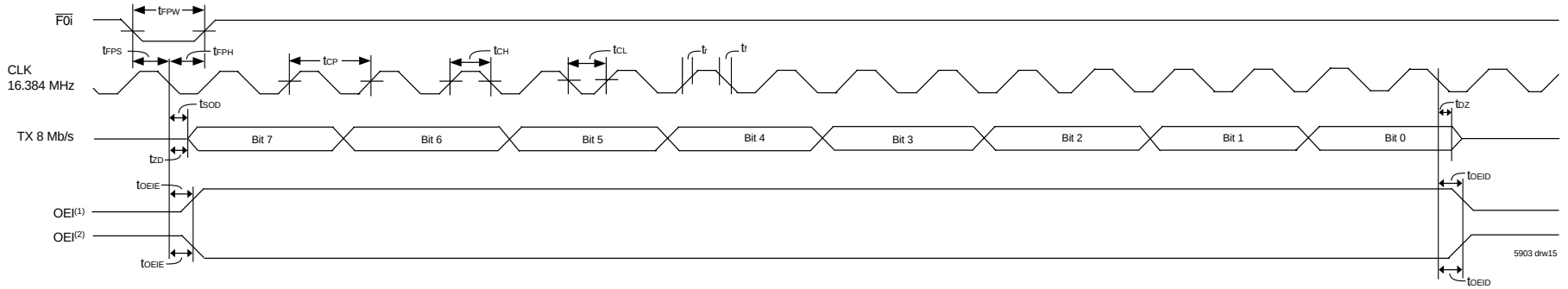


Figure 12. Syncronous Bus Timing



NOTES:
1. When OEPOL = 1, OEI is HIGH when TX is active and LOW when TX is in three-state.
2. When OEPOL = 0, OEI is LOW when TX is active and HIGH when TX is in three-state.

Figure 13. Output Enable Indicator Timing (8 Mb/s ST-BUS®)

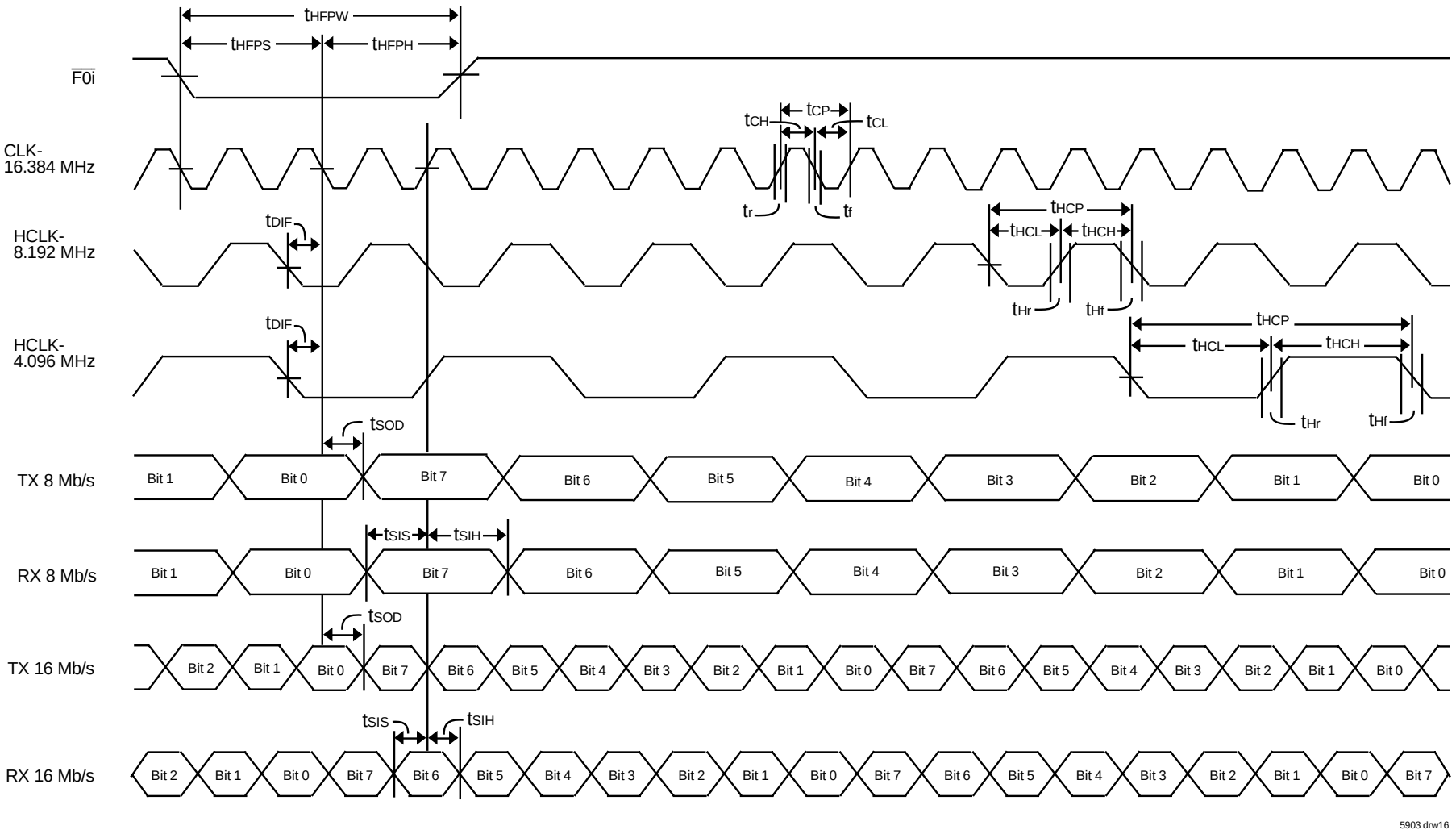


Figure 14. WFPS Timing

AC ELECTRICAL CHARACTERISTICS(1) — SERIAL STREAM (ST-BUS® and GCI)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{SIS}	RX Setup Time	2	—	—	ns
t_{SIH}	RX Hold Time	10	—	—	ns
t_{SOD}	TX Delay – Active to Active	—	—	22	ns
t_{DZ}(1)	TX Delay – Active to High-Z	—	—	22	ns
t_{ZD}(1)	TX Delay – High-Z to Active	—	—	22	ns
t_{ODE}(1)	Output Driver Enable (ODE) Delay	—	—	30	ns
t_{OEIE}	Output Enable Indicator (OEI) Enable	—	—	40	ns
t_{OEID}	Output Enable Indicator (OEI) Disable	—	—	25	ns
t_{RZ}	Active to High-Z on Master Reset	—	—	30	ns
t_{ZR}	High-Z to Active on Master Reset	—	—	30	ns
t_{Rs}	Reset pulse width	100	—	—	ns

NOTE:
1. High-Impedance is measured by pulling to the appropriate rail with R_L (1KΩ), with timing corrected to cancel time taken to discharge C_L (150 pF).

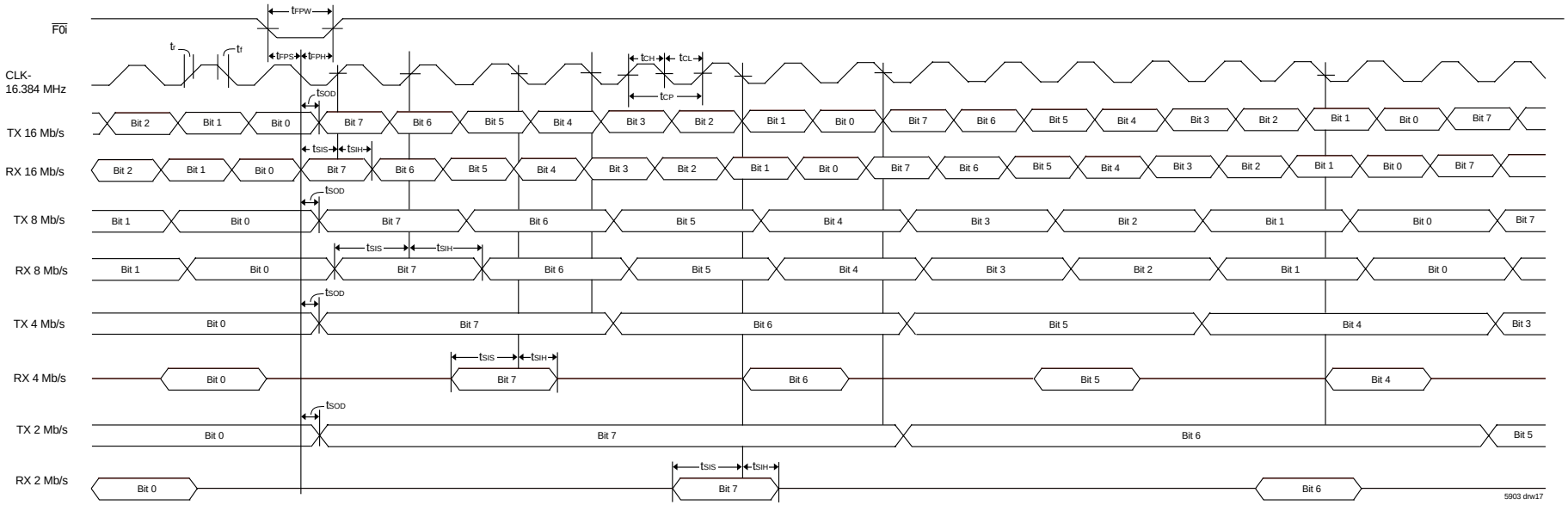


Figure 15. ST-BUS® Timing

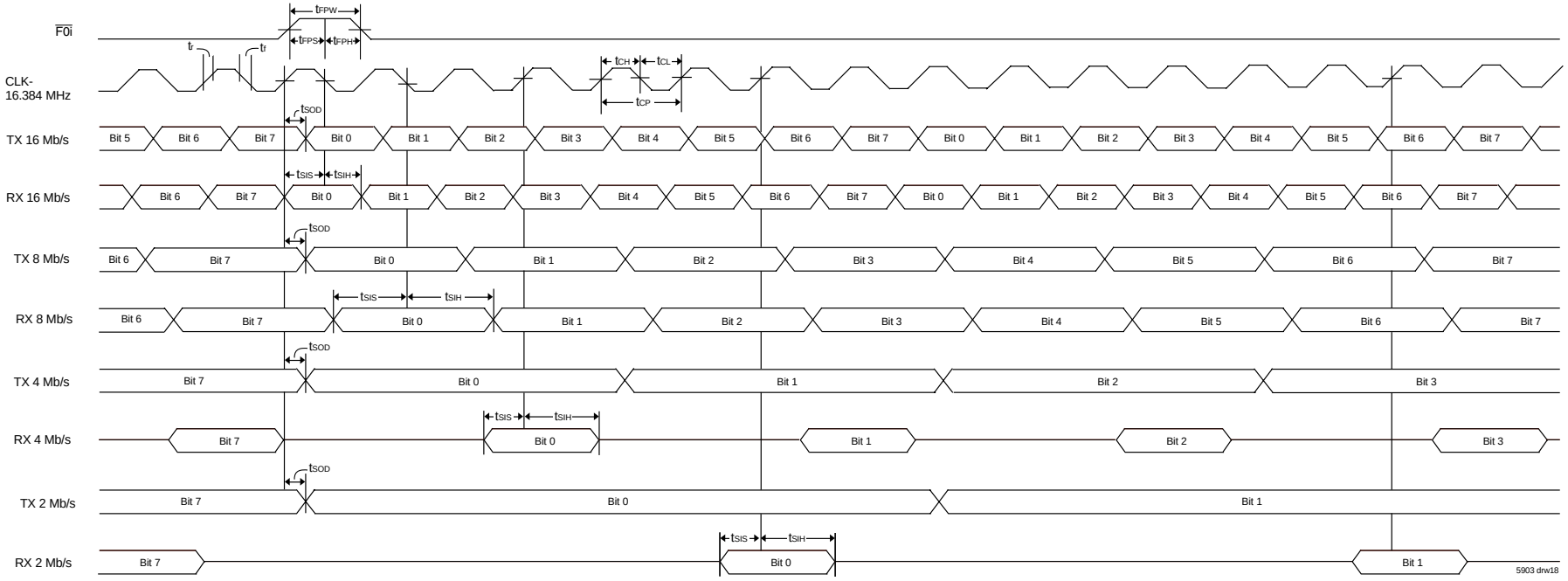
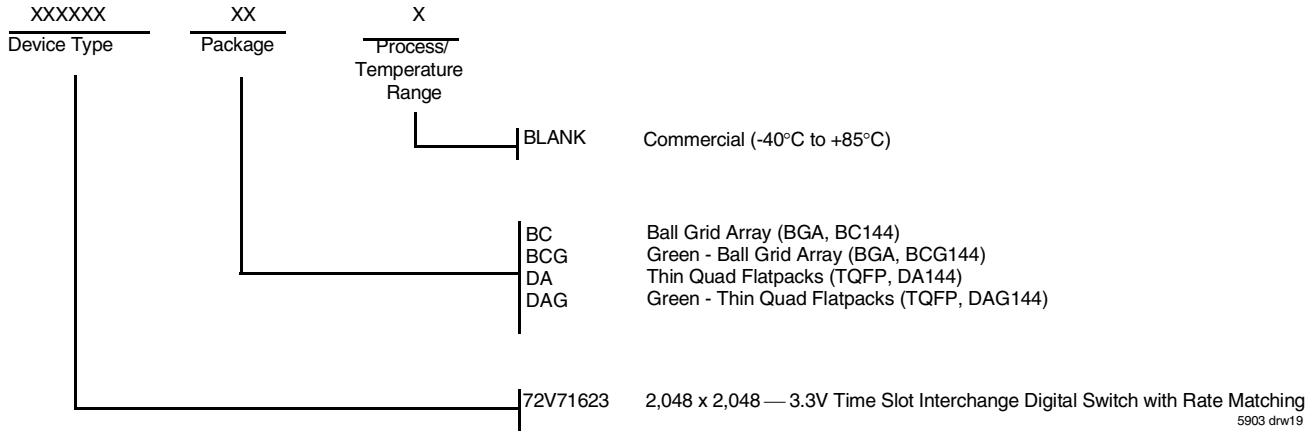


Figure 16. GCI Timing

ORDERING INFORMATION



5903 drw19

DATASHEET DOCUMENT HISTORY

6/07/2000	pgs. 3 and 4.
10/10/2000	pgs. 1 through 28.
11/20/2000	pgs. 10 and 11.
03/09/2001	pg. 19
08/20/2001	pg. 22.
10/22/2001	pg. 1.
1/04/2002	pgs. 1 and 19.
5/17/2002	pg. 26
3/10/2005	pgs. 1, 4, 6, 10, and 26
3/22/2005	pgs. 1-3, 26, 28
3/23/2005	pgs. 4, 5, 13, 28
2/09/2009	pg. 28 removed IDT from orderable part number

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