

# DAC1653D/DAC1658D

Dual 16-bit DAC: 10 Gbps JESD204B interface: x2, x4 and x8 interpolating

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Advance data sheet

## 1. General description

The DAC1653D and the DAC1658D are high-speed high-performance 16-bit dual channel Digital-to-Analog Converters (DACs). The devices provide sample rates up to 1.5 Gsps with selectable x2, x4 and x8 interpolation filters optimized for multi-carrier and broadband wireless transmitters.

When both devices are referred to in this data sheet, the following convention will be used: DAC165xD.

The DAC165xD integrates a JEDEC JESD204B compliant high-speed serial input data interface running up to 10 Gbps allowing dual channel input sampling at up to 750 Msps over four differential lanes. It offers numerous advantages over traditional parallel digital interfaces:

- Easier Printed-Circuit Board (PCB) layout
- Lower radiated noise
- Lower pin count
- Self-synchronous link
- Skew compensation
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 compliant
- Harmonic clocking support
- Assured FPGA interoperability

There are two versions of the DAC165xD:

- Low common-mode output voltage (part identification DAC1653D)
- High common-mode output voltage (part identification DAC1658D)

An optional on-chip digital modulator converts the complex I/Q pattern from baseband to IF. The mixer frequency is set by writing to the Serial Peripheral Interface (SPI) control registers associated with the on-chip 40-bit Numerically Controlled Oscillator (NCO). This accurately places the IF carrier in the frequency domain. The 16-bit phase adjustment feature, the 12-bit digital gain and the 16-bit digital offset enable full control of the analog output signals.

The DAC165xD is fully compliant with device subclass 1 of the JEDEC JESD204B standard, guaranteeing deterministic and repeatable interface latency using the differential SYSREF signal. The device also supports harmonic clocking to reduce system-level clock synthesis and distribution challenges.

The Advance Information presented herein represents a product that is developmental or prototype. The noted characteristics are design targets. Integrated Device Technologies, Inc. (IDT) reserves the right to change any circuitry or specifications without notice.



Multiple Device Synchronization (MDS) enables multiple DAC channels to be sample synchronous MDS and phase coherent to within one DAC clock period. MDS is ideal for LTE and LTE-A MIMO transceiver applications.

The DAC165xD includes a  $\times 2$ ,  $\times 4$  or  $\times 8$  divider to achieve the best possible noise performance at the analog outputs, allowing harmonic clocking through the system. The internal regulator adjusts the full-scale output current between 8.1 mA and 34 mA.

The device is available in a VFQFP-N 56 package (8 mm  $\times$  8 mm). It is supported by customer demo boards that are supplied with or without FPGA logic devices.

## 2. Features and benefits

- dual channel 16-bit resolution
- 1.50 Gbps maximum output update rate
- JEDEC JESD204B device subclass I compliant: SYSREF based deterministic and repeatable interface latency
- Multiple device synchronization enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period
- 1, 2 or 4 configurable JESD204B serial input lanes running up to 10 Gbps with embedded termination and programmable equalization
- 750 Msps maximum baseband input data rate
- SPI interface (3-wire or 4-wire mode) for control setting and status monitoring
- differential scalable output current from 8.1 mA to 34 mA
- embedded NCO with 40-bit programmable frequency and 16-bit phase adjustment
- embedded complex (IQ) digital modulator
- 1.2 V and 3.3 V power supplies
- flexible SPI power supply (1.8 V or 1.2 V) ensuring compatibility with on-board SPI bus
- flexible differential SYNC signals power supply (1.8 V or 1.2 V) ensuring compatibility with on-board devices
- SFDR<sub>RBW</sub> = 85 dBc typical ( $f_s = 1.50$  Gbps; interpolation  $\times 2$ ; bandwidth = 250 MHz;  $f_{out} = 150$  MHz)
- NSD =  $-164$  dBm/Hz typical ( $f_o = 20$  MHz)
- IMD3 = 85 dBc typical ( $f_s = 1.50$  Gbps; interpolation  $\times 2$ ;  $f_{o1} = 152$  MHz;  $f_{o2} = 155.1$  MHz)
- one carrier ACLR = 77 dB typical ( $f_s = 1.50$  Gbps;  $f_{NCO} = 230$  MHz)
- RF enable/disable pin and RF automatic mute
- clock divider by 2, 4 and 6 available at the input of the clock path
- group delay compensation
- external analog offset control (10-bit auxiliary DACs)
- power-down mode and sleep mode controls
- on-chip 0.7 V reference
- industrial temperature range  $-40$  °C to  $+85$  °C
- low and high common-mode output voltage
- VFQFP-N 56 package (8 mm  $\times$  8 mm)

### 3. Applications

- Wireless infrastructure radio base station transceivers, including: LTE-A, LTE, MC-GSM, W-CDMA, TD-SCDMA
- LMDS/MMDS, point-to-point microwave backhaul
- Direct Digital Synthesis (DDS) instruments
- High-definition video broadcast production equipment
- Automated Test Equipment (ATE)

### 4. Ordering information

**Table 1. Ordering information**

Type number	Package		
	Name	Description	Version
DAC1653D1G5NLG	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	PSC-4110
DAC1653D1G25NLG	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	PSC-4110
DAC1653D1G0NLG	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	PSC-4110
DAC1658D1G5HN	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	PSC-4110
DAC1658D1G25NLG	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	PSC-4110
DAC1658D1G0NLG	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	PSC-4110

## 5. Block diagram

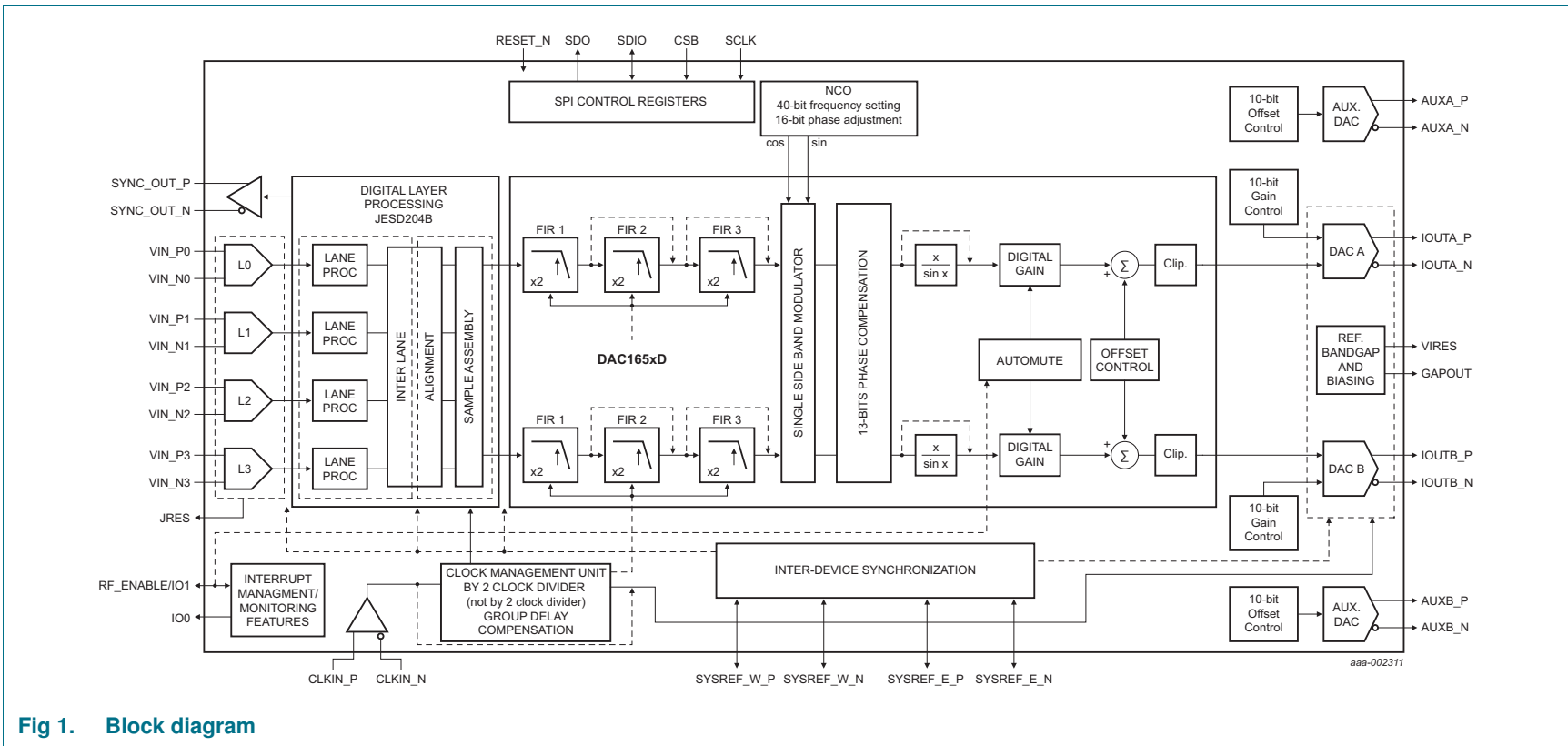
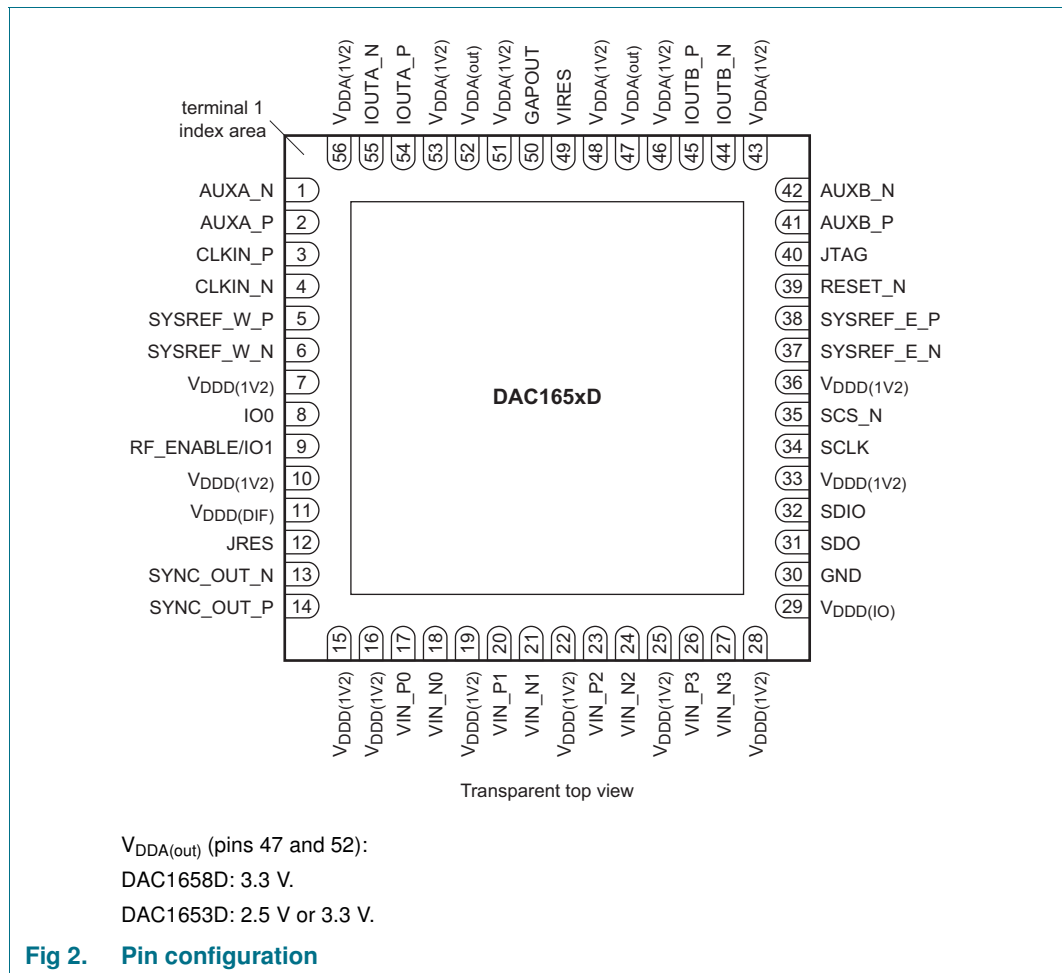


Fig 1. Block diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Type <sup>[1]</sup>	Description
AUXA_N	1	O	complementary auxiliary DAC A output current
AUXA_P	2	O	auxiliary DAC A output current
CLKIN_P	3	I	DAC clock positive input
CLKIN_N	4	I	DAC clock negative input
SYSREF_W_P	5	I/O	multiple devices synchronization positive signal, west side
SYSREF_W_N	6	I/O	multiple devices synchronization negative signal, west side
V <sub>DDD(1V2)</sub>	7	P	1.2 V digital power supply
IO0	8	O	IO port bit 0
RF_ENABLE/IO1	9	I/O	IO port bit 1 or RF enable pin (see Section automute)
V <sub>DDD(1V2)</sub>	10	P	1.2 V digital power supply

Table 2. Pin description ...continued

Symbol	Pin	Type <sup>[1]</sup>	Description
V <sub>DDD(DIFF)</sub>	11	P	flexible power supply for SYNC differential signals (1.2 V or 1.8 V; see <a href="#">Section 11.2.1.1</a> )
JRES	12	I/O	Calibration resistor (6 kΩ) for serial lanes termination
SYNC_OUT_N	13	O	synchronization request to transmitter, complementary output
SYNC_OUT_P	14	O	synchronization request to transmitter
V <sub>DDD(1V2)</sub>	15	P	1.2 V digital power supply for JESD204B SYNCB/reference interface
V <sub>DDD(1V2)</sub>	16	P	1.2 V digital power supply for JESD204B Lane 0
VIN_P0	17	I <sup>[2]</sup>	serial interface lane 0 positive input
VIN_N0	18	I <sup>[2]</sup>	serial interface lane 0 negative input
V <sub>DDD(1V2)</sub>	19	P	1.2 V digital power supply for JESD204B Lane 0 and Lane 1
VIN_P1	20	I <sup>[2]</sup>	lane 1 serial interface positive input
VIN_N1	21	I <sup>[2]</sup>	serial interface lane 1 negative input
V <sub>DDD(1V2)</sub>	22	P	1.2 V digital power supply for JESD204B Lane 1 and Lane 2
VIN_P2	23	I <sup>[2]</sup>	serial interface lane 2 positive input
VIN_N2	24	I <sup>[2]</sup>	serial interface lane 2 negative input
V <sub>DDD(1V2)</sub>	25	P	1.2 V digital power supply for JESD204B Lane 2 and Lane 3
VIN_P3	26	I <sup>[2]</sup>	serial interface lane 3 positive input
VIN_N3	27	I <sup>[2]</sup>	serial interface lane 3 negative input
V <sub>DDD(1V2)</sub>	28	P	1.2 V digital power supply for JESD204B Lane 3
V <sub>DDD(IO)</sub>	29	P	flexible power supply for SPI IOs and IO0/IO1 signals (1.2 V or 1.8 V; see section xxxx)
GND	30	G	connect to ground
SDO	31	O	SPI data output
SDIO	32	I/O	SPI data input/output
V <sub>DDD(1V2)</sub>	33	P	1.2 V digital power supply
SCLK	34	I	SPI clock
SCS_N	35	I	SPI chip select (active LOW)
V <sub>DDD(1V2)</sub>	36	P	1.2 V digital power supply
SYSREF_E_N	37	I/O	multiple devices synchronization negative signal, east side
SYSREF_E_P	38	I/O	multiple devices synchronization positive signal, east side
RESET_N	39	I	general reset (active LOW)
JTAG	40	G	JTAG connection (connect to ground)
AUXB_P	41	O	auxiliary DAC B output current
AUXB_N	42	O	complementary auxiliary DAC B output current
V <sub>DDA(1V2)</sub>	43	P	1.2 V analog power supply
IOU <sub>T</sub> B_N	44	O	DAC B output current
IOU <sub>T</sub> B_P	45	O	complementary DAC B output current
V <sub>DDA(1V2)</sub>	46	P	1.2 V analog power supply
V <sub>DDA(out)</sub>	47	P	DAC1658D: 3.3 V analog power supply DAC1653D: 2.5 V or 3.3 V analog power supply

**Table 2.** Pin description ...continued

Symbol	Pin	Type <sup>[1]</sup>	Description
V <sub>DDA(1V2)</sub>	48	P	1.2 V PLL analog power supply
VIRES	49	I/O	DAC biasing resistor
GAPOUT	50	I/O	band gap input/output voltage
V <sub>DDA(1V2)</sub>	51	P	1.2 V PLL analog power supply
V <sub>DDA(out)</sub>	52	P	DAC1658D: 3.3 V analog power supply DAC1653D: 2.5 V or 3.3 V analog power supply
V <sub>DDA(1V2)</sub>	53	P	1.2 V analog power supply
IOUTA_P	54	O	complementary DAC A output current
IOUTA_N	55	O	DAC A output current
V <sub>DDA(1V2)</sub>	56	P	1.2 V analog power supply

[1] P: power supply; G: ground; I: input; O: output.

[2] JESD204B input lanes can be swapped between P and N using dedicated registers. The order of lanes can be updated logically (see [Section 11.7.5.4](#)).

## 7. Limiting values

**Table 3.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DDA(out)</sub>	analog supply voltage	DAC1658D: 3.3 V DAC1653D: 2.5 V or 3.3 V	-0.5	+4.6	V
V <sub>DD(1V2)</sub>	digital supply voltage (1.2 V)		-0.5	+1.5	V
V <sub>DDA(1V2)</sub>	analog supply voltage (1.2 V)		-0.5	+1.5	V
V <sub>I</sub>	input voltage	input pins referenced to GND	-0.5	<tbid>	V
V <sub>O</sub>	output voltage	pins IOUTA_P; IOUTA_N; IOUTB_P; IOUTB_N; AUXA_P; AUXA_N; AUXB_P and AUXB_N; referenced to GND	-0.5	+4.6	V
V <sub>DD(IO)</sub>	I/O digital supply voltage	pins SDO; SDIO; SCLK; SCS_N; RESET_N; JTAG; IO0; RF_ENABLE/IO1	-0.5	2.1	V
V <sub>DD(dif)</sub>	differential digital supply voltage	pins SYNC_OUT_P; SYNC_OUT_N	-0.5	≤ V <sub>DD(IO)</sub>	V
T <sub>stg</sub>	storage temperature		-55	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C
T <sub>j</sub>	junction temperature		-40	+125	°C

## 8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
<b>JEDEC 4L board</b>				
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1] 19	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1] 6.8	K/W
<b>Application board</b>				
$R_{th(j-a)}$	thermal resistance from junction to ambient	6 layers	[2] 15.9	K/W
		8 layers	[2] 15.6	K/W
		12 layers	[2] 14.0	K/W

[1] In compliance with JEDEC test board; in free air with 64 thermal vias, class 5.

[2] In free air with 64 thermal vias, class 5.

## 9. Static characteristics

### 9.1 Common characteristics

Table 5. Common characteristics

$V_{DDA1V2} = 1.2\text{ V}$ ;  $V_{DDD1V2} = 1.2\text{ V}$ ; Typical values measured at  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ;  $R_L = 50\text{ }\Omega$ ;  $I_{O(is)} = 20\text{ mA}$ ; maximum sample rate used; no auxiliary DAC; no inverse (sinus  $x$ ) /  $x$ ; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
<b>Voltages</b>							
$V_{DDA}$	analog supply voltage	DAC1658D: 3.3 V	C	3.15	3.3	3.45	V
		DAC1653D: 2.5 V or 3.3 V	C	2.38	2.5 / 3.3	3.45	V
$V_{DDD(1V2)}$	digital supply voltage (1.2 V)		C	1.14	1.2	1.26	V
$V_{DDA(1V2)}$	analog supply voltage (1.2 V)		C	1.1	1.2	1.3	V
$V_{DDD(IO)}$	I/O digital supply voltage		C	1.14	1.2	2.1	V
			C	1.14	1.8	2.1	V
$V_{DDD(dif)}$	differential digital supply voltage	$V_{DDD(dif)} \leq V_{DDD(IO)}$	C	1.14	1.2	2.1	V
			C	1.14	1.8	2.1	V
<b>Clock inputs (pins CLKIN_P, CLKIN_N)</b>							
$V_i$	input voltage	$ V_{gpd}  < 50\text{ mV}$	C	[2] 825	-	<td>	mV
$V_{idth}$	input differential threshold voltage	$ V_{gpd}  < 50\text{ mV}$	C	[2] -100	-	+100	mV
$R_i$	input resistance		D	-	<td>	-	M $\Omega$
$C_i$	input capacitance		D	-	<td>	-	pF

**Table 5. Common characteristics ...continued**

$V_{DDA1V2} = 1.2\text{ V}$ ;  $V_{DD1V2} = 1.2\text{ V}$ ; Typical values measured at  $T_{amb} = +25\text{ °C}$ ;  $R_L = 50\ \Omega$ ;  $I_{O(fs)} = 20\text{ mA}$ ; maximum sample rate used; no auxiliary DAC; no inverse (sinus  $x$ ) /  $x$ ; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
<b>Digital inputs/outputs (SYSREF_W_P/SYSREF_W_N, SYSREF_E_P/SYSREF_E_N)</b>							
$V_i$	input voltage	$ V_{gpd}  < 50\text{ mV}$	C	[2] 825	-	<tbid>	mV
$V_{idth}$	input differential threshold voltage	$ V_{gpd}  < 50\text{ mV}$	C	[2] -100	-	+100	mV
$R_i$	input resistance		D	-	100	-	$\Omega$
$C_i$	input capacitance		D	-	<tbid>	-	pF
<b>Digital inputs (pins SDO, SDIO, SCLK, SCS_N, RESET_N)</b>							
$V_{IL}$	LOW-level input voltage		C	GND	-	$0.3V_{DD(1O)}$	V
$V_{IH}$	HIGH-level input voltage		C	$0.7V_{DD(1O)}$	-	$V_{DD(1O)}$	V
<b>Digital inputs (VINx_P/VINx_N) compliant with the LV-OIF-11G-SR; CML format</b>							
$V_{cm}$	common-mode voltage	AC coupling is mandatory; controlled by SPI register	C	0.580	-	1.126	V
$V_{pp-diff}$	differential peak-to-peak voltage	at 6 Gbps	C	80	-	-	mV
		at 7.5 Gbps	C	80	-	-	mV
		at 10 Gbps	C	110	-	-	mV
$Z_{diff}$	differential impedance	controlled by SPI register	I	71	100	190	$\Omega$
$H_i-Z_{diff}$	differential high impedance		D	-	64	-	k $\Omega$
DR	data rate		D	-	-	10	Gbps
<b>Digital outputs (pins SYNC_OUT_P and SYNC_OUT_N)</b>							
$V_{cm}$	common-mode voltage	controlled by SPI register			-		
		$V_{DDdif} = 1.8\text{ V}$	C	1.0	-	1.7	V
		$V_{DDdif} = 1.2\text{ V}$	C	0.4	-	1.1	V
$V_{O(diff)(swing)}$	swing differential output voltage		C	100	-	1200	mV
DR	data rate	for test modes	D	-	-	1	Gbps
<b>Digital outputs (pins SDO, SDIO)</b>							
$V_{OL}$	LOW-level output voltage		C	-	-	$0.3V_{DDIO}$	V
$V_{OH}$	HIGH-level output voltage		C	$0.7V_{DDIO}$	-	-	V
<b>Reference voltage output (pin GAPOUT)</b>							
$V_{O(ref)}$	reference output voltage	$T_{amb} = 25\text{ °C}$	I	-	0.70	-	V

**Table 5. Common characteristics ...continued**

$V_{DDA1V2} = 1.2\text{ V}$ ;  $V_{DD1V2} = 1.2\text{ V}$ ; Typical values measured at  $T_{amb} = +25\text{ °C}$ ;  $R_L = 50\ \Omega$ ;  $I_{O(fs)} = 20\text{ mA}$ ; maximum sample rate used; no auxiliary DAC; no inverse (sinus  $x$ ) /  $x$ ; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
$I_{O(ref)}$	reference output current	external voltage = 0.70 V	D	-	<tbid>	-	$\mu\text{A}$
$\Delta V_{O(ref)}$	reference output voltage variation		D	-	<tbid>	-	ppm/°C

**Analog auxiliary outputs (pins AUXA\_P, AUXA\_N, AUXB\_P and AUXB\_N)**

$I_{O(fs)}$	full-scale output current	auxiliary DAC A; differential inputs	I	-	3.1	-	mA
		auxiliary DAC B; differential inputs	I	-	3.1	-	mA
$V_{O(aux)}$	auxiliary output voltage		C	0	-	2	V
$N_{DAC(aux)mono}$	auxiliary DAC monotonicity	guaranteed	D	-	10	-	bits

**DAC output timing**

$f_s$	sampling rate	DAC165xD1G50	C	-	-	1500	Msp
		DAC165xD1G25	C	-	-	1250	Msp
		DAC165xD1G	C	-	-	1000	Msp
$t_s$	settling time	$t_o = \pm 0.5\text{LSB}$	D	-	20	-	ns

**NCO frequency range;  $f_s = 1000\text{ Msp}$**

$f_{NCO}$	NCO frequency		D	0	-	$f_s$	MHz
$f_{step}$	step frequency	Normal mode	D	-	$f_s / 2^{40}$	-	Hz
		Low power mode (see Section 11.2.3.5)	D	-	$f_s / 2^5$	-	Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2]  $|V_{gpd}|$  represents the ground potential difference voltage. This is the voltage that results from current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltages.

## 9.2 Specific characteristics

**Table 6. Specific characteristics**

$V_{DDA1V2} = 1.2\text{ V}$ ;  $V_{DDD1V2} = 1.2\text{ V}$ ;  $V_{DDA3V3} = 3.3\text{ V}$ ; Typical values measured at  $T_{amb} = +25\text{ °C}$ ;  $R_L = 50\ \Omega$ ;  $I_{O(fs)} = 20\text{ mA}$ ; maximum sample rate used; no auxiliary DAC; no inverse (sinus  $x$ ) /  $x$ ; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658D: High common-mode			DAC1653D: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
<b>Currents</b>										
$I_{DDA}$	analog supply current (3.3 V)	all use cases	C	-	63	-	-	123	-	mA
$I_{DDD(IO)}$	digital supply current for IO pins	Link to SPI IO0/IO1 activity	C	-	1	-	-	1	-	mA
$I_{DDD(SYNC)}$	digital supply current for SYNC pins	$V_{DDD(diff)} = 1.2\text{ V}$	C	-	11	-	-	11	-	mA
		$V_{DDD(diff)} = 1.8\text{ V}$	C	-	19	-	-	19	-	mA
$I_{DDD}$	digital supply current	$f_s = 250\text{ Msps}$ ; $\times 2$ interpolation; NCO off; MDS off; invsync off; phase correction off; four JESD204B lanes at 1.25 Gbps	C	-	75	-	-	75	-	mA
		$f_s = 650\text{ Msps}$ ; $\times 2$ interpolation; NCO off; MDS off; invsync off; phase correction off; four JESD204B lanes at 3.25 Gbps	C	-	140	-	-	140	-	mA
		$f_s = 1000\text{ Msps}$ ; $\times 2$ interpolation; NCO off; MDS off; invsync off; phase correction off; four JESD204B lanes at 5 Gbps	C	-	197	-	-	197	-	mA
		$f_s = 1474.56\text{ Msps}$ ; $\times 2$ interpolation; NCO off; MDS off; invsync off; phase correction off; four JESD204B lanes at 7.3728 Gbps	C	-	274	-	-	274	-	mA
		$f_s = 1474.56\text{ Msps}$ ; $\times 2$ interpolation; NCO at 150 MHz; MDS off; invsync off; phase correction on; four JESD204B lanes at 7.3728 Gbps	C	-	340	-	-	340	-	mA
$I_{DDA(1V2)}$	analog supply current (1.2 V)		C	-	206	-	-	206	-	mA

**Table 6. Specific characteristics ...continued**

$V_{DDA1V2} = 1.2\text{ V}$ ;  $V_{DD1V2} = 1.2\text{ V}$ ;  $V_{DDA3V3} = 3.3\text{ V}$ ; Typical values measured at  $T_{amb} = +25\text{ °C}$ ;  $R_L = 50\ \Omega$ ;  $I_{O(fs)} = 20\text{ mA}$ ; maximum sample rate used; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658D: High common-mode			DAC1653D: Low common-mode			Unit		
				Min	Typ	Max	Min	Typ	Max			
<b>Power</b>												
$P_{tot}$	total power dissipation	$f_s = 250\text{ Msps}$ ; $\times 2$ interpolation; NCO on; MDS off; invsinc on; phase correction on; four JESD204B lanes at 1.25 Gbps $V_{DDA} = 3.3\text{ V}$ $V_{DDA} = 2.5\text{ V}$	C	-	-	-	-	-	mW			
			C	-	645	-	-	844	-	mW		
			C	-	-	-	-	746	-	mW		
		$f_s = 650\text{ Msps}$ ; $\times 2$ interpolation; NCO on; MDS off; invsinc off; phase correction off; four JESD204B lanes at 3.25 Gbps $V_{DDA} = 3.3\text{ V}$ $V_{DDA} = 2.5\text{ V}$	C	-	724	-	-	922	-	mW		
			C	-	-	824	72	824	-	mW		
		$f_s = 1000\text{ Msps}$ ; $\times 2$ interpolation; NCO on; MDS off; invsinc off; phase correction off; four JESD204B lanes at 5 Gbps $V_{DDA} = 3.3\text{ V}$ $V_{DDA} = 2.5\text{ V}$	C	-	743	-	-	991	-	mW		
			C	-	-	-	-	893	-	mW		
		$f_s = 1474.56\text{ Msps}$ ; $\times 2$ interpolation; NCO on; MDS off; invsinc off; phase correction off; four JESD204B lanes at 7.3728 Gbps $V_{DDA} = 3.3\text{ V}$ $V_{DDA} = 2.5\text{ V}$	C	-	885	-	-	1083	-	mW		
			C	-	-	-	-	985	-	mW		
			full power-down	C	-	1.2	-	-	1.2	-	mW	
		<b>Analog outputs (pins IOUTA_P, IOUTA_N, IOUTB_P, IOUTB_N)</b>										
		$I_{O(fs)}$	full-scale output current		D	8.1	-	34	8.1	-	34	mA

**Table 6. Specific characteristics ...continued**

$V_{DDA1V2} = 1.2\text{ V}$ ;  $V_{DD1V2} = 1.2\text{ V}$ ;  $V_{DDA3V3} = 3.3\text{ V}$ ; Typical values measured at  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ;  $R_L = 50\ \Omega$ ;  $I_{O(fs)} = 20\text{ mA}$ ; maximum sample rate used; no auxiliary DAC; no inverse (sinus  $x$ ) /  $x$ ; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658D: High common-mode			DAC1653D: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
$V_O$	output voltage		D	1.5	-	$V_{DDA}$	0	-	1.8	V
$V_{O(cm)}$	common-mode output voltage		D	2.2	3.05	-	-	0.5	-	V
$R_o$	output resistance		D	0	250	-	-	250	-	k $\Omega$

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics DAC165xD1G50**

$V_{DDA1V2} = 1.2\text{ V}$ ;  $V_{DD1V2} = 1.2\text{ V}$ ;  $V_{DDA3V3} = 3.3\text{ V}$ ; Typical values measured at  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ;  $RL = 50\ \Omega$ ;  $I_{O(f_s)} = 20\text{ mA}$ ; maximum sample rate used; no auxiliary DAC; no inverse (sinus  $x$ ) /  $x$ ; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	High common-mode			Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
SFDR	spurious-free dynamic range	$f_{data} = 737.28\text{ MHz}$ ; $f_s = 1474.56\text{ Msps}$ ; $B = f_s / 2$								
		$f_o = 20\text{ MHz}$ at $-1\text{ dBFS}$	I	-	85	-	-	85	-	dBc
		$f_o = 20\text{ MHz}$ at $-7\text{ dBFS}$	I	-	<td>	-	-	<td>	-	dBc
		$f_o = 20\text{ MHz}$ at $-14\text{ dBFS}$	I	-	<td>	-	-	<td>	-	dBc
		$f_o = 150\text{ MHz}$ at $-1\text{ dBFS}$ ; $V_{DDA} = 3.3\text{ V}$	I	-	83	-	-	83	-	dBc
		$f_o = 150\text{ MHz}$ at $-1\text{ dBFS}$ ; $V_{DDA} = 2.5\text{ V}$	I	-	83	-	-	81	-	dBc
		$f_o = 150\text{ MHz}$ at $-7\text{ dBFS}$	I	-	<td>	-	-	<td>	-	dBc
IMD3	third-order intermodulation distortion	$f_{o1} = 21\text{ MHz}$ ; $f_{o2} = 22\text{ MHz}$ ; $-7\text{ dBFS}$ ; $f_s = 1474.56\text{ Msps}$ ; $\times 2$ interpolation	I	-	86	-	-	86	-	dBc
		$f_{o1} = 152.1\text{ MHz}$ ; $f_{o2} = 155.1\text{ MHz}$ ; $-7\text{ dBFS}$ ; $f_s = 1474.56\text{ Msps}$ ; $\times 2$ interpolation	I	-	84	-	-	82	-	dBc
ACPR	adjacent channel power ratio	$f_s = 1474.56\text{ Msps}$ ; $\times 2$ interpolation; $f_o = 40\text{ MHz}$								
		1 WCDMA carrier; $B = 5\text{ MHz}$	D	-	82	-	-	82	-	dBc
		4 WCDMA carriers; $B = 20\text{ MHz}$	D	-	75	-	-	75	-	dBc
NSD	noise spectral density	$f_s = 1474.56\text{ Msps}$ ; $\times 2$ interpolation; $f_o = 20\text{ MHz}$ at $-1\text{ dBFS}$	D	-	-164	-	-	-162	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

**Table 8. Dynamic characteristics DAC165xD1G25**

$V_{DDA1V2} = 1.2\text{ V}$ ;  $V_{DDD1V2} = 1.2\text{ V}$ ;  $V_{DDA3V3} = 3.3\text{ V}$ ; Typical values measured at  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ;  $RL = 50\ \Omega$ ;  $I_{O(f_s)} = 20\text{ mA}$ ; maximum sample rate used; no auxiliary DAC; no inverse (sinus  $x$ ) /  $x$ ; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	High common-mode			Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
SFDR	spurious-free dynamic range	$f_{data} = 614.4\text{ MHz}$ ; $f_s = 1228.8\text{ Msps}$ ; $B = f_s / 2$								
		$f_o = 20\text{ MHz}$ at $-1\text{ dBFS}$	I	-	84	-	-	84	-	dBc
		$f_o = 20\text{ MHz}$ at $-7\text{ dBFS}$	I	-	<td>	-	-	<td>	-	dBc
		$f_o = 20\text{ MHz}$ at $-14\text{ dBFS}$	I	-	<td>	-	-	<td>	-	dBc
		$f_o = 150\text{ MHz}$ at $-1\text{ dBFS}$ ; $V_{DDA} = 3.3\text{ V}$	I	-	83	-	-	83	-	dBc
		$f_o = 150\text{ MHz}$ at $-1\text{ dBFS}$ ; $V_{DDA} = 2.5\text{ V}$	I	-	83	-	-	81	-	dBc
		$f_o = 150\text{ MHz}$ at $-7\text{ dBFS}$ $f_o = 150\text{ MHz}$ at $-14\text{ dBFS}$	I I	- -	<td> <td>	- -	- -	<td> <td>	- -	dBc dBc
IMD3	third-order intermodulation distortion	$f_{o1} = 21\text{ MHz}$ ; $f_{o2} = 22\text{ MHz}$ ; $-7\text{ dBFS}$ ; $f_s = 1228.8\text{ Msps}$ ; $\times 2$ interpolation	I	-	85	-	-	85	-	dBc
		$f_{o1} = 152.1\text{ MHz}$ ; $f_{o2} = 155.1\text{ MHz}$ ; $-7\text{ dBFS}$ ; $f_s = 1228.8\text{ Msps}$ ; $\times 2$ interpolation	I	-	84	-	-	82	-	dBc
ACPR	adjacent channel power ratio	$f_s = 1228.8\text{ Msps}$ ; $\times 2$ interpolation; $f_o = 40\text{ MHz}$								
		1 WCDMA carrier; $B = 5\text{ MHz}$	D	-	82	-	-	82	-	dBc
		4 WCDMA carriers; $B = 20\text{ MHz}$	D	-	75	-	-	75	-	dBc
NSD	noise spectral density	$f_s = 1228.8\text{ Msps}$ ; $\times 2$ interpolation; $f_o = 20\text{ MHz}$ at $-1\text{ dBFS}$	D	-	-164	-	-	-162	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

**Table 9. Dynamic characteristics DAC165xD1G**

$V_{DDA1V2} = 1.2\text{ V}$ ;  $V_{DDD1V2} = 1.2\text{ V}$ ;  $V_{DDA3V3} = 3.3\text{ V}$ ; Typical values measured at  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ;  $RL = 50\ \Omega$ ;  $I_{O(f_s)} = 20\text{ mA}$ ; maximum sample rate used; no auxiliary DAC; no inverse (sinus  $x$ ) /  $x$ ; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	High common-mode			Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
SFDR	spurious-free dynamic range	$f_{data} = 491.52\text{ MHz}$ ; $f_s = 983.04\text{ Msps}$ ; $B = f_s / 2$								
		$f_o = 20\text{ MHz}$ at $-1\text{ dBFS}$	I	-	84	-	-	84	-	dBc
		$f_o = 20\text{ MHz}$ at $-7\text{ dBFS}$	I	-	<td>	-	-	<td>	-	dBc
		$f_o = 20\text{ MHz}$ at $-14\text{ dBFS}$	I	-	<td>	-	-	<td>	-	dBc
		$f_o = 150\text{ MHz}$ at $-1\text{ dBFS}$ ; $V_{DDA} = 3.3\text{ V}$	I	-	83	-	-	83	-	dBc
		$f_o = 150\text{ MHz}$ at $-1\text{ dBFS}$ ; $V_{DDA} = 2.5\text{ V}$	I	-	83	-	-	81	-	dBc
		$f_o = 150\text{ MHz}$ at $-7\text{ dBFS}$ $f_o = 150\text{ MHz}$ at $-14\text{ dBFS}$	I I	- -	<td> <td>	- -	- -	<td> <td>	- -	dBc dBc
IMD3	third-order intermodulation distortion	$f_{o1} = 21\text{ MHz}$ ; $f_{o2} = 22\text{ MHz}$ ; $-7\text{ dBFS}$ ; $f_s = 983.04\text{ Msps}$ ; $\times 2$ interpolation	I	-	85	-	-	85	-	dBc
		$f_{o1} = 152.1\text{ MHz}$ ; $f_{o2} = 155.1\text{ MHz}$ ; $-7\text{ dBFS}$ ; $f_s = 983.04\text{ Msps}$ ; $\times 2$ interpolation	I	-	84	-	-	82	-	dBc
ACPR	adjacent channel power ratio	$f_s = 983.04\text{ Msps}$ ; $\times 2$ interpolation; $f_o = 40\text{ MHz}$								
		1 WCDMA carrier; $B = 5\text{ MHz}$ 4 WCDMA carriers; $B = 20\text{ MHz}$	D D	- -	82 75	- -	- -	82 75	- -	dBc dBc
NSD	noise spectral density	$f_s = 983.04\text{ Msps}$ ; $\times 2$ interpolation; $f_o = 20\text{ MHz}$ at $-1\text{ dBFS}$	D	-	-164	-	-	-162	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

## 11. Application information

### 11.1 General description

The DAC165xD is a dual 16-bit DAC operating up to 1.50 Gbps. A maximum input data rate up to 750 Msps is supported to enable more capability for wideband and multicarrier systems. The incorporated quadrature modulator and 40-bit Numerically Controlled Oscillator (NCO) simplifies the frequency selection of the system. This is also possible because of the  $\times 2$ ,  $\times 4$  or  $\times 8$  interpolation filters which remove undesired images.

The DAC165xD supports the following JESD204B key features:

- 10-bit/8-bit decoding
- Code group synchronization
- Inter-Lane Alignment (ILA)
- $1 + x^{14} + x^{15}$  scrambling polynomial
- Character replacement
- TX/RX synchronization management via SYNC synchronization signals
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device (subclass 1 compliant)
- number L of serial lanes: 1, 2, 4
- number M of data converters: 1 or 2
- number F of octets per frame: 1, 2, 4
- number S of samples per frame: 1, 2
- embedded test pattern (PRBS31, JTSPAT)

The DAC165xD can be interfaced with any logic device that features high-speed SERializer/DESerializer (SERDES) functionality. This macro is now widely available in Field-Programmable Gate Array (FPGA) of different vendors. Standalone SERDES ICs can also be used.

The DAC165xD includes polarity swapping for each of the lanes and additionally offers lane swapping to enhance the intrinsic board layout simplification of the JESD204B standard. Each physical lane can be configured logically as lane 0, lane 1, lane 2 or lane 3.

This device is MCDA-ML compliant, offering inter-lane alignment between several devices. An IDT proprietary mechanism in combination with the JESD204B subclass I clause enables maintenance of sample alignment between devices up to the final analog output stage. Output samples are automatically aligned to the SYSREF signal generated by a dedicated IC or by the FPGA itself. A system with several DAC165xDs can produce data with a guaranteed alignment of less than 1 DAC output clock period. The DAC165xD incorporates two differential SYSREF ports (located on opposite sides of the IC) to simplify the PCB layout design. The device also enables independent link reinitialization.

The DAC165xD generates two complementary current outputs on pins IOUTA\_P/IOUTA\_N and IOUTB\_P/IOUTB\_N, corresponding to channel 'A' and 'B', respectively, providing a nominal full-scale output current of 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

The DAC165xD requires configuration before operating. It features an SPI slave interface to access the internal registers. Some of these registers also provide information about the JESD204B interface status. Optionally, an interrupt capability can be programmed using those registers to ensure ease of use of the device.

Because of the JESD204B standardization, the DAC165xD does not require any adjustment from the Transmit Logic Device (TLD) to capture the input data streams. Some autolock features can be monitored using the SPI registers.

The DAC165xD supports the following LMF configuration as described in the JESD204B standard (register LMF\_CTRL; see [Table 123](#)):

**Table 10. LMF configuration**

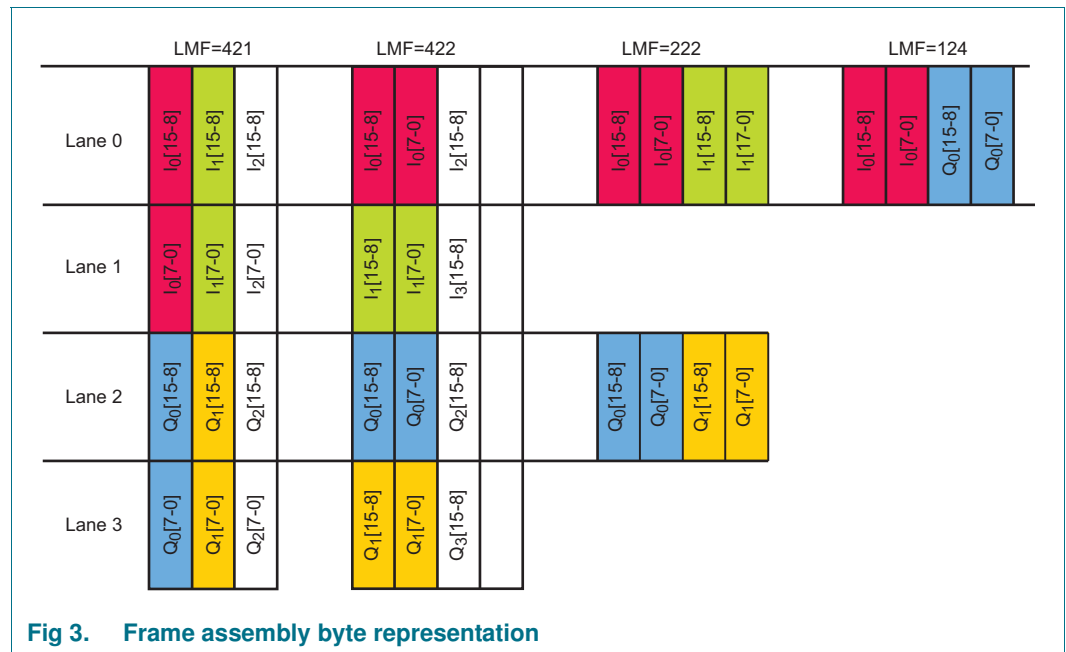
L-M-F	S <sup>[1]</sup>	HD <sup>[2]</sup>
1-2-4	1	0
2-2-2	1	0
4-2-2	2	0
4-2-1	1	1

[1] S is the number of samples per frame.

[2] HD is the high-density bit as described in the JESD204B specification.

A new IDT auto-mute feature enables switching off of the RF output signal as a result of various internal events occurring.

The DAC165xD requires supplies of both 3.3 V and 1.2 V. The 1.2 V supply has separate digital and analog power supply pins. The SPI power supply is flexible. It can be set to 1.2 V or 1.8 V (see [Section 11.2.1.1](#)).



**Fig 3. Frame assembly byte representation**

## 11.2 Device operation

The DAC165xD provides a lot of flexibility in its way of working through its SPI registers. The SPI registers are divided in blocks of registers. Each block is associated with some global functions which are described below. [Section 11.11](#) shows an overview of all register blocks, including the register descriptions.

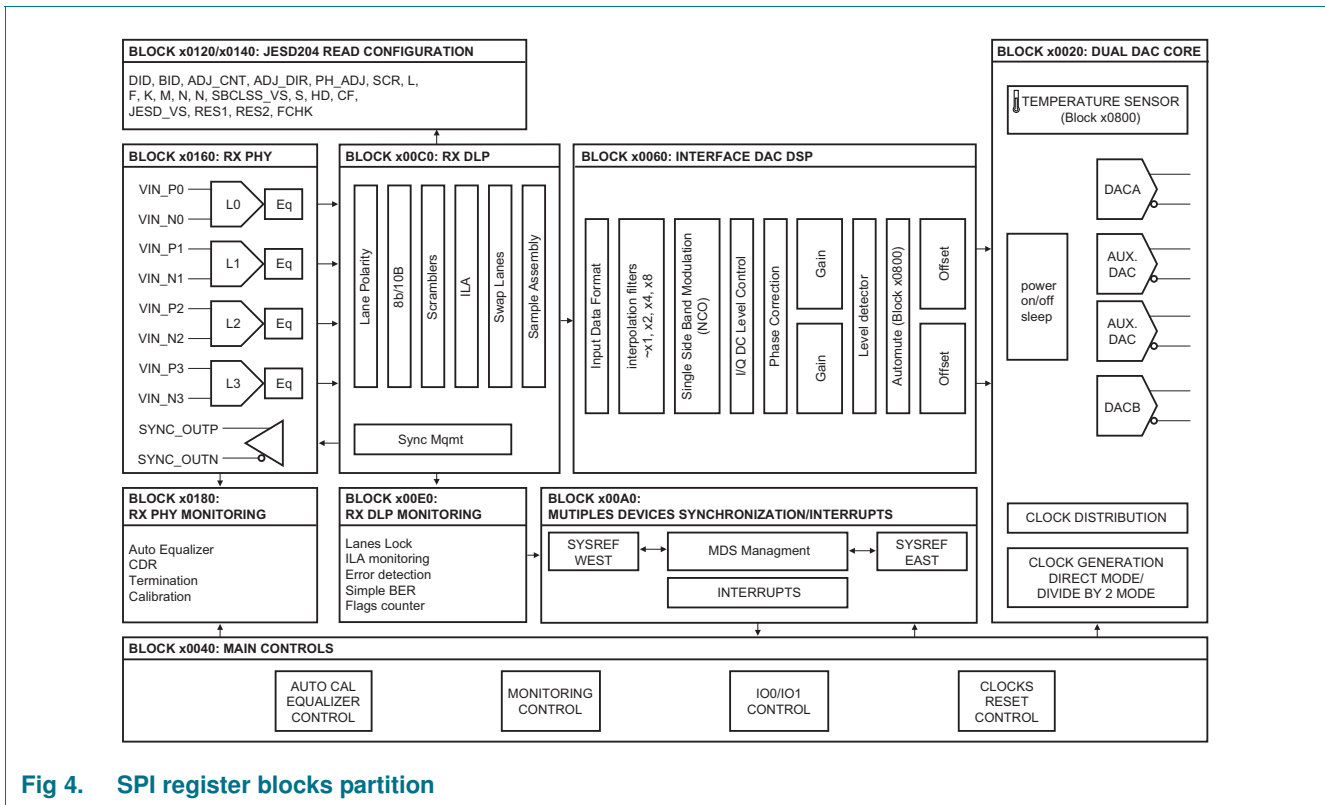


Fig 4. SPI register blocks partition

### 11.2.1 SPI configuration block

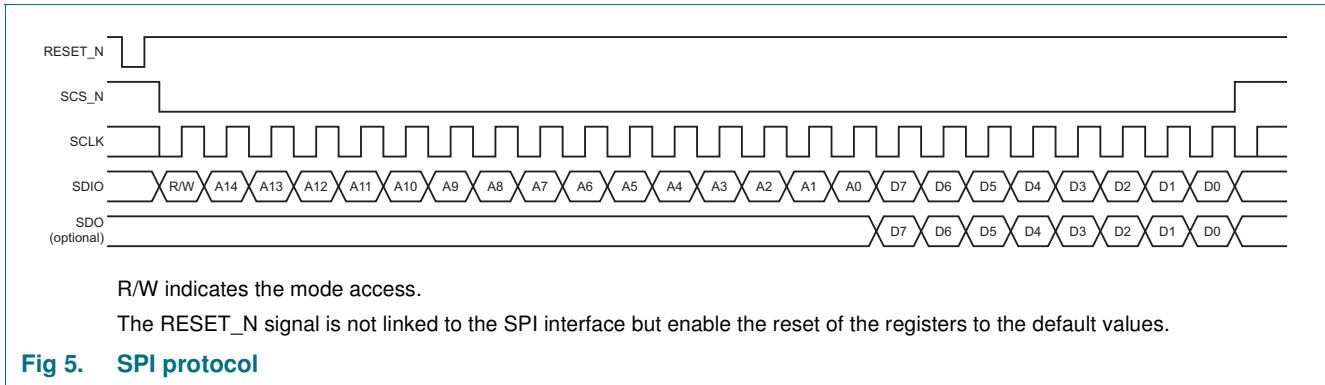
This block of registers specifies how the SPI controller and the identification of the chip work.

#### 11.2.1.1 Protocol description

The DAC16xD serial interface is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both Write mode and Read mode. The reference voltage of the interface is  $V_{DD(I/O)}$ . Depending on the power supply level of the SPI master device, it can be set to either 1.2 V or 1.8 V.

This interface can be configured as a 3-wire type (SDIO as bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pins, input and output ports, respectively). In both configurations, SCLK acts as the serial clock and SCS\_N acts as the serial chip select.

The DAC16xD SPI-interface is a slave-device. Multiple slave-devices can be attached to the same master interface as long as each device has its own serial chip select signal (SCS\_N).



**Table 11. Read mode or Write mode access description**

R/W	Description
0	Write mode operation
1	Read mode operation

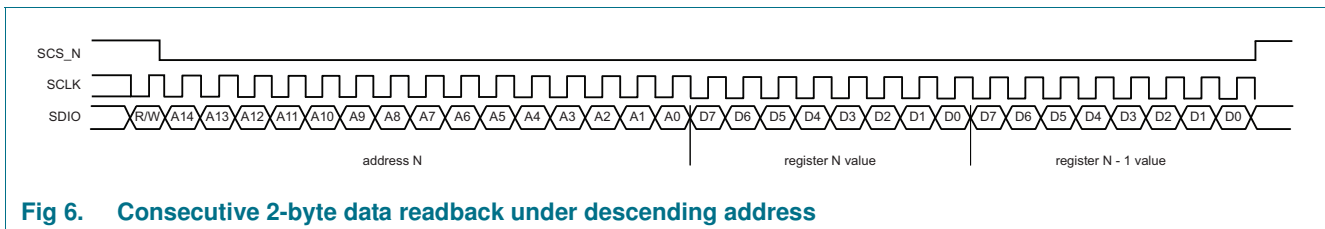
A[14:0] indicates which register is being addressed. If a multiple transfer occurs, this address points to the first register to be accessed.

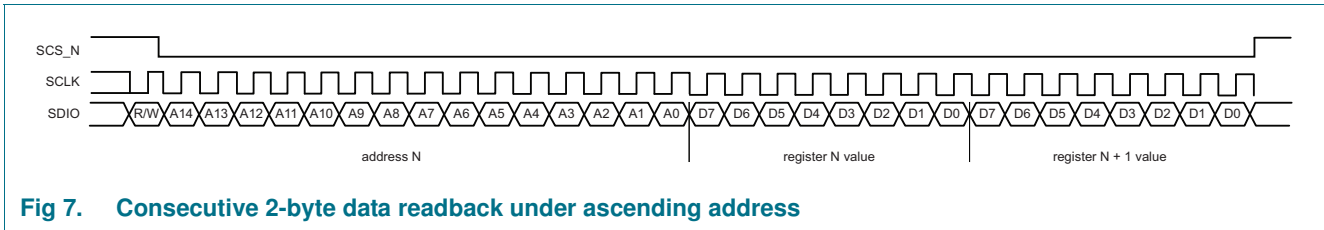
**11.2.1.2 SPI controller configuration**

The 3-wire or 4-wire mode is set by bit SPI\_4W of register SPI\_CFG\_A (see [Table 39](#)). The default mode is 3-wire mode.

A software SPI reset can be called via bit SPI\_RST of register SPI\_CFG\_A (see [Table 39](#)). This reset reinitializes all SPI registers, except register SPI\_CFG\_A and SPI\_CFG\_B, to their default settings. Reset the device to its default value at start-up time to avoid any uncontrolled states, even if the DAC165xD uses the Power-On Reset (POR) module. Only a hardware reset on pin RESET\_N can reset to their default values.

The SPI streaming mode is enabled by default. In this mode, the Read or Write process carries on as long as the SCS\_N signal is low. The streaming mode requires a first address 'n' to be set at the beginning of the SPI sequence. The following data are associated from this address in an ascending (auto-increment) or descending (auto-decrement) mode. This ascending/descending mode is specified by bit SPI\_ASC of register SPI\_CFG\_A. Figures below represent the readback of 2 bytes data in a 3 wires mode for the ascendant and descendant mode.





**Fig 7. Consecutive 2-byte data readback under ascending address**

The streaming mode can be disabled by setting bit SPI\_SINGL of register SPI\_CFG\_B (see [Table 39](#)). In this single-byte mode, only 1 byte of data can be written or read, whatever the state of the SCS\_N signal.

### 11.2.1.3 Double buffering and Transfer mode

Some register functions (like the NCO frequency value) are split over multiple registers. If this is the case, the first address consists of the LSB byte and the highest address in the MSB byte. When programming these registers sequentially, some unexpected behavior can occur at the DAC output. It is preferable to program this set of registers simultaneously. A double buffering feature is available on some registers allowing sequential programming of the first buffers and transferring the values to the final register simultaneously.

The transfer request is done by setting the TRANSFER\_BIT bit of register SPI\_CFG\_C register (see [Table 44](#)). The device clears this bit (autoclear) indicating to the SPI master device that the transfer is complete.

The SPI\_RBACK\_BUFF bit of register SPI\_CFG\_B (see [Table 39](#)) allows the reading back of the first stage of buffers (in case the register is double buffered).

The following registers are double buffered:

**Table 12. Double buffered registers**

See [Table 38](#)

Address	Register
0062h	NCO_PH_OFFSET_LSB
0063h	NCO_PH_OFFSET_MSB
0064h	NCO_FREQ_B0
0065h	NCO_FREQ_B1
0066h	NCO_FREQ_B2
0067h	NCO_FREQ_B3
0068h	NCO_FREQ_B4
0069h	PH_CORR_CTRL_0
006Ah	PH_CORR_CTRL_1
006Bh	DAC_A_DGAIN_LSB
006Ch	DAC_A_DGAIN_MSB
006Dh	DAC_B_DGAIN_LSB
006Eh	DAC_B_DGAIN_MSB
006Fh	DAC_OUT_CTRL
0070h	DAC_LVL_DET
0071h	DAC_A_OFFSET_LSB

**Table 12. Double buffered registers ...continued**

See [Table 38](#)

Address	Register
0072h	DAC_A_OFFSET_MSB
0073h	DAC_B_OFFSET_LSB
0074h	DAC_B_OFFSET_MSB
0075h	IQ_LVL_CTRL
0076h	I_DC_LVL_LSB
0077h	I_DC_LVL_MSB
0078h	Q_DC_LVL_LSB
0079h	Q_DC_LVL_MSB

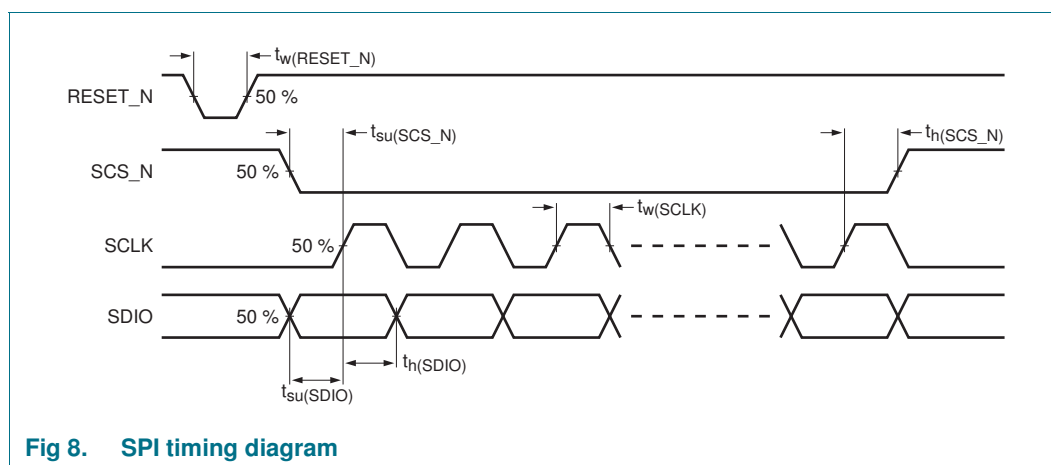
### 11.2.1.4 Device description

Registers CHIP\_TYPE, CHIP\_ID\_0, CHIP\_ID\_1 and CHIP\_VS (see [Table 38](#)) represent the ID card of the device.

Registers VEND\_ID\_LSB and VEND\_ID\_MSB (see [Table 38](#)) represent the IDT manufacturer identifier.

### 11.2.1.5 SPI timing description

The SPI interface can operate at a frequency of up to 25 MHz. [Figure 8](#) shows the SPI timing.



**Fig 8. SPI timing diagram**

The SPI timing characteristics are given in [Table 13](#).

**Table 13. SPI timing characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{\text{SCLK}}$	SCLK frequency	-	-	25	MHz
$t_w(\text{SCLK})$	SCLK pulse width	30	-	-	ns
$t_{su}(\text{SCS\_N})$	SCS_N set-up time	20	-	-	ns
$t_h(\text{SCS\_N})$	SCS_N hold time	20	-	-	ns
$t_{su}(\text{SDIO})$	SDIO set-up time	10	-	-	ns
$t_h(\text{SDIO})$	SDIO hold time	5	-	-	ns
$t_w(\text{RESET\_N})$	RESET_N pulse width	<a href="#">1</a> 30	-	-	ns

- [1] The RESET\_N signal is not linked to the SPI interface, but enables the reset of the registers to the default values.

### 11.2.2 Main device configuration

The registers of block MAIN are used for the main configuration of the DAC165xD.

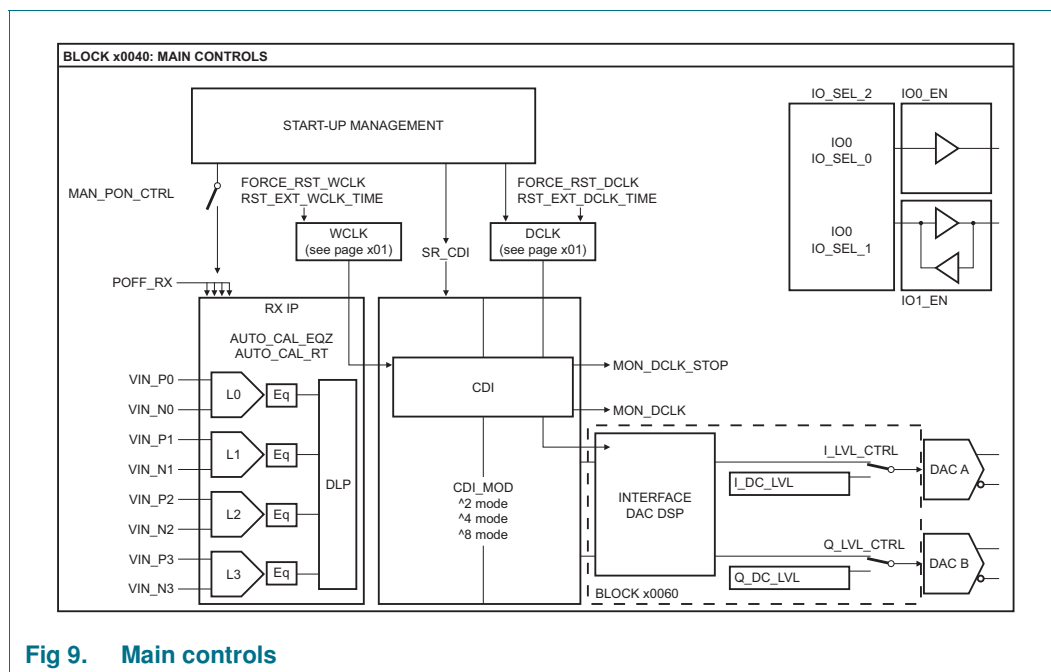


Fig 9. Main controls

At start-up, the two clocks WCLK and DCLK are forced to reset states to avoid that the DAC outputs any dummy signal through bits FORCE\_RST\_DCLK and FORCE\_RST\_WCLK of the MAIN\_CTRL register (see Table 51). The device configuration has to be done before releasing these two clocks.

Here are some guidelines to ensure correct SPI programming. As DCLK and WCLK are kept to reset the programming sequence of the registers is not important:

1. Proceed to a software reset of all SPI registers (see Section 11.2.1.2)
2. Specify the Interpolation mode (see Table 14)
3. Specify the clocks configuration (see Section 11.2.6.1):
  - a. Divider bypass or Divider by 2 mode
  - b. WCLK division ratio
4. Specify the Clock domain interface mode (Section 11.2.6.1 and Table 23)
5. Specify the JESD204B LMF configuration (see Section 11.7.5.9)
6. Specify the JESD204B logical lanes order (see Section 11.7.5.4)
7. Specify which JESD204B physical lanes have to be turned off using the POFF\_RX bits of register MAIN\_CTRL (see Table 51)
8. Release the WCLK and DCLK reset by deasserting the bits FORCE\_RST\_DCLK and FORCE\_RST\_WCLK of the MAIN\_CTRL register (see Table 51)

Other SPI configurations can be added using these basic settings.

11.2.3 Interface DAC DSP block

This module is the interface between the data processing in the high-speed serial receiver and the dual DAC core. The controls of the Digital Signal Processing (DSP) of the DAC are specified to set up the interpolation filter, and enable or disable the various gains and offsets of the data digital path. The data signals have already been processed by the Digital Lane Processing (DLP, see Section 11.11.7). They are provided to this module through the Clock Domain Interface (Section 11.2.6.1). This module is clocked by the digital clock DCLK.

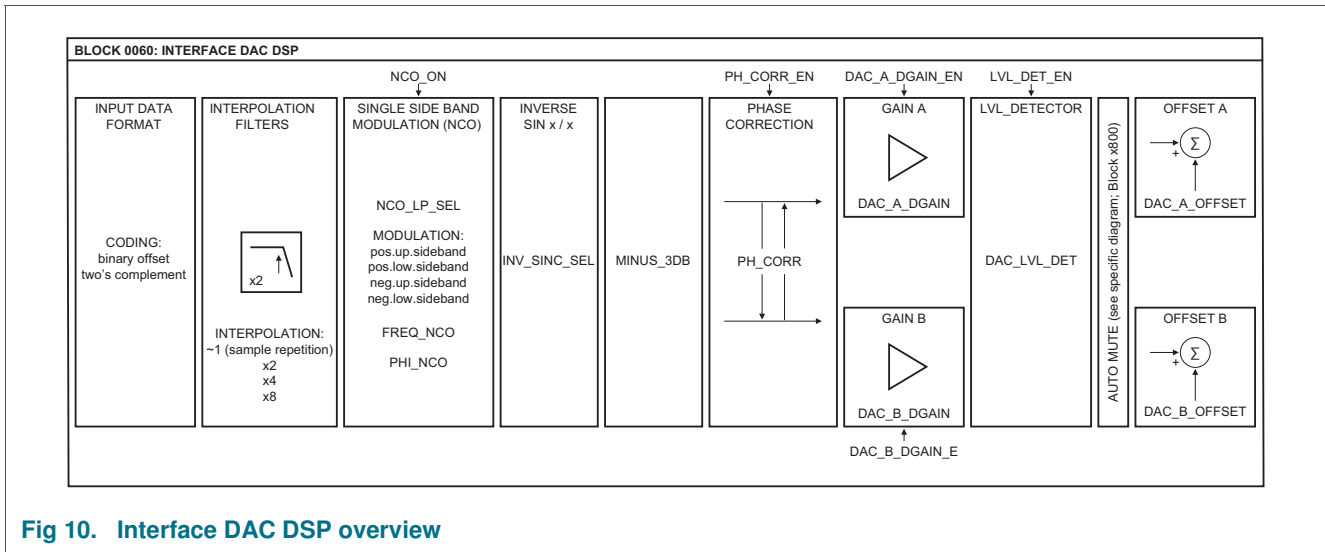


Fig 10. Interface DAC DSP overview

11.2.3.1 Input data format

After decoding in the high-speed serial receiver, the data representation can be specified as binary offset coding or as two's complement coding using register CODING\_IQ (see Table 67).

11.2.3.2 Finite Impulse Response (FIR) filters

The DAC165xD provides three interpolation filters described by their coefficients in Table 15. The three interpolation FIR filters have a stop band attenuation of at least 80 dBc and a pass band ripple of less than 0.0005 dB.

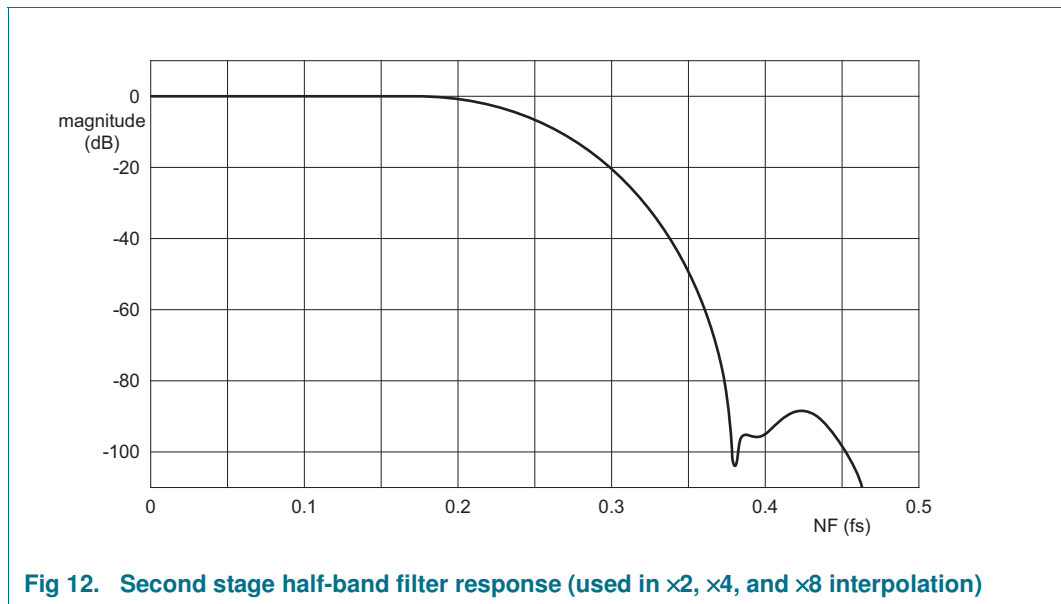
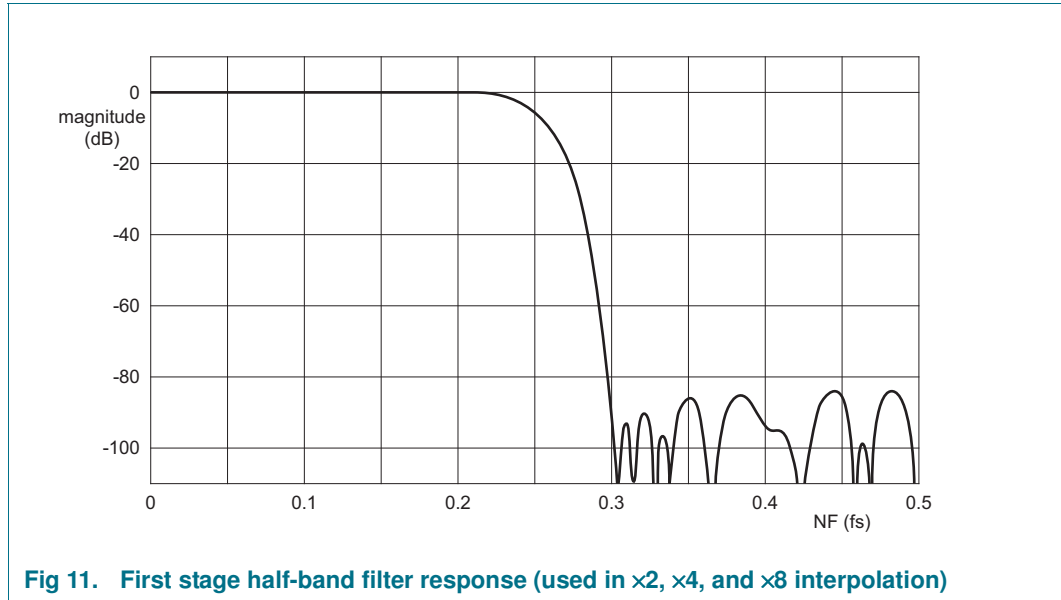
The interpolation ratio can be set through register TX\_CFG (see Table 59).

Table 14. Interpolation

Symbol	Access	Value	Description
INTERPOLATION[1:0]	R/W		interpolation
		00	no interpolation/~x1 interpolation
		01	x2 interpolation
		10	x4 interpolation
		11	x8 interpolation

The 'no interpolation' or '~x1' (quasi x1) mode is in fact a degenerated x2 interpolation mode where the samples are repeated twice.

**Remark:** The INTERPOLATION setting must be coupled with the DCLK and WCLK clock configurations and with CDI mode (see [Section 11.2.1](#)).



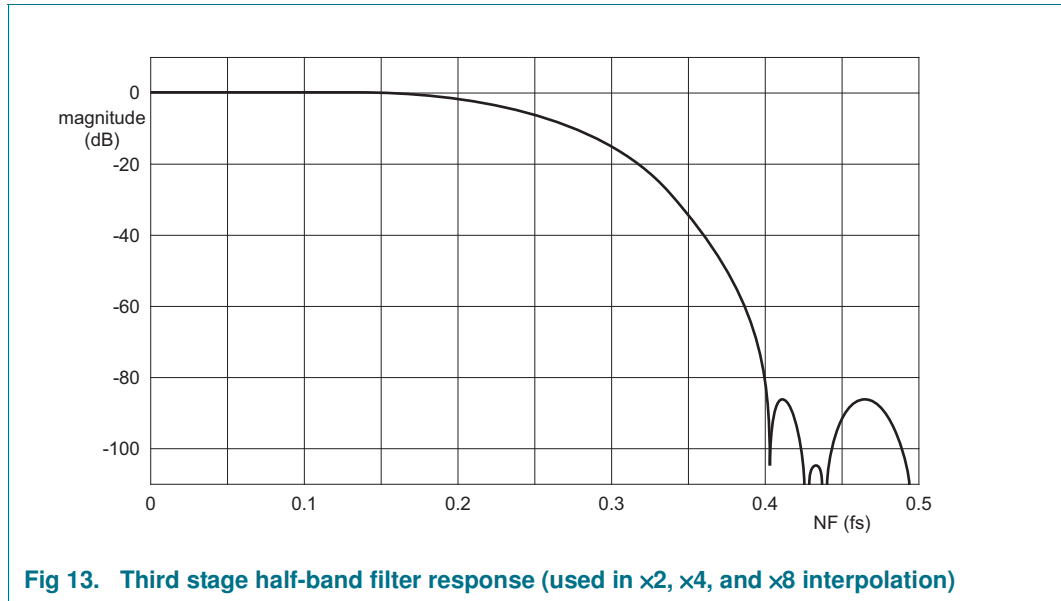


Fig 13. Third stage half-band filter response (used in x2, x4, and x8 interpolation)

Table 15: Interpolation filter coefficients

First interpolation filter			Second interpolation filter			Third interpolation filter		
Lower	Upper	Value	Lower	Upper	Value	Lower	Upper	Value
-	H(27)	+65536	H(11)	-	+32768	H(7)	-	+1024
H(26)	H(28)	+41501	H(10)	H(12)	+20272	H(6)	H(8)	+615
H(25)	H(29)	0	H(9)	H(13)	0	H(5)	H(9)	0
H(24)	H(30)	-13258	H(8)	H(14)	-5358	H(4)	H(10)	-127
H(23)	H(31)	0	H(7)	H(15)	0	H(3)	H(11)	0
H(22)	H(32)	+7302	H(6)	H(16)	+1986	H(2)	H(12)	+27
H(21)	H(33)	0	H(5)	H(17)	0	H(1)	H(13)	0
H(20)	H(34)	-4580	H(4)	H(18)	-654	H(0)	H(14)	-3
H(19)	H(35)	0	H(3)	H(19)	0	-	-	-
H(18)	H(36)	+2987	H(2)	H(20)	+159	-	-	-
H(17)	H(37)	0	H(1)	H(21)	0	-	-	-
H(16)	H(38)	-1951	H(0)	H(22)	-21	-	-	-
H(15)	H(39)	0	-	-	-	-	-	-
H(14)	H(40)	+1250	-	-	-	-	-	-
H(13)	H(41)	0	-	-	-	-	-	-
H(12)	H(42)	-773	-	-	-	-	-	-
H(11)	H(43)	0	-	-	-	-	-	-
H(10)	H(44)	+456	-	-	-	-	-	-
H(9)	H(45)	0	-	-	-	-	-	-
H(8)	H(46)	-252	-	-	-	-	-	-
H(7)	H(47)	0	-	-	-	-	-	-
H(6)	H(48)	+128	-	-	-	-	-	-
H(5)	H(49)	0	-	-	-	-	-	-
H(4)	H(50)	-58	-	-	-	-	-	-

**Table 15: Interpolation filter coefficients ...continued**

First interpolation filter			Second interpolation filter			Third interpolation filter		
Lower	Upper	Value	Lower	Upper	Value	Lower	Upper	Value
H(3)	H(51)	0	-	-	-	-	-	-
H(2)	H(52)	+22	-	-	-	-	-	-
H(1)	H(53)	0	-	-	-	-	-	-
H(0)	H(54)	-6	-	-	-	-	-	-

The dependency of the FIR1 output Y(m) on its inputs X(m) is defined by [Equation 1](#):

$$Y(m) = \frac{1}{H(27)} \times \sum_{n=0}^{n=54} [H(n):X(m-n)] \tag{1}$$

The dependency of the FIR2 output Y(m) on its inputs X(m) is defined by [Equation 2](#):

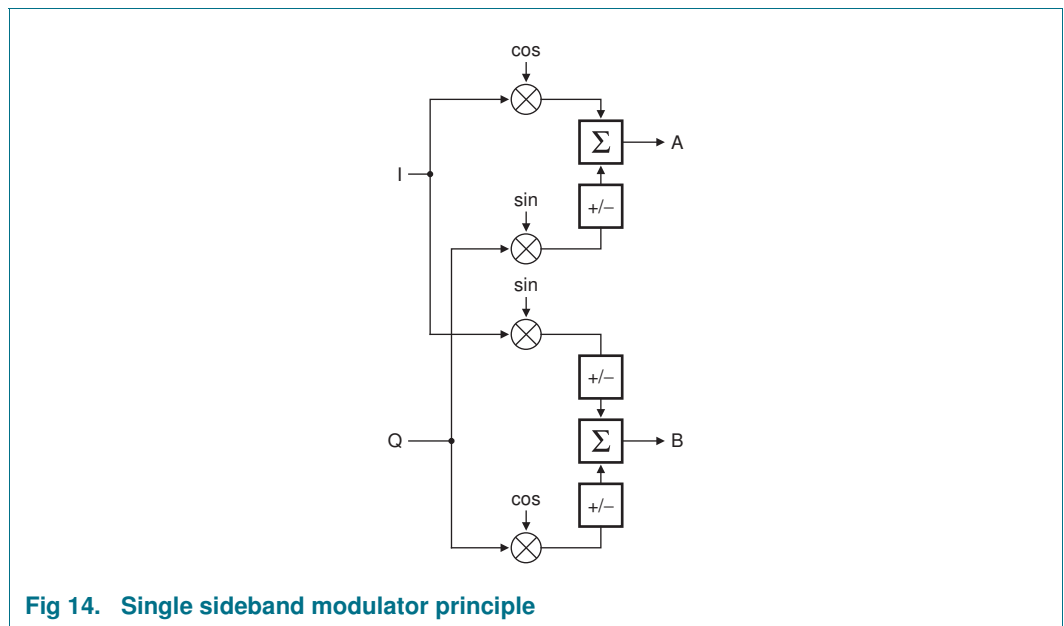
$$Y(m) = \frac{1}{H(11)} \times \sum_{n=0}^{n=22} [H(n):X(m-n)] \tag{2}$$

The dependency of the FIR3 output Y(m) on its inputs X(m) is defined by [Equation 3](#):

$$Y(m) = \frac{1}{H(7)} \times \sum_{n=0}^{n=14} [H(n):X(m-n)] \tag{3}$$

**11.2.3.3 Single SideBand Modulator (SSBM)**

The single sideband modulator is a quadrature modulator that enables the mixing of the I data and Q data with the sine and cosine signals generated by the NCO to generate path A and B as described in [Figure 14](#).



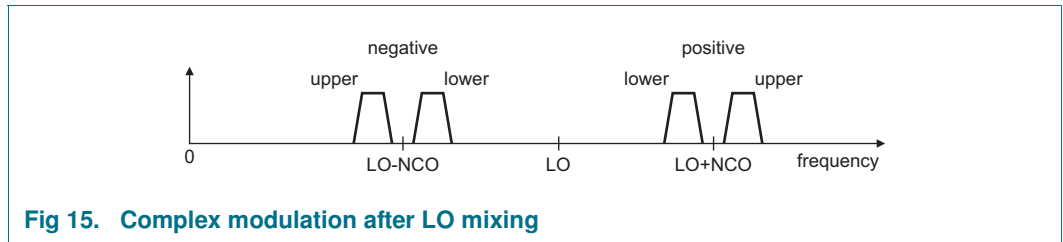
**Fig 14. Single sideband modulator principle**

[Table 16](#) shows the various possibilities set by register MODULATION (see [Table 59](#)).

**Table 16. Complex modulator operation mode**

MODULATION[2:0]	Mode	Path A	Path B
000	bypass	$I(t)$	$Q(t)$
001	positive upper sideband	$I(t) \times \cos(\omega_{NCO} \times t) - Q(t) \times \sin(\omega_{NCO} \times t)$	$I(t) \times \sin(\omega_{NCO} \times t) + Q(t) \times \cos(\omega_{NCO} \times t)$
010	positive lower sideband	$I(t) \times \cos(\omega_{NCO} \times t) + Q(t) \times \sin(\omega_{NCO} \times t)$	$I(t) \times \sin(\omega_{NCO} \times t) - Q(t) \times \cos(\omega_{NCO} \times t)$
011	negative upper sideband	$I(t) \times \cos(\omega_{NCO} \times t) - Q(t) \times \sin(\omega_{NCO} \times t)$	$-I(t) \times \sin(\omega_{NCO} \times t) - Q(t) \times \cos(\omega_{NCO} \times t)$
100	negative lower sideband	$I(t) \times \cos(\omega_{NCO} \times t) + Q(t) \times \sin(\omega_{NCO} \times t)$	$-I(t) \times \sin(\omega_{NCO} \times t) + Q(t) \times \cos(\omega_{NCO} \times t)$
others	not defined	-	-

The effect of the MODULATION parameter is better viewed after mixing the A and B signal with a LO frequency through an IQ modulator.



**Fig 15. Complex modulation after LO mixing**

**11.2.3.4 40-bit NCO**

The SSBM used the complex signals coming from the NCO (Numeric Complex Oscillator) to mix the I and Q signals. The 5 registers NCO\_FREQ\_B0 to NCO\_FREQ\_B4 over 40 bits (see [Table 61](#)) can set the frequency.

The frequency is calculated with [Equation 4](#):

$$f_{NCO} = \frac{M \times f_s}{2^{40}} \tag{4}$$

Where:

- M is the value set in the bits NCO\_FREQ[39:0] of the NCO frequency registers (see [Table 61](#)).
- $f_s$  is the final DAC output clock sampling frequency

The registers NCO\_PH\_OFFSET\_LSB and NCO\_PH\_OFFSET\_MSB over 16 bits from 0° to 360° (see [Table 60](#)) can set the phase of the NCO.

The default settings represent an NCO frequency of 96 MHz when using a DAC clock of 640 Msps. For other DAC clock frequencies, use [Equation 4](#) to define the associated NCO frequency.

### 11.2.3.5 NCO low power

When using NCO low power (bit NCO\_LP\_SEL; see [Table 59](#)), the five most significant bits of register NCO\_FREQ\_B4 (bits NCO\_FREQ[39:32]; bits [31:0] are masked by zero; see [Table 61](#)) can set the frequency.

The frequency is calculated with [Equation 5](#):

$$f_{NCO} = \frac{M \times f_s}{2^{40}} \quad (5)$$

Where:

- M is the value set in the bits NCO\_FREQ[39:0] of the NCO frequency registers (see [Table 61](#)).
- $f_s$  is the DAC clock sampling frequency

### 11.2.3.6 Inverse sinc / x

A selectable FIR filter is incorporated to compensate the sinc / x effect caused by the roll-off effect of the DAC. The coefficients are represented in [Table 17](#). This feature is controlled by register INV\_SINC\_SEL (see [Table 59](#)).

**Table 17. Inversion filter coefficients**

Inversion filter		
Lower	Upper	Value
H(1)	H(9)	+1
H(2)	H(8)	-4
H(3)	H(7)	+13
H(4)	H(6)	-51
H(5)	-	+610

**Remark:** The transfer function of this features adds some gain to the signals and some saturation can occur with a level of distortion in the output spectrum as result. Update the digital gain accordingly to avoid this saturation.

### 11.2.3.7 Minus 3dB

During normal operation, a full-scale pattern is also full-scale at the DAC output. When the I data and the Q data approach full-scale simultaneously, saturation can occur. The Minus 3dB function (bit MINUS\_3DB of register DAC\_OUT\_CTRL; see [Table 64](#)) can be used to reduce the 3 dB gain in the modulator. It retains a full-scale range at the DAC output without added interferers.

### 11.2.3.8 Phase correction

The IQ modulator which follows the DACs can have a phase imbalance resulting in undesired sidebands. By adjusting the phase between the I and Q channels, the unwanted sideband can be reduced.

Without compensation the I and Q channels have a phase difference of  $\pi / 2$  (90°). The registers PH\_CORR\_CTRL\_0 and PH\_CORR\_CTRL\_1 (see [Table 62](#)) ensure a phase variation from 75.7° to 104.3° by steps 0.0035°. The two registers define a signed value

that ranges from -4096 to +4095. The equation:  $PH\_CORR[12:0] / 16384$  gives the resulting phase compensation (in radians). The phase correction can be enabled by register  $PH\_CORR\_EN$  (see [Table 62](#)).

**11.2.3.9 Digital gain**

The full-scale output current for each DAC is the sum of the two complementary current outputs:

- $I_{OA(fs)} = I_{IOUTA\_P} + I_{IOUTA\_N}$
- $I_{OB(fs)} = I_{IOUTB\_P} + I_{IOUTB\_N}$

The IQ-modulator can have an amplitude imbalance which results in undesired sidebands. The unwanted sideband can be reduced by adjusting the amplitude of signals A and B. The two gains are purely digital and could be enabled by registers  $DAC\_A\_GAIN\_EN$  and  $DAC\_B\_GAIN\_EN$  (see [Table 64](#)).

The output current of DAC A depends on the digital input data and the gain factor defined by bits  $DAC\_A\_DGAIN[11:0]$  of register  $DAC\_A\_DGAIN\_MSB$  and register  $DAC\_A\_DGAIN\_LSB$  (see [Table 63](#)).

$$I_{IOUTA\_P} = I_{OA(fs)} \times \frac{(DAC\_A\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right) \tag{6}$$

$$I_{IOUTA\_N} = I_{OA(fs)} \times \left(1 - \frac{(DAC\_A\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right)\right) \tag{7}$$

The output current of DAC B depends on the digital input data and the gain factor defined by bits  $DAC\_B\_DGAIN[11:0]$  of register  $DAC\_B\_DGAIN\_MSB$  and  $DAC\_B\_DGAIN\_LSB$  (see [Table 63](#)).

$$I_{IOUTB\_P} = I_{OB(fs)} \times \frac{(DAC\_B\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right) \tag{8}$$

$$I_{IOUTB\_N} = I_{OB(fs)} \times \left(1 - \frac{(DAC\_B\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right)\right) \tag{9}$$

[Table 18](#) shows the output current as a function of the input data, when  $I_{OA(fs)} = I_{OB(fs)} = 20\text{ mA}$ .

**Table 18. DAC transfer function**

Data	I15 to I0/Q15 to Q0 (binary coding)	I15 to I0/Q15 to Q0 (two's complement coding)	IOUTA_P/ IOUTB_P	IOUTA_N/ IOUTB_N
0	0000 0000 0000 0000	1000 0000 0000 0000	0 mA	20 mA
...	...	...	...	...
32768	1000 0000 0000 0000	0000 0000 0000 0000	10 mA	10 mA
...	...	...	...	...
65535	1111 1111 1111 1111	0111 1111 1111 1111	20 mA	0 mA

11.2.3.10 Auto-mute

The DAC165xD provides a new auto-mute feature allowing muting the DAC analog output if a conditional event occurs. The auto-mute feature is based on a state machine as described in figure1 and on the control of the digital gains.

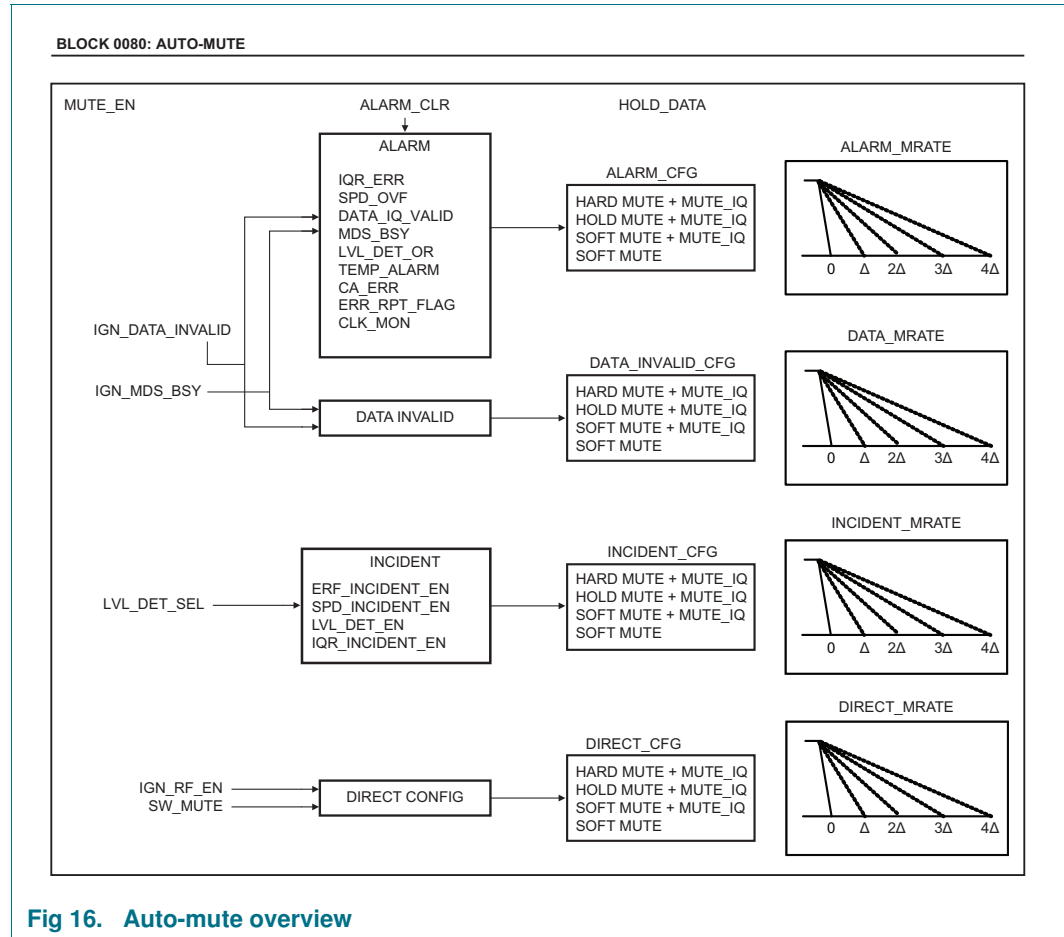


Fig 16. Auto-mute overview

In normal operating mode, the state machine is in IDLE state. The digital gains are specified by the user.

Various mute events can be detected in the DAC. These trigger the MUTE state. Once the MUTE state is entered, the DAC automatically sets the digital gains to zero using several mute actions. The mute actions SOFT mute and HOLD mute drop to zero gradually. The mute action HARD mute drop to zero instantly (see Figure 18).

When the digital gains have been set to zero, the state machine enters the WAIT state. In this state, the gains are kept at zero. The state machine stays in this mode until the end of the wait period and the mute event is not deasserted.

When the mute event is cleared and the wait period elapsed, the state machine enters the DEMUTE state. In this state, the digital gains are set again to the initial values. This is done relatively to the mute rate setting. If during this state, a new mute event is triggered, the state machine enters the MUTE state again. The gain decreases from the current gains values, not from the initial ones.

When the digital gains reach the initial values, the state machine enters the IDLE state again.

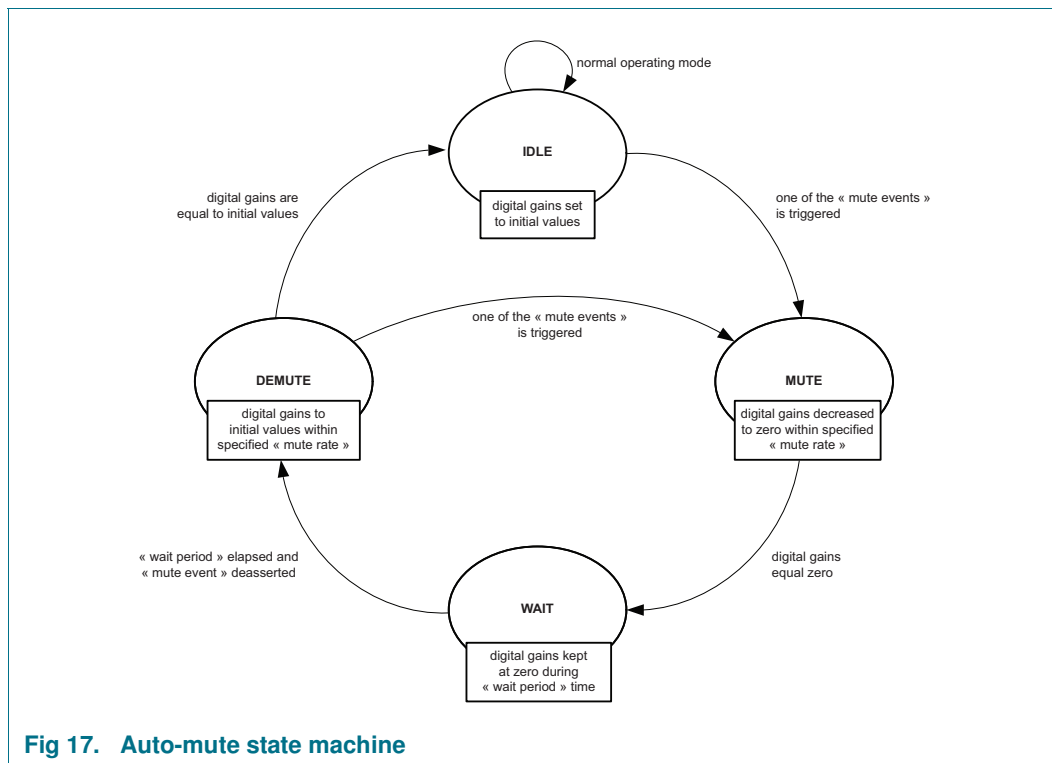


Fig 17. Auto-mute state machine

The mute feature is set by enabling bit MUTE\_EN in register MUTE\_CTRL\_0 (see [Table 72](#)).

### Mute events

The MUTE action is triggered by one of the following mute events. Each of them is linked to either an error detection, a status change or signal power monitoring:

- **SPI\_SW\_MUTE:**  
Software event that can be requested by the host interface through the SPI bus.
- **RF\_EN:**  
Hardware event that can be requested by the host interface through pin RFTX\_ENABLE/IO0
- **CLK\_MON:**  
Event linked to the monitoring of the clocks in the receiver physical layer control block.
- **MON\_DCLK\_ERR:**  
Event triggered when a clock error occurs in the CDI (see [Section 11.2.6.1](#)).
- **CA\_ERR:**  
Event triggered when a clock error occurs in the DLP (see [Section 11.7.3](#)).
- **TEMP\_ALARM:**  
Event triggered when the temperature sensor measures a temperature that exceeds the threshold value. TEMP\_SEL\_MAN must be specified first (see [Table 81](#)).

- **ERR\_RPT\_FLAG:**  
Event triggered when DATA\_INVALID is detected by the DLP (see [Section 11.7.3](#)).
- **LVL\_DET\_OR:**  
Event triggered when the signal levels exceed the LVL\_DET (see [Table 64](#)) on channel X or Y. LVL\_DET\_EN and LVL\_DET must be set first (see [Table 64](#) and [Table 65](#)).
- **MDS\_BSY:**  
Event triggered while the MDS process is busy aligning the DAC (see [Section 11.6](#)).
- **DATA\_IQ\_VALID:**  
Event is triggered when DATA\_INVALID is detected by the DLP (see [Section 11.7.3](#)).
- **SPD\_OVF:**  
Event triggered when the Signal Power Detector (SPD) average value is exceeding the threshold value ([Section 11.2.4.2](#)).
- **IQR\_ERR:**  
Event triggered when the IQ signal is out of range (see [Section 11.2.4.3](#)).

The monitoring of these events can also be done using the interrupt process available in the DAC165xD (see [Section 11.7](#)). Once the interrupt is detected, the host controller (e.g. an FPGA) can read back the events flags in registers INTR\_FLAGS\_0 and INTR\_FLAGS\_1 (see [Table 79](#)) and determine the actions to be taken.

#### Ignore events option

Set bits IGN\_RT\_EN, IGN\_MDS\_BSY, and IGN\_DATA\_V\_IQ of the mute control register (see [Table 72](#)) for the mute controller to ignore certain events.

#### Mute event categories

The MUTE state is entered when one of the mute events is asserted. The mute events are Four categories of mute events can be distinguished: ALARM, DATA, INCIDENT, and DIRECT (see [Table 19](#)).

Table 19. Mute event categories

Mute event	ALARM <sup>[1]</sup>		DATA		INCIDENT		DIRECT	
	Enable	Disable	Enable	Disable	Enable	Disable	Enable	Disable
SPI_SW_MUTE							default <sup>[2]</sup>	
RF_EN							default	IGN_RF_EN
CLK_MON	ALARM_EN [0] <sup>[3]</sup>							
MON_DCLK_ERR	ALARM_EN [1] <sup>[3]</sup>							
CA_ERR	ALARM_EN [2] <sup>[3]</sup>							
TEMP_ALARM	ALARM_EN [3] <sup>[3]</sup>							
ERR_RPT_FLAG	ALARM_EN [4] <sup>[3]</sup>		default		ERF_INCIDENT_EN			
LVL_DET_OR	ALARM_EN [5] <sup>[3]</sup>							
MDS_BSY	ALARM_EN [6] <sup>[3]</sup>	IGN_MDS_BSY	default	IGN_MDS_BSY				
DATA_IQ_VALID	ALARM_EN [7] <sup>[3]</sup>	IGN_DATA_V_IQ	default	IGN_DATA_V_IQ				
SPD_OVF	ALARM_EN [8] <sup>[3]</sup>				SPD_INCIDENT_EN			
IQR_ERR	ALARM_EN [9] <sup>[3]</sup>				IQR_INCIDENT_EN			

[1] All ALARM mute events can be disabled using bit IGN\_ALARM. However, their detection can still be monitored using the INTERRUPT module.

[2] This bit is not auto-clear.

[3] The ALARM mute events must be cleared with bit ALARM\_CLR to move from the WAIT state to the DEMUTE state.

### Priority between categories

The priority in which the auto-mute module evaluates its inputs is:

- Priority 1: DIRECT
- Priority 2: ALARM
- Priority 3: DATA
- Priority 4: INCIDENT

### Mute actions

Four mute actions can be selected for each of the four previous mute event categories.

The digital data can also be reset to its default value (bits I\_DC\_LVL and Q\_DC\_LVL; see [Table 67](#)) to avoid disturbances in the FIR filters.

Register MUTE\_CTRL\_1 (see [Table 72](#)):

- Hard\_mute + mute IQ:  
The digital gains of the DACs are set to zero (within 1 DAC clock period). The digital path is filled with the default I and Q levels.
- Hold\_mute + mute IQ:  
The outputs of the DACs are kept to the current value (within 1 DAC clock period). The digital path is filled with the default I and Q levels.  
**Remark:** Bit HOLD\_DATA (see [Table 72](#)) must be enabled for this action. If this bit is not set, the overall Hold\_mute + mute IQ actions are not taken into account.
- Soft\_mute + mute IQ:  
The digital gains of the DACs are swept down to zero at the MUTE\_RATE value (see [Table 72](#)). The digital path is filled with the default I and Q levels.
- Soft\_mute:  
The outputs of the DACs are swept down to zero at the MUTE\_RATE value (see [Table 72](#)). The digital path is kept with the received values.  
**Remark:** As the DC offsets are applied after the digital gain, the outputs are still impacted by their values, even if a mute action event occurs.

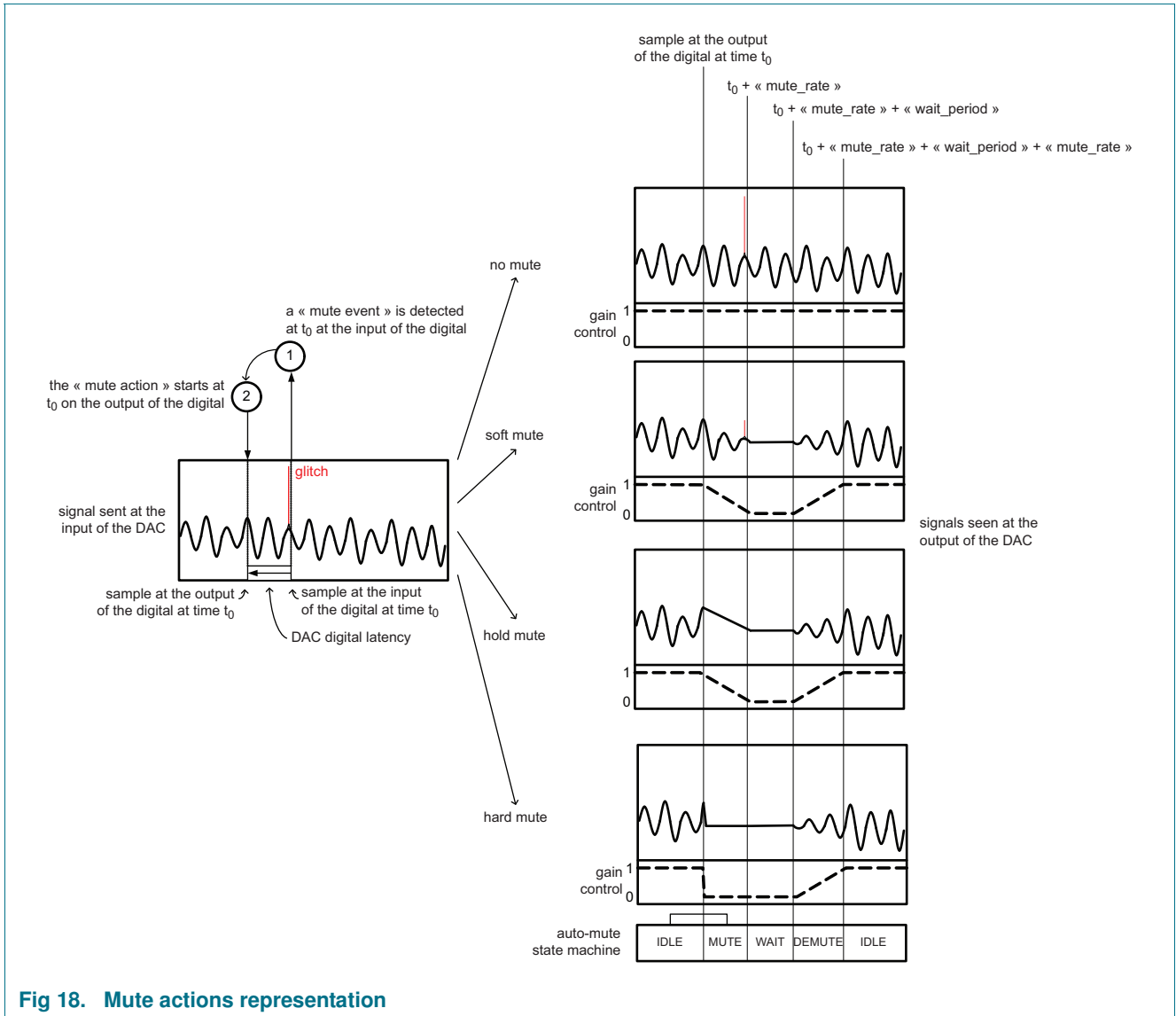


Fig 18. Mute actions representation

**Mute rate**

The time period used to decrease or increase the gains during a MUTE or DEMUTE state is called mute rate. Each mute action category has its own mute rate available through the registers ALARM\_MRATE, DATA\_MRATE, INCIDENT\_MRATE and DIRECT\_MRATE.

**Table 20. Mute rate availability**

Through ALARM\_MRATE, DATA\_MRATE, INCIDENT\_MRATE, and DIRECT\_MRATE.

DAC clock	750 MHz	1 GHz	1.5 GHz
Period x8 (ns)	10.67	8.00	5.33
Value	Mute rate (ns)	Mute rate (ns)	Mute rate (ns)
0000	10.67	8.00	5.33
0001	21.34	16.00	10.66
0010	42.68	32.00	21.32
0011	85.36	64.00	42.64

**Table 20. Mute rate availability ...continued**  
Through ALARM\_MRATE, DATA\_MRATE, INCIDENT\_MRATE, and DIRECT\_MRATE.

DAC clock	750 MHz	1 GHz	1.5 GHz
Period x8 (ns)	10.67	8.00	5.33
Value	Mute rate (ns)	Mute rate (ns)	Mute rate (ns)
0100	170.72	128.00	85.28
0101	341.44	256.00	170.56
0110	682.88	512.00	341.12
0111	1,365.76	1,024.00	682.24
1000	2,731.52	2,048.00	1,364.48
1001	3,642.47	2,731.00	1,819.53
1010	5,463.04	4 096.00	2,728.96
1011	7,283.61	5,461.00	3,638.39
1100	10,926.08	8,192.00	5,457.92
1101	14,557.88	10,915.00	7,272.12
1110	21,852.16	16,384.00	10,915.84
1111	43,704.32	32,768.00	21,831.68

#### Mute wait period

The wait period time can be calculated with [Equation 10](#):

$$\text{wait period} = (\text{MUTE\_WAIT\_PERIOD} + 1) \times 8 \times \text{DAC\_CLK\_PERIOD} \quad (10)$$

At 1 Gbps, this gives a wait period between 8 ns and 527  $\mu$ s.

#### DEMUTE triggering

When the mute action is either a DIRECT, an INCIDENT or a DATA mute action, the WAIT state is enabled as long as the wait period is not elapsed and the event is not released.

When the mute action is an ALARM mute action, the WAIT state is enabled as long as the alarm controller is not reset using bit ALARM\_CLR (see [Table 72](#)).

#### 11.2.3.11 Digital offset adjustment

When the DAC165xD analog output is DC connected to the next stage, the digital offset correction (bits DAC\_A\_OFFSET[15:0] and DAC\_B\_OFFSET[15:0]; see [Table 66](#)) can be used to adjust the common-mode level at the output of each DAC. [Table 21](#) shows the variation range of the digital offset.

**Table 21. Digital offset adjustment**

DAC_A_OFFSET[15:0] DAC_B_OFFSET[15:0] (two's complement)	Offset applied
1000 0000 0000 0000	-32768
1000 0000 0000 0001	-32767
...	...
1111 1111 1111 1111	-1

**Table 21. Digital offset adjustment ...continued**

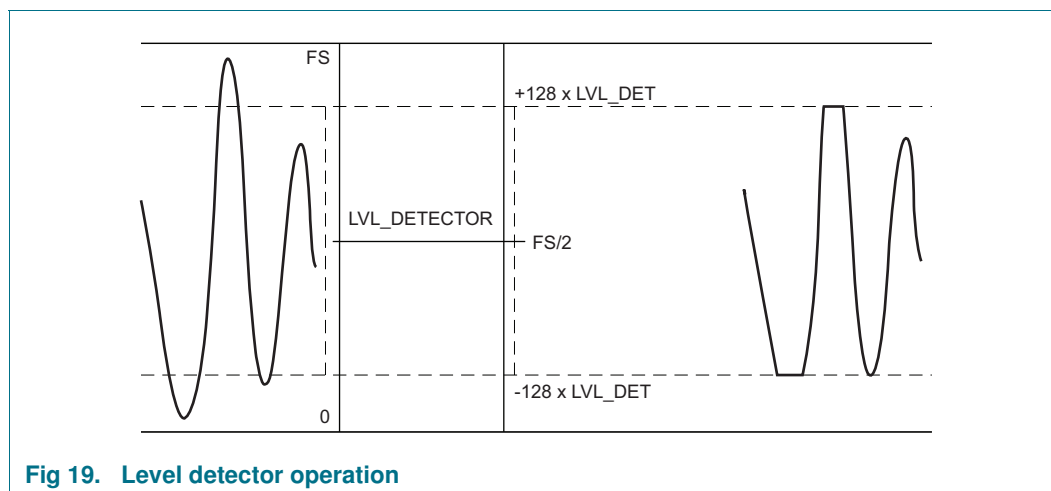
DAC_A_OFFSET[15:0] DAC_B_OFFSET[15:0] (two's complement)	Offset applied
0000 0000 0000 0000	0
0000 0000 0000 0001	+1
...	...
0111 1111 1111 1110	+32766
0111 1111 1111 1111	+32767

## 11.2.4 Signal detectors

### 11.2.4.1 Level detector

A level detector feature is available at the end of the digital path. It can be enabled using bit LVL\_DET\_EN (see [Table 64](#)). This feature specifies a signal output range limited (or clipped) to  $-128 \times \text{LVL\_DET}$  to  $+128 \times \text{LVL\_DET}$  around the half Full-Scale (FS) (see [Table 65](#)). If the signal value enters the upper or lower clipping area, it is clipped to  $+128 \times \text{LVL\_DET}$  or  $-128 \times \text{LVL\_DET}$ , respectively). [Figure 19](#) shows this behavior.

Use this feature in combination with the auto-mute feature to avoid unexpected spectral spurs after the clipping of the signal (see [Section 11.2.3.10](#)).



**Fig 19. Level detector operation**

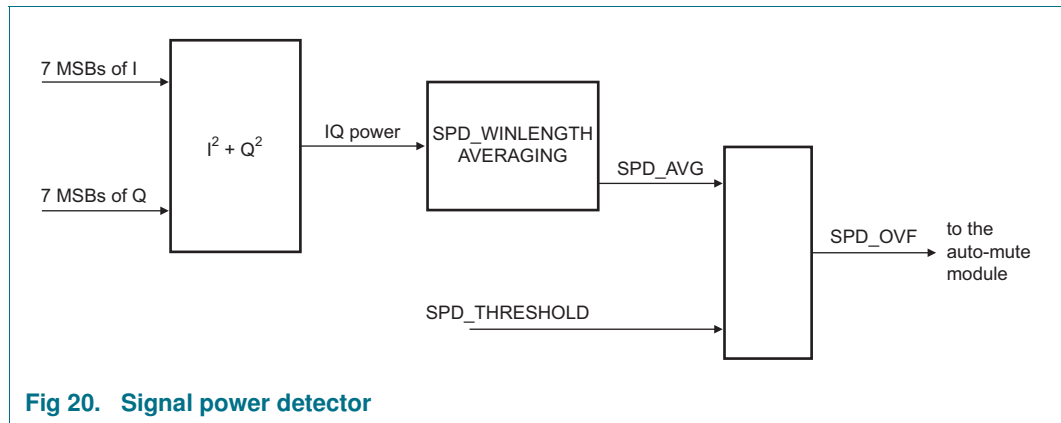
**Table 22. Level detector values**

LVL_DET[7:0]	Peak excursion from full-scale / 2	Code output range (binary offset)	dBFS value $10\log(\text{peak excursion} \times 2 / 65536)$
00h	0	32768	NaN
...	...	...	...
19h	3200	32568 to 35968	-10.1 dBFS
...	...	...	...
80h	16384	16384 to 49152	-3 dBFS
...	...	...	...

**Table 22. Level detector values ...continued**

LVL_DET[7:0]	Peak excursion from full-scale / 2	Code output range (binary offset)	dBFS value $10\log(\text{peak excursion} \times 2 / 65536)$
CBh	25984	6784 to 58752	-1 dBFS
...	...	...	...
FFh	32768	0 to 65536	0 dBFS

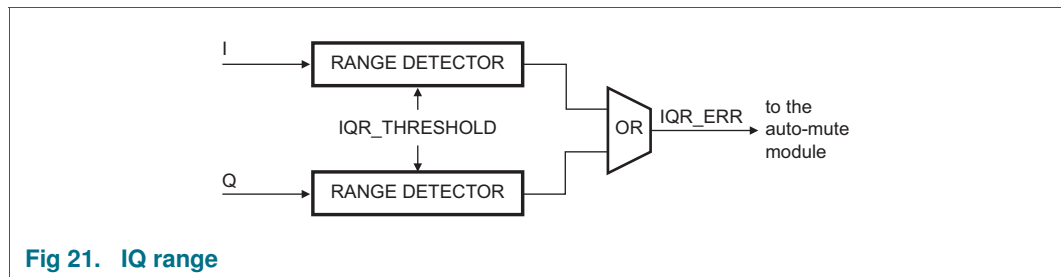
### 11.2.4.2 Signal Power Detector (SPD)



The Signal Power Detector (SPD) takes the 7 MSBs of the I and Q signal to determine the IQ power of an IQ-pair. Averaging is done over the programmable number ( $2^6, 2^7$  to  $2^{21}$ ) of IQ-pairs using the SPD\_WINLENGTH register (see Table 69). If the SPD\_AVG bit (see Table 69) exceeds the 16-bits threshold value, the SPD overflow (SPD\_OVF) flag becomes active and can invoke a mute action depending on the mute control settings.

The SPD can have a large response time because of the samples average based algorithm. This must be taken into account at system level.

### 11.2.4.3 IQ Range (IQR)



The IQ range detector checks if the I and Q signal values are within the range specified by register IQR\_THRESHOLD compared to the center value (= 0 if the data are in 2 complement's representation or 32768 if the data are in binary offset representation):

$$-IQR\_THRESHOLD < I - \text{center value} < +IQR\_THRESHOLD$$

$$-IQR\_THRESHOLD < Q - \text{center value} < +IQR\_THRESHOLD$$

## 11.2.5 Pin RF\_ENABLE

Pin 9 is a multipurpose pin that can be configured as a RF\_ENABLE pin. In this configuration, the pin is set as an input. On rising edge it can trigger the DIRECT\_CFG mute events container (see [Section 11.2.3.10](#)).

The following registers must be set to configure pin 9 in RF\_ENABLE mode (these are the default values at start-up time):

- IO\_EN[1] must be set to '0' to set the pin to input mode
- IGN\_RF\_EN (see [Table 72](#)) must be disabled to allow the triggering of the event
- MUTE\_SIGNAL (see [Table 72](#)) must be disabled

## 11.2.6 Analog core of the dual DAC

This section refers to the analog configuration required to set up the dual DAC core. The clock and output stages are described as well as the internal registers (Block x0020; see [Figure 22](#) and [Table 45](#)) used to configure the clock tree inside the chip.

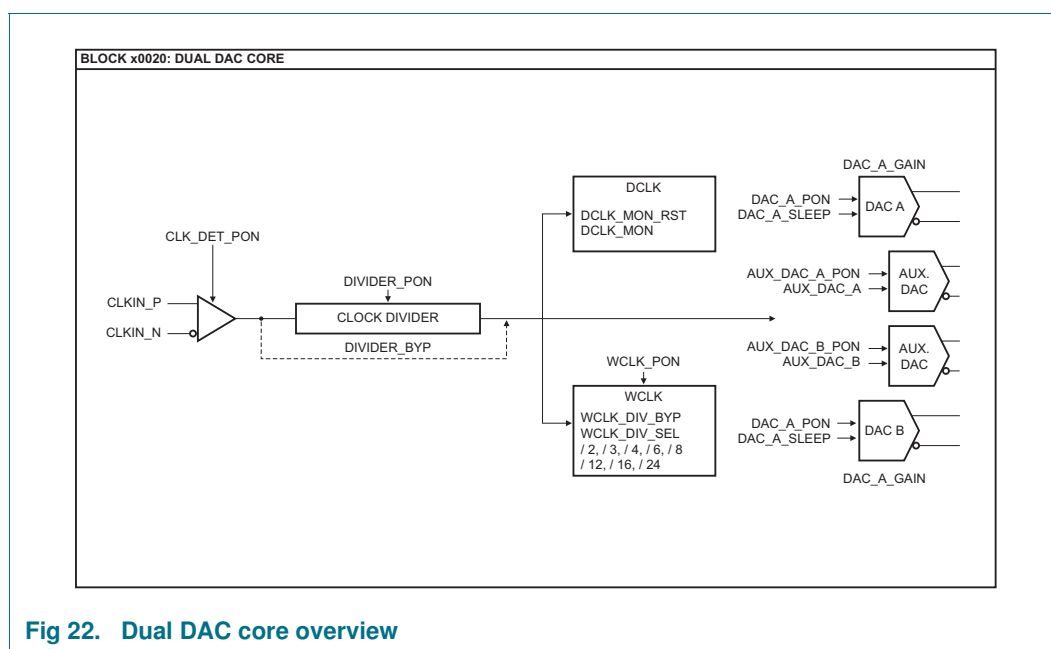


Fig 22. Dual DAC core overview

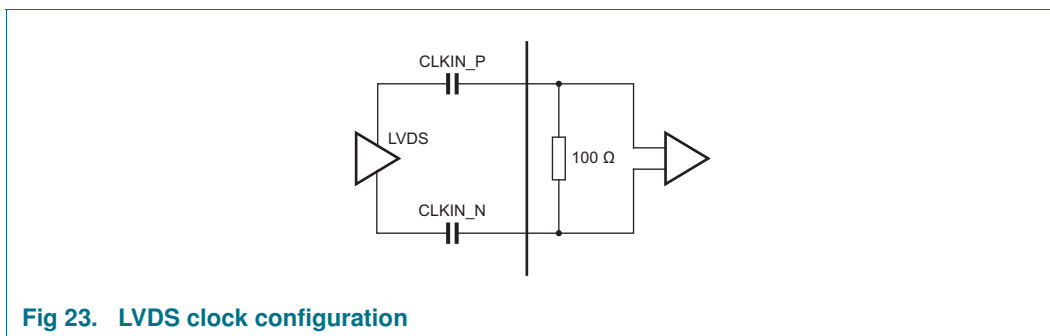
### 11.2.6.1 Clocks

The DAC165xD requires one single differential clock (CLKIN\_P, CLKIN\_N) for the whole device (including the digital data path, the dual DAC core and the JESD204B interface).

During the reset phase (RESET\_N asserted), the input clock must be stable and running, ensuring a proper reset of the complete device.

#### Clock input external configuration

The DAC165xD incorporates one differential clock input, CLKIN\_N/CLKIN\_P, with embedded 100 Ω differential resistor. The clock input can be LVDS but it can also be interfaced with CML.



### Clock frequency input range

The DAC165xD can only operate in two modes:

- Direct clocking mode:  
The input clock frequency is limited to 1500 MHz
- Divided clocking mode:  
The input clock is internally divided by 2, 4, 6, or 8. The maximum input frequency is 3 GHz. This mode allows the programming of the group delay feature.

### Clocks internal configuration

The following registers must be specified to configure the DAC165xD in Direct clocking mode (see [Table 46](#)):

- <td>

The final clock is referred to as the "DAC clock". This is the clock that is going directly to the dual DAC core and is running at maximum speed. From this DAC clock two digital clocks are derived: DCLK and WCLK.

DCLK is the digital clock used for all logic related to the Digital Signal Processing (DSP) of the DAC. DCLK is automatically generated from the registers PON\_DAC\_CORE\_CFG\_0, INTERPOLATION (see [Table 59](#)) and CDI\_MOD. Registers DCLK\_MON and DCLK\_MON\_RST (see [Table 47](#)) can be used to monitor this automatic generation. This flag can also raise the interrupt feature (see Interrupt section).

WCLK is the digital clock used for all logic related to the Digital Lane Processing (DLP) of the input interface. This clock must be enabled by bit WCLK\_PON (see [Table 47](#)). The divider ratio WCLK\_DIV\_SEL (see [Table 47](#)) must be specified using the following equation:

$$\frac{WCLK}{DAC\_Clock} = \frac{M}{(L \times INTERPOLATION)} \quad (11)$$

Where:

- M stands for the number of DACs used inside the DAC165xD (M = 2)  
**Remark:** DAC165xD is a dual core device therefore M = 2. It is possible to use the device in a single core manner, but the configuration must be set to M = 2 and the related lanes and DAC core must be powered off.
- L stands for the number of serial input lanes used (L = 1, L = 2, or L = 4)

- INTERPOLATION stands for the interpolation factor specified in register INTERPOLATION (see [Table 59](#)).

[Table 23](#) shows the results for nominal use cases

**Table 23. WCLK\_DIV selection**

LMF configuration	Interpolation ratio	WCLK/DAC clock	WCLK_DIV_BYP	WCLK_DIV_SEL
421 / 422	2	1/4	0	010
	4	1/8	0	100
	8	1/16	0	110
222	2	1/2	0	000
	4	1/4	0	010
	8	1/8	0	100
124	2	1	1	xxx
	4	1/2	0	000
	8	1/4	0	010
211	2	1/2	0	000
	4	1/4	0	010
	8	1/8	0	100

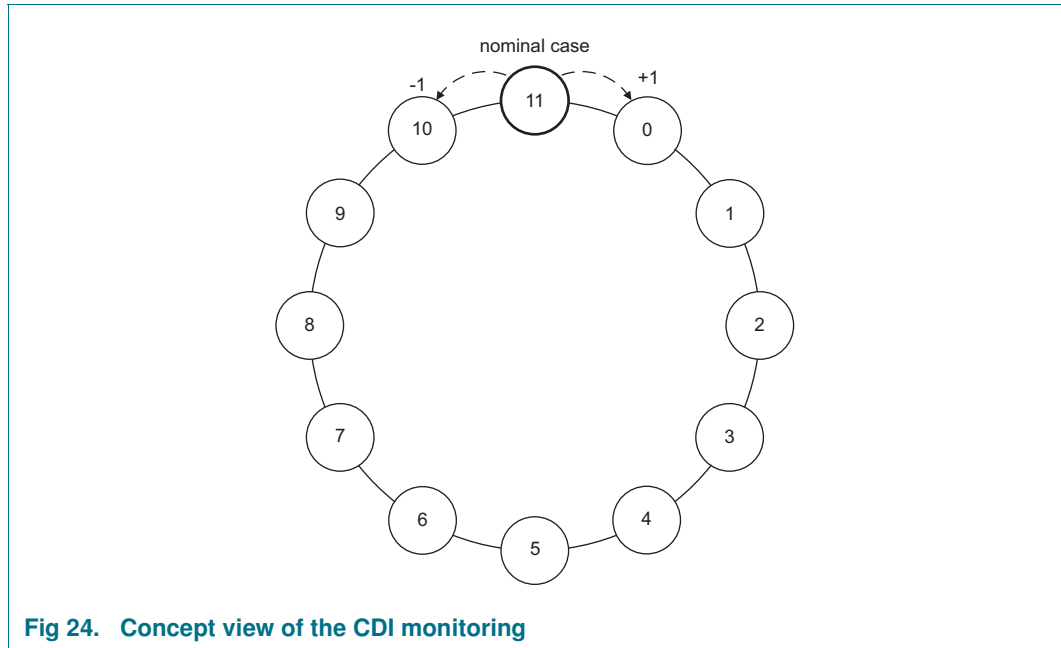
### Clock Domain Interface (CDI)

A CDI logic handles the error-free data transition from the WCLK clock domain to the DCLK domain. It consists of 12 buffers that absorb the phase variation between the two clocks. The reliability of the data transmission depends on the clock-frequency ratios and therefore on the interpolation mode. The CDI must be set in the same mode as the interpolation ratio to be properly configured. This mode is configured with register CDI\_CTRL (see [Table 56](#)).

**Table 24. Interpolation and CDI modes**

Interpolation	CDI mode	Maximum input data rate (MSPs)
~1	Mode 0 (^2)	750
×2	Mode 0 (^2)	750
×4	Mode 1 (^4)	375
×8	Mode 2 (^8)	187.5

Ideally, buffer number 11 is selected as the reference. If jitter of +/- 1 clock cycle is injected between the clocks occurs, the pointer can oscillate between buffers 10 and 0. If more jitter is injected, the range increases to buffers 9 and 1, etc.



**Fig 24. Concept view of the CDI monitoring**

This buffer position can be monitored using register MON\_DCLK (see [Table 57](#)).

The variation of the buffer location could also raise an interrupt (see [Section 11.7](#)).

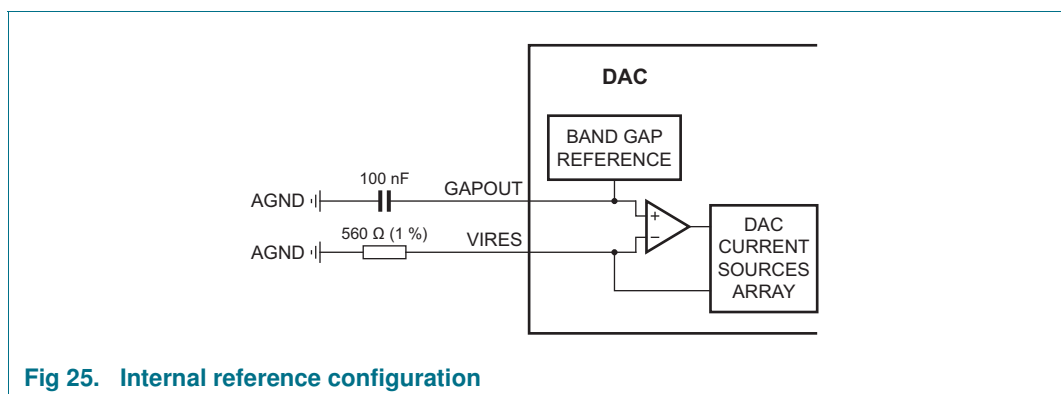
### 11.3 Analog dual DAC core

The DAC165xD core consists of two DACs. Each of them can be independently set to Power-down mode or Sleep mode if using the DAC in single channel mode is preferred (DAC\_A\_PON, DAC\_B\_PON; see [Table 48](#)).

#### 11.3.1 Regulation

The DAC165xD reference circuitry integrates an internal band gap reference voltage which delivers a 0.7 V reference on the GAPOUT pin. Decouple pin GAPOUT using a 100 nF capacitor.

The reference current is generated via an external resistor of 560 Ω (1 %) connected to VIRES.



**Fig 25. Internal reference configuration**

Figure 25 shows the optimal configuration for temperature drift compensation because the band gap reference voltage can be matched to the voltage across the feedback resistor.

The DAC current can also be adjusted by applying an external reference voltage to the non-inverting input pin GAPOUT and disabling the internal band gap reference voltage (bit BGAP\_PON; see Table 46).

11.3.2 Full-scale current adjustment

The default full-scale current ( $I_{O(fs)}$ ) is 20 mA. However, further adjustments, ranging from 8.1 mA to 34 mA, can be made to both DACs independently using the serial interface.

The settings applied to DAC\_A\_GAIN[9:0] (see Table 45) define the full-scale current of DAC A:

$$I_{O(fs)} \mu A = 8100 + DAC\_A\_GAIN[9:0] \times 25.3 \tag{12}$$

The DAC\_B\_GAIN[9:0] (see Table 45) define the full-scale current of DAC B:

$$I_{O(fs)} \mu A = 8100 + DAC\_B\_GAIN[9:0] \times 25.3 \tag{13}$$

11.4 Analog output

11.4.1 DAC1658D: High common-mode output voltage

The device has two output channels, each producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IOUTA\_P/IOUTA\_N and IOUTB\_P/IOUTB\_N. Connect these pins using a load resistor  $R_L$  to the 3.3 V analog power supply ( $V_{DDA(3V3)}$ ).

Figure 26 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of NMOS current sources and associated switches for each segment.

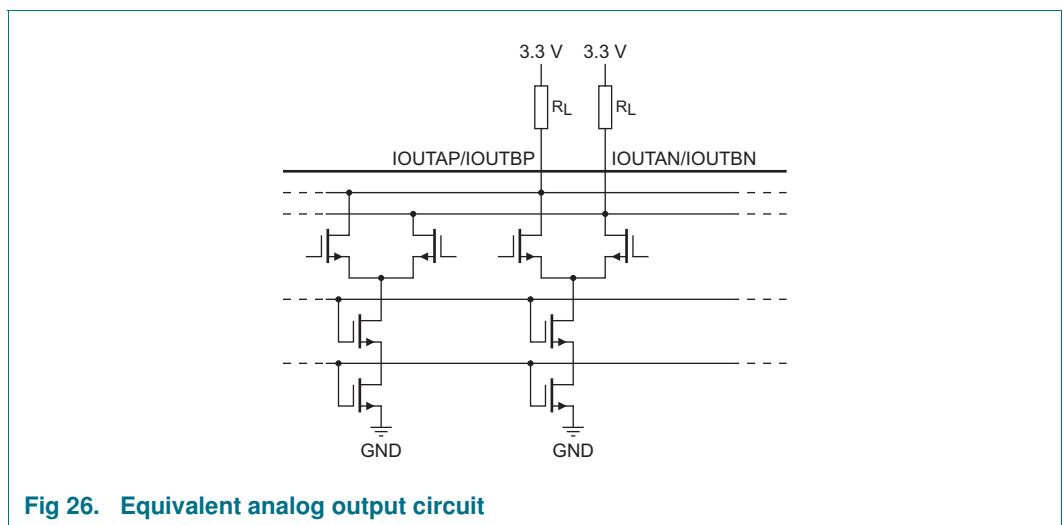


Fig 26. Equivalent analog output circuit

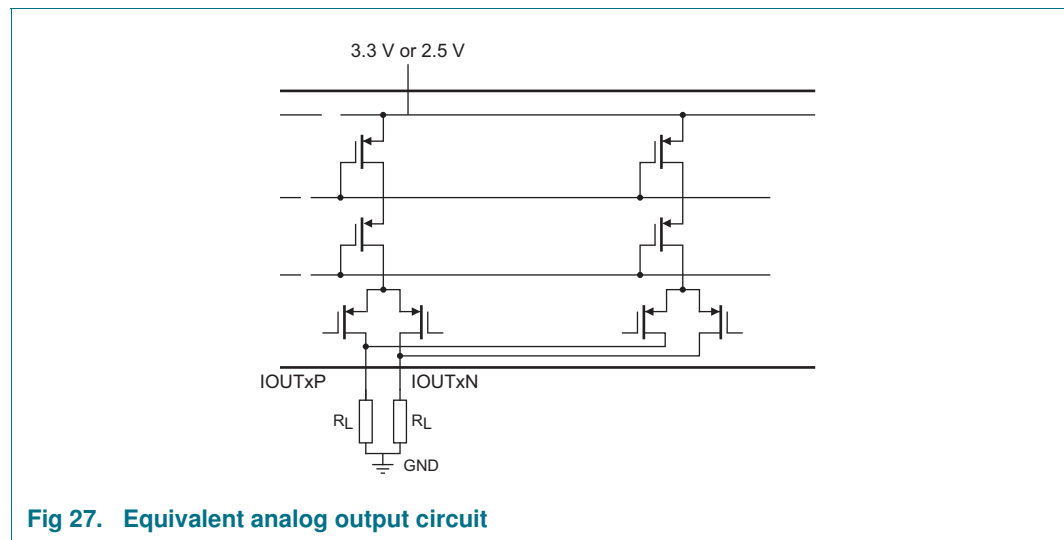
The cascode source configuration increases the output impedance of the source, which improves the dynamic performance of the DAC because there is less distortion.

Depending on the application, the various stages and the targeted performances, the device can be used for an output level of up to 2 V (p-p).

**11.4.2 DAC1653D: Low common-mode output voltage**

The device has two output channels, each producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IOUTA\_P/IOUTA\_N and IOUTB\_P/IOUTB\_N. Connect these pins using a load resistor  $R_L$  to the analog ground (GND).

Figure 27 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of PMOS current sources and associated switches for each segment.



**Fig 27. Equivalent analog output circuit**

**11.4.2.1 Auxiliary DACs**

The DAC1653D integrates two auxiliary DACs, which are used to compensate any offset between the DACs and the next stage in the transmission path. Both auxiliary DACs have a 10-bit resolution and are current sources (referenced to ground). Both of them can be disabled using bits DAC\_A\_AUX\_PON and DAC\_B\_AUX\_PON of the Auxiliary DACs registers (see Table 49).

The full-scale output current for each DAC is the sum of the two complementary current outputs:

- $I_{OAUXA(fs)} = I_{AUXA\_P} + I_{AUXA\_N}$
- $I_{OAUXB(fs)} = I_{AUXB\_P} + I_{AUXB\_N}$

The output current depends on the digital input data set by SPI registers DAC\_A\_AUX\_MSB (bits DAC\_A\_AUX[9:2]), DAC\_A\_AUX\_LSB (bits DAC\_A\_AUX[1:0]), DAC\_B\_AUX\_MSB (bits DAC\_B\_AUX[9:2]) and DAC\_B\_AUX\_LSB (bits DAC\_B\_AUX[1:0]; see Table 49).

$$I_{AUXA\_P} = I_{OAUXA(fs)} \times \left( \frac{DATAA}{1023} \right) \tag{14}$$

$$I_{AUXA\_N} = I_{OAUXA(f_s)} \times \left( \frac{1023 - DATAA}{1023} \right) \tag{15}$$

$$I_{AUXB\_P} = I_{OAUXB(f_s)} \times \left( \frac{DATAB}{1023} \right) \tag{16}$$

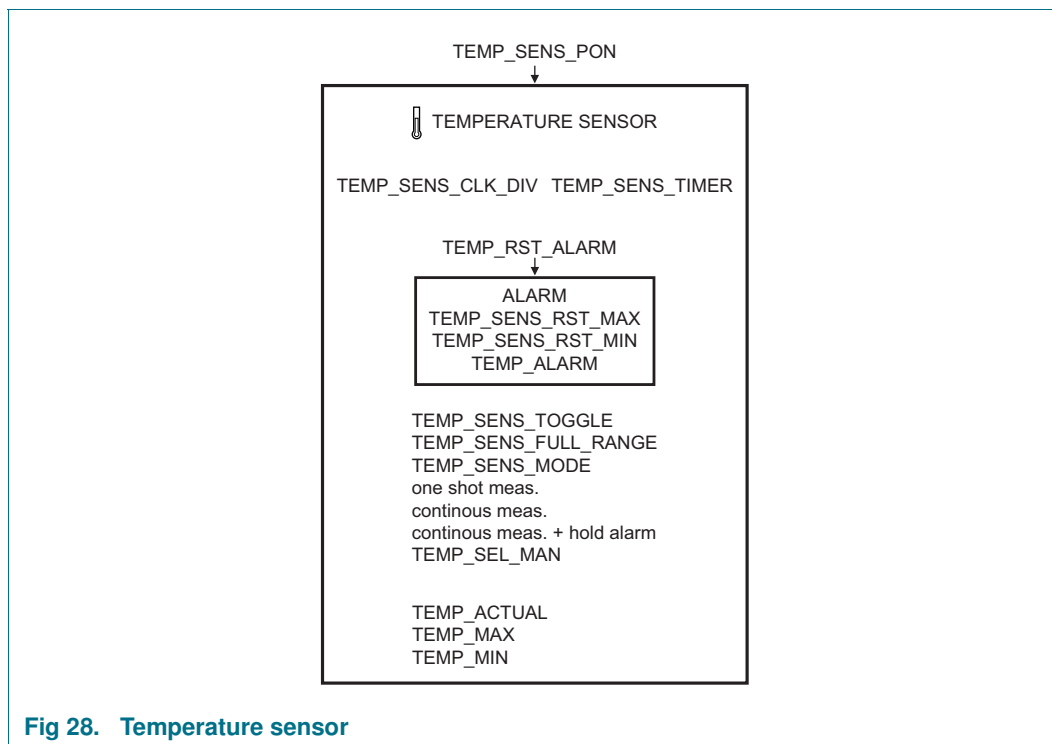
$$I_{AUXB\_N} = I_{OAUXB(f_s)} \times \left( \frac{1023 - DATAB}{1023} \right) \tag{17}$$

Table 25 shows the output current as a function of the auxiliary DACs data DATAA and DATAB Equation 14 to Equation 17.

**Table 25. Auxiliary DAC transfer function**

DATAA; DATAB	DAC_A_AUX[9:2]/ DAC_A_AUX[1:0]; DAC_B_AUX[9:0]/ DAC_B_AUX[1:0] (binary coding)	I <sub>AUXA_P</sub> ; I <sub>AUXB_P</sub> (mA)	I <sub>AUXA_N</sub> ; I <sub>AUXB_N</sub> (mA)
0	00 0000 0000	0	2.2
...	...	...	...
512	10 0000 0000	1.1	1.1
...	...	...	...
1023	11 1111 1111	2.2	0

## 11.5 Temperature sensor



**Fig 28. Temperature sensor**

The DAC165xD embeds a temperature sensor to monitor the temperature inside the chip. This module is based on a 6-bit resolution ADC clocked at  $DAC\_CLK / (8 \times TS\_CLKDIV)$ . The mode of measurements is configurable as a one shot measurement, continuous measurements or continuous measurements with alarm flag held in case of temperature exceeding a preset threshold. In continuous mode, the measurement is done every  $TS\_TIMER$  cycles. The  $TEMPS\_LVL$  specifies the threshold level that is compared with the measured value. If the measured value exceeds the threshold, the  $TEMP\_ALARM$  flag is set and triggers a mute action (see [Section 11.2.3.10](#)). The maximum and minimum temperatures measured are stored in registers  $TEMP\_MAX$  (see [Table 85](#)) and  $TEMP\_MIN$  (see [Table 86](#)). The current temperature is stored in register  $TEMP\_ACTUAL$  (see [Table 84](#)). Once the  $TEMP\_ALARM$  flag is set, it must be reset using the  $TEMP\_SENS\_RST\_ALARM$  bit of the temperature sensor control register (see [Table 80](#)). The maximum and minimum temperature can also be reset using bits  $TEMP\_SENS\_RST\_MAX$  and  $TEMP\_SENS\_RST\_MIN$  of the temperature sensor control register (see [Table 80](#)).

The value stored in the maximum, current, and minimum registers represents the output value of the ADC. This value must be matched to the real temperature.

$$T (^{\circ}C) = \alpha \times ADC\_value \quad (18)$$

Where:

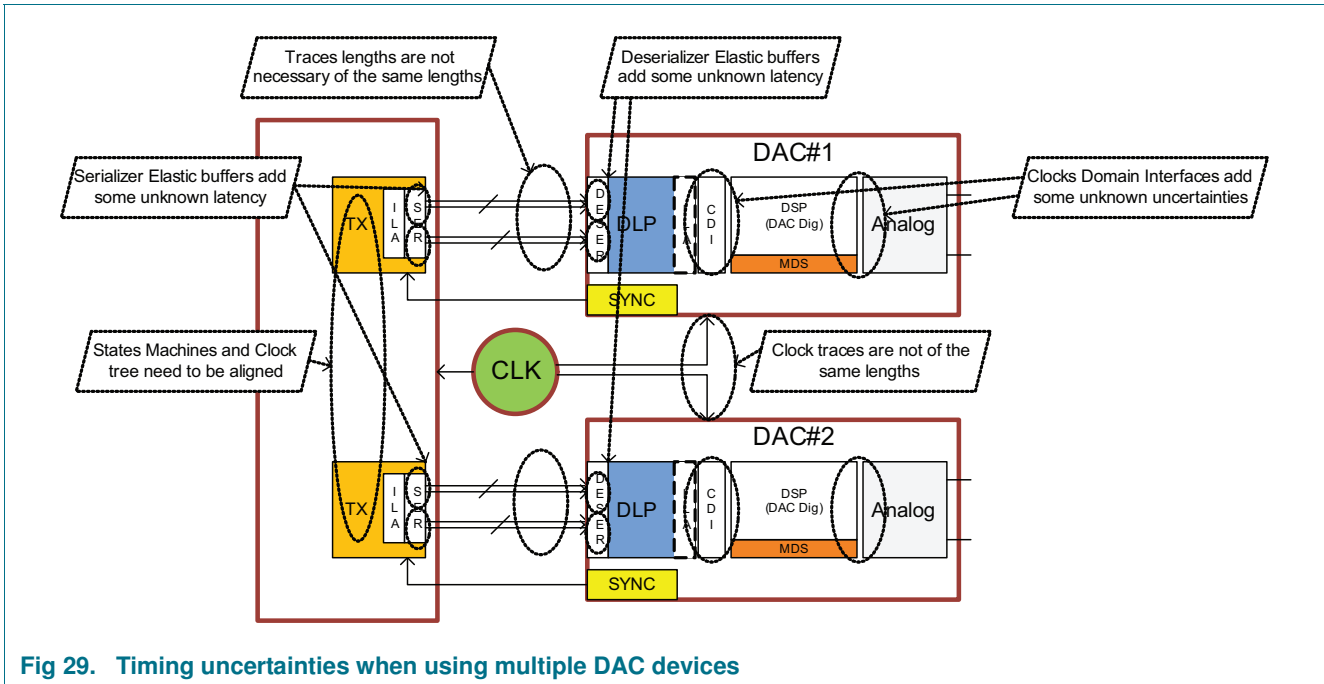
- $\alpha = \langle tbd \rangle$

## 11.6 Multiple Devices Synchronization (MDS); JESD204B subclass I

The MDS feature enables multiple DAC channels to be sampled synchronously and phase coherently to within one DAC clock period. This feature is part of the JESD204B standard but the implementation adds some unique features that simplify the PCB design.

### 11.6.1 Non-deterministic latency of a system

In a system using multiple DAC devices, there are numerous sources of timing uncertainties. [Figure 29](#) gives an overview of these uncertainties.



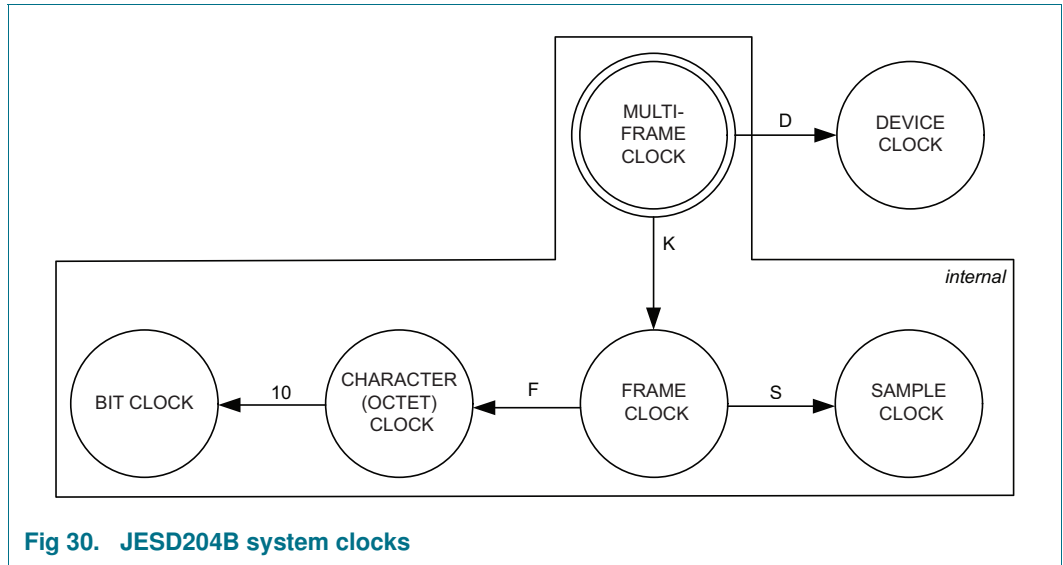
**Fig 29. Timing uncertainties when using multiple DAC devices**

The sources of uncertainties are shared between the Transmitter device (TX), the Receiver devices (RX), the PCB layout and the architectures of the JESD204B system clocks. A single device can detect timing drift and uncertainties, but not at system level. Therefore a synchronization process is required to enable the system to output the analog signals of all the RX devices in a coherent way. Moreover, the system becomes predictable if from one start-up to another one, the overall latency is deterministic.

The MDS feature of the DAC165xD has been implemented in compliance with the JESD204B subclass 1 specification to fulfill these requirements.

### 11.6.2 JESD204B system clocks

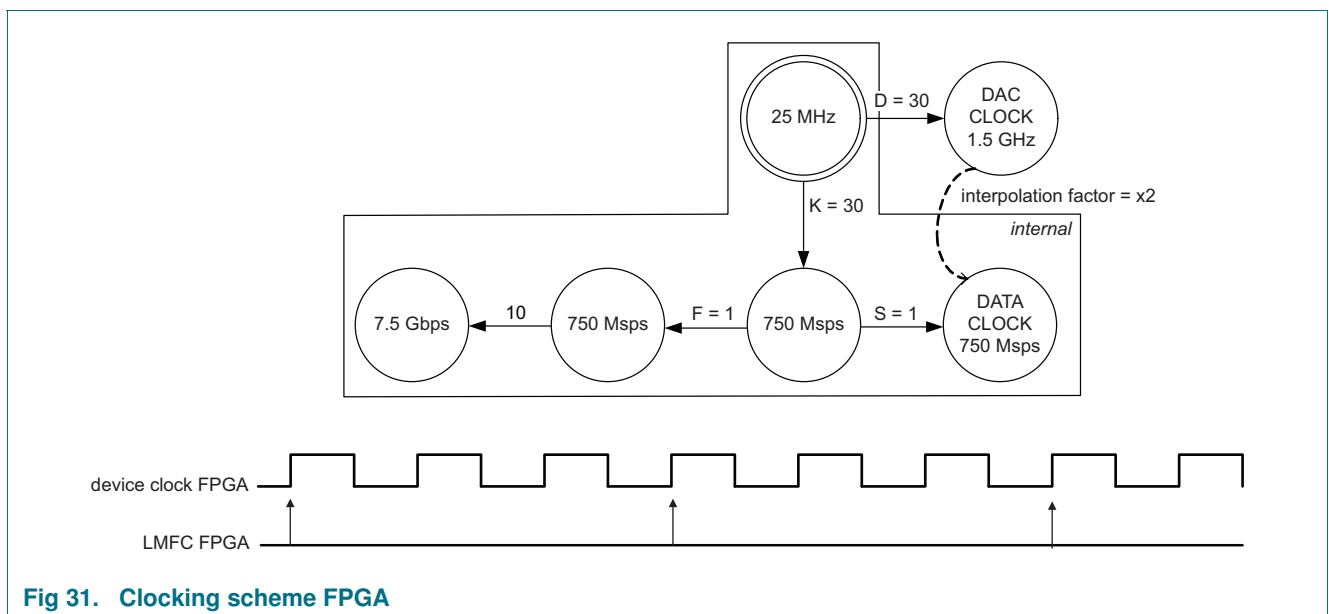
There are various system 'clocks' that are used in the JESD204B specification. However, only one of them is seen at system level, the device clock, which is provided to the device. The other clocks are related to the JESD204B standard and are used to assemble/deassemble the data in octets and then in 10B words (see JESD204B standard). [Figure 30](#) and [Table 26](#) show the relationship between them.

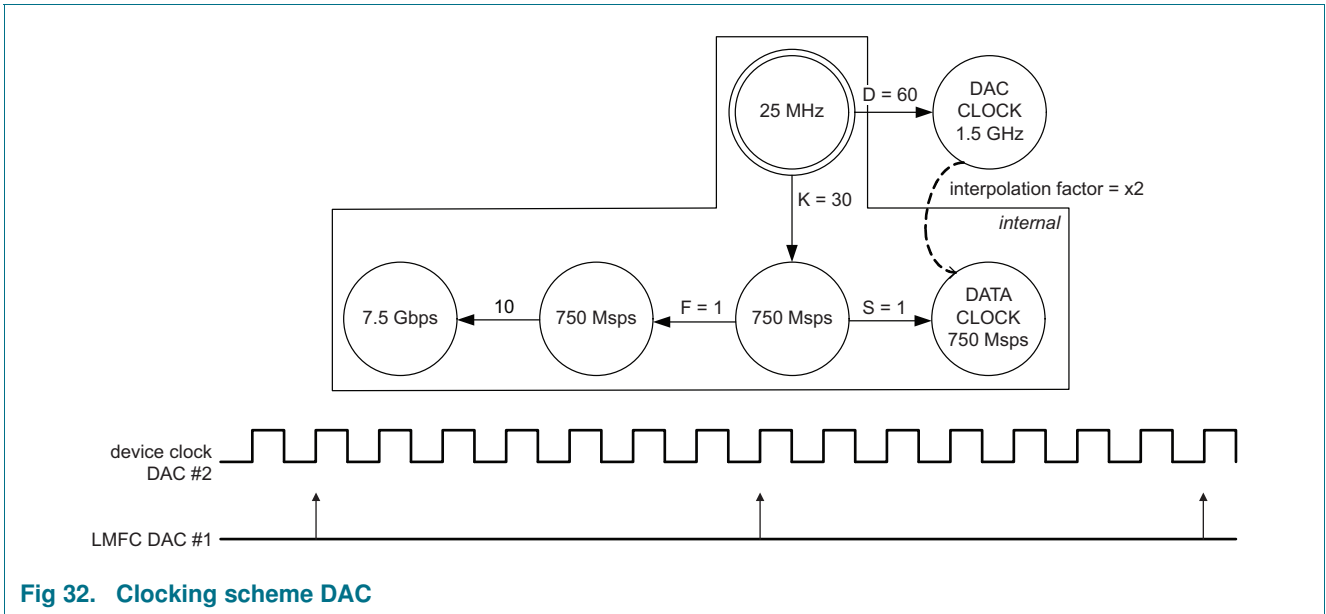


**Table 26. Relationship between various clocks**

Clock name	Ratio with respect to multi-frame clock	Comments regarding JESD204B specification
multi-frame clock	1	-
frame clock	$\times K$	$\text{Ceil}(17 / F) \leq K \leq \text{min}(32, \text{floor}(1024 / F))$
character clock	$\times F \times K$	$F = 1$ to 256
bit clock	$\times 10 \times F \times K$	8b/10b encoding
sample clock	$\times S \times K$	$S = 1$ to 32
device clock	$\times D$	D is integer

From a system point of view, the TX and RX must share the same values for the internal clocks but not necessarily the same device clocks. Figure 31 and Figure 32 show the clocking scheme for an FPGA and a DAC working in an LMF-S = 421-1 configuration.



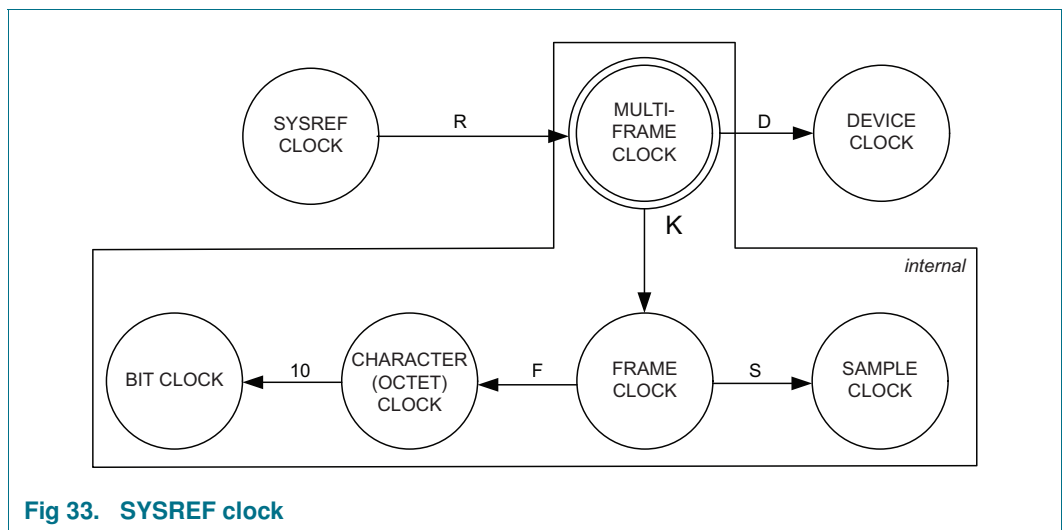


**Fig 32. Clocking scheme DAC**

As all clocks can be derived from the Multi-Frame Clock (MFC), this clock becomes the reference for a JESD204B system. Each device used in the system has its own local version of the MFC. These local version are called Local Multi-Frame Clock (LMFC). Due to the timing uncertainties the phase relationships between all the device LMFCs are unknown. The goal of MDS is to be able to realign all LMFCs in a fixed and accurate way.

**11.6.3 SYSREF clock**

To align all the LMFCs within the system, a new clock named SYSREF (SYSTEM REFERENCE) is used. This clock is linked to the multi-frame clock by a ratio  $R$ . It is a low frequency signal. However, the edges of the signal must be sharp enough as it is sampled by the device clock.



**Fig 33. SYSREF clock**

The SYSREF signals must be propagated to all the devices of the system. They are used to release the LMFC, so they are all aligned over the devices. The SYSREF signal is sampled by the device clocks. To ensure that all phases of the signals are aligned at the source, the SYSREF signals and the device clocks must be generated from the same clock IC.

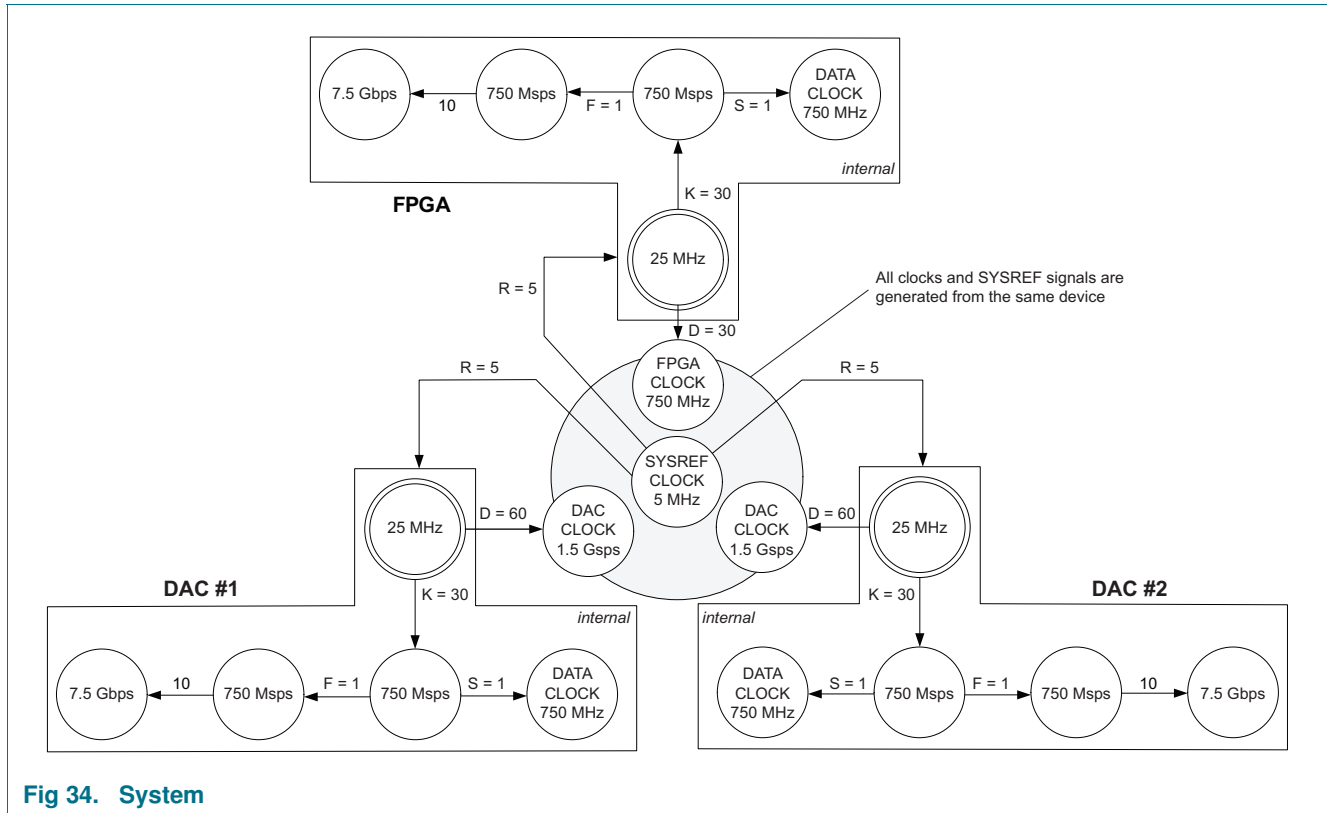
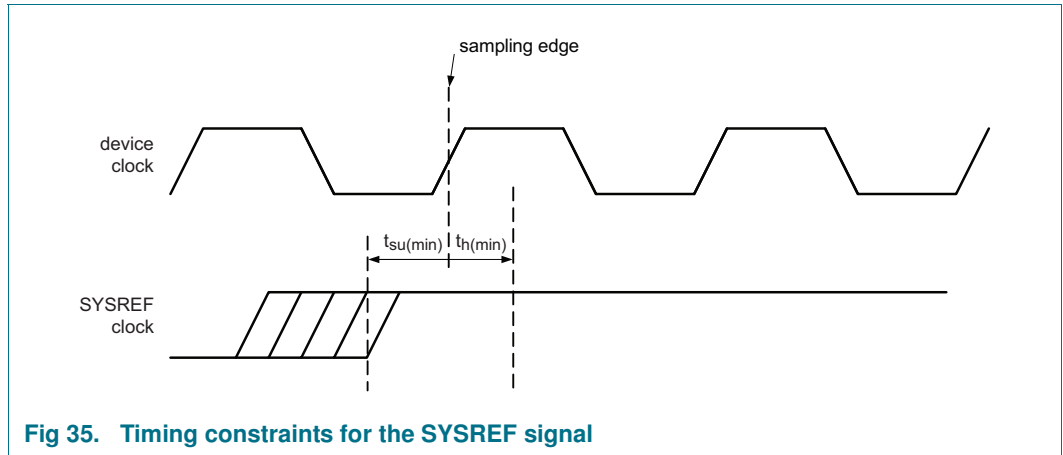


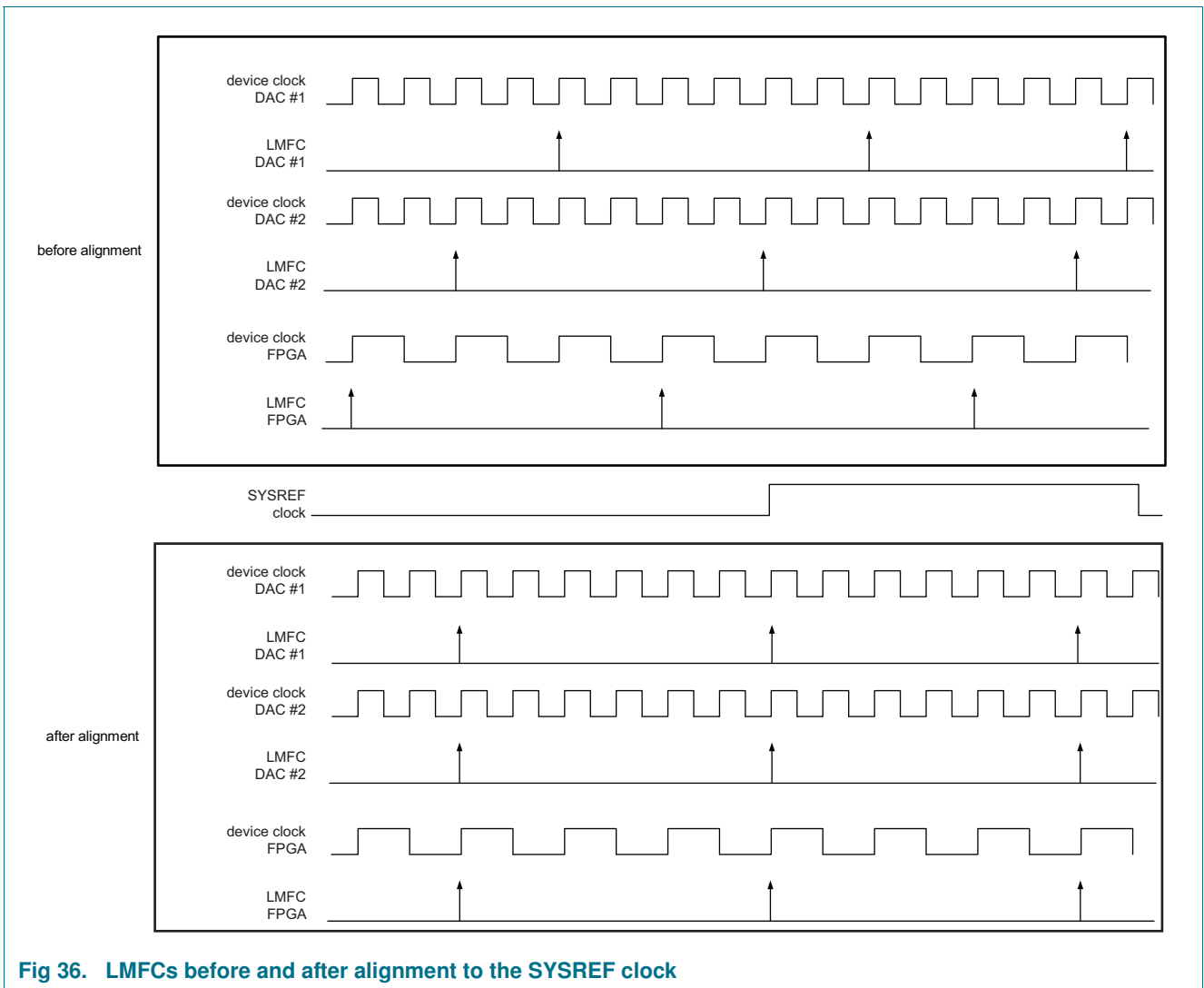
Fig 34. System

All the JESD204B devices sample the SYSREF signal with their own device clocks. The edge detection of the SYSREF signal is used as a system timing reference and the device phase-align their LMFCs to the closest edge of the SYSREF. To ensure an accurate alignment within all devices, the SYSREF signal must show the same phase at the input port of all the DAC devices to synchronize. Therefore, the trace lengths of the SYSREF signals must be equal for all the DAC devices. As the SYSREF signal is sampled by the device clock, the minimum setup ( $t_{su(min)}$ ) and hold ( $t_{h(min)}$ ) time are specified with respect to the Device Clock timing (see [Figure 35](#)).



**Fig 35. Timing constraints for the SYSREF signal**

The following figure shows the LMFCs before and after alignment to the SYSREF clock.



**Fig 36. LMFCs before and after alignment to the SYSREF clock**

11.6.4 MDS implementation

The DAC165xD MDS implementation is based on two modules as described in [Figure 37](#):

- **M1:**

This module contains the SYSREF detector that is sampled at the DAC clock and the control loop used to create a  $LMFC_{MDS}$  signal. The control loop is clocked with the digital clock. The digital clock equals DAC clock / 8.

**Remark:** The DAC clock and the device clock can differ when using the clock divider. In this section DAC clock is referring to the final clock used to sample the DAC cores.

- **M2:**

This module compares the phase of the  $LMFC_{RCV}$  received from the JESD204B digital lane processing to the phase of the  $LMFC_{MDS}$  and shifts the position of the buffer to align the data path to the  $LMFC_{MDS}$ .

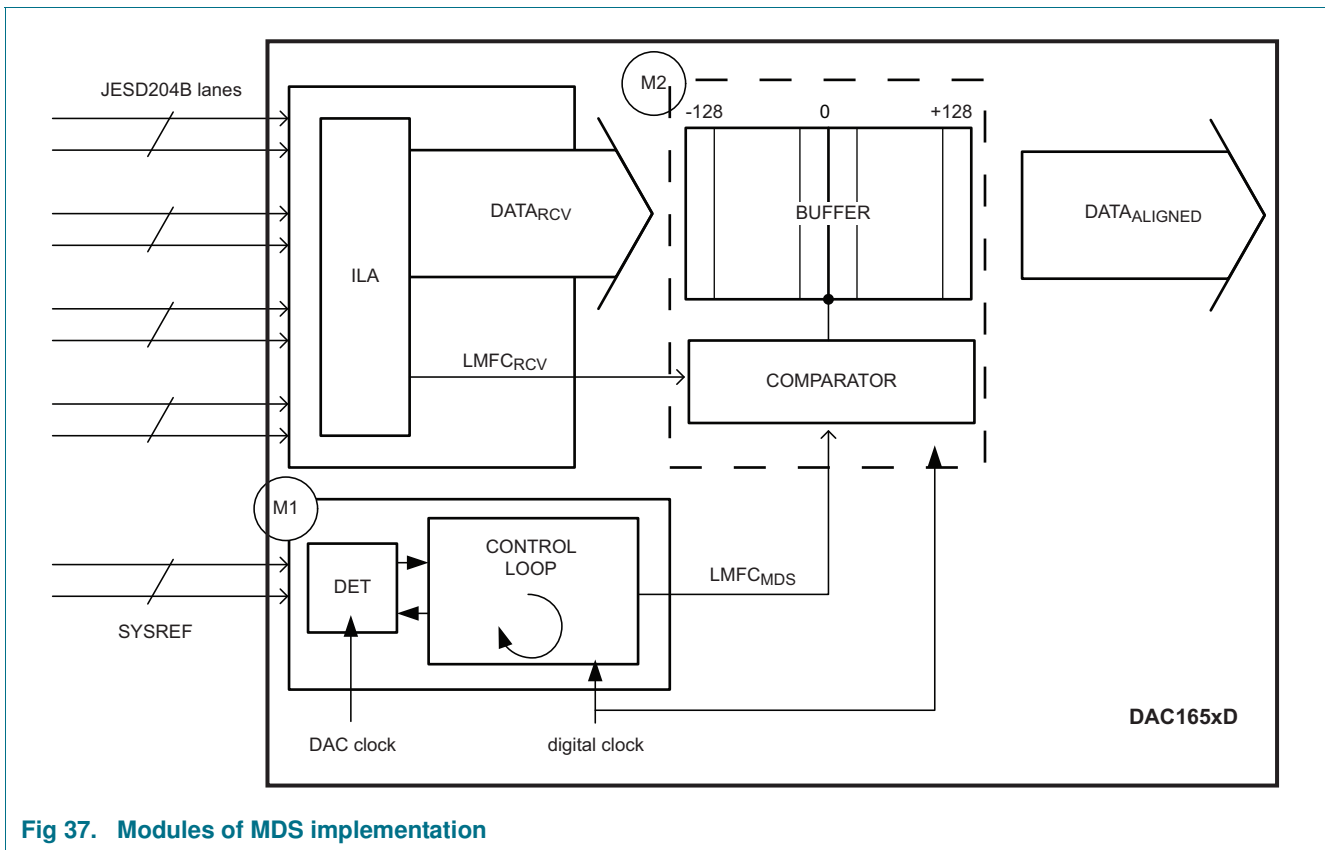


Fig 37. Modules of MDS implementation

11.6.4.1 Capturing the SYSREF signal

Module M1 ensures the capture of the SYSREF signal at DAC clock accuracy. This is done by an early-late detector and a control-loop. The control-loop must capture several SYSREF edges to deliver an accurate  $LMFC_{MDS}$  signal to the M2 module. The Initialization of the control-loop is triggered by the edge detection of the SYSREF signal (see [Figure 38](#)). It stands for 30 digital clock cycles, after which the capture process starts. The capture is done during the capture window and is repeated at the end of every control

loop period until the signal is locked. The SYSREF edge must occur within the capture window. The capture process must be delayed to match this constraint. This is done by programming the capture delay register.

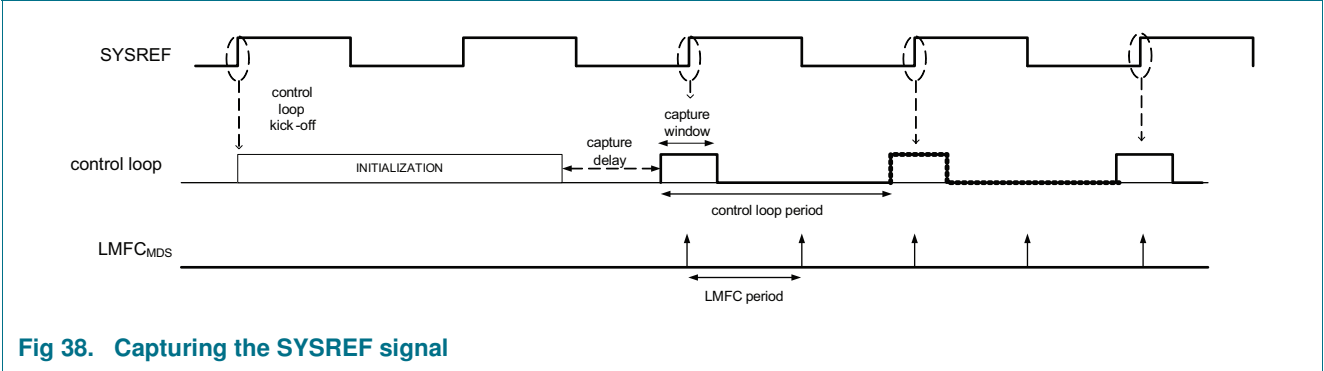


Fig 38. Capturing the SYSREF signal

Figure 39 shows an example on how to set up the M1 module.

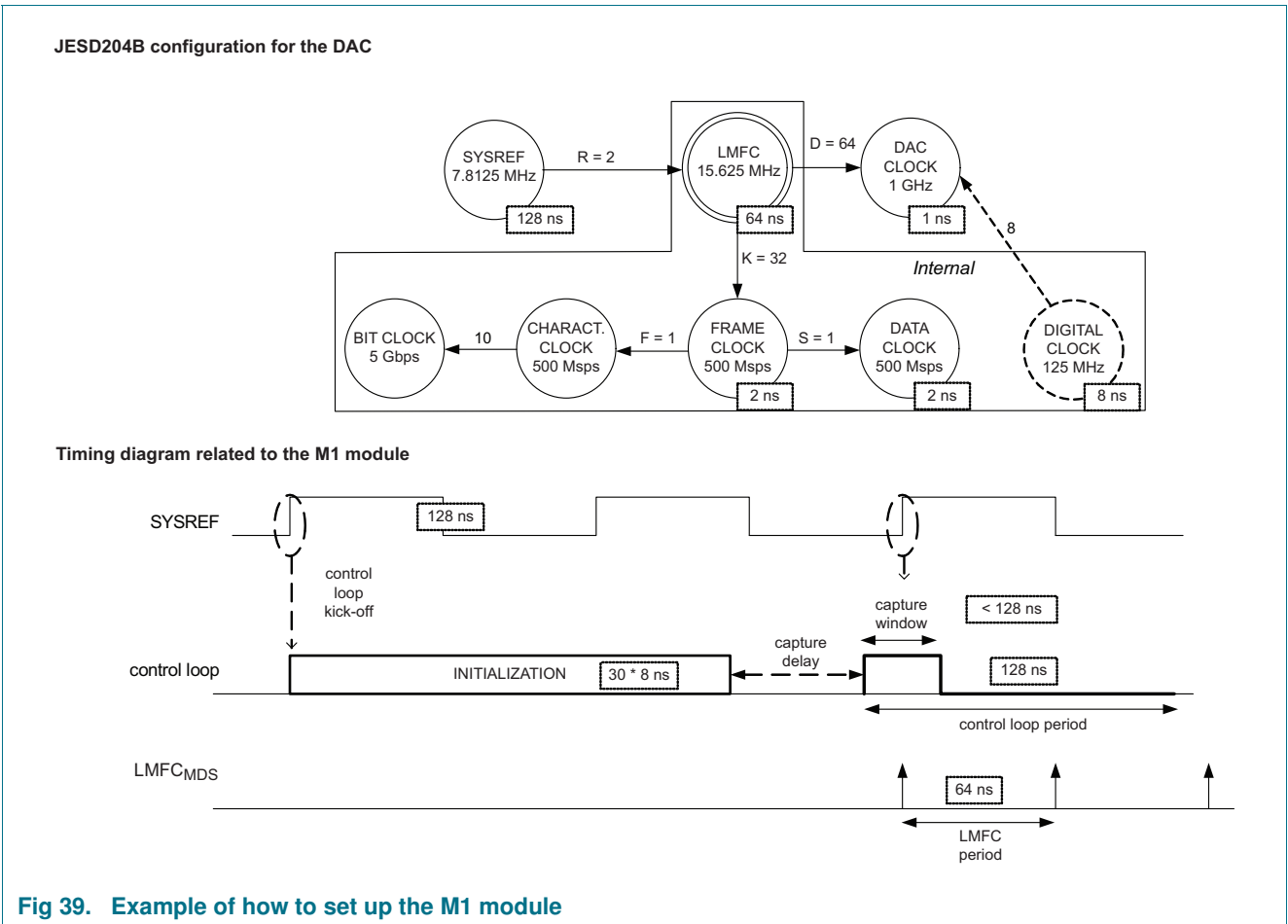


Fig 39. Example of how to set up the M1 module

The DAC165xD requires the following parameters:

- **LMFC\_PERIOD (register x0AA):**  
Period of the LMFC in digital clock cycles (e.g.  $8 \times 8$  ns)

- **CAPTURE\_DELAY (register x0AC):**

Must be tuned using the following equation:

$$\textit{initialization} + \textit{capture delay} = n \times \textit{SYSREF period}$$

Example:

$$(30 \times 8 \textit{ ns}) + (2 \times 8 \textit{ ns}) = 2 \times 128 \textit{ ns}$$

The capture delay is expressed in digital clock period (for example  $2 \times 8 \textit{ ns}$ )

- **Capture window and control loop period:**

These are specified using MDS\_WIN\_HIGH and MDS\_WIN\_LOW registers (respectively x0A9 and x0A8; see [Table 98](#)). They are expressed in digital clock cycles and must be set using the following equations:

$$\textit{capture window} = 2 \times (\textit{MDS\_WIN\_HIGH} + 1)$$

$$\textit{control loop period} = \textit{capture window} + \textit{MDS\_WIN\_LOW} + 1$$

**Remark:** The capture window must be smaller than the SYSREF period.

At the end of the capture process, the LMFC<sub>MDS</sub> signal is provided to the M2 module and the MDS\_LOCK bit of the MDS status register (see [Table 109](#)) is set to 1. If the M1 module cannot lock, the MDS\_BSY flag is kept high and a mute action can be held (see [Section 11.2.3.10](#), [Table 72](#), and [Table 73](#)).

#### 11.6.4.2 Aligning the LMFCs and the data

Module M2 ensures the phase alignment of the LMFC<sub>RCV</sub> to the closest LMFC<sub>MDS</sub> edge. The LMFC<sub>RCV</sub> is issued from the digital lane processing by analyzing the ILA sequence using the multi-frames /A/ symbols present. The transmitter (TX) is expected to have its self-synchronization process to the global MFC<sub>SYSTEM</sub>. It generates the ILA sequence based on the aligned LMFC<sub>TX</sub>. The total latency of the link is compounded of a fixed value (due to PCB traces, devices internal fixed delays, etc.) and an undeterministic value (due to elastic buffers, clocks domains interface, etc.). By buffering the data and the LMFC<sub>RCV</sub> after the inter-lane alignment process, the M2 module is capable to adjust the position of the buffer delay to match the recovered LMFC<sub>MDS</sub>.

[Figure 40](#) shows the alignment process for two links. The two links have two different total latencies but due to the LMFC<sub>TX</sub> and LMFC<sub>MDS</sub> phase synchronization to the MFC<sub>SYSTEM</sub>, the various devices are capable to align to the same MFC<sub>SYSTEM</sub> edge in a fixed and deterministic way.

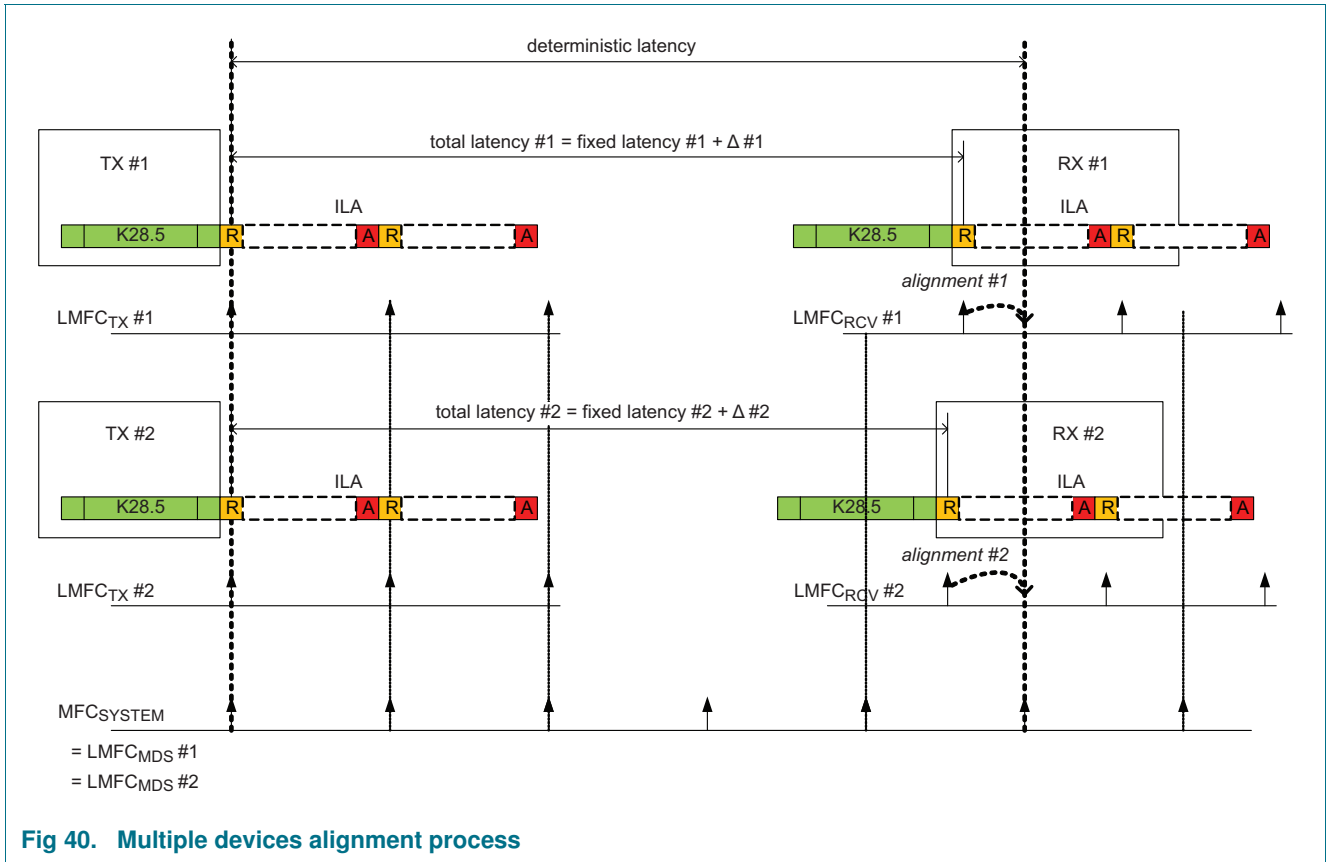
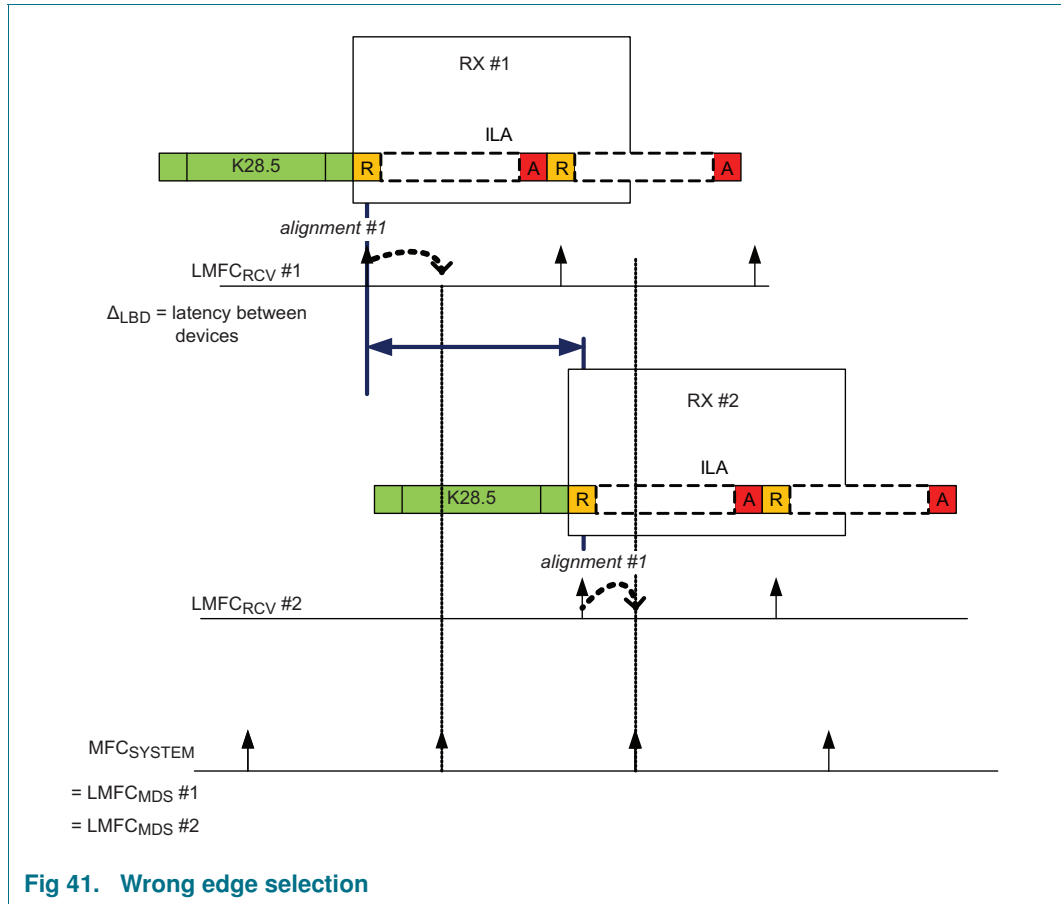
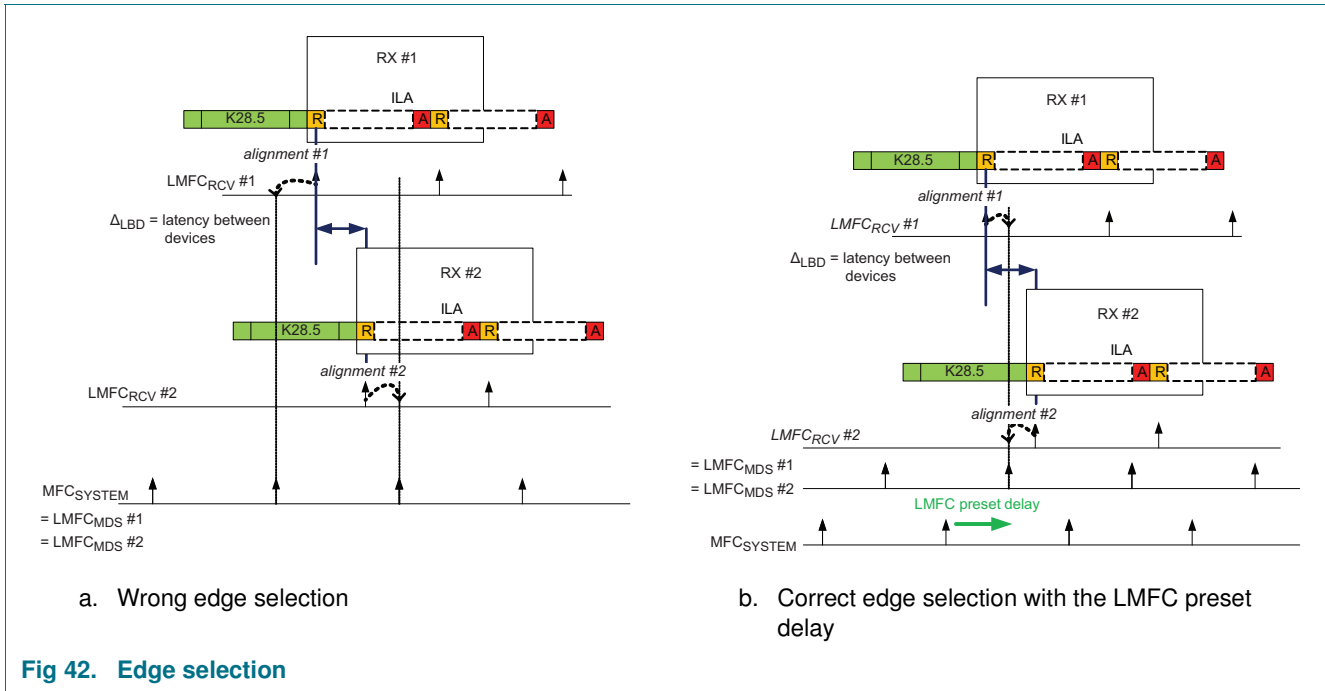


Fig 40. Multiple devices alignment process

Take special care when selecting the  $\text{MFC}_{\text{SYSTEM}}$  period. A longer period is better than a short one. In general, the  $\text{MFC}_{\text{SYSTEM}}$  period must be at least two times the maximum latency between devices to avoid a wrong edge selection as shown in [Figure 41](#).



In some cases, the latency between devices is small, but the edge is wrongly selected due to the closest edge criteria. To avoid this, a LMFC preset delay can be applied on all the LMFC<sub>MDS</sub> signals. It is important that all the DAC devices receive the same LMFC preset value. If not the latency is not exactly the same. This parameter is set with the LMFC\_PRST register (see [Table 100](#)) expressed in digital clock cycles. This value must be adjusted manually for each newly designed system.



**11.6.4.3 Monitoring the MDS process**

The buffer adjustment performed using the M1 and M2 modules can be read back using the MDS\_ADJ\_DLY register (see [Table 108](#)). Bits 7 to 3 of this register represent the coarse delay expressed in digital clock cycles whereas bits 2 to 0 represent the fine adjustment in DAC clock cycles. The buffer adjustment has a default value of 80h.

**11.6.4.4 Adding adjustment offset**

The DAC165xD allows adding an offset on top of the automatic adjustment. This is available via register MDS\_OFFSET\_DLY (see [Table 97](#)). The offset range is from -16 to 15 digital clock cycles. This offset value can be set at the start-up time as well as in at later period. This enables compensating a layout error or adding a specific phase to one DAC device.

Another adjustment delay can be set but only after a first automatic alignment using the manual adjustment delay register MDS\_MAN\_ADJ\_DLY (see [Table 94](#)).

**11.6.4.5 Selecting the SYSREF input port**

The DAC165xD incorporates two SYSREF differential ports: SYSREF\_E\_P/N (East side of the device) and SYSREF\_W\_P/N (West side of the device). One of these ports can be selected as the input for the SYSREF signal. Which port is selected is device dependent. One DAC165xD uses the Eastern SYSREF while another DAC165xD uses the Western SYSREF (see [Figure 43](#)).

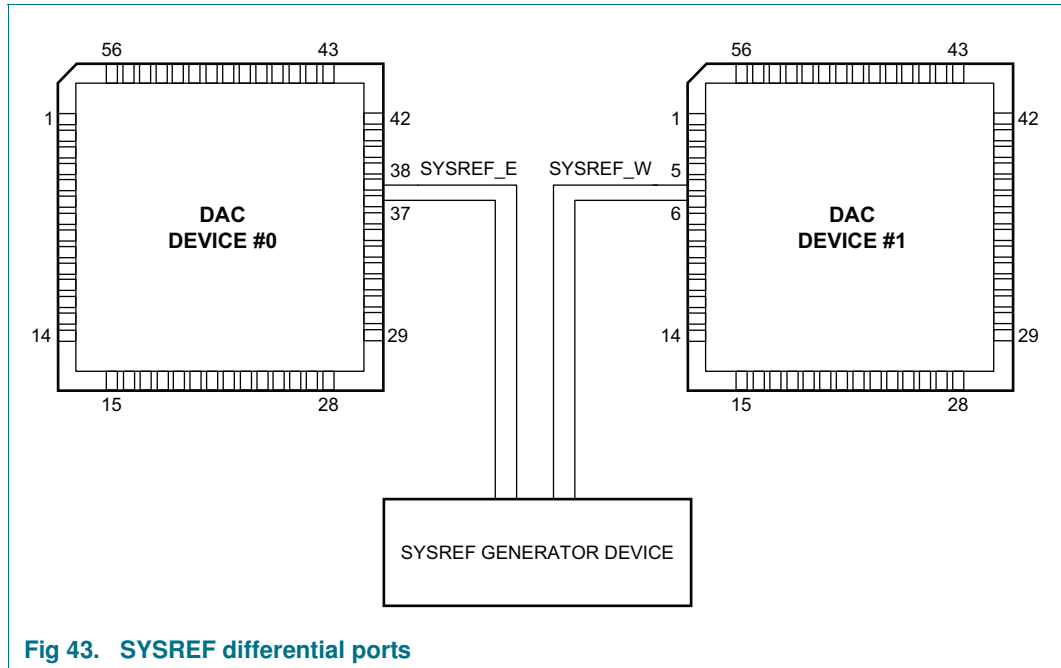


Fig 43. SYSREF differential ports

Register MDS\_EAST\_WEST (see [Table 90](#)) is used to select between the East port or the West port. Each SYSREF input buffer has an optional internal differential resistor termination of about 100 Ω. This resistor can be enabled with registers MDS\_SEL\_EAST\_RT and MDS\_SEL\_WEST\_RT (see [Table 92](#)). The clock edge (rising/falling) on which the SYSREF signal is sampled can also be selected using registers MDS\_SEL\_FE\_EAST and MDS\_SEL\_FE\_WEST (see [Table 92](#)).

## 11.7 Interrupts

In some cases it may be useful if the host-controller is notified that a certain internal event has taken place by means of an interrupt. The DAC165xD includes a simple interrupt (INTR) controller for this purpose.

The INTR-signal can be made available on one of the I/O pins. The polarity is programmable (see section IO\_MUX selection).

### 11.7.1 Events monitored

The DAC165xD monitors various internal events and indicates their occurrence in the INTR\_FLAGS registers (see [Table 79](#)). The following event can be observed:

- INTR\_DLP:
 

Digital Lane Processing (DLP) has its own interrupt controller. The result of this slave controller is provided to the main interrupt controller through the INTR\_DLP bit (see [Section 11.7.3](#)).
- MDS\_BSY and  $\overline{\text{MDS\_BSY}}$ :
 

Refer to the activity of the MDS controller. During the synchronization phase, the MDS\_BUSY signal is high, and come low once finished.

  - MDS\_BSY reflects the start of the activity of the MDS controller
  - $\overline{\text{MDS\_BSY}}$  reflects the end of the activity of the MDS controller

- TEMP\_ALARM:  
Indicates that the temperature measured by the on-chip temperature sensor exceeds the threshold temperature (see [Section 11.5](#)).
- LVL\_DET\_OR:  
Indicates that one of the level detectors is enabled.
- CA\_ERR:  
Indicates a DLP clock error.
- CLK\_MON:  
Indicates a CDI clock error.
- DCLK\_ERR\_MON:  
Indicates a drift on the DCLK as specified by register INTR\_MON\_DCLK\_RANGE (see [Table 77](#)).
- ERR\_RPT\_FLAG:  
Indicates the transmission of error reporting via the SYNCB interface.
- ALARM\_STATE:  
Indicates when an auto-mute event occurs (see [Section 11.2.3.10](#)).

### 11.7.2 Enabling interrupts

An indication if an 0→1 transition of the corresponding monitor- or error indicator activates the INTR-signal can be given using the INTR\_EN\_0 and INTR\_EN\_1 registers (see [Table 78](#)). The INTR\_FLAGS (see [Table 79](#)) registers indicate which of the selected events has invoked the interrupt. When bit INTR\_RST (see [Table 77](#)) is set to 1 the flags and the INTR-signal are reinitialized.

### 11.7.3 Digital Lane Processing (DLP) interrupt controller

The DLP has its own interrupt controller that reports to the main interrupt controller. This DLP interrupt controller is managed from the SPI registers of block x00E0 (see [Figure 44](#)).

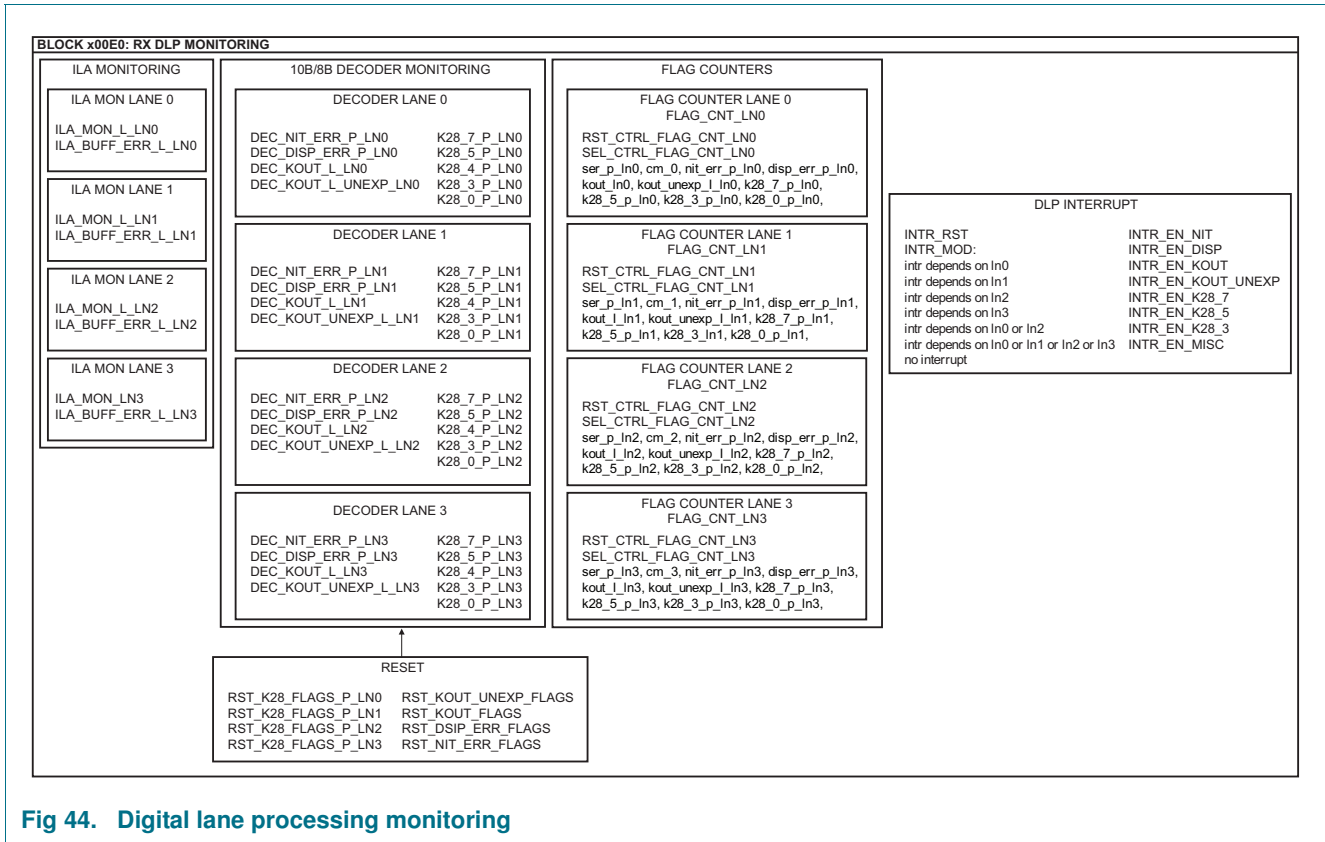


Fig 44. Digital lane processing monitoring

As this interrupt controller is dedicated to the JESD204B serial interface the INTR\_MODE bits (see [Table 140](#)) must be specified according to the LMF configuration used in the system.

Table 27. INTR\_MOD settings

INTR_MOD	Interrupt setting <sup>[1]</sup>	Nominal LMF use <sup>[2]</sup>
000	DLP interrupt depends on lane 0	124
001	DLP interrupt depends on lane 1	124
010	DLP interrupt depends on lane 2	124
011	DLP interrupt depends on lane 3	124
100	DLP interrupt depends on lane 0 or lane 2	222
101	DLP interrupt depends on lane 0 or lane 1 or lane 2 or lane 3	421 / 422
110	Hold_flagcnt <sup>[3]</sup>	-
111	no interrupt	-

[1] The lane numbering refers to the logical lanes (see [Section 11.7.4](#)).

[2] Any mode can also be used for debug purposes.

[3] The "HOLD\_FLAG\_CNT" feature is explained in [Section 11.7.6.1](#).

Register INTR\_DLP is reinitialized when the bit INTR\_RST control is set to logic 1 (see [Table 77](#)).

The DLP events that can be monitored with the interrupt controller are programmable via register INTR\_EN (see [Table 78](#)). Those events are related to the lanes specified by the INTR\_MOD bits in register INTR\_SER\_CTRL (see [Table 140](#)). They can be enabled by the following bits:

- INTR\_EN\_NIT: A Not-In-Table (NIT) error has occurred on one of the lanes
- INTR\_EN\_DISP: A disparity error has occurred on one of the lanes
- INTR\_EN\_KOUT: K control characters have been detected on one of the lanes
- INTR\_EN\_KOUT\_UNEXP: An unexpected K control character has been detected on one of the lanes
- INTR\_EN\_K28\_7: A K28.7 symbol has been detected on one of the lanes
- INTR\_EN\_K28\_5: A K28.5 symbol has been detected on one of the lanes
- INTR\_EN\_K28\_3: A K28.3 symbol has been detected on one of the lanes
- INTR\_EN\_MISC: An event related to the INTR\_MISC\_EN register (see [Table 134](#)) has occurred

Register INTR\_MISC\_EN (see [Table 134](#)) refers to two kinds of events, mainly for debug purposes:

- Lane x has reached the CS\_INIT state (see [Table 30](#))
- An error has occurred in the ILA alignment process on lane x

When register INTR\_DLP is invoked, the “FLAGS” registers must be read to determine which event has occurred:

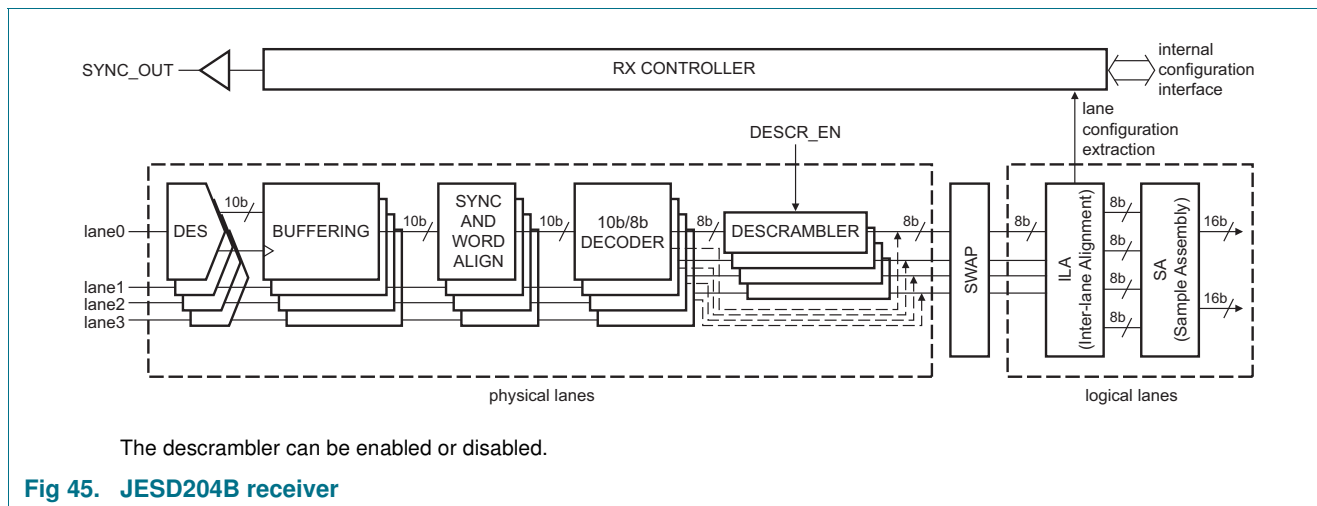
- An INTR\_EN\_NIT event is related to the DEC\_NIT\_ERR\_LNx bits of register DEC\_FLAGS (see [Table 127](#))
- An INTR\_EN\_DISP event is related to the DEC\_DISP\_ERR\_LNx bits of register DEC\_FLAGS (see [Table 127](#))
- An INTR\_EN\_KOUT event is related to the DEC\_KOUT\_LNx bits of register KOUT\_FLAGS (see [Table 128](#))
- An INTR\_EN\_KOUT\_UNEXP event is related to the DEC\_KOUT\_UNEXP\_LNx bits of register KOUT\_UNEXP\_FLAGS (see [Table 130](#))
- An INTR\_ENA\_K28\_7 event is related to the K28\_7\_LNx bits of register K28\_FLAG (see [Table 129](#))
- An INTR\_EN\_K28\_5 event is related to the K28\_5\_LNx bits of register K28\_FLAG (see [Table 129](#))
- An INTR\_EN\_K28\_3 event is related to the K28\_3\_LNx bits of register K28\_FLAG (see [Table 129](#))
- An INTR\_EN\_MISC event is related to the CS\_STATE\_LNx bits of register CS\_STATE\_LNX (see [Table 132](#)) and the ILA\_BUFF\_ERR\_LNx bits of register ILA\_BUFF\_ERR register (see [Table 126](#))

All flag bits can be reset using register RST\_FLAGS\_MON (see [Table 139](#)).

**Remark:** Checking the CS\_STATE\_LNx = CS\_INIT interrupts allows to indirectly test the SYNC\_REQUEST of the DAC. This feature can help if one does not want to use the differential SYNC\_OUT signal.

### 11.7.4 JESD204B physical and logical lanes

The DAC165xD integrates a JESD204B serial interface with a high flexibility of configuration.



**Fig 45. JESD204B receiver**

Because of various implementations for JESD204B transmitter devices, a flexible configuration of the physical lanes is required. This configuration allows the lane polarity to invert individually and to arbitrary swap the lane order. Identifying the lane numbers can be confusing because of the lane swapping. Two terms, physical and logical, are used in this document to explicitly identify the lanes.

#### Physical lanes:

The DAC165xD integrates four JESD204B serial receivers that are referenced via the pinning information (see [Figure 2](#)).

- Physical lane 0 refers to the signal coming from pins VIN\_P0 and VIN\_N0
- Physical lane 1 refers to the signal coming from pins VIN\_P1 and VIN\_N1
- Physical lane 2 refers to the signal coming from pins VIN\_P2 and VIN\_N2
- Physical lane 3 refers to the signal coming from pins VIN\_P3 and VIN\_N3

#### Logical lanes:

The DAC165xD incorporates a Swap lanes module (see [Figure 45](#)) that allows a remapping of the lane numbers to be compatible with the system implementation.

- Logical lane 0 refers to the lane specified with the LN\_SEL\_LN0 bits in register LN\_SEL (see [Table 118](#))
- Logical lane 1 refers to the lane specified with the LN\_SEL\_LN1 bits in register LN\_SEL (see [Table 118](#))
- Logical lane 2 refers to the lane specified with the LN\_SEL\_LN2 bits in register LN\_SEL (see [Table 118](#))
- Logical lane 3 refers to the lane specified with the LN\_SEL\_LN3 bits in register LN\_SEL (see [Table 118](#))

The following naming convention is used to distinguish between the physical lanes and the logical lanes in the SPI registers: “P\_LNx” is used to identify the physical lanes. “L\_LNx” is used to identify the logical lanes. “x” stands for the lane number in both cases.

11.7.5 RX Digital Lane Processing (DLP)

Digital lane processing is the module containing all JESD204B interface controls except the PHY deserializer.

Figure 46 shows the registers for the configuration of the digital lane processing.

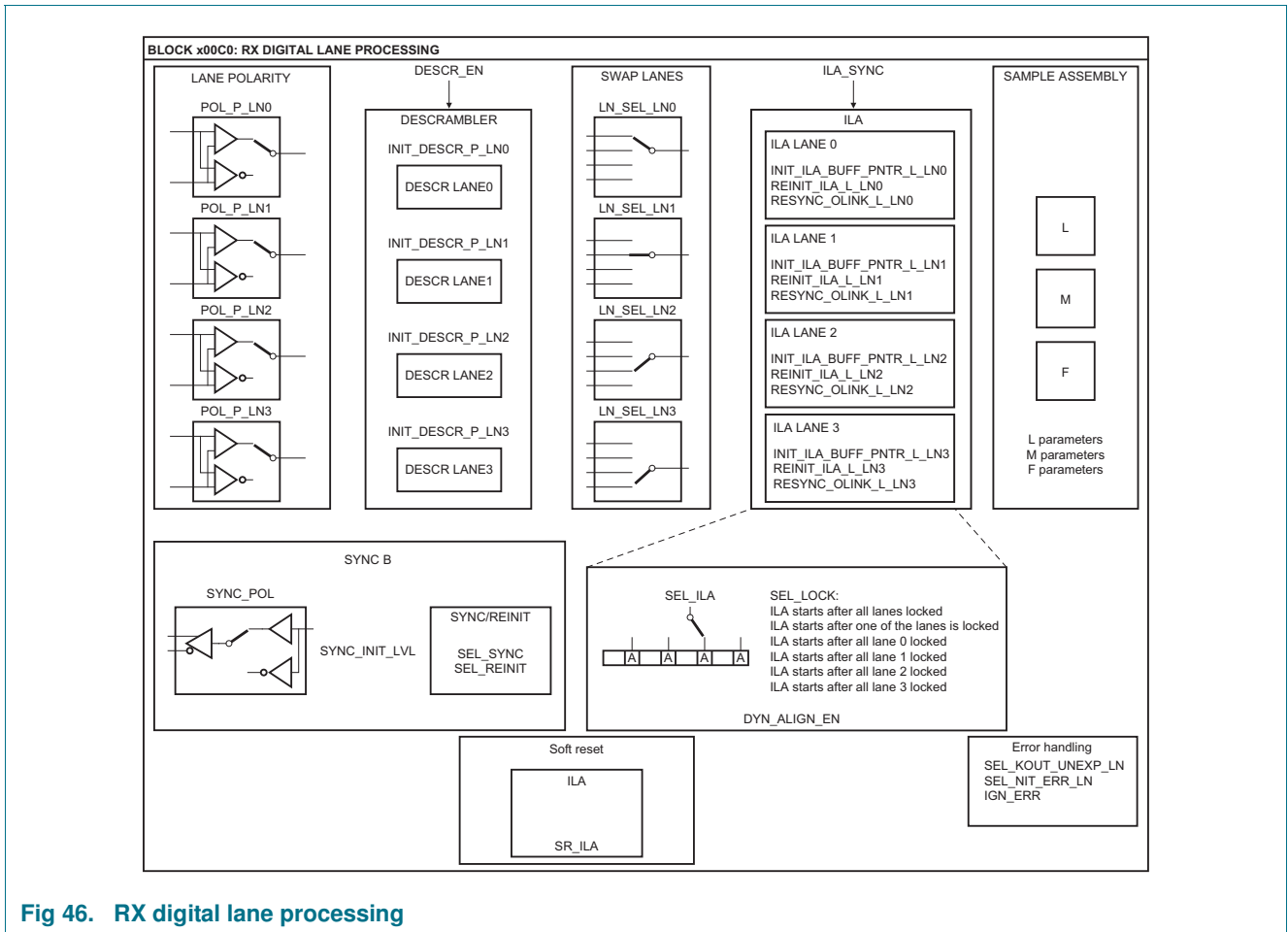


Fig 46. RX digital lane processing

11.7.5.1 Lane polarity

Each physical lane polarity can be individually inverted with the POL\_P\_LNx bits of register P\_LN\_POL (see Table 117). Using this feature transforms the 10 bits from ABCDEFGHIJ to ABCDEFGHIJ.

11.7.5.2 Lane clocking edge

Each physical lane can be sampled either by the rising edge or the falling edge of the internal clocking system. This is accomplished by asserting/deasserting the SEL\_RF\_F10\_P\_LNx bits of register CA\_CTRL (see Table 112).

### 11.7.5.3 Scrambling

The descrambler is a 16-bit parallel self-synchronous descrambler based on the polynomial  $1 + x^{14} + x^{15}$ . From the JESD204B specification, the scrambling/descrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence. After two received bytes, the descrambler is correctly set up to decode the data in the proper way. However, if the initial state of the descrambler bits is set incorrectly, the two first decoded bytes are decoded incorrectly. The JESD204B specification proposes an initial state for both scrambler and descrambler to avoid this.

Using registers INIT\_DESCR\_P\_LNx (see [Table 119](#)) any kind of initial state can be set in the DAC165xD. The descrambling process starts when the ILA sequence has finished. This process can be turned off by deasserting bit DESCR\_EN in register ILA\_CTRL\_1 (see [Table 113](#)).

The first samples cannot be sent to the DSP using the FORCE\_1ST\_SAMP bits of register SR\_SCR. This avoids the use of the two incorrectly decoded samples.

### 11.7.5.4 Lane swapping and selection

If the physical lanes do not match with the ordering of the transmitter lanes, they can be reordered using the lane swapping module. As the DAC165xD allows various LMF configurations (see [Table 123](#)), it is important that the lane swapping respects the following reordering constraints linked to the L value (see [Table 28](#)).

**Table 28. Logical lanes versus L values**

L value		Logical lanes used for the Sample assembly module
Binary	Decimal	
100	4	logical lane 0 logical lane 1 logical lane 2 logical lane 3
010	2	logical lane 0 logical lane 2
001	1	logical lane 0

The selection of the logical lanes can be specified by the LN\_SEL\_L\_LNx bits of register LN\_SEL (see [Table 118](#)).

[Table 29](#) shows the possible choices regarding the value of the L parameter.

**Table 29. Lane mapping between Logical and Physical lanes regarding the L value**

L	4	2	1
logical lane 0	physical lane 0	physical lane 0	physical lane 0
	or	or	or
	physical lane 1	physical lane 1	physical lane 1
	or	or	or
	physical lane 2	physical lane 2	physical lane 2
logical lane 1	physical lane 0	not used	not used
	or		
	physical lane 1		
	or		
	physical lane 2		
logical lane 2	physical lane 0	physical lane 0	not used
	or	or	
	physical lane 1	physical lane 1	
	or	or	
	physical lane 2	physical lane 2	
logical lane 3	physical lane 0	not used	not used
	or		
	physical lane 1		
	or		
	physical lane 2		

#### 11.7.5.5 Word locking and Code Group Synchronization (CGS)

When the bits are received from the RX physical layer, DLP has to identify the MSB and LSB boundaries of the 10-bit codes from the bitstream. This can be monitored using the LOCK\_CNT\_MON\_P\_LN01 and LOCK\_CNT\_MON\_P\_LN23 registers (see [Table 131](#)).

When all lanes are locked, the values of the registers are stable and the code group synchronization process can start. This process is described by the JESD204B specification and is represented by the state machine shown in [Figure 47](#).

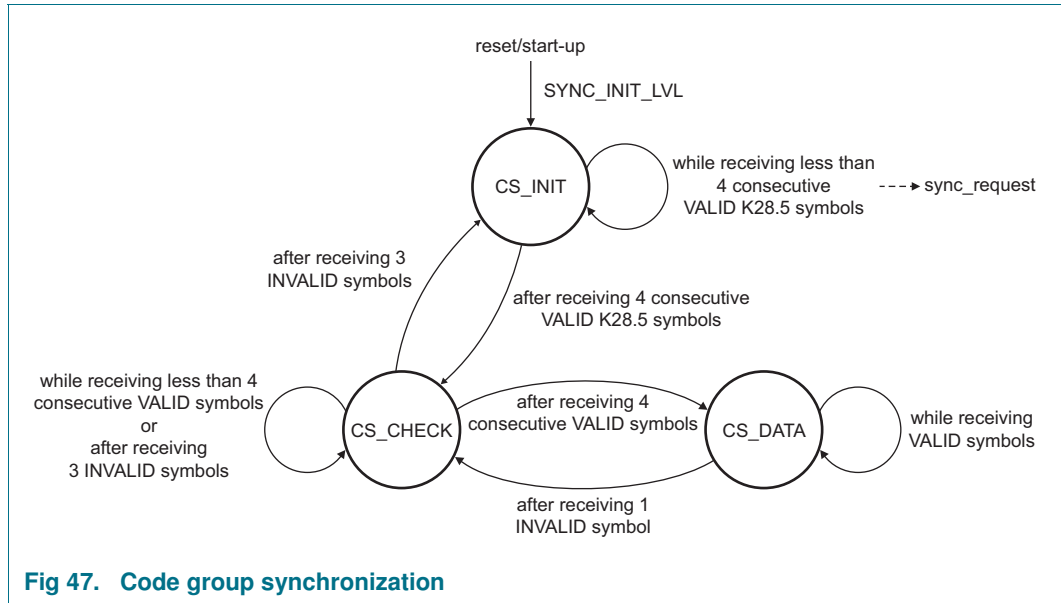


Fig 47. Code group synchronization

The CGS states of each lane can be monitored using the CSYNC\_STATE\_P\_LNx bits of register CSYNC\_STATE\_P\_LNx (see Table 132). The definition of each state can be found in Table 30.

Table 30. Code group synchronization state machine

CSYNC_STATE_P_LNx[1:0]	Name	Definition
00	CSYNC_INIT	looking for K28_5 (/K/) symbol
01	CSYNC_CHECK	four consecutive K28_5 (/K/) symbols have been received
10	CSYNC_DATA	code group synchronization achieved

11.7.5.6 SYNC configuration

The SYNC signal is the feedback signal that is sent to the transmitter device to ensure the JESD204B link synchronization. When all lanes are in CSYNC\_INIT state a sync\_request is sent to the SYNC buffer that is linked to pins SYNC\_OUT\_P and SYNC\_OUT\_N (see Figure 2).

The polarity of this buffer is controlled by bit SYNC\_POL of register SYNC\_OUT\_MOD (see Table 116). By default the synchronization request is active low. The synchronization request signal can be specified by bits SEL\_SYNC and SYNC\_INIT\_LVL of register SYNC\_OUT\_MOD. Bit SYNC\_INIT\_LVL of register SYNC\_OUT\_MOD only specifies the state of the sync\_request signal after resetting the CGS state machine (at start-up time or after device reset only).

Table 31. Sync\_request control

SEL_SYNC[2:0]	Description
000	sync_request active when state machine of one of the lanes is in CS_INIT mode
001	sync_request active when state machine of all lanes is in CS_INIT mode
010	sync_request active when state machine of lane 0 is in CS_INIT mode
011	sync_request active when state machine of lane 1 is in CS_INIT mode

**Table 31. Sync\_request control ...continued**

SEL_SYNC[2:0]	Description
100	sync_request active when state machine of lane 2 is in CS_INIT mode
101	sync_request active when state machine of lane 3 is in CS_INIT mode
110	sync_request fixed to 1
111	sync_request fixed to 0

### 11.7.5.7 Inter-lane alignment

This module handles the alignment of the logical lanes based on the ILA sequence described in the JESD204B specification. Inter-lane alignment starts when all lanes are locked and at reception of the first non-K28.5 (or /K/) symbol.

During the ILA sequence, the K28.3 (/A/ symbol) is used to align the data streams. During this sequence, the length (K) of the multi-frame is measured. This value is used by the lane monitoring and correction process. The value is also used for the MDS circuitry, where the SYSREF signal is expected to be a multiplication of the multi-frame length (K) in the JESD204B specification.

During the second multi-frame, the JESD204B configuration data of each physical lane is stored in register blocks x0120 and x0140 (see [Figure 48](#) and [Figure 49](#)). The DAC165xD does not do anything with these configuration data. They are only made available for the host controller.

BLOCK x0120: JESD204 READ CONFIGURATION				
LANE 0 JESD204 CONFIGURATION			LANE 1 JESD204 CONFIGURATION	
CONFIG 0	P_LN0_DID		CONFIG 0	P_LN1_DID
CONFIG 1	P_LN0_AD_JCNT	P_LN0_BID	CONFIG 1	P_LN1_ADJ_CNT
CONFIG 2	P_LN0_ADJ_DIR	P_LN0_LID	CONFIG 2	P_LN1_ADJ_DIR
	P_LN0_ADJ_PH			P_LN1_ADJ_PH
CONFIG 3	P_LN0_SCR	P_LN0_L	CONFIG 3	P_LN1_SCR
CONFIG 4	P_LN0_F		CONFIG 4	P_LN1_F
CONFIG 5		P_LN0_K	CONFIG 5	P_LN1_K
CONFIG 6	P_LN0_M		CONFIG 6	P_LN1_M
CONFIG 7	P_LN0_CS	P_LN0_N	CONFIG 7	P_LN1_CS
CONFIG 8	P_LN0_SBC_LSS_VS	P_LN0_N'	CONFIG 8	P_LN1_SBC_LSS_VS
CONFIG 9	P_LN0_JESD_VS	P_LN0_S	CONFIG 9	P_LN1_JESD_VS
CONFIG 10	P_LN0_HD	P_LN0_CF	CONFIG 10	P_LN1_HD
CONFIG 11	P_LN0_RES1		CONFIG 11	P_LN1_RES1
CONFIG 12	P_LN0_RES2		CONFIG 12	P_LN1_RES2
CONFIG 13	P_LN0_FCHK		CONFIG 13	P_LN1_FCHK

**Fig 48. JESD204 read configuration for physical lanes 0 and 1**

BLOCK x0140: JESD204 READ CONFIGURATION					
LANE 2 JESD204 CONFIGURATION			LANE 3 JESD204 CONFIGURATION		
CONFIG 0	P_LN2_DID		CONFIG 0	P_LN3_DID	
CONFIG 1	P_LN2_ADJ_CNT	P_LN2_BID	CONFIG 1	P_LN3_ADJ_CNT	P_LN3_BID
CONFIG 2	P_LN2_ADJ_DIR P_LN2_ADJ_PH	P_LN2_LID	CONFIG 2	P_LN3_ADJ_DIR P_LN3_ADJ_PH	P_LN3_LID
CONFIG 3	P_LN2_SCR	P_LN2_L	CONFIG 3	P_LN3_SCR	P_LN3_L
CONFIG 4	P_LN2_F		CONFIG 4	P_LN3_F	
CONFIG 5		P_LN2_K	CONFIG 5		P_LN3_K
CONFIG 6	P_LN2_M		CONFIG 6	P_LN3_M	
CONFIG 7	P_LN2_CS	P_LN2_N	CONFIG 7	P_LN3_CS	P_LN3_N
CONFIG 8	P_LN2_SBCLSS_VS	P_LN2_N'	CONFIG 8	P_LN3_SBCLSS_VS	P_LN3_N
CONFIG 9	P_LN2_JESD_VS	P_LN2_S	CONFIG 9	P_LN3_JESD_VS	P_LN3_S
CONFIG 10	P_LN2_HD	P_LN2_CF	CONFIG 10	P_LN3_HD	P_LN3_CF
CONFIG 11	P_LN2_RES1		CONFIG 11	P_LN3_RES1	
CONFIG 12	P_LN2_RES2		CONFIG 12	P_LN3_RES2	
CONFIG 13	P_LN2_FCHK		CONFIG 13	P_LN3_FCHK	

Fig 49. JESD204 read configuration for physical lanes 2 and 3

The inter-lane alignment synchronization is enabled by default, but it can be disabled using bit ILA\_SYNC of register ILA\_CTRL\_1 register (see [Table 113](#)). When ILA is disabled, the lane-alignment can be done manually using registers MAN\_ALIGN\_P\_LN10 and MAN\_ALIGN\_P\_LN32 (see [Table 115](#)). The manual mode must first be enabled using bit FORCE\_ALIGN of register FORCE\_ALIGN (see [Table 114](#)).

The ILA module uses a 16-bit buffer for each lane. The first /A/ symbol received over the lanes is used as reference. The /A/ symbols of the other lanes, which are received later, are compared to the first one to be all aligned. The initial location of the symbols is predefined by the INIT\_ILA\_BUFF\_PNTR\_L\_LNxy registers (see [Table 119](#)). The alignment can be monitored with the ILA\_MON\_L\_LNxy bits of register ILA\_MON (see [Table 125](#)). If the lane difference is too great, a buffer out-of-range error occurs, which can be monitored with bits ILA\_BUFF\_ERR\_L\_LNx of register ILA\_BUFF\_ERR (see [Table 126](#)). In this specific case, a reinitialization of the full link can be requested by setting the REINIT\_ILA\_L\_LNx bits of register REINIT\_CTRL (see [Table 121](#)).

The JESD204B specification also mentions a dynamic realignment mode where a monitoring process is checking the /A/-symbol location. This can realign the data stream if two successive /A/ symbols are found at the same new position. By default this monitoring and correction process is disabled to avoid any moving latency over the link, but one can enable the feature by setting the DYN\_ALIGN\_EN bit of register FORCE\_ALIGN (see [Table 114](#)).

11.7.5.8 Character replacement

Character replacement, as specified by the JESD204B specification, can occur at the end of the frame (K28.7 or /F/ symbol) or at the end of the multi-frame (K28.3 or /A/ symbol). By default this feature is enabled, but it can be disabled using bit FRAME\_ALIGN\_EN of the ILA\_CTRL\_0 register (see [Table 111](#)).

**Remark:** The DAC165xD can handle multi-frame length values (K) between  $\text{ceil}(17 / F)$  and 32 but with the restriction that the number of octets in a multi-frame must always be even. This implies that if  $F = 1$ , a value of  $K = 17$  is not allowed. When  $F = 1$  only even values  $> 17$  are allowed. Working with  $F = 1$  and  $K = 17$  often implies that the character replacement process is not reliable.

#### 11.7.5.9 Sample assembly

Sample assembly handles the assembly of the data based on the LMF parameters described by register LMF\_CTRL (see [Table 123](#)). The following configurations are supported:

- LMF = 421
- LMF = 422
- LMF = 222
- LMF = 124

Sample assembly is based on the logical lanes definition when updating the L value.

#### 11.7.5.10 Resynchronization over links

The DAC165xD recognizes a K28.5 (/K/) symbols sequence coming over its lanes. This identification allows resynchronization of the device if the RESYNC\_OLINK\_P\_LNx bits of register REINIT\_CTRL are set correctly (see [Table 121](#)).

#### 11.7.5.11 Symbols detection monitoring and error handling

The DLP decodes the 10-bit words to 8-bit words. The decoding table is specified in the IEEE 802.3-2005 specification. During decoding, the disparity is calculated according to the disparity rules mentioned in the same specification. The JESD204B specification also defines the following definitions:

- VALID:  
The code group is found in the column of the 10b/8b decoding tables according to the current running disparity.
- DISPARITY ERROR:  
The received code group exists in the 10b/8b decoding table, but is not found in the correct column according to the current running disparity.
- NOT-IN-TABLE (NIT) ERROR:  
The received code group is not found in the 10b/8b decoding table of either disparity.
- INVALID:  
A code group that either shows a disparity error or that does not exist in the 10b/8b decoding table.

**Remark:** The 8b/10b decoder only provides reliable information in the CSYNC\_CHK and CSYNC\_DATA states. During CSYNC\_INIT state, the DLP is "hunting" for the correct position of the K28.5 (/K/) symbols in the received bitstream. Therefore the DISPARITY ERROR/NOT-IN-TABLE/ INVALID flags are not yet consistent and are not be used in the internal monitoring.

The Not-In-Table error (NIT) and Disparity error (DISP) can be monitored using the DEC\_NIT\_ERR\_P\_LNx and DEC\_DISP\_ERR\_P\_LNx bits of register DEC\_FLAGS (see [Table 127](#)). Both are considered invalid, but the DAC165xD has some flexibility in this definition. The specified invalid errors can also be totally ignored by setting the bit IGN\_ERR of register ERR\_HNDLNG to logic 1 (see [Table 120](#)). This specific mode is designed for debug purposes only, especially when sample error measurement needs to be executed.

The VALID/INVALID status of the decoded word can trigger the MUTE feature using the DATA\_V\_IQ\_CFG bits of register MUTE\_CTRL\_1 (see [Table 72](#); see [Section 11.2.3.10](#)).

The following comma symbols are detected during data transmission irrespective of the running disparity:

/K/ = K28.5

/F/ = K28.7

/A/ = K28.3

/R/ = K28.0

/Q/ = K28.4

Their single detection is monitored in registers KOUT\_FLAG (see [Table 128](#)) and K28\_FLAG (see [Table 129](#)).

During the data transmission phase, only K28.3 (/A/) and K28.7 (/F/) symbols are expected. Sometimes (e.g. wrong bit transmission), a code group is interpreted as a K character that is not K28.3 or K28.7. If this occurs a KOUT\_UNEXP flag is asserted that can be read using the DEC\_KOUT\_UNEXP\_L\_LNx bits of register KOUT\_UNEXP\_FLAG (see [Table 130](#)).

All the previous flags can be reset using the RST\_FLAGS\_MON register (see [Table 139](#)). Detection of them can also assert the DLP interrupt (see [Section 11.7.3](#)).

## 11.7.6 Monitoring and test modes

The DAC165xD embeds various monitoring and test modes that are useful during the prototyping phase of a system.

**Remark:** The test capability linked to observing specific characters, errors or state machine statuses is not reviewed in this section. It is up to the reader to define specific modes based on the DAC165xD capability.

### 11.7.6.1 Flag counters

Due to the high data rate of the JESD204B serial interface, it is hard to monitor events that occur on the lanes in real time. Four multi-purpose counters have been added to the design to help this monitoring. Each counter is 16 bits wide and is linked to one lane. It increments its value each time a specific event occurs. These flags counters can be read using the FLAG\_CNT\_LNx registers (see [Table 135](#)) and reset using the RST\_CTRL\_FLAG\_CNT\_LNxx bits of the CTRL\_FLAG\_CNT\_LNxx registers (see [Table 138](#)). The flag counters can also be reset automatically when DLP is reset by setting the AUTO\_RST\_FLAG\_CNTRS bit of register RST\_BUF\_ERR\_FLAGS (see [Table 133](#)) to logic 1.

The specification of the event that increments the counter is done by setting the SEL\_CTRL\_FLAG\_CNT\_LNxx bits of the CTRL\_FLAG\_CNT\_LNxx registers (see [Table 138](#)) to one of the sources described in [Table 32](#).

**Table 32. Counter source**

*Default settings are shown highlighted.*

SEL_CTRL_FLAG_CNT_LNxx[2:0]	Source
000	not-in-table error
001	disparity error
010	K symbol not found
011	unexpected K symbol found
100	K28_7 (/F) symbol found
<b>101</b>	<b>K28_5 (/K) symbol found</b>
110	K28_3 (/A) symbol found
111	K28_0 (/R) symbol found

When the counter is reaching its maximum value (0xFFFF), this value is held until the next counter reset. Bit HOLD\_FLAG\_CNT\_EN of RST\_BUFF\_ERR\_FLAGS register (see [Table 133](#)) gives two options for when a counter reaches the maximum value.

**Table 33. HOLD\_FLAG\_CNT\_EN options**

*Default settings are shown highlighted.*

HOLD_FLAG_CNT_EN	Option
<b>0</b>	<b>All counters are independent. Each counter continues its own counting.</b>
1	All counters are linked. When one counter reached the maximum value and stops, all other counters stop as well.

When the counters are stopped, an interrupt can be activated (see [Section 11.7.3](#)).

This feature makes it possible to, for instance, analyze the occurrence of character replacement or NIT errors.

#### 11.7.6.2 Sample Error Rate (SER)

A sample error rate feature is implemented in the DAC165xD to analyze the quality of the transmission. Due to the 8b10b encoding, the analysis is done at sample level only and not at bit level. The transmitter sends a constant data over the link and the DAC165xD compared this received value to the value specified in the SER\_LVL\_LSB and SER\_LVL\_MSB registers (see [Table 136](#)). Enable the scrambling on both transmitter and receiver side to add more random effect on the data. The SER\_LVL\_MSB and SER\_LVL\_LSB are specifying a 16-bit value at the lane level, it means the device can be considered as operating in one of two modes:

- F = 2 mode:  
The lane is receiving 16-bit data specified by SER\_LVL\_MSB and SER\_LVL\_LSB.
- F = 1 mode:  
The lane is receiving alternately 8-bit data specified by SER\_LVL\_MSB and SER\_LVL\_LSB.

The SER mode requires that the DAC is already synchronized (using CGS and ILA sequence). The kick-off of the measurement is done by setting the SER\_MOD bit of register SER\_INTR\_CTRL (see [Table 140](#)). In this mode, the flags counters are used to count the number of 16-bit samples that do not match the SER\_LVL value. This mode enables the establishing of the sample error rate of each lane.

### 11.7.6.3 JTSPAT test

The Jitter Tolerance Scrambled PATtern (JTSPAT) is an 1180-bit pattern intended for receiving jitter tolerance testing for scrambled systems. The JTSPAT test pattern consists of two copies of JSPAT and an additional 18 characters intended to cause extreme late and early phases in the CDR PLL followed by a sequence, which can cause an error (i.e. an isolated bit following a long run). This pattern was developed to stress the receiver within the boundary conditions established by scrambling.

**Table 34. Jitter tolerance scrambled pattern symbols sequence [\[1\]](#)**

D1.4 0111010010	D16.2 0110110101	D24.7 0011001110	D30.4 1000011101	D9.6 1001010110	D10.5 0101011010
D16.2 1001000101	D7.7 1110001110	D24.0 0011001011	D13.3 1011000011	D23.4 0001011101	D13.2 1011000101
D13.7 1011001000	D1.4 0111010010	D7.6 1110000110	D0.2 1001110101	D21.5 1010101010	D22.1 0110101001
D23.4 0001011101	D20.0 0010110100	D27.1 1101101001	D30.7 1000011110	D17.7 1000110001	D4.3 1101010011
D6.6 0110010110	D23.5 0001011010	D7.3 1110001100	D19.3 1100101100	D27.5 110101010	D19.3 1100100011
D5.3 1010010011	D22.1 0110101001	D5.0 1010010100	D15.5 0101111010	D24.7 0011001110	D16.3 1001001100
D1.2 0111010101	D23.5 0001011010	D29.2 1011100101	D31.1 0101001001	D10.4 0101011101	D4.2 0010100101
D5.5 1010011010	D10.2 0101010101	D21.5 1010101010	D10.2 0101010101	D21.5 1010101010	D20.7 0010110111
D11.7 1101001000	D20.7 0010110111	D18.7 0100110001	D29.0 1011100100	D16.6 0110110110	D25.3 1001100011
D1.0 1000101011	D18.1 0100111001	D30.5 1000011010	D5.2 1010010101	D21.6 1010100110	D1.4 0111010010
D16.2 0110110101	D24.7 0011001110	D30.4 1000011101	D9.6 1001010110	D10.5 0101011010	D16.2 1001000101
D7.7 1110001110	D24.0 0011001011	D13.3 1011000011	D23.4 001011101	D13.2 1011000101	D13.7 1011001000
D1.4 0111010010	D7.6 1110000110	D0.2 1001110101	D21.5 1010101010	D22.1 0110101001	D23.4 0001011101
D20.0 0010110100	D27.1 1101101001	D30.7 1000011110	D17.7 1000110001	D4.3 1101010011	D6.6 0110010110
D23.5 0001011010	D7.3 1110001100	D19.3 1100101100	D27.5 1101101010	D19.3 1100100011	D5.3 1010010011

**Table 34. Jitter tolerance scrambled pattern symbols sequence ...continued<sup>[1]</sup>**

D22.1 0110101001	D5.0 1010010100	D15.5 0101111010	D24.7 0011001110	D16.3 1001001100	D1.2 0111010101
D23.5 0001011010	D27.3 1101100011	D3.0 1100010100	D3.7 1100011110	D14.7 0111001000	D28.3 0011101100
D30.3 0111100011	D30.3 1000011100	D7.7 1110001110	D7.7 0001110001	D20.7 0010110111	D11.7 1101001000
D20.7 0010110111	D8.7 0100110001	D29.0 1011100100	D16.6 0110110110	D25.3 1001100011	D1.0 1000101011
D18.1 0100111001	D30.5 1000011010	D5.2 1010010101	D21.6 1010100110		

[1] This table must be read, starting from the top, left-to-right first and then line-by-line to follow the sequence.

The DAC165xD embeds a JTSPAT checker. The control registers are located in the JESD204 receiver monitoring registers block (see [Table 141](#)).

#### 11.7.6.4 DLP strobe

The data coming out of the ILA module can be sampled by setting the DLP\_STROBE bit of register MISC\_CTRL (see [Table 122](#)). On each lane two octets are stored, which can be read out through registers P\_LNxx\_SMPL\_MSB and P\_LNxx\_SMPL\_LSB (see [Table 153](#) and [Table 155](#)). The selection of the lane to read out the data is done by registers P\_LN10\_SEL and P\_LN32\_SEL (see [Table 154](#) and [Table 156](#)).

#### 11.7.7 IO-mux

The DAC165xD uses two general purpose pins, IO0 and IO1. IO0 is always an output. IO1 can be configured as an input or as an output by setting the IO\_EN bit of register EHS\_CTRL (see [Table 55](#)).

When acting as an input, the IO1 pin is referred as the RF enable feature (see [Section 11.2.5](#)).

When acting as an output, the two IO pins are multiplexed to internal signals that can be useful for debug purposes. [Table 35](#) shows the main configuration when using registers bit IO\_SEL\_x in register IO\_MUX\_CTRL\_x. The definitions of the three registers depend on the "Indicator" and the "Range" values used to specify the signal that is sent through pins IO0 and IO1 (see [Table 35](#) and [Table 36](#)).

**Table 35. Definition of IO\_SEL registers**

Register name	b7	b6	b5	b4	b3	b2	b1	b0
IO_SEL_2	IO1 indicator[1:0]	x	x	x	IO0 indicator[1:0]	x	x	x
IO_SEL_1				IO1 range[7:0]				
IO_SEL_0				IO0 range[7:0]				

**Table 36. Output signals for combination of indicators and ranges**

Indicator[1:0]	Range[7:0]	Output signal
00	xxxx xxx0	IO0: WCLK IO1: DCLK
00	xxxx 0011	synchronization request
10	1111 0000	end of ILA
10	1111 0001	end of ILA
11	1100 0000	interrupt
11	1100 0001	interrupt
11	1111 even	IO0: fixed to logic 1 IO1: fixed to logic 0
11	1111 odd	IO0: fixed to logic 0 IO1: fixed to logic 1

### 11.7.8 DLP latency

The variable delay (latency uncertainty) is the result of uncertainties and variation in design implementations along the path between the transmit logic device and the DAC165xD. The Inter-Lane Alignment (ILA) module present in Digital Layer Processing (DLP) realigns the input streams to the last data received.

**Table 37. Digital layer processing latency**

Symbol	Parameter	Conditions	Test <sup>[1]</sup>	Min	Typ	Max	Unit
$t_d$	delay time	digital layer processing delay	D	11	-	26	cycles <sup>[2]</sup>

[1] D = guaranteed by design.

[2] WCLK clock cycle.

## 11.8 JESD204B PHY receiver

Each JESD204B lane owns its own physical deserializer (RX PHY) that provides the 10-bit data stream to the DLP module. The SPI registers of block x0160 control the various features of the RX PHY, like the equalizer, the common-mode voltage and the resistor termination. The registers of x0180 monitor the status of these controls.

**Remark:** Most of the main controls (power on/off, PLL clock dividers, etc.) are automatically set while specifying the LMF mode (see [Section 11.7.5.9](#)) and/or by the MAIN\_CTRL register (see [Table 51](#)).

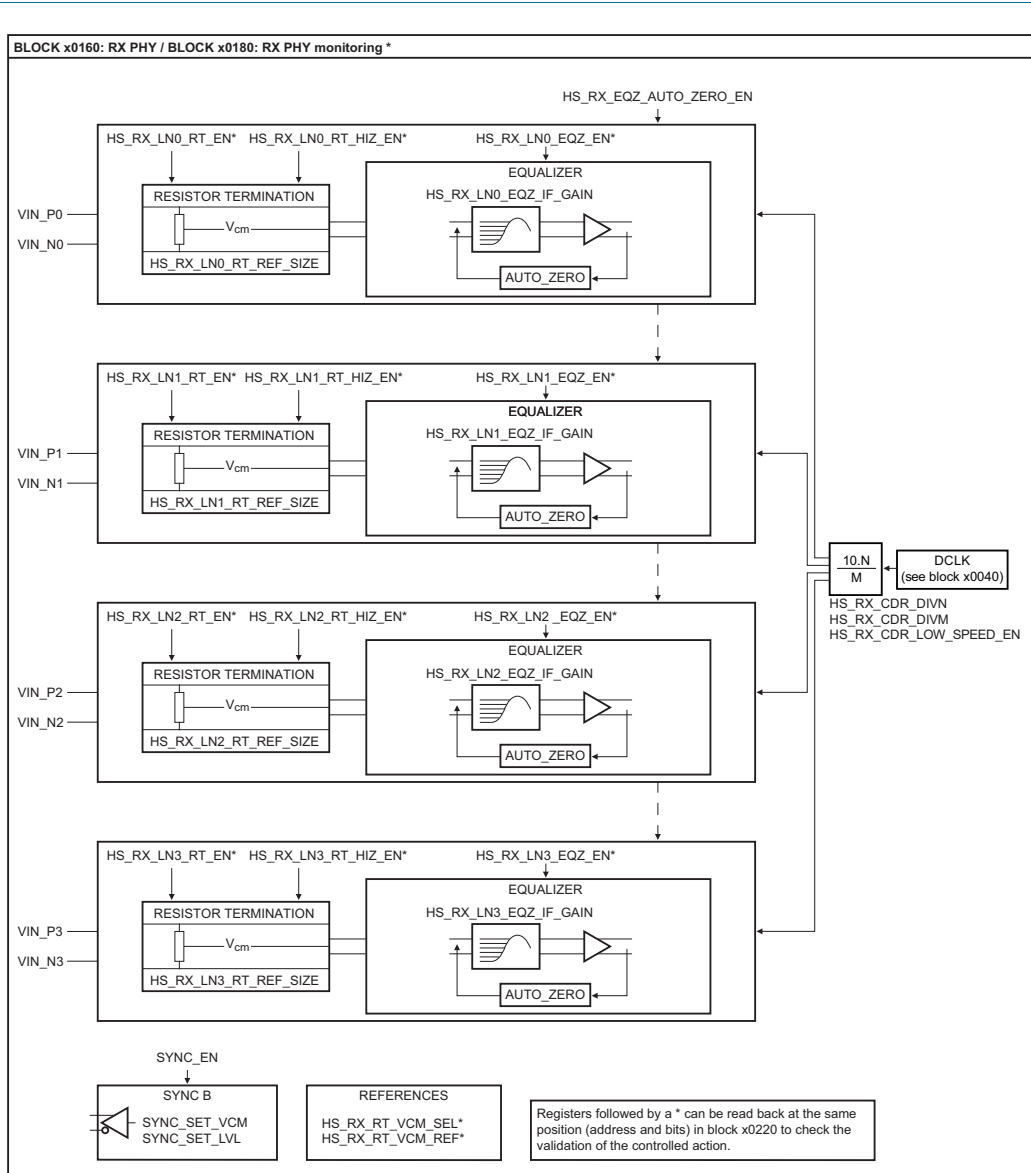


Fig 50. RX PHY control overview

### 11.8.1 Lane input

Each lane is Current Mode Logic (CML) compliant.

The common-mode voltage and the termination resistor can be programmed using register  $HS\_RX\_RT\_VCM$  (see Table 163) and registers  $HS\_RX\_x\_RT\_REF\_SIZE$  (see Table 165 and Table 166). When not used, the lane input buffer can be set to a high impedance mode (register  $HS\_RX\_RT\_CTRL$ ; see Table 164).

AC-coupling is always required (see Figure 51).

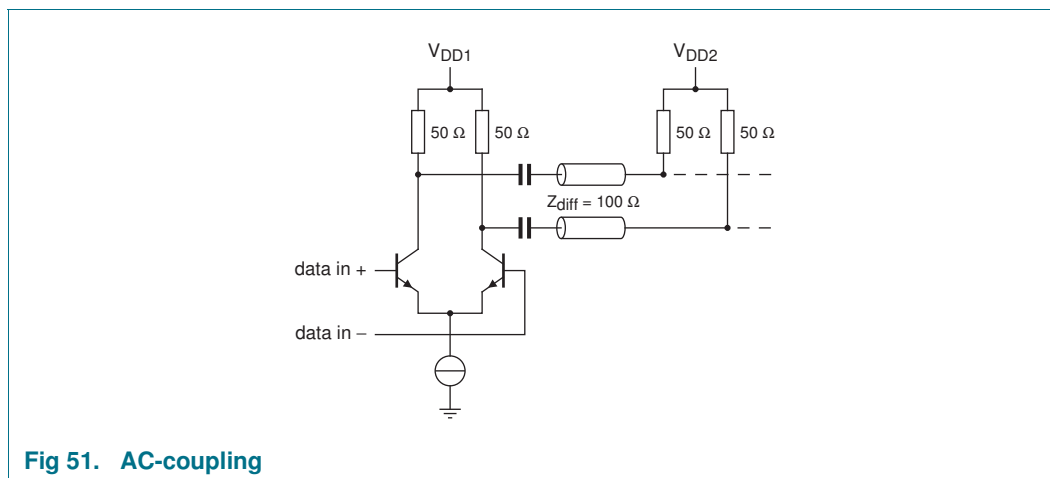


Fig 51. AC-coupling

### 11.8.2 Equalizer

The DAC165xD embeds an internal equalizer (bits HS\_RX\_LNx\_EQZ\_EN in register HS\_RX\_EQZ\_CTRL; see [Table 171](#)) in each high-speed serial lane. This improves the interference robustness between signals by amplifying the high-frequency jumps in the data conserving the energy of the low-frequencies ones. The equalizer can be programmed depending on the quality of the channel used (PCB traces/layout, connectors, etc.).

The auto-zero feature (bit HS\_RX\_EQZ\_AUTO\_ZERO\_EN in register HS\_RX\_EQZ\_CTRL; see [Table 160](#)) is enabled by default for the deserializer to adapt itself to the common-mode of the received signal. This feature can be set manually. It uses an external algorithm that controls the DAC165xD via the SPI bus.

Set the equalizer gains to control the high-frequency and low-frequency jumps of the data (bits HS\_RX\_0\_EQZ\_IF\_GAIN[2:0] of register HS\_RX\_LNx\_EQZ\_GAIN; see [Table 161](#)).

### 11.8.3 Deserializer

The deserializer performs the incoming data clock recovery and also the serial-to-parallel conversion. One global PLL provides the same reference clock to the four lanes. The PLL configuration is automatically done when specifying the LMF parameters (see [Table 10](#)).

When using the DAC165xD with a low serial input data rate (lower than 1.5 Gbps), it is recommended to enable the low speed mode of the Clock Data Recovery (CDR) unit by writing x84 in register HS\_RX\_CDR\_DIVX (see [Table 158](#)).

### 11.8.4 PHY test mode

A special test mode is available for measurement purposes only. The recovered clock of each CDR unit can be transmitted to the SYNC buffer after a frequency division by 20. This is done by setting the SYNC\_TST\_DATA\_EN bit of register SYNC\_SEL\_CTRL to logic 1 (see [Table 168](#)). Bit SYNC\_TST\_DATA\_SEL[1:0] is used to specify which CDR clock is used.

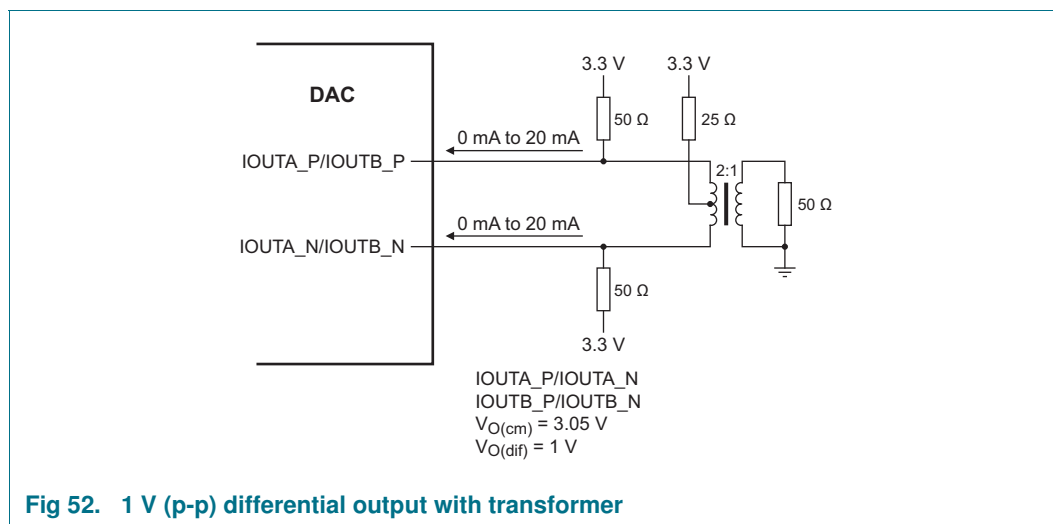
**11.9 Output interfacing configuration**

**11.9.1 DAC1658D: High common-mode output voltage**

**11.9.1.1 Basic output configuration**

Using a differentially coupled transformer output provides optimum distortion performance. In addition, it helps to match the impedance and provides electrical isolation.

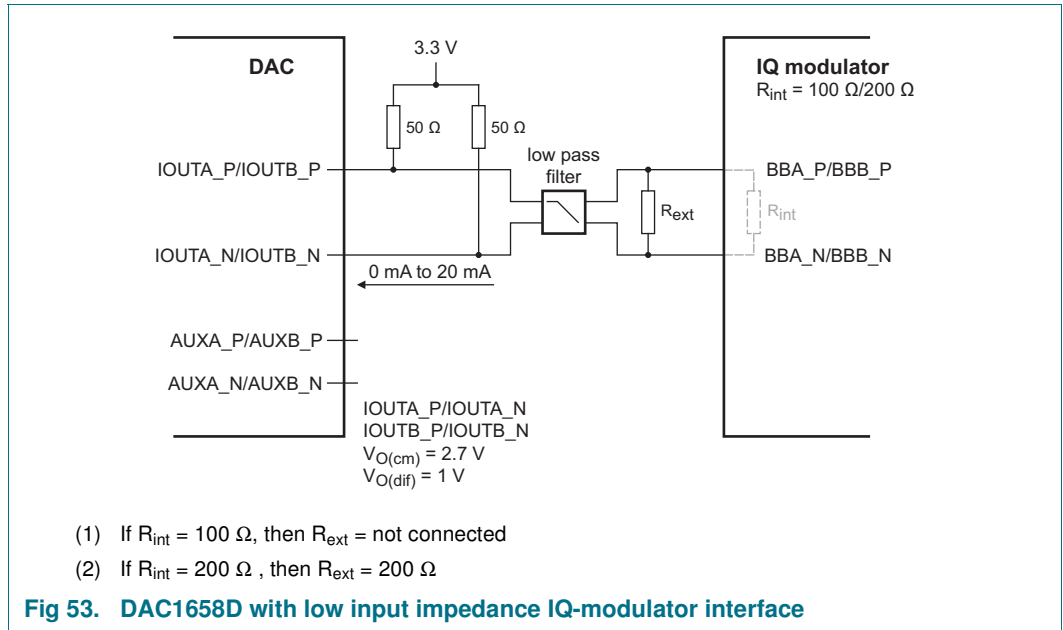
The DAC1658D can generate a differential output of 1 V (p-p). In this configuration, connect the center tap of the transformer to a 25 Ω resistor, which is connected to the 3.3 V analog power supply. This adjusts the DC common-mode to around 3.05 V (see [Figure 52](#)).



**11.9.1.2 Low input impedance IQ-modulator interface**

The DAC1658D can be easily connected to low input impedance IQ-modulators. The image of the local oscillator can be canceled using the digital offset control in the device.

[Figure 53](#) shows an example of a connection between the DAC1658D and a low input impedance modulator.



### 11.9.1.3 IQ-modulator - DC interface

When the system operation requires to keep the DC component of the spectrum, the DAC1658D can use a DC interface to connect an IQ-modulator. In this case, the image of the local oscillator can be canceled using the digital offset control in the device.

Figure 54 shows an example of a connection to an IQ modulator with a 1.7 V common input level.

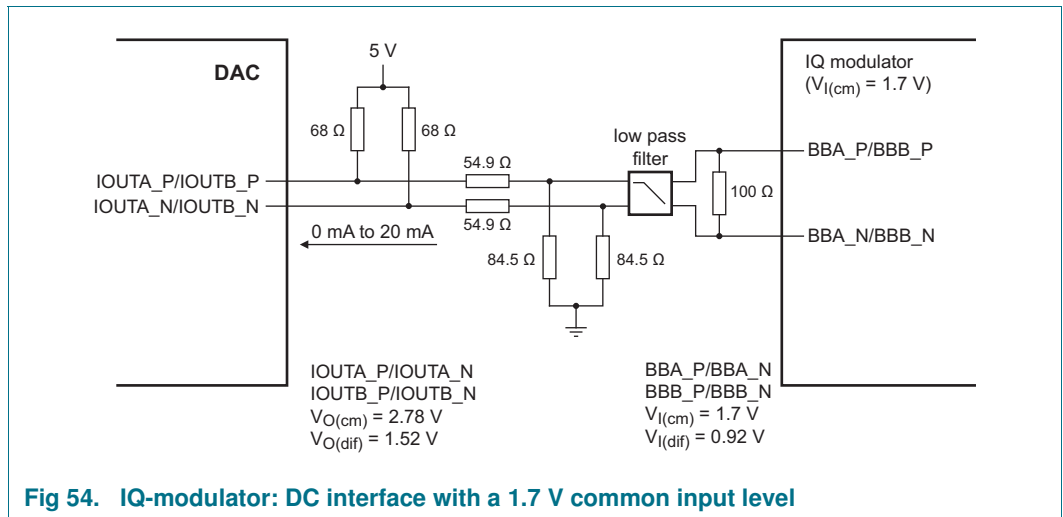
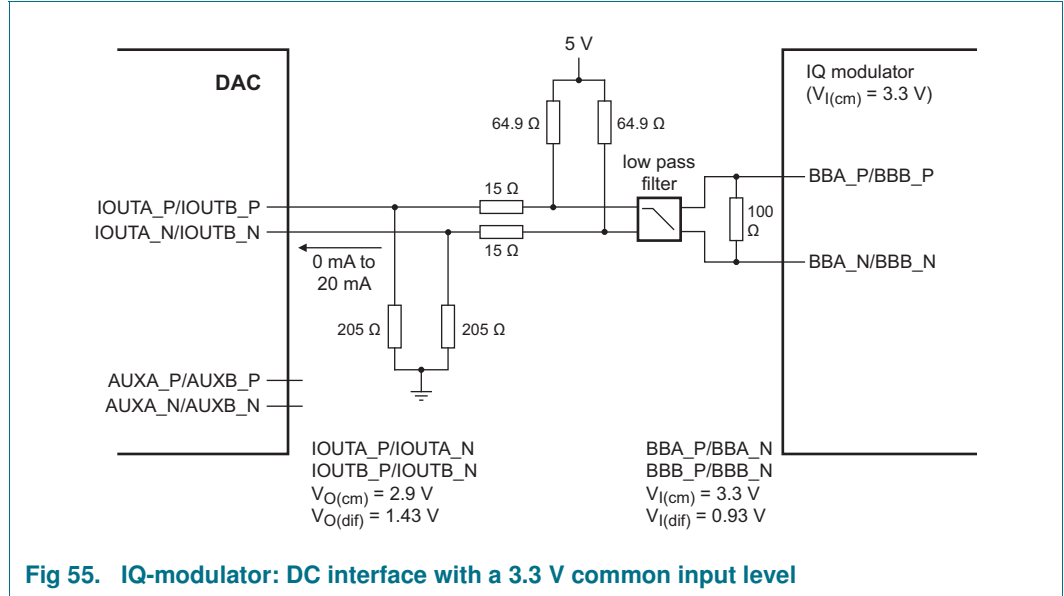
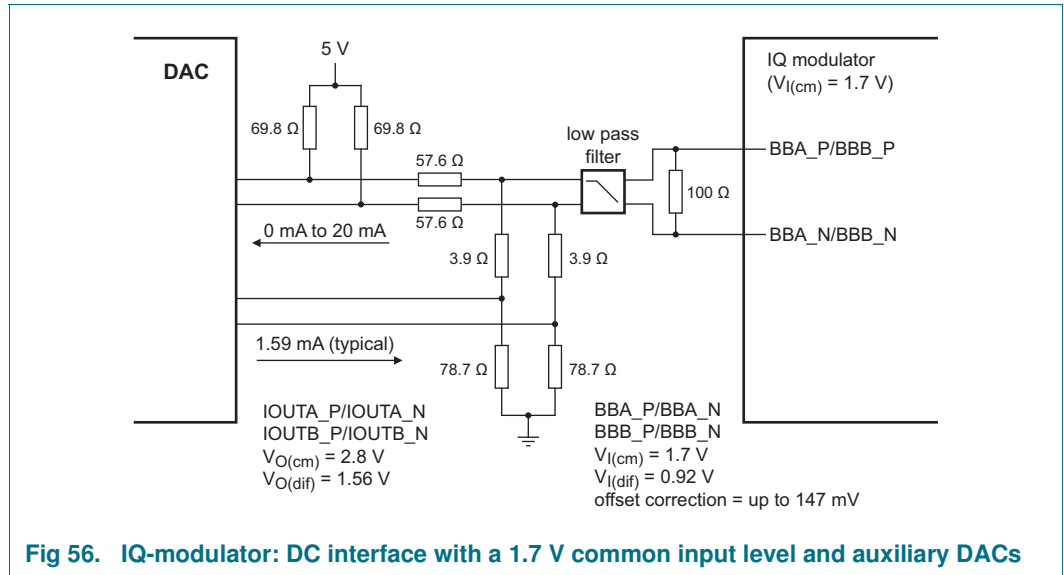


Figure 55 shows an example of a connection to an IQ-modulator with a 3.3 V common input level.



The auxiliary DACs can be used to control the offset within an accurate range or with accurate steps.

Figure 56 shows an example of a connection to an IQ-modulator with a 1.7 V common input level and auxiliary DACs.



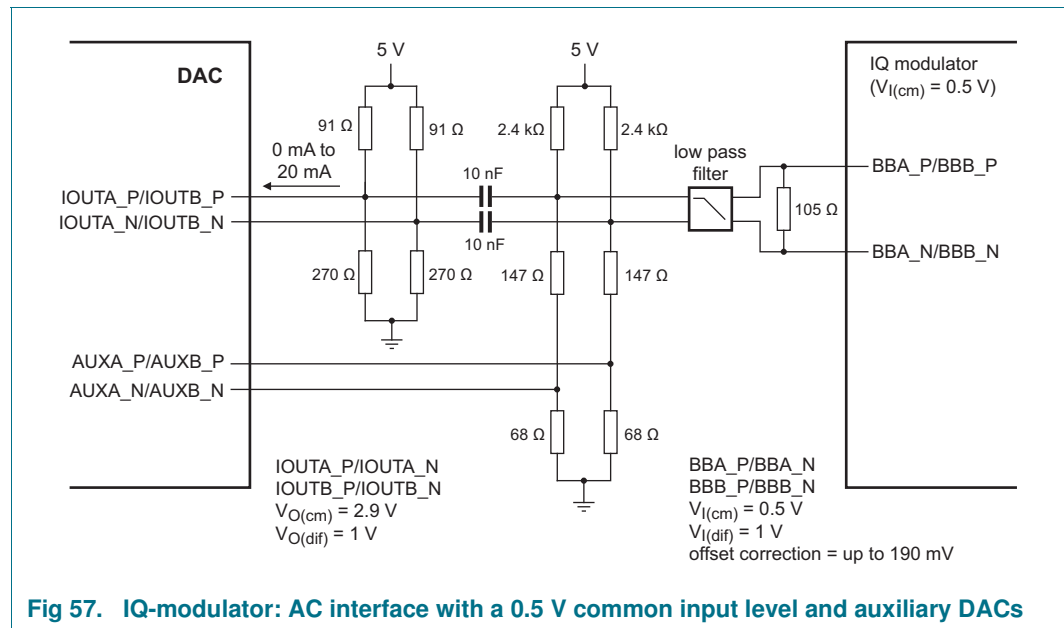
The constraints to adjust the interface are:

- The output compliance range of the DAC
- The output compliance range of the auxiliary DACs
- The input common-mode level of the IQ-modulator
- The range of offset correction

### 11.9.1.4 IQ-modulator - AC interface

Use the DAC1658D AC-coupled when the IQ-modulator common-mode voltage is close to ground. The auxiliary DACs are required for local oscillator cancelation.

Figure 57 shows an example of a connection to an IQ-modulator with a 0.5 V common input level and auxiliary DACs.



### 11.9.2 DAC1653D: Low common-mode output voltage

#### 11.9.2.1 Basic output configuration

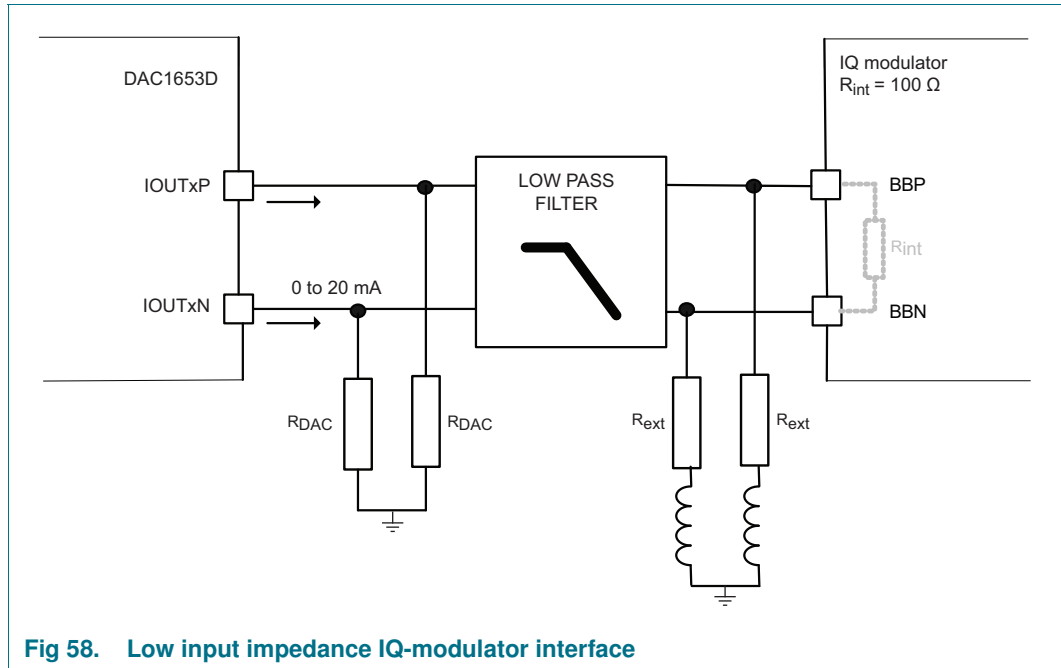
Using a differentially coupled transformer output provides optimum distortion performance. In addition, it helps to match the impedance and provides electrical isolation.

The DAC1653D can generate a differential output of 1 V (p-p). In this configuration, connect the center tap of the transformer to a 25 Ω resistor, which is connected to the GND. This adjusts the DC common-mode to around 0.25 V (see Figure 52).

#### 11.9.2.2 Low input impedance IQ-modulator interface

The DAC1653D can be easily connected to low input impedance IQ-modulators. The image of the local oscillator can be canceled using the digital offset control in the device.

Figure 53 shows an example of a connection between the DAC1653D and a low input impedance modulator.

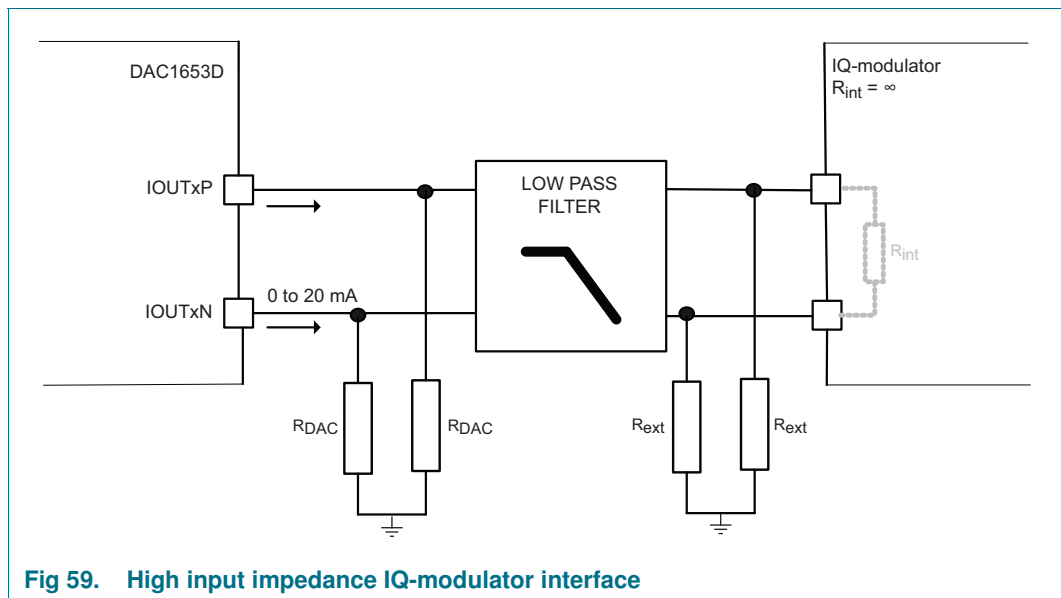


**Fig 58. Low input impedance IQ-modulator interface**

### 11.9.2.3 High input impedance IQ-modulator interface

The DAC1653D can be easily connected to high input impedance IQ-modulators. The image of the local oscillator can be canceled using the digital offset control in the device.

[Figure 59](#) shows an example of a connection between the DAC1653D and a high input impedance modulator.



**Fig 59. High input impedance IQ-modulator interface**

## 11.10 Design recommendations

### 11.10.1 Power and grounding

Use a separate power supply regulator for the generation of the 1.2 V analog power (pins 43, 48, 51, 56) and the 1.2 V digital power (pins 7, 10, 33, 36) to ensure optimal performance.

High-speed input lanes are powered by a 1.2 V power supply that can require a dedicated power supply. Pins 15, 16, 19, 22, 25, 28 can be connected to either the global 1.2 V power supply or to a dedicated one.

Also, include individual LC decoupling for the following six sets of power pins:

- $V_{DDA(1V2)}$  (pins 43, 46, 48, 51, 53 and 56)
- $V_{DDD(1V2)}$  (core: pins 7, 10, 15, 16, 19, 22, 25, 28, 33 and 36)
- $V_{DDA(3V3)}$  (pins 47 and 52)
- $V_{DDD(IO)}$  (pin 29)
- $V_{DDD(DIFF)}$  (pin 11)

Use at least two capacitors for each power pin decoupling. Locate these capacitors as close as possible to the DAC165xD power pins.

Use a separate LDO for the generation of the 1.2 V analog power ( $V_{DDA(1V2)}$ ) and the 1.2 V digital power ( $V_{DDD(1V2)}$ ) to ensure the best performance.

The die pad is used for both the power dissipation and electrical grounding. Insert several vias (typically  $7 \times 7$ ) to connect the internal ground plane to the top layer die area.

## 11.11 Registers

### 11.11.1 SPI configuration block

#### 11.11.1.1 SPI configuration block register allocation map

[Table 38](#) shows an overview all the interface DAC DSP registers.

**Table 38. Interface DAC DSP register allocation map**

Register name	R/W	Bit definition									Default	
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex	
0000h SPI_CFG_A	R/W	SPI_RST	-	SPI_ASC	SPI_4W	MIRROR[3:0]				0000 0000	00h	
0001h SPI_CFG_B	R/W	SPI_SINGLE	-	SPI_READ_BUFF	-	-	-	-	-	0000 0000	00h	
0002h DEV_PWR_MOD	R/W	-	-	-	-	-	-	DEV_PWR_MOD[1:0]		0000 0000	00h	
0003h CHIP_TYPE	R	CHIP_TYPE[7:0]									0000 0100	04h
0004h CHIP_ID_0	R	DAC_CAL[1:0]		DAC_CMO	DAC_AUX	DAC_M[1:0]		DAC_RES[1:0]		0000 0100	04h	
0005h CHIP_ID_1	R	RESERVED[1:0]		JESD204A_VS[1:0]		FRONTEND[1:0]		DSP[1:0]		0001 1011	1Bh	
0006h CHIP_VS	R	CHIP_VS[7:0]									0000 0000	00h
000Ch VENDOR_ID_LSB	R	VENDOR_ID[7:0]									1001 1100	9Ch
000Dh VENDOR_ID_MSB	R	VENDOR_ID[15:8]									0001 1111	1Fh
000Fh SPI_CFG_C	R/W	-	-	-	-	-	-	-	TRANSFER_BIT	0000 0000	00h	

## 11.11.1.2 SPI configuration block bit definition detailed description

The tables in this section contain detailed descriptions of the SPI configuration registers.

**Table 39. SPI configuration registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0000h	SPI_CFG_A	7	SPI_CFG_RST	R/W		reset SPI configuration
					0	<b>no action</b>
					1	sets all registers (except 000h/0001h) to their defaults (reserved for LSB first)
		5	SPI_ASC	R/W		auto-increment/auto-decrement
					0	<b>ascend off (auto-decrement)</b>
			1	ascend on (auto-increment)		
4	SPI_4W	R/W		SDO active; 3-wire/4-wire SPI interface		
			0	<b>3-wire SPI-interface</b>		
			1	4-wire SPI-interface		
3 to 0	MIRROR[3:0]	R/W		mirror check (write protection for this register)		
0001h	SPI_CFG_B	7	SPI_SINGLE	R/W		streaming mode/one-byte mode
					0	<b>streaming mode</b>
					1	one-byte mode (independent of CSB)
5	SPI_READ_BUFF	R/W		read back registers		
			0	<b>read back resynchronization registers</b>		
			1	read back buffer registers (double buffers)		

**Table 40. Device power mode register**

Default values are shown highlighted.

DEV_PWR_MODE (address 0002h)				
Bit	Symbol	Access	Value	Description
1 to 0	DEV_PWR_MOD[1:0]	R/W	0000 0000	device power mode; reserved

**Table 41. Chip type register**

Default values are shown highlighted.

CHIP_TYPE (address 0003h)				
Bit	Symbol	Access	Value	Description
7 to 0	CHIP_TYPE[7:0]	R	0000 0100	chip type; high-speed DAC

Table 42. Chip registers

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description	
0004h	CHIP_ID_0	7 to 6	DAC_CAL[1:0]	R		DAC calibration	
					<b>00</b>	<b>uncalibrated DAC</b>	
					01	reserved	
					10	reserved	
				11	calibrated DACs		
		5	DAC_CMO	R			DAC common-mode output
					<b>0</b>	<b>low common-mode output</b>	
				1	high common-mode output		
		4	DAC_AUX	R			auxiliary DAC
					<b>0</b>	<b>no auxiliary DAC</b>	
				1	auxiliary DAC		
		3 to 2	DAC_M[1:0]	R			number of converters (M)
					00	single (M = 1)	
					<b>01</b>	<b>dual (M = 2)</b>	
					10	quad (M = 4)	
				11	octal (M = 8)		
1 to 0	DAC_RES[1:0]	R			DAC resolution		
			<b>00</b>	<b>16-bits</b>			
			01	14-bits			
			10	12-bits			
		11	10-bits				
0005h	CHIP_ID_1	7 to 6	RESERVED	R	xx	reserved	
		5 to 4	JESD204A_VS[1:0]	R		JESD204 version	
					00	JESD204A	
					<b>01</b>	<b>JESD204B</b>	
				1x	reserved		
		3 to 2	FRONTEND[1:0]	R			frontend interfaces
					00	CMOS	
					01	LVDS	
					<b>10</b>	<b>JESD204X</b>	
				11	reserved		
1 to 0	DSP[1:0]	R			digital signal processing		
			00	none			
			01	upfir			
			10	ifssbm			
		<b>11</b>	<b>upfir and ifssbm</b>				
0006h	CHIP_VS	7 to 0	CHIP_VS[7:0]	R	0000 0000	fixed or optional value from eFuse	

**Table 43. Chip vendor identification registers***Default values are shown highlighted.*

Address	Register	Bit	Symbol	Access	Value	Description
000Ch	VEND_ID_LSB	7 to 0	VEND_ID[7:0]	R	1001 1100	vendor identification (LSB)
000Dh	VEND_ID_MSB	7 to 0	VEND_ID[15:8]	R	0001 1111	vendor identification (MSB)

**Table 44. SPI configuration register***Default values are shown highlighted.*

SPI_CFG_C (address 0003h)				
Bit	Symbol	Access	Value	Description
0	TRANSFER_BIT	R/W		transfer resynchronized registers
			0	resynchronized registers preserve current value
			1	resynchronized registers are updated with values that are set using SPI

## 11.11.2 Dual DAC core block

This block of registers specifies the main analog features of the DAC cores.

### 11.11.2.1 Dual DAC core block register allocation map

[Table 45](#) shows an overview of all the dual DAC core registers.

**Table 45. Dual DAC core block register allocation map**

Register name	R/W	Bit definition								Default	
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0020h PON_DDC_CFG_0	R/W	SEL_CLK	BGAP_PON	RESERVED[1:0]		DAC_B_PON	RESERVED	DAC_A_PON	RESERVED	1111 1111	FFh
0022h WCLKGENCFG	R/W	CLK_MON_RST	CLK_MON	-	WCLK_PON	WCLK_DIV_BY	WCLK_DIV_SEL[2:0]			0101 0010	52h
0037h DAC_A_AGAIN_LSB	R/W	DAC_A_AGAIN[7:0]								0010 0000	20h
0038h DAC_A_AGAIN_MSB	R/W	DAC_A_AGAIN_PON	-	-	-	-	DAC_A_AGAIN_X2	DAC_A_AGAIN[9:8]		1000 0011	83h
0039h DAC_B_AGAIN_LSB	R/W	DAC_B_AGAIN[7:0]								0010 0000	20h
003Ah DAC_B_AGAIN_MSB	R/W	DAC_B_AGAIN_PON	-	-	-	-	DAC_B_AGAIN_X2	DAC_B_AGAIN[9:8]		1000 0011	83h
003Bh DAC_A_AUX_LSB	R/W	DAC_A_AUX[7:0]								1000 0000	80h
003Ch DAC_A_AUX_MSB	R/W	DAC_A_AUX_PON	-	-	-	-	-	DAC_A_AUX[9:8]		1000 0000	80h
003Dh DAC_B_AUX_LSB	R/W	DAC_B_AUX[7:0]								1000 0000	80h
003Eh DAC_B_AUX_MSB	R/W	DAC_B_AUX_PON	-	-	-	-	-	DAC_B_AUX[9:8]		1000 0000	80h

### 11.11.2.2 Dual DAC core block bit definition detailed description

The tables in this section contain detailed descriptions of the dual DAC core registers.

**Table 46. Dual DAC core power configuration register**

Default values are shown highlighted.

PON_DDC_CFG_0 (address 0020h)				
Bit	Symbol	Access	Value	Description
7	SEL_CLK	R/W	0	DAC clock inactive
			1	DAC clock provided via clock-in
6	BGAP_PON	R/W	0	Bandgap references power-down
			1	Bandgap references enabled
5 to 4	RESERVED	R/W	1	reserved to 11
3	DAC_B_PON	R/W	0	DAC B power-down
			1	DAC B enabled
2	RESERVED	R/W	1	reserved to 1
1	DAC_A_PON	R/W	0	DAC A power-down
			1	DAC A enabled
0	RESERVED	R/W	1	reserved to 1

**Table 47. Word clock generation configuration register**

Default values are shown highlighted.

WCLK_GEN_CFG (address 0022h)				
Bit	Symbol	Access	Value	Description
7	CLK_MON_RST	R/W	0	no action
			1	reset clk_mon_flag
6	CLK_MON	R	0	clk_mon OK
			1	clk_mon failure
4	WCLK_PON	R/W	0	word clock disabled (power-down)
			1	word clock enabled (see <a href="#">Section 11.2.6.1</a> )
3	WCLK_DIV_BYP	R/W	0	word clock depends on wclk_div_sel
			1	WCLK = DAC clock
2 to 0	WCLK_DIV_SEL[2:0]	R/W	000	WCLK = DAC clock / 2 (see <a href="#">Table 23</a> )
			001	WCLK = DAC clock / 3
			010	WCLK = DAC clock / 4
			011	WCLK = DAC clock / 6
			100	WCLK = DAC clock / 12
			110	WCLK = DAC clock / 16
			111	WCLK = DAC clock / 24

**Table 48. Analog gain control registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0037h	DAC_A_AGAIN_LSB	7 to 0	DAC_A_AGAIN[7:0]	R/W	-	least significant 8 bits for analog gain DAC A
0038h	DAC_A_AGAIN_MSB	7	DAC_A_AGAIN_PON	R/W	<b>0</b>	Analog gain DAC A power <b>on</b> (see <a href="#">Section 11.4</a> )
		1			off	
		1 to 0	DAC_A_AGAIN[9:8]		-	most significant 2 bits for analog gain DAC A
0039h	DAC_B_AGAIN_LSB	7 to 0	DAC_B_AGAIN[7:0]	R/W	-	least significant 8 bits for analog gain DAC B
003Ah	DAC_B_AGAIN_MSB	7	DAC_B_AGAIN_PON	R/W	<b>0</b>	Analog gain DAC B power <b>on</b> (see <a href="#">Section 11.4</a> )
		1			off	
		1 to 0	DAC_B_AGAIN[9:8]		-	most significant 2 bits for analog gain DAC B

**Table 49. Auxiliary DACs registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
003Bh	DAC_A_AUX_LSB	7 to 0	DAC_A_AUX[7:0]	R/W	-	least significant 8 bits for auxiliary DAC A
003Ch	DAC_A_AUX_MSB	7	DAC_A_AUX_PON	R/W	<b>0</b>	auxiliary DAC A power <b>on</b> (see <a href="#">Section 11.4.2.1</a> )
		1			off	
		1 to 0	DAC_A_AUX[9:8]		-	most significant 2 bits for auxiliary DAC A
003Dh	DAC_B_AUX_LSB	7 to 0	DAC_B_AUX[7:0]	R/W	-	least significant 8 bits for auxiliary DAC B
003Eh	DAC_B_AUX_MSB	7	DAC_B_AUX_PON	R/W	<b>0</b>	auxiliary DAC B power <b>on</b> (see <a href="#">Section 11.4.2.1</a> )
		1			off	
		1 to 0	DAC_B_AUX[9:8]		-	most significant 2 bits for auxiliary DAC B

### 11.11.3 Main controls block

This block of registers specifies the main configuration of the different clocking systems used in the DAC165xD.

#### 11.11.3.1 Main controls block register allocation map

[Table 50](#) shows an overview of all the main controls registers.

**Table 50. Main controls block register allocation map**

Register name	R/W	Bit definition								Default <sup>[1]</sup>		
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex	
0040h	MAIN_CTRL	R/W	PD_P_LN_RX[3:0]			RESERVED[1:0]		FORCE_RST_DCLK	FORCE_RST_WCLK	0000 0011	03h	
0041h	DCSMU_AUTO_CTRL	R/W	MAN_PON_CTRL	-	-	RESERVED[3:0]			AUTO_CAL_EQ	0000 1100	0Ch	
0042h	DCSMU_AUTO_RT	R/W	-	-	-	-	-	RESERVED	AUTO_CAL_RT	0000 0000	00h	
0044h	RST_EXT_WCLK	R/W	RST_EXT_WCLK_TIME[7:0]								0100 0000	40h
0045h	RST_EXT_DCLK	R/W	RST_EXT_DCLK_TIME[7:0]								0100 0000	40h
0047h	EHS_CTRL	R/W	-	-	IO_DIR[1:0]		IO_EHS[1:0]		SDO_EHS[1:0]		0001 1010	1Ah
004Bh	CDI_CTRL	R/W	SR_CDI	-	-	-	-	CDI_MODE[1:0]		0000 0000	00h	
0050h	IO_MUX_CTRL0	R/W	IO_SEL_0[7:0]								1111 1111	FFh
0051h	IO_MUX_CTRL1	R/W	IO_SEL_1[7:0]								1111 1111	FFh
0052h	IO_MUX_CTRL2	R/W	IO_SEL_2[7:0]								1111 1111	FFh
0054h	MON_DCLK	R	MON_DCLK_STOP	-	-	-	MON_DCLK[3:0]			uuuu uuuu	uuh	
0055h	MON_DCLK_FLAGS	R	MON_DCLK_FLAGS[7:0]								uuuu uuuu	uuh

[1] u = undefined at power-up or after reset.

### 11.11.3.2 Main controls block bit definition detailed description

The tables in this section contain detailed descriptions of the main controls registers.

**Table 51. Main controls register**

Default values are shown highlighted.

MAIN_CTRL (address 0040h)				
Bit	Symbol	Access	Value	Description
7 to 4	PD_P_LN_RX[3:0]	R/W	-	power-down of the physical lane receiver bit 7 = lane 3 bit 6 = lane 2 bit 5 = lane 1 bit 4 = lane 0
3 to 2	RESERVED[1:0]	R/W	00	reserved to 00
1	FORCE_RST_DCLK	R/W	0	digital clock reset release digital clock reset
			1	force digital clock reset
0	FORC_RST_WCLK	R/W	0	work clock reset release work clock reset
			1	force work clock reset

**Table 52. Start-up automatic control register**

Default values are shown highlighted.

DCSMU_AUTO_CTRL (address 0041h)				
Bit	Symbol	Access	Value	Description
7	MAN_PON_CTRL	R/W	0	start-up auto-control pon_rx-phy and pon_dacs controlled by start-up management unit
			1	manual control of pon_rx_phy and pon_dacs
4 to 1	RESERVED[3:0]	R/W	0000	reserved to 0000
0	AUTO_CAL_EQ	R/W	0	automatic calibration equalizer disabled (use auto-zero)
			1	enabled

**Table 53. Start-up automatic calibration resistance termination register**

Default values are shown highlighted.

DCSMU_AUTO_RT (address 0042h)				
Bit	Symbol	Access	Value	Description
1	RESERVED	R/W	0	reserved to 0
0	AUTO_CAL_RT	R/W	0	auto-calibration resistance termination disabled
			1	enabled

**Table 54. Clock extension registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0044h	RST_EXT_WCLK	7 to 0	RST_EXT_WCLK_TIME[7:0]	R/W	-	specify extension time reset, expressed in WCLKclock periods 8 bits for the extension time reset
0045h	RST_EXT_DCLK	7 to 0	RST_EXT_DCLK_TIME[7:0]	R/W	-	specify extension time reset, expressed in DCLK period 8 bits for the extension time reset

**Table 55. EHS control register**

Default values are shown highlighted.

EHS_CTRL (address 0047h)					
Bit	Symbol	Access	Value	Description	
5 to 4	IO_EN[1:0]	R/W	10	IO control direction	
3 to 2	IO_EHS[1:0]	R/W	10	IO EHS-drive control	
1 to 0	SDO_EHS[1:0]	R/W	10	SDO/SDIO EHS-drive control	

**Table 56. Clock domain interface reset register**

Default values are shown highlighted.

CDI_CTRL (address 004Bh)					
Bit	Symbol	Access	Value	Description	
7	CDI_SW_RST	R/W		CDI block software reset control	
			0	no action	
			1	perform a software reset on CDI	
1 to 0	CDI_MOD[1:0]	R/W		CDI mode specification (see <a href="#">Table 24</a> )	
			00	cdi_mode 0 (^2 mode)	
			01	cdi_mode 1 (^4 mode)	
			10	cdi_mode 2 (^8 mode)	
			11	not used	

**Table 57. Type identification registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0050h	IO_MUX_CTRL_0	7 to 0	IO_SEL_0[7:0]	R/W	-	io_mux select for IO 0
0051h	IO_MUX_CTRL_1	7 to 0	IO_SEL_1[7:0]	R/W	-	io_mux select for IO 1
0052h	IO_MUX_CTRL_2	7 to 0	IO_SEL_2[7:0]	R/W	-	io_mux select for io[1:0]
0054h	MON_DCLK	7	MON_DCLK_STOP	R	-	stop digital clock monitoring
		3 to 0	MON_DCLK[3:0]		-	digital clock monitoring
0055h	MON_DCLK_FLAGS	7 to 0	MON_DCLK_FLAGS[7:0]	R	-	digital clock monitoring flags

### 11.11.4 Interface DAC DSP block

This block of registers specifies the main features of the digital signal processing of the DAC165xD.

#### 11.11.4.1 Interface DAC DSP block register allocation map

[Table 58](#) shows an overview all the interface DAC DSP registers.

**Table 58. Interface DAC DSP register allocation map**

Register name	R/W	Bit definition								Default <sup>[1]</sup>	
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0060h TX_CFG	R/W	NCO_EN	NCO_LP_SEL	INV_SINC_SEL	MODULATION[2:0]			INTERPOLATION[1:0]		0000 0001	01h
0062h NCO_PH_OFFSET_LSB <sup>[2]</sup>	R/W	NCO_PH_OFFSET[7:0]								0000 0000	00h
0063h NCO_PH_OFFSET_MSB <sup>[2]</sup>	R/W	NCO_PH_OFFSET[15:8]								0000 0000	00h
0064h NCO_FREQ_B0 <sup>[2]</sup>	R/W	NCO_FREQ[7:0]								0110 0110	66h
0065h NCO_FREQ_B1 <sup>[2]</sup>	R/W	NCO_FREQ[15:8]								0110 0110	66h
0066h NCO_FREQ_B2 <sup>[2]</sup>	R/W	NCO_FREQ[23:16]								0110 0110	66h
0067h NCO_FREQ_B3 <sup>[2]</sup>	R/W	NCO_FREQ[31:24]								0010 0110	66h
0068h NCO_FREQ_B4 <sup>[2]</sup>	R/W	NCO_FREQ[39:32]								0010 0110	26h
0069h PH_CORR_CTRL_0 <sup>[2]</sup>	R/W	PH_CORR[7:0]								0000 0000	00h
006Ah PH_CORR_CTRL_1 <sup>[2]</sup>	R/W	PH_COR_EN	-	-	PH_COR[12:8]					0000 0000	00h
006Bh DAC_A_DGAIN_LSB <sup>[2]</sup>	R/W	DAC_A_DGAIN[7:0]								1101 0100	50h
006Ch DAC_A_DGAIN_MSB <sup>[2]</sup>	R/W	-	-	-	-	DAC_A_DGAIN[11:8]			0000 1011		0Bh
006Dh DAC_B_DGAIN_LSB <sup>[2]</sup>	R/W	DAC_B_DGAIN[7:0]								1101 0100	50h
006Eh DAC_B_DGAIN_MSB <sup>[2]</sup>	R/W	-	-	-	-	DAC_B_DGAIN[11:8]			0000 0010		0Bh

Table 58. Interface DAC DSP register allocation map ...continued

Register name		R/W	Bit definition								Default <sup>[1]</sup>	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
006Fh	DAC_OUT_CTRL <sup>[2]</sup>	R/W	-	-	-	-	A_DGAIN_EN	B_DGAIN_EN	MINUS_3DB	LVL_DET_EN	0000 0000	00h 00h
0070h	DAC_LVL_DET <sup>[2]</sup>	R/W	LVL_DET[7:0]								1111 1111	FFh FFh
0071h	DAC_A_OFFSET_LSB <sup>[2]</sup>	R/W	DAC_A_OFFSET[7:0]								0000 0000	00h 00h
0072h	DAC_A_OFFSET_MSB <sup>[2]</sup>	R/W	DAC_A_OFFSET[15:8]								0000 0000	00h 00h
0073h	DAC_B_OFFSET_LSB <sup>[2]</sup>	R/W	DAC_B_OFFSET[7:0]								0000 0000	00h 00h
0074h	DAC_B_OFFSET_MSB <sup>[2]</sup>	R/W	DAC_B_OFFSET[15:8]								0000 0000	00h 00h
0075h	CODING_IQ <sup>[2]</sup>	R/W	CODING	RESERVED[2:0]			I_LVL_CTRL[1:0]		Q_LVL_CTRL[1:0]		1000 0000	80h 80h
0076h	I_DC_LVL_LSB <sup>[2]</sup>	R/W	I_DC_LVL[7:0]								0000 0000	00h 00h
0077h	I_DC_LVL_MSB <sup>[2]</sup>	R/W	I_DC_LVL[15:8]								1000 0000	80h 80h
0078h	Q_DC_LVL_LSB <sup>[2]</sup>	R/W	Q_DC_LVL[7:0]								0000 0000	00h 00h
0079h	Q_DC_LVL_MSB <sup>[2]</sup>	R/W	Q_DC_LVL[15:8]								1000 0000	80h 80h
007Ah	SPD_CTRL	R/W	SPD_EN	-	-	-	SPD_WINLENGTH				0000 0000	00h 00h
007Bh	SPD_THRESHOLD_LSB	R/W	SPD_THRESHOLD[7:0]								0000 0000	00h 00h
007Ch	SPD_THRESHOLD_MSB	R/W	SPD_THRESHOLD[15:8]								0000 0000	00h 00h
007Dh	SPD_AVG_LSB	R	SPD_AVG[7:0]								uuuu uuuu	uuh uuh
007Eh	SPD_AVG_MSB	R	SPD_AVG[15:8]								uuuu uuuu	uuh uuh

[1] u = undefined at power-up or after reset.

[2] These registers use a double buffer (see [Section 11.2.1.3](#)).

## 11.11.4.2 Interface DAC DSP block bit definition detailed description

The tables in this section contain detailed descriptions of the interface DAC DSP registers.

**Table 59. Transmission configuration register**

Default values are shown highlighted.

TX_CFG (address 0060h)				
Bit	Symbol	Access	Value	Description
7	NCO_EN	R/W		NCO (see <a href="#">Section 11.2.3.4</a> )
			<b>0</b>	<b>NCO disabled, the NCO phase is reset to 0</b>
			1	NCO enabled
6	NCO_LP_SEL	R/W		NCO low-power selection (see <a href="#">Section 11.2.3.5</a> )
			<b>0</b>	<b>low-power NCO disabled</b>
			1	low-power NCO enabled (frequency and phase given by the five MSB of the registers 06h and 08h, respectively)
5	INV_SIN_SEL	R/W		inverse (sin x) / x function selection (see <a href="#">Section 11.2.3.6</a> )
			<b>0</b>	<b>disabled</b>
			1	enabled
4 to 2	MODULATION[2:0]	R/W		modulation (see <a href="#">Section 11.2.3.3</a> )
			<b>000</b>	<b>dual DAC: no modulation</b>
			001	positive upper single sideband upconversion
			010	positive lower single sideband upconversion
			011	negative upper single sideband upconversion
			100	negative lower single sideband upconversion
			others	not defined
1 to 0	INTERPOLATION[1:0]	R/W		interpolation (see <a href="#">Section 11.2.3.2</a> )
			00	no interpolation
			<b>01</b>	<b>×2 interpolation</b>
			10	×4 interpolation
			11	×8 interpolation

**Table 60. Numerically controlled oscillator phase offset registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0062h	NCO_PH_OFFSET_LSB	7 to 0	NCO_PH_OFFSET[7:0]	R/W	-	least significant 8 bits for the NCO phase offset
0063h	NCO_PH_OFFSET_MSB	7 to 0	NCO_PH_OFFSET[15:8]	R/W	-	most significant 8 bits for the NCO phase offset (see <a href="#">Section 11.2.3.4</a> )

**Table 61. Numerically controlled oscillator frequency registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0064h	NCO_FREQ_B0	7 to 0	NCO_FREQ[7:0]	R/W	-	NCO frequency (see <a href="#">Section 11.2.3.4</a> ) least significant 8 bits for the NCO frequency setting
0065h	NCO_FREQ_B1	7 to 0	NCO_FREQ[15:8]	R/W	-	intermediate 8 bits for the NCO frequency setting
0066h	NCO_FREQ_B2	7 to 0	NCO_FREQ[23:16]	R/W	-	intermediate 8 bits for the NCO frequency setting
0067h	NCO_FREQ_B3	7 to 0	NCO_FREQ[31:24]	R/W	-	intermediate 8 bits for the NCO frequency setting
0068h	NCO_FREQ_B4	7 to 0	NCO_FREQ[39:32]	R/W	-	most significant 8 bits for the NCO frequency setting

**Table 62. DAC output phase correction factor registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0069h	PH_CORR_CTRL_0	7 to 0	PH_CORR[7:0]	R/W	-	DAC output phase correction factor (LSB) least significant 8 bits for the DAC output phase correction factor
006Ah	PH_CORR_CTRL_1	7	PH_CORR_EN	R/W	0	DAC output phase correction control <b>DAC output phase correction disabled</b>
					1	DAC output phase correction enabled (see <a href="#">Section 11.2.3.8</a> )
		4 to 0	PH_CORR[12:8]	R/W		DAC output phase correction factor (MSB)
					00000	most significant 5 bits for the DAC output phase correction factor

**Table 63. DAC digital gain control registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
006Bh	DAC_A_DGAIN_LSB	7 to 0	DAC_A_DGAIN[7:0]	R/W	-	DAC A digital gain control (see <a href="#">Section 11.2.3.9</a> ) least significant 8 bits for DAC A digital gain
006Ch	DAC_A_DGAIN_MSB	3 to 0	DAC_A_DGAIN[11:8]	R/W	-	most significant 4 bits for DAC A digital gain
006Dh	DAC_B_DGAIN_LSB	7 to 0	DAC_B_DGAIN[7:0]	R/W	-	DAC B digital gain control (see <a href="#">Section 11.2.3.9</a> ) least significant 8 bits for DAC B digital gain
006Eh	DAC_B_DGAIN_MSB	3 to 0	DAC_B_DGAIN[11:8]	R/W	-	most significant 4 bits for DAC B digital gain

**Table 64. DAC output control register**

Default values are shown highlighted.

DAC_OUT_CTRL (address 006Fh)				
Bit	Symbol	Access	Value	Description
3	DAC_A_DGAIN_EN	R/W		DAC A digital gain control (see <a href="#">Section 11.2.3.9</a> )
			0	disable
			1	enable
2	DAC_B_DGAIN_EN	R/W		DAC B digital gain control (see <a href="#">Section 11.2.3.9</a> )
			0	disable
			1	enable
1	MINUS_3DB	R/W		DAC attenuation control (see <a href="#">Section 11.2.3.7</a> )
			0	unity gain
			1	-3 dB gain
0	LVL_DET_EN	R/W		Digital DAC output level detector control
			0	disable
			1	enable (see <a href="#">Section 11.2.4.1</a> )

**Table 65. Register level detector**

Default values are shown highlighted.

DAC_LVL_DET (address 0070h)				
Bit	Symbol	Access	Value	Description
7 to 0	LVL_DET[7:0]	R/W	-	Digital DAC output level detector value (see <a href="#">Section 11.2.4.1</a> )

**Table 66. DAC digital offset registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0071h	DAC_A_OFFSET_LSB	7 to 0	DAC_A_OFFSET[7:0]	R/W		DAC A digital offset value (see <a href="#">Section 11.2.3.11</a> )
					-	least significant 8 bits for DAC A digital offset
0072h	DAC_A_OFFSET_MSB	3 to 0	DAC_A_OFFSET[15:8]	R/W	-	most significant 8 bits for DAC A digital offset
0073h	DAC_B_OFFSET_LSB	7 to 0	DAC_B_OFFSET[7:0]	R/W		DAC B digital offset value (see <a href="#">Section 11.2.3.11</a> )
					-	least significant 8 bits for DAC B digital offset
0074h	DAC_B_OFFSET_MSB	3 to 0	DAC_B_OFFSET[15:8]	R/W	-	most significant 8 bits for DAC B digital offset

**Table 67. Input word coding register**

Default values are shown highlighted.

CODING_IQ (address 0075h)				
Bit	Symbol	Access	Value	Description
7	CODING	R/W	-	coding of input word (see <a href="#">Section 11.2.3.1</a> )
			0	two's complement coding
			1	unsigned format
6 to 4	RESERVED[2:0]	R/W	000	reserved to 000
3 to 2	I_LVL_CTRL[1:0]	R/W		specifies output from CDI for the I path
			<b>00</b>	<b>normal operation (CDI data output sent to digital signal processing input)</b>
			01	if data enable = 1: normal operation if data enable = 0: digital signal processing input = I_DC_LVL register value
			10	digital signal processing input = I_DC_LVL
			11	digital signal processing input = I_DC_LVL
1 to 0	Q_LVL_CTRL[1:0]	R/W		specifies output from CDI for the Q path
			<b>00</b>	<b>normal operation (CDI data output sent to digital signal processing input)</b>
			01	if data enable = 1: normal operation if data enable = 0: digital signal processing input = Q_DC_LVL register value
			10	digital signal processing input = Q_DC_LVL
			11	digital signal processing input = Q_DC_LVL

**Table 68. LSB/MSB of I/Q levels register**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0076h	I_DC_LVL_LSB	7 to 0	I_DC_LVL[7:0]	R/W	0000 0000	least significant 8 bits for I_DC_LVL
0077h	I_DC_LVL_MSB	7 to 0	I_DC_LVL[15:8]	R/W	1000 0000	most significant 8 bits for I_DC_LVL
0078h	Q_DC_LVL_LSB	7 to 0	Q_DC_LVL[7:0]	R/W	0000 0000	least significant 8 bits for Q_DC_LVL
0079h	Q_DC_LVL_MSB	7 to 0	Q_DC_LVL[15:8]	R/W	1000 0000	most significant 8 bits for Q_DC_LVL

**Table 69. Signal power detector control register**

Default values are shown highlighted.

SPD_CTRL (address 007Ah)				
Bit	Symbol	Access	Value	Description
7	SPD_EN	R/W	-	Signal power detector:
			0	disabled
			1	enabled
3 to 0	SPD_WINLENGTH[3:0]	R/W		SPD averages $2^{(\text{winlength} + 6)}$ ; IQ pairs
			0000	average 64 pairs ( $2^6$ samples)
			0001	average 128 pairs ( $2^7$ samples)
			0010	average 256 pairs ( $2^8$ samples)
			0011	average 512 pairs ( $2^9$ samples)
			0100	average 1024 pairs ( $2^{10}$ samples)
			0101	average 2048 pairs ( $2^{11}$ samples)
			0110	average 4096 pairs ( $2^{12}$ samples)
			0111	average 8192 pairs ( $2^{13}$ samples)
			1000	average 16384 pairs ( $2^{14}$ samples)
			1001	average 32768 pairs ( $2^{15}$ samples)
			1010	average 65536 pairs ( $2^{16}$ samples)
			1011	average 131073 pairs ( $2^{17}$ samples)
			1100	average 262144 pairs ( $2^{18}$ samples)
			1101	average 524288 pairs ( $2^{19}$ samples)
			1110	average 1048576 pairs ( $2^{20}$ samples)
1111	average 2097152 pairs ( $2^{21}$ samples)			

**Table 70. SPD LSB/MSB registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
007Bh	SPD_THRESHOLD_LSB	7 to 0	SPD_THRESHOLD[7:0]	R/W	0000 0000	least significant 8 bits for SPD_THRESHOLD
007Ch	SPD_THRESHOLD_MSB	7 to 0	SPD_THRESHOLD[15:8]	R/W	0000 0000	most significant 8 bits for SPD_THRESHOLD
007Dh	SPD_AVG_LSB	7 to 0	SPD_AVG[7:0]	R/W	uuuu uuuu	least significant 8 bits for SPD_AVG
007Eh	SPD_AVG_MSB	7 to 0	SPD_AVG[15:8]	R/W	uuuu uuuu	most significant 8 bits for SPD_AVG

### 11.11.5 Mute, interrupt, and temperature control

This block of registers specifies the main features of the mute, interrupt and temperature control of the DAC165xD.

#### 11.11.5.1 Mute, interrupt and temperature control register allocation map

[Table 71](#) shows an overview all the interface Mute, interrupt and temperature control registers.

**Table 71. Mute, interrupt and temperature control register allocation map**

Register name		R/W	Bit definition								Default <sup>[1]</sup>	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0080h	MUTE_CTRL_0	R/W	HOLD_DATA	LVL_DET_SEL[1:0]	LVL_DET_EN	MUTE_EN	MUTE_RATE[2:0]				0000 0100	04h
0081h	MUTE_CTRL_1	R/W	ALARM_CFG[1:0]		DATA_V_IQ_CFG[1:0]		CLIP_CFG[1:0]		DIRECT_CFG[1:0]		0000 0000	00h
0082h	MUTE_CTRL_2	R/W	MUTE_CTRL_ALARM_RST	IGN_RF_EN	IGN_MDS_BSY	IGN_DATA_IQ_VAL	-	-	-	MUTE_SIGNAL	0000 0000	00h
0083h	MUTE_ALARM_EN_0	R/W	DATA_IQ_VAL	MDS_BSY	LVL_DET_A	LVL_DET_B	TEMP_ALARM	CLK_ALIGN_ERR	DCLK_ERR_MON	CLK_MON	0000 0000	00h
0084h	MUTE_ALARM_EN_1	R/W	-	-	-	-	-	-	MC_ALARM_EN[9]	MC_ALARM_EN[8]	0000 0000	00h
0085h	MUTE_RATE_CTRL_0	R/W	ALARM_MUTE_RATE[3:0]				DIRECT_MUTE_RATE[3:0]				0111 1100	7Ch
0086h	MUTE_RATE_CTRL_1	R/W	INCIDENT_MUTE_RATE[3:0]				DATA_MUTE_RATE[3:0]				0111 1100	7Ch
0087h	MUTE_WAIT_PERIOD_LSB	R/W	MUTE_WAIT_PER[7:0]								0100 0000	40h
0088h	MUTE_WAIT_PERIOD_MSB	R/W	MUTE_WAIT_PERIOD[15:8]								0000 0000	00h
0089h	IQ_RANGE_LIMIT_LSB	R/W	IQ_RANGE_LIMIT[7:0]								0000 0000	00h
008Ah	IQ_RANGE_LIMIT_MSB	R/W	IQ_RANGE_LIMIT[15:8]								0000 0000	00h
008Ch	INTR_CTRL	R/W	-	-	-	-	INTR_RST	INTR_DCLK_MON_RANGE_[2:0]			0000 0000	00h

**Table 71. Mute, interrupt and temperature control register allocation map ...continued**

Register name	R/W	Bit definition									Default <sup>[1]</sup>	
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex	
008Dh INTR_EN_0	R/W	INTR_EN[7:0]									0000	00h
008Eh INTR_EN_1	R/W	-	INTR_EN[9:8]			RESERVED[4:0]					0000	03h
008Fh INTR_FLAGS_0	R/W	INTR_DLP	MDS_BSY[1:0]		TEMP_ALARM	LVL_DET_OR	CLK_ALIGN_ERR	CLK_MON	DCLK_ERR_MON	uuuu	uuh	
0090h INTR_FLAGS_1	R/W	-	RPT_FLAG_ERR	MUTE_CTRL_ALARM	-	-	-	-	-	uuuu	uuh	
0092h TEMP_CTRL	R/W	TEMP_SENS_PON	TEMP_SENS_RST_ALARM	TEMP_SENS_FULL_RANGE	TEMP_SENS_TOGGLE	TEMP_SENS_RST_MAX	TEMP_SENS_RST_MIN	TEMP_SENS_MOD[1:0]		0000	00h	
0093h TEMP_LEVEL	R/W	-	-	TEMP_SEL_MAN[5:0]					0000	00h		
0094h TEMP_CLK_DIV	R/W	TEMP_CLK_DIV[7:0]									0000	00h
0095h TEMP_TIMER	R/W	TEMP_TIMER[7:0]									0000	00h
0096h TEMP_OUT	R	TEMP_SENS_OUT	TEMP_ALARM	TEMP_ACTUAL[5:0]					uuuu	uuh		
0097h TEMP_MAX	R	-	-	TEMP_MAX[5:0]					uuuu	uuh		
0098h TEMP_MIN	R	-	-	TEMP_MIN[5:0]					uuuu	uuh		
0099h DSP_SMPL_CTRL	R/W	-	-	-	DSP_READ_SEL	DSP_STROBE	DSP_SMPL_SEL[2:0]			0000	00h	
009Ah DSP_READ_LSB	R	DSP_READ[7:0]									uuuu	uuh

Table 71. Mute, interrupt and temperature control register allocation map ...continued

Register name		R/W	Bit definition								Default <sup>[1]</sup>		
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex	
009Bh	DSP_READ_LSIB	R										uuuu uuuu	uuh
009Ch	DSP_READ_MSIB	R										uuuu uuuu	uuh
009Dh	DSP_READ_MSB	R										uuuu uuuu	uuh

[1] u = undefined at power-up or after reset.

### 11.11.5.2 Mute, interrupt and temperature control bit definition detailed description

The tables in this section contain detailed descriptions of the Mute, interrupt and temperature control registers.

**Table 72. Mute control registers**

*Default values are shown highlighted.*

Address	Register	Bit	Symbol	Access	Value	Description
0080h	MUTE_CTRL_0			R/W		mute control (see <a href="#">Section 11.2.3.10</a> )
		7	HOLD_DATA		<b>0</b>	<b>disables hold feature</b>
					1	enables hold feature
		6 to 5	LVL_DET_SEL[1:0]		<b>00</b>	<b>no mute action</b>
					01	mute on lvl_det_a
					10	mute on lvl_det_b
					11	mute on lvl_det_a or lvl_det_b
		4	LVL_DET_EN		<b>0</b>	disable level detection
					1	enable level detection
		3	MUTE_EN		<b>0</b>	<b>disable mute feature</b>
					1	enable mute feature (see <a href="#">Section 11.2.3.10</a> )
		2 to 0	MUTE_RATE[2:0]			controls the rate of the mute feature at 1 GHz (values below are approximate values for 1 GHz)
					000	~8 ns (immediate)
					001	~125 ns
					010	~500 ns
					<b>100</b>	<b>~1 μs</b>
					101	~2 μs
					110	~4 μs
					111	~8 μs

**Table 72. Mute control registers ...continued**  
 Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0081h	MUTE_CTRL_1	7 to 6	ALARM_CFG[1:0]	R/W	<b>00</b>	<b>hard mute and mute_iq</b>
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	soft mute
		5 to 4	DATA_V_IQ_CFG[1:0]		<b>00</b>	<b>hard mute and mute_iq</b>
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	soft mute
		3 to 2	LVL_DET_CFG[1:0]		<b>00</b>	<b>hard mute and mute_iq</b>
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	soft mute
		1 to 0	DIRECT_CFG[1:0]		<b>00</b>	<b>hard mute and mute_iq</b>
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	soft mute
0082h	MUTE_CTRL_2	7	ALARM_CLR	R/W	<b>0</b>	<b>no action</b>
					1	reset alarm flags
		6	IGN_RF_EN		<b>0</b>	<b>no action</b>
					1	ignore rfx_en state
		5	IGN_MDS_BSY		<b>0</b>	<b>no action</b>
					1	ignore mds_bsy state
		4	IGN_DATA_V_IQ		<b>0</b>	<b>no action</b>
					1	ignore internal data-enable state
0	MUTE_SIGNAL		<b>0</b>	<b>no action</b>		
			1	mute signal (uses direct_cfg)		

**Table 73. Mute alarm enable registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0083h	MUTE_ALARM_EN_0					enables alarm condition for mute action (see <a href="#">Section 11.2.3.10</a> )
		7	DATA_IQ_VAL	R/W	<b>0</b> 1	<b>1 → 0</b> 0 → 1
		6	MDS_BSY	R/W	<b>0</b> 1	<b>0 → 1</b> 1 → 0
		5	LVL_DET_A	R/W	<b>0</b> 1	<b>0 → 1</b> 1 → 0
		4	LVL_DET_B	R/W	<b>0</b> 1	<b>0 → 1</b> 1 → 0
		3	TEMP_ALARM	R/W	<b>0</b> 1	<b>0 → 1</b> 1 → 0
		2	CLK_ALIGN_ERR	R/W	<b>0</b> 1	<b>0 → 1</b> 1 → 0
		1	DCLK_ERR_MON	R/W	<b>0</b> 1	<b>0 → 1</b> 1 → 0
		0	CLK_MON	R/W	<b>0</b> 1	<b>0 → 1</b> 1 → 0
0084h	MUTE_ALARM_EN_1	1	MC_ALARM_EN[9]	R/W	-	0 → 1
		0	MC_ALARM_EN[8]	R/W	-	0 → 1

**Table 74. Mute rate control registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0085h	MUTE_RATE_CTRL_0	7 to 4	ALARM_MUTE_RATE[3:0]	R/W	-	sets mute and unmute rate in case of an alarm event
		3 to 0	DIRECT_MUTE_RATE[3:0]	R/W	-	sets mute and unmute rate in case of direct mute control
0086h	MUTE_RATE_CTRL_1	7 to 4	INCIDENT_MUTE_RATE[3:0]	R/W	-	sets mute and unmute rate in case of an incident
		3 to 0	DATA_MUTE_RATE[3:0]	R/W	-	sets mute and unmute rate in case of a data-enable change

**Table 75. Mute wait period LSB/MSB registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0087h	MUTE_WAIT_PERIOD_LSB	7 to 0	MUTE_WAIT_PERIOD[7:0]	R/W	-	least significant 8 bits for MUTE_WAIT_PERIOD
0088h	MUTE_WAIT_PERIOD_MSB	7 to 0	MUTE_WAIT_PERIOD[15:8]	R/W	-	most significant 8 bits for MUTE_WAIT_PERIOD

**Table 76. IQ range limit LSB/MSB registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0089h	IQ_RANGE_LIMIT_LSB	7 to 0	IQ_RANGE_LIMIT[7:0]	R/W	-	least significant 8 bits for IQ_RANGE_LIMIT
008Ah	IQ_RANGE_LIMIT_MSB	7 to 0	IQ_RANGE_LIMIT[15:8]	R/W	-	most significant 8 bits for IQ_RANGE_LIMIT

**Table 77. Interrupt control register**

Default values are shown highlighted.

INTR_CTRL (address 008Ch)					
Bit	Symbol	Access	Value	Description	
3	INTR_RST	R/W		i_intr and i_flags reset	
			0	disabled	
			1	enabled (see <a href="#">Section 11.7</a> )	
2 to 0	INTR_DCLK_MON_RANGE[2:0]	R/W		interrupt condition as related to the DCLK monitoring (see <a href="#">Figure 24</a> )	
			000	mon_dclk_flag when mon_dclk drifts to (1   9)	
			001	mon_dclk_flag when mon_dclk drifts to (2   8)	
			010	mon_dclk_flag when mon_dclk drifts to (3   7)	
			011	mon_dclk_flag when mon_dclk drifts to (4   6)	
			100	mon_dclk_flag when mon_dclk drifts to (5)	
			others	mon_dclk_flag disabled	

**Table 78. Interrupt enable registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
008Dh	INTR_EN_0	7 to 0	INTR_EN[7:0]	R/W	-	enables usage of intr_src[7:0] for intr_flags[7:0]
008E	INTR_EN_1	6 to 5	INTR_EN[9:8]	R/W	-	enables usage of intr_src[14:8] for intr_flags[14:8] (see <a href="#">Section 11.7.2</a> )

**Table 79. Interrupt flags registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
008Fh	INTR_FLAGS_0	7	INTR_DLP	R	-	intr_dlp active
		6	<u>MDS_BSY</u>		-	indicates transition 1 → 0 on mds_busy
		5	MDS_BSY		-	indicates transition 0 → 1 on mds_busy
		4	TEMP_ALARM		-	indicates transition 0 → 1 on temp_alarm
		3	CLIP_DET_OR		-	indicates transition 0 → 1 on clip_detect (a or b)
		2	CLK_ALIGN_ERR		-	indicates transition 0 → 1 on clock_align_monitor
		1	CLK_MON		-	indicates transition 0 → 1 on clkmon (div8)
		0	MON_DCLK_ERR		-	indicates transition 0 → 1 on mon_dclk_error_flags
0090h	INTR_FLAGS_1	6	ERR_RPT_FLAG	R	-	indicates transition 0 → 1 on err_rpt_flag
		5	MUTE_CTRL_ALARM		-	indicates alarm event detected by mute_ctrl
		4 to 0	RESERVED		-	reserved

**Table 80. Temperature sensor control register**

Default values are shown highlighted.

TEMP_SENS_CTRL register (address 0092h)					
Bit	Symbol	Access	Value	Description	
7	TEMP_SENS_PON	R/W		temperature sensor power	
			0	disabled (power-down)	
			1	enabled (see <a href="#">Section 11.5</a> )	
6	TEMP_SENS_RST_ALARM	R/W		reset temperature sensor alarm	
			0	no action	
			1	reset temp_sensor_alarm flag	
5	TEMP_SENS_FULLRANGE	R/W		temperature sensor full range	
			0	sweep 22 to 63	
			1	sweep 0 to 63	
4	TEMP_SENS_TOGGLE	R/W		temperature sensor toggle	
			0	wait for 0 → 1 transition	
			1	wait for 1 → 0 transition	
3	TEMP_SENS_RST_MAX	R/W		temperature sensor, maximum reset	
			0	no action	
			1	reset temp_max_value	
2	TEMP_SENS_RST_MIN	R/W		temperature sensor, minimum reset	
			0	no action	
			1	reset temp_min_value	

**Table 80. Temperature sensor control register ...continued**

Default values are shown highlighted.

TEMP_SENS_CTRL register (address 0092h)				
Bit	Symbol	Access	Value	Description
1 to 0	TEMP_SENS_MOD[1:0]	R/W		temperature sensor mode
			00	raw mode (direct access to temperature sensor)
			01	one-shot measurement
			10	continuous measurement
			11	continuous measurement (hold temp_alarm_flag)

**Table 81. Temperature sensor level register**

Default values are shown highlighted.

TEMPS_LVL (address 0093h)				
Bit	Symbol	Access	Value	Description
5 to 0	TEMP_SEL_MAN[5:0]	R/W	-	temperature sensor level selection usage depends on ts_mode: ts_mode = "00": applied directly to temp_sensor ts_mode = "others": sets threshold for temp_alarm

**Table 82. Temperature sensor clock divider register**

Default values are shown highlighted.

TEMPS_CLK_DIV (address 0094h)				
Bit	Symbol	Access	Value	Description
7 to 0	TS_CLK_DIV[7:0]	R/W	-	sets clock frequency temp_sensor_ctrl (dclk / ts_clkdiv)

**Table 83. Temperature sensor timer register**

Default values are shown highlighted.

TEMP_SENS_TIMER (address 0095h)				
Bit	Symbol	Access	Value	Description
7 to 0	TEMP_SENS_TIMER[7:0]	R/W	-	sets number of wait cycles between measurements

**Table 84. Temperature sensor output register**

Default values are shown highlighted.

TEMP_SENS_OUT (address 0096h)				
Bit	Symbol	Access	Value	Description
7	TEMP_SENS_OUT	R	-	temperature sensor output (for use in raw mode)
6	TEMP_ALARM	R	-	temp_actual > temp_threshold flag
5 to 0	TEMP_ACTUAL[5:0]	R	-	temp_actual (result of last measurement)

**Table 85. Maximum temperature register**

Default values are shown highlighted.

TEMP_MAX (address 0097h)				
Bit	Symbol	Access	Value	Description
5 to 0	TEMP_MAX[5:0]	R	-	maximum temp_actual found since last ts_rst_max

**Table 86. Minimum temperature register***Default values are shown highlighted.*

TEMP_MIN (address 0098h)				
Bit	Symbol	Access	Value	Description
5 to 0	TEMP_MIN[5:0]	R	-	minimum temp_actual found since last ts_rst_max

**Table 87. DSP sample control register***Default values are shown highlighted.*

DSP_SMPL_CTRL (address 0099h)				
Bit	Symbol	Access	Value	Description
4	DSP_READ_SEL	R/W	0	DSP_READ[31:0] ← MC_STATUS[31:0]
			1	DSP_READ[31:0] ← DSP_SMPL[31:0]
3	DSP_STROBE	R/W	0	<b>no action</b>
			1	update DSP sample
2 to 0	DSP_SMPL_SEL[2:0]	R/W	000	DSP_SMPL ← Q_0 and I_0
			001	DSP_SMPL ← Q_1 and I_1
			010	DSP_SMPL ← Q_2 and I_2
			011	DSP_SMPL ← Q_3 and I_3
			100	DSP_SMPL ← Q_TST and I_TST
			101	DSP_SMPL ← X_TST
			110	DSP_SMPL ← MC_TST

**Table 88. DSP read LSB/MSB registers***Default values are shown highlighted.*

Address	Register	Bit	Symbol	Access	Value	Description
009Ah	DSP_READ_LSB	7 to 0	DSP_READ[7:0]	R	-	least significant 8 bits for DSP_READ
009Bh	DSP_READ_LSIB	7 to 0	DSP_READ[15:8]	R	-	least significant intermediate 8 bits for DSP_READ
009Ch	DSP_READ_MSIB	7 to 0	DSP_READ[23:16]	R	-	most significant intermediate 8 bits for DSP_READ
009Dh	DSP_READ_MSB	7 to 0	DSP_READ[31:24]	R	-	most significant 8 bits for DSP_READ

### 11.11.6 Multiple devices synchronization and interrupt block

This block of registers specifies the configuration of the SYSREF signals (East and West) and how they are used for the Multiple Devices Synchronization (MDS) feature. It also specifies the interrupts.

#### 11.11.6.1 Multiple devices synchronization and interrupt block register allocation map

[Table 89](#) shows an overview of all the multiple devices synchronization and interrupt registers.

**Table 89. Multiple devices synchronization and interrupt block register allocation map**

Register name		R/W	Bit definition								Default <sup>[1]</sup>	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
00A0h	MDS_MAIN	R/W	MDS_EQ_CHECK[1:0]		MDS_MAN	MDS_SREF_DIS	MDS_EAST_WEST	MDS_MOD[1:0]		MDS_EN	0000 0000	00h
00A1h	MDS_VS1_CTRL	R/W	ISSUE_COND[1:0]		RESERVED	MDS_DAISSY_KEEP_SREF	I_REINIT_MODE[1:0]		-	-	0000 0110	06h
00A2h	MDS_IO_CTRL	R/W	-	-	-	-	MDS_SEL_FE_E	MDS_SEL_RT_E	MDS_SEL_FE_W	MDS_SEL_RT_W	0000 0000	00h
00A3h	MDS_MISC_CTRL_0	R/W	MDS_RUN	MDS_NCO	RESERVED[2:0]			MDS_PW[2:0]			0001 0000	10h
00A4h	MDS_MAN_ADJUST_DLY	R/W	MDS_MAN_ADJ_DLY[7:0]								1000 0000	80h
00A5h	MDS_AUTO_CYCLES	R/W	MDS_AUTO_CYCLES[7:0]								1000 0000	80h
00A6h	MDS_MISC_CTRL_1	R/W	RESERVED[2:0]			MDS_RELOCK	MDS_LOCK_DLY[3:0]			0000 1111	0Fh	
00A7h	MDS_OFFSET_DLY	RW	-	-	-	MDS_OFFSET_DLY[4:0]			0000 0000	00h		
00A8h	MDS_WIN_LOW	R/W	MDS_WIN_PERIOD_A[7:0]								0000 1111	0Fh
00A9h	MDS_WIN_HIGH	R/W	MDS_WIN_PERIOD_B[7:0]								0000 0111	07h
00AAh	LMFC_PERIOD	R/W	LMFC_PERIOD[7:0]								0000 1000	08h
00ABh	LMFC_PRST	R/W	LMFC_PRESET[7:0]								0000 0100	04h

Table 89. Multiple devices synchronization and interrupt block register allocation map ...continued

Register name			R/W	Bit definition							Default <sup>[1]</sup>	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin
00ACh	MDS_CNT_PRESET	R/W	MDS_CNT_PRESET[7:0]							0000 0010	02h	
00ADh	SYNC_LMFC_PE	R/W	SYNC_LMFC_PE[7:0]							0000 0100	04	
00AEh	MDS_SYNC_CTRL	R/W	-	-	-	MDS_SYNC_INIT	-	SYNC_FINE_DLY[2:0]		0000 0100	04h	
00B0h	MDS_DAISSY_CYCLES	R/W	MDS_DAISSY_CYCLES[7:0]							0000 0100	04h	
00B1h	MDS_WAIT_CYCLES	R/W	MDS_WAIT_CYCLES							0000 0100	04h	
00B3h	ERR_RPT_CTRL	R/W	-	-	-	-	-	ERR_RPT_CTRL[2:0]		0000 0000	00h	
00B4h	ERR_RPT_POS	R/W	ERR_RPT_POS[7:0]									
00B5h	MDS_ADJ_DLY	RW	MDS_ADJ_DLY[7:0]							uuuu uuuu	uuh	
00B6h	MDS_STATUS_0	R	EARLY	LATE	EQUAL	MDS_EQ	EARLY_ERR	LATE_ERR	EQUAL_FOUND	MDS_ACTIVE	uuuu uuuu	uuh
00B7h	MDS_STATUS_1	R	RPT_FLAG_ERR	MDS_BSY_MON	ADD_ERR	RESERVED[1:0]		MDS_PRERUN	MDS_LOCKOUT	MDS_LOCK	uuuu uuuu	uuh

[1] u = undefined at power-up or after reset.

### 11.11.6.2 Multiple devices synchronization and interrupt block bit definition detailed description

The tables in this section contain detailed descriptions of the multiple devices synchronization and interrupt registers.

**Table 90. MDS main register**

Default values are shown highlighted.

MDS_MAIN (address 00A0h)				
Bit	Symbol	Access	Value	Description
7 to 6	MDS_EQ_CHCK[1:0]	R/W		MDS equalizer check: lock mode
			<b>00</b>	<b>lock when (early = 1 and late = 1)</b>
			01	lock when (early = 1, late = 1 and equal = 1)
			10	lock when equal = 1
			11	force lock (equal-check = 1)
5	MDS_MAN	R/W		control adjustment delays
			<b>0</b>	<b>auto-control adjustment delays</b>
			1	manual control adjustment delays
4	MDS_SREF_DIS	R/W		sref generation
			<b>0</b>	<b>disabled</b>
			1	enabled
3	MDS_EAST_WEST	R/W		MDS input/output (see <a href="#">Section 11.6</a> )
			0	west used as MDS input
			1	east used as MDS input
2 to 1	MDS_MOD[1:0]	R/W		MDS mode (see <a href="#">Section 11.6</a> )
			00	mds_vs0 all-slave mode
			01	mds_vs0 master mode
			10	mds_vs1 without daisy-chain control
			11	mds_vs1 with daisy-chain control
0	MDS_EN	R/W		MDS function control
			<b>0</b>	<b>disabled</b>
			1	enabled (see <a href="#">Section 11.6</a> )

**Table 91. MDS version 1 control register**

Default values are shown highlighted.

MDS_VS1_CTRL (address 00A1h)				
Bit	Symbol	Access	Value	Description
7 to 6	DLP_ISSUE_COND[1:0]	R/W		digital lane processing issue condition that generates an error in the MDS module
			00	$\overline{\text{dlp\_issue}} \leq (\overline{\text{dlp\_lock}}) \text{ OR } (\overline{\text{dlp\_sync}})$
			01	$\overline{\text{dlp\_issue}} \leq (\overline{\text{dlp\_lock}}) \text{ AND } (\overline{\text{dlp\_sync}})$
			10	$\overline{\text{dlp\_issue}} \leq (\overline{\text{dlp\_lock}})$
			11	$\overline{\text{dlp\_issue}} \leq (\overline{\text{dlp\_sync}})$
5	RESERVED	R/W	0	reserved to 0

**Table 91. MDS version 1 control register ...continued**

Default values are shown highlighted.

MDS_VS1_CTRL (address 00A1h)				
Bit	Symbol	Access	Value	Description
4	MDS_DAISSY_KEEP_SREF	R/W		controls the SREF signal generation in daisy chain mode, for easy resynchronization
			0	daisy control timer switches sref off (see <a href="#">Section 11.6</a> )
			1	sref used for daisy chain remains active
3 to 2	I_REINIT_MOD[1:0]	R/W		reinitialization mode
			00	assert synchronization request
			01	assert synchronization request and reset DLP
			10	assert synchronization request and reset MDS controller
			11	no action (ignore dlp_issue)

**Table 92. MDS IO control register**

Default values are shown highlighted.

MDS_IO_CTRL (address 00A2h)				
Bit	Symbol	Access	Value	Description
3	MDS_SEL_FE_EAST	R/W		MDS east falling edge/rising edge operation (see <a href="#">Section 11.6</a> )
			0	falling edge
			1	rising edge
2	MDS_SEL_EAST_RT	R/W		MDS east internal resistor termination activation (see <a href="#">Section 11.6</a> )
			0	inactive
			1	active
1	MDS_SEL_FE_WEST	R/W		MDS west falling edge/rising edge operation (see <a href="#">Section 11.6</a> )
			0	falling edge
			1	rising edge
0	MDS_SEL_WEST_RT	R/W		MDS west internal resistor termination activation (see <a href="#">Section 11.6</a> )
			0	inactive
			1	active

**Table 93. MDS miscellaneous control register**

Default values are shown highlighted.

MDS_MISC_CTRL_0 (address 00A3h)				
Bit	Symbol	Access	Value	Description
7	MDS_RUN	R/W		starts the MDS module
			0	no action
			1	(0 → 1) transition restarts evaluation counter
6	MDS_NCO	R/W		NCO synchronization
			0	disabled
			1	enabled
5 to 3	RESERVED	R/W		reserved to 0
2 to 0	MDS_PW[2:0]	R/W		pulse width of MDS (in output clock periods)
			<b>000</b>	<b>1 DAC clock period</b>
			001	2 DAC clock periods
			010 to 111	(mds_pw – 1) × 4 DAC clock periods

**Table 94. MDS manual adjustment delay register**

Default values are shown highlighted.

MDS_MAN_ADJ_DLY (address 00A4h)				
Bit	Symbol	Access	Value	Description
7 to 0	MDS_MAN_ADJ_DLY[6:0]	R/W		adjustment delay value
			0	if MDS_MAN = 0 then initial value adjustment delay
			1	if MDS_MAN = 1 then controls adjustment delay

**Table 95. MDS automatic evaluation cycles register**

Default values are shown highlighted.

MDS_AUTO_CYCLES (address 00A5h)				
Bit	Symbol	Access	Value	Description
7 to 0	MDS_AUTO_CYCLES[7:0]	R/W	-	number of evaluation cycles applied for MDS.

**Table 96. MDS miscellaneous control register**

Default values are shown highlighted.

MDS_MISC_CTRL_1 (address 00A6h)				
Bit	Symbol	Access	Value	Description
7 to 5	RESERVED	R/W	0	reserved to 0
4	MDS_RELOCK	R/W		relock mode
			<b>0</b>	<b>no action</b>
			1	relock when lockout occurs
3 to 0	MDS_LOCK_DLY[3:0]	R/W	-	number of succeeding 'equal' detections until lock

**Table 97. MDS offset delay register**

Default values are shown highlighted.

MDS_OFFSET_DLY (address 00A7h)				
Bit	Symbol	Access	Value	Description
4 to 0	MDS_OFFSET_DLY[6:0]	R/W	-	delay offset for dataflow (two's complement [-16 to 15])

**Table 98. MDS window registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
00A8h	MDS_WIN_LOW	7 to 0	MDS_WIN_PERIOD_A[7:0]	R/W	-	determines MDS window LOW time
00A9h	MDS_WIN_HIGH	7 to 0	MDS_WIN_PERIOD_B[7:0]	R/W	-	determines MDS window HIGH time

**Table 99. LMFC period register**

Default values are shown highlighted.

LMFC_PERIOD (address 00AAh)				
Bit	Symbol	Access	Value	Description
7 to 0	LMFC_PERIOD[7:0]	R/W	-	determines the LMFC period

**Table 100. LMFC preset register**

Default values are shown highlighted.

LMFC_PRST (address 00ABh)				
Bit	Symbol	Access	Value	Description
7 to 0	LMFC_PRST[7:0]	R/W	-	delays the LMFC period as related to the internal sref signal

**Table 101. MDS position preset register**

Default values are shown highlighted.

MDS_POS_PRESET (address 00ACh)				
Bit	Symbol	Access	Value	Description
7 to 0	MDS_POS_PRST[7:0]	R/W	-	determines the sref position as related to the sysref signal

**Table 102. SYNC versus LMFC position edge register**

Default values are shown highlighted.

SYNC_LMFC_PE register (address 00ADh)				
Bit	Symbol	Access	Value	Description
7 to 0	SYNC_LMFC_PE[7:0]	R/W	-	determines the SYNC position edge as related to LMFC

**Table 103. MDS synchronization register**

Default values are shown highlighted.

MDS_SYNC_CTRL (address 00AEh)				
Bit	Symbol	Access	Value	Description
4	MDS_SYNC_INIT	R/W	0	MDS synchronization initialization initial state SYNC = '0'.
			1	initial state SYNC = '1'.
2 to 0	SYNC_FINE_TUN_DLY[2:0]	R/W	-	fine-tuning SYNC position (sync_rq × (dacclk – accuracy))

**Table 104. MDS daisy cycles register**

Default values are shown highlighted.

MDS_DAISSY_CYCLES (address 00B0h)				
Bit	Symbol	Access	Value	Description
7 to 0	MDS_DAISSY_CYCLES[7:0]	R/W	-	number of digital clock periods required to synchronize daisy partner

**Table 105. MDS wait cycles register**

Default values are shown highlighted.

MDS_WAIT_CYCLES (address 00B1h)				
Bit	Symbol	Access	Value	Description
7 to 0	MDS_WAIT_CYCLES[7:0]	R/W	-	number of daisy cycles required before releasing DLP

**Table 106. Pulswidth error report control register**

Default values are shown highlighted.

PW_ERR_RPT_CTRL (address 00B3h)				
Bit	Symbol	Access	Value	Description
2 to 0	PW_ERR_RPT_CTRL[2:0]	R/W		error reporting pulse width
			00x	no error reporting pulse width
			010	err_rpt_pulse_width = 2 DAC clock periods
			011	err_rpt_pulse_width = 4 DAC clock periods
			100	err_rpt_pulse_width = 8 DAC clock periods
			101	err_rpt_pulse_width = 16 DAC clock periods
			110	err_rpt_pulse_width = 32 DAC clock periods
			111	err_rpt_pulse_width = 64 DAC clock periods

**Table 107. Error report position register**

Default values are shown highlighted.

ERR_RPT_POS (address 00B4h)				
Bit	Symbol	Access	Value	Description
6 to 0	ERR_RPT_POS[7:0]	R/W	-	determines err_rpt position as related to LMFC

**Table 108. MDS adjustment delay register**

Default values are shown highlighted.

MDS_ADJ_DLY (address 00B5h)				
Bit	Symbol	Access	Value	Description
6 to 0	MDS_ADJ_DLY[6:0]	R	-	actual value adjustment delay

**Table 109. MDS status registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
00B6h	MDS_STATUS_0	7	EARLY	R		early signal (sampled) from early-to-late detector
					0	false
					1	true
		6	LATE	R		late signal (sampled) from early-to-late detector
					0	false
					1	true
		5	EQUAL	R		equal signal (sampled) from early-to-late detector
					0	false
					1	true
		4	MDS_LOCK	R		result equal-check
					0	false
					1	true
		3	EARLY_ERR	R		adjustment delay maximum value stops the search
					0	false
					1	true
		2	LATE_ERR	R		adjustment delay minimum value stops the search
					0	false
					1	true
		1	EQUAL_FOUND	R		evaluation logic has detected equal condition
					0	false
					1	true
		0	MDS_ACTIVE			evaluation logic active
					0	false
					1	true

**Table 109. MDS status registers ...continued***Default values are shown highlighted.*

Address	Register	Bit	Symbol	Access	Value	Description
00B7h	MDS_STATUS_1	6	MDS_BSY_MON	R		indicates that the MDS state machine is busy
		5	ADJ_DLY_ERR	R		adjustment delay error
					0	OK
			1	delay offset cannot be applied within available range		
		4 to 2	RESERVED	R		reserved
		1	MDS_LOCKOUT	R		MDS_LOCKOUT detected flag
					0	false
			1	true		
		0	MDS_LOCK	R		MDS_LOCK flag
					0	false
	1	true				

### 11.11.7 RX Digital Lane Processing (DLP) block

This block of registers specifies the configuration of the digital lane processing.

#### 11.11.7.1 RX digital lane processing block register allocation map

[Table 110](#) shows an overview of all the RX digital lane processing registers.

**Table 110. RX digital lane processing block register allocation map**

Register name		R/W	Bit definition								Default			
			b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex		
00C2h	ILA_CTRL_0	R/W	RESERVED[3:0]				-	-	FRAME_ALIGN_EN	SR_ILA	0000 0000	00h		
00C5h	DEC_CTRL	R/W	WORD_SWP_P_LN3	WORD_SWP_P_LN2	WORD_SWP_P_LN1	WORD_SWP_P_LN0	SEL_RF_F10_P_LN3	SEL_RF_F10_P_LN2	SEL_RF_F10_P_LN1	SEL_RF_F10_P_LN0	0000 0000	00h		
00C7h	ILA_CTRL_1	R/W	-	RESERVED[1:0]		SEL_LOCK[2:0]		ILA_SYNC	DATA_DESCR_EN	0000 0011	03h			
00C8h	FORCE_ALIGN	R/W	-	-	RESERVED[3:0]			DYN_REALIGN_EN	FORCE_ALIGN	0000 0000	00h			
00C9h	MAN_ALIGN_P_LN_1_0	R/W	MAN_ALIGN_P_LN1[3:0]				MAN_ALIGN_P_LN0[3:0]				0000 0000	00h		
00CAh	MAN_ALIGN_P_LN_3_2	R/W	MAN_ALIGN_P_LN3[3:0]				MAN_ALIGN_P_LN2[3:0]				0000 0000	00h		
00CCh	SYNC_OUT_MODE	R/W	SEL_REINIT[2:0]			SYNC_POL	SYNC_INIT_LVL	SEL_SYNC[3:0]			0000 0000	00h		
00CDh	P_LN_POL	R/W	-	-	-	-	POL_P_LN3	POL_P_LN2	POL_P_LN1	POL_P_LN0	0000 0000	00h		
00CEh	P_LN_SEL	R/W	SEL_P_LN3[1:0]		SEL_P_LN2[1:0]		SEL_P_LN1[1:0]		SEL_P_LN0[1:0]		1110 0100	E4h		
00D0h	SR_SCR	R/W	FORCE_FRST_SAMP_LOW	-	-	-	SR_SCR_LN3	SR_SCR_LN2	SR_SCR_LN1	SR_SCR_LN0	0000 0000	00h		
00D1h	INIT_DESCR_P_LN0_MSB	R/W	INIT_DESCR_P_LN0[15:8]									0000 0000	00h	
00D2h	INIT_DESCR_P_LN0_LSB	R/W	-	INIT_DESCR_P_LN0[7:1]									0000 0000	00h
00D3h	INIT_DESCR_P_LN1_MSB	R/W	INIT_DESCR_P_LN1[15:8]									0000 0000	00h	

**Table 110. RX digital lane processing block register allocation map ...continued**

Register name		R/W	Bit definition									Default		
			b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex		
00D4h	INIT_DESCR_P_LN1_LSB	R/W	-	INIT_DESCR_P_LN1[7:1]									0000 0000	00h
00D5h	INIT_DESCR_P_LN2_MSB	R/W	INIT_DESCR_P_LN2[15:8]									0000 0000	00h	
00D6h	INIT_DESCR_P_LN2_LSB	R/W	-	INIT_DESCR_P_LN2[7:1]									0000 0000	00h
00D7h	INIT_DESCR_P_LN3_MSB	R/W	INIT_DESCR_P_LN3[15:8]									0000 0000	00h	
00D8h	INIT_DESCR_P_LN3_LSB	R/W	-	INIT_DESCR_P_LN3[7:1]									0000 0000	00h
00D9h	INIT_ILA_BUFF_PNTR_L_LN_1_0	R/W	INIT_ILA_BUFF_PNTR_L_LN1[3:0]				INIT_ILA_BUFF_PNTR_L_LN0[3:0]					1000 1000	88h	
00DAh	INIT_ILA_BUFF_PNTR_L_LN_3_2	R/W	INIT_ILA_BUFF_PNTR_L_LN3[3:0]				INIT_ILA_BUFF_PNTR_L_LN2[3:0]					1000 1000	88h	
00DBh	ERR_HNDLNG	R/W	DISP_ERR_LN3_EN	DISP_ERR_LN2_EN	DISP_ERR_LN1_EN	DISP_ERR_LN0_EN	-	-	-	IGN_ERR	0000 0000	00h		
00DCh	REINIT_CTRL	R/W	REINIT_ILA_L_LN3	REINIT_ILA_L_LN2	REINIT_ILA_L_LN1	REINIT_ILA_L_LN0	RESYNC_OLINK_P_LN3	RESYNC_OLINK_P_LN2	RESYNC_OLINK_P_LN1	RESYNC_OLINK_P_LN0	0000 0000	00h		
00DDh	MISC_CTRL	R/W	DLP_STROBE	-	-	-	-	-	RESERVED[1:0]		0000 0000	00h		
00DEh	LMF_CTRL	R/W	L[2:0]			M[1:0]			F[2:0]			1001 0010	92h	

### 11.11.7.2 RX digital lane processing block bit definition detailed description

The tables in this section contain detailed descriptions of the RX digital lane processing registers.

**Table 111. Inter-lane alignment control register**

Default settings are shown highlighted.

ILA_CTRL_0 (address 00C2h)				
Bit	Symbol	Access	Value	Description
7 to 4	RESERVED	R/W	0000	reserved to 0
1	FRAME_ALIGN_EN	R/W		frame alignment
			0	<b>no action</b>
			1	enable frame alignment
0	SR_ILA	R/W		soft reset inter-lane alignment
			0	<b>no action</b>
			1	reset

**Table 112. Clock alignment control register**

CA_CTRL (address 00C5h)				
Bit	Symbol	Access	Value	Description
7	WORD_SWP_P_LN3	R/W		physical lane 3 bit swapping
			0	<b>dout_ca_ln3[7:0] = din_ca_ln3[7:0]</b>
			1	dout_ca_ln3[7:0] = din_ca_ln3[0:7]
6	WORD_SWP_P_LN2	R/W		physical lane 2 bit swapping
			0	<b>dout_ca_ln2[7:0] = din_ca_ln2[7:0]</b>
			1	dout_ca_ln2[7:0] = din_ca_ln2[0:7]
5	WORD_SWP_P_LN1	R/W		physical lane 1 bit swapping
			0	<b>dout_ca_ln1[7:0] = din_ca_ln1[7:0]</b>
			1	dout_ca_ln1[7:0] = din_ca_ln1[0:7]
4	WORD_SWP_P_LN0	R/W		physical lane 0 bit swapping
			0	<b>dout_ca_ln0[7:0] = din_ca_ln0[7:0]</b>
			1	dout_ca_ln0[7:0] = din_ca_ln0[0:7]
3	SEL_RF_F10_P_LN3	R/W		physical lane 3 sampling mode
			0	<b>din_ca_ln3 sampled at falling edge f10_ln3</b>
			1	din_ca_ln3 sampled at rising edge f10_ln3
2	SEL_RF_F10_P_LN2	R/W		physical lane 2 sampling mode (see <a href="#">Section 11.7.5.2</a> )
			0	<b>din_ca_ln2 sampled at falling edge f10_ln2</b>
			1	din_ca_ln2 sampled at rising edge f10_ln2
1	SEL_RF_F10_P_LN1	R/W		physical lane 1 sampling mode (see <a href="#">Section 11.7.5.2</a> )
			0	<b>din_ca_ln1 sampled at falling edge f10_ln1</b>
			1	din_ca_ln1 sampled at rising edge f10_ln1

Table 112. Clock alignment control register ...continued

CA_CTRL (address 00C5h)				
Bit	Symbol	Access	Value	Description
0	SEL_RF_F10_P_LN0	R/W		physical lane 0 sampling mode (see <a href="#">Section 11.7.5.2</a> )
			0	<b>din_ca_in0 sampled at falling edge f10_in0</b>
			1	din_ca_in0 sampled at rising edge f10_in0

Table 113. Inter-lane alignment control register

ILA_CTRL_1 (address 00C7h)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.7</a> )
6 to 5	RESERVED	R/W	00	reserved to 0
4 to 2	SEL_LOCK[2:0]	R/W		inter-lane alignment start mode
			000	<b>inter-lane alignment can only start if all (4 or 2) lanes are locked</b>
			001	inter-lane alignment can start if one of the (4 or 2) lanes are locked
			010	inter-lane alignment can start if lane 0 is locked
			011	inter-lane alignment can start if lane 1 is locked
			100	inter-lane alignment can start if lane 2 is locked
			101	inter-lane alignment can start if lane 3 is locked
1	ILA_SYNC	R/W		inter-lane alignment enable
			0	inter-lane alignment synchronization disabled
			1	<b>inter-lane alignment synchronization enabled</b>
0	DATA_DESCR_EN	R/W		data descrambling (see <a href="#">Section 11.7.5.3</a> )
			0	disabled
			1	<b>enabled</b>

Table 114. Force alignment register

FORCE_ALIGN (address 00C8h)				
Bit	Symbol	Access	Value	Description
5 to 2	MAN_LOCK_LN_MSB[3:0]	R/W	-	most significant 4 bits of man_lock_ln
1	DYN_REALIGN_EN	R/W		dynamic realignment mode
			0	<b>no dynamic realignment</b>
			1	dynamic realignment (and monitoring) enabled
0	FORCE_ALIGN	R/W		lane alignment mode
			0	<b>automatic lane alignment based on /A/ symbols</b>
			1	manual lane alignment based on man_align_inx

**Table 115. Manual alignment registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.7</a> )
00C9h	MAN_ALIGN_P_LN_1_0	7 to 4	MAN_ALIGN_P_LN1[3:0]	R/W	0h	indicates alignment data-delay for physical lane 1 [1..15]
		3 to 0	MAN_ALIGN_P_LN0[3:0]		0h	indicates alignment data-delay for physical lane 0 [1..15]
00CAh	MAN_ALIGN_P_LN_3_2	7 to 4	MAN_ALIGN_P_LN3[3:0]	R/W	0h	indicates alignment data-delay for physical lane 3 [1..15]
		3 to 0	MAN_ALIGN_P_LN2[3:0]		0h	indicates alignment data-delay for physical lane 2 [1..15]

**Table 116. Synchronization output modes register**

Default settings are shown highlighted.

SYNC_OUT_MOD (address 00CCh)					
Bit	Symbol	Access	Value	Description	
4	SYNC_POL	R/W	0	synchronization polarity (see <a href="#">Section 11.7.5.6</a> ) <b>sync_out is active when LOW</b>	
			1	sync_out is active when HIGH	
3	SYNC_INIT_LVL	R/W	0	synchronization initialization level (see <a href="#">Section 11.7.5.6</a> ) synchronization starts with '0'	
			1	synchronization starts with '1'	
2 to 0	SEL_SYNC[2:0]	R/W	000	synchronization mode (see <a href="#">Section 11.7.5.6</a> ) <b>sync_request active when state machine of one of the lanes is in CS_INIT mode</b>	
			001	sync_request active when state machine of all lanes is in CS_INIT mode	
			010	sync_request active when state machine of lane 0 is in CS_INIT mode	
			011	sync_request active when state machine of lane 1 is in CS_INIT mode	
			100	sync_request active when state machine of lane 2 is in CS_INIT mode	
			101	sync_request fixed to 1	
			110	sync_request fixed to 0	

**Table 117. Physical lane polarity register**

P_LN_POL (address 00CDh)					
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.1</a> )	
3	POL_P_LN3	R/W	0	physical lane 3 data polarity <b>no action</b>	
			1	invert all data bits of lane 3	
2	POL_P_LN2	R/W	0	physical lane 2 data polarity <b>no action</b>	
			1	invert all data bits of lane 2	

Table 117. Physical lane polarity register ...continued

P_LN_POL (address 00CDh)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.1</a> )
1	POL_P_LN1	R/W		physical lane 1 data polarity
			0	<b>no action</b>
			1	invert all data bits of lane 1]
0	POL_P_LN0	R/W		physical lane 0 data polarity
			0	<b>no action</b>
			1	invert all data bits of lane 0

Table 118. Physical lane selection register

Default settings are shown highlighted.

P_LN_SEL register (address 00CEh)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.4</a> and <a href="#">Section 11.7.5.4</a> )
7 to 6	SEL_P_LN3[1:0]	R/W		lane 3 data mapping
			00	physical lane 3 is mapped to internal lane 0
			01	physical lane 3 is mapped to internal lane 1
			10	physical lane 3 is mapped to internal lane 2
			<b>11</b>	<b>physical lane 3 is mapped to internal lane 3</b>
5 to 4	SEL_P_LN2[1:0]	R/W		lane 2 data mapping
			00	physical lane 2 is mapped to internal lane 0
			01	physical lane 2 is mapped to internal lane 1
			<b>10</b>	<b>physical lane 2 is mapped to internal lane 2</b>
			11	physical lane 2 is mapped to internal lane 3
3 to 2	SEL_P_LN1[1:0]	R/W		lane 1 data mapping
			00	physical lane 1 is mapped to internal lane 0
			<b>01</b>	<b>physical lane 1 is mapped to internal lane 1</b>
			10	physical lane 1 is mapped to internal lane 2
			11	physical lane 1 is mapped to internal lane 3
1 to 0	SEL_P_LN0[1:0]	R/W		lane 0 data mapping
			<b>00</b>	<b>physical lane 0 is mapped to internal lane 0</b>
			01	physical lane 0 is mapped to internal lane 1
			10	physical lane 0 is mapped to internal lane 2
			11	physical lane 0 is mapped to internal lane 3

**Table 119. Descrambler initialization values registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.3</a> )
00D1h	INIT_DESCR_P_LN0_MSB	7 to 0	INIT_DESCR_P_LN0[15:8]	R/W	00h	initialization value for physical lane 0 descrambler 8 most significant bits
00D2h	INIT_DESCR_P_LN0_LSB	6 to 0	INIT_DESCR_P_LN0[7:1]	R/W	00h	initialization value for physical lane 0 descrambler 7 least significant bits
00D3h	INIT_DESCR_P_LN1_MSB	7 to 0	INIT_DESCR_P_LN1[15:8]	R/W	00h	initialization value for physical lane 1 descrambler 8 most significant bits
00D4h	INIT_DESCR_P_LN1_LSB	6 to 0	INIT_DESCR_P_LN1[7:1]	R/W	00h	initialization value for physical lane 1 descrambler 7 least significant bits
00D5h	INIT_DESCR_P_LN2_MSB	7 to 0	INIT_DESCR_P_LN2[15:8]	R/W	00h	initialization value for physical lane 2 descrambler 8 most significant bits
00D6h	INIT_DESCR_P_LN2_LSB	6 to 0	INIT_DESCR_P_LN2[7:1]	R/W	00h	initialization value for physical lane 2 descrambler 7 least significant bits
00D7h	INIT_DESCR_P_LN3_MSB	7 to 0	INIT_DESCR_P_LN3[15:8]	R/W	00h	initialization value for physical lane 3 descrambler 8 most significant bits
00D8h	INIT_DESCR_P_LN3_LSB	6 to 0	INIT_DESCR_P_LN3[7:1]	R/W	00h	initialization value for physical lane 3 descrambler 7 least significant bits
00D9h	INIT_ILA_BUFF_PNTR_L_LN01	7 to 4	INIT_ILA_BUFFPTR_P_LN1[3:0]	R/W	88h	initialization value for logical lane 1 ILA buffer pointer (see <a href="#">Section 11.7.5.7</a> )
		3 to 0	INIT_ILA_BUFF_PNTR_P_LN0[3:0]	R/W	88h	initialization value for logical lane 0 ILA buffer pointer (see <a href="#">Section 11.7.5.7</a> )
00DAh	INIT_ILA_BUFF_PNTR_L_LN23	7 to 4	INIT_ILA_BUFF_PNTR_L_LN3[3:0]	R/W	88h	initialization value for logical lane 3 ILA buffer pointer (see <a href="#">Section 11.7.5.7</a> )
		3 to 0	INIT_ILA_BUFF_PNTR_L_LN2[3:0]	R/W	88h	initialization value for logical lane 2 ILA buffer pointer (see <a href="#">Section 11.7.5.7</a> )

**Table 120. Error handling register**

Default settings are shown highlighted.

ERR_HNDLNG (address 00DBh)					
Bit	Symbol	Access	Value	Description	
7	DISP_ERR_LN3_EN	R/W	0	no action	
			1	<b>not-in-table errors passed to frame assembler</b>	
6	DISP_ERR_LN2_EN	R/W	0	no action	
			1	<b>not-in-table errors passed to frame assembler</b>	

**Table 120. Error handling register ...continued**

Default settings are shown highlighted.

ERR_HNDLNG (address 00DBh)				
Bit	Symbol	Access	Value	Description
5	DISP_ERR_LN1_EN	R/W	0	no action
			1	<b>not-in-table errors passed to frame assembler</b>
4	DISP_ERR_LN0_EN	R/W	0	no action
			1	<b>not-in-table errors passed to frame assembler</b>
0	IGN_ERR	R/W	0	general error mode (see <a href="#">Section 11.7.5.11</a> )
			1	<b>no action</b> ignore disparity/nit-errors at lane-controller

**Table 121. Reinitialization control register**

Default settings are shown highlighted.

REINIT_CTRL (address 00DCh)				
Bit	Symbol	Access	Value	Description
7	REINIT_ILA_L_LN3	R/W	0	logical lane 3, ila buffer out-of-range check (see <a href="#">Section 11.7.5.7</a> )
			1	<b>no action</b> lane 3 ila buffer out-of-range_error activates reinitialization
6	REINIT_ILA_L_LN2	R/W	0	logical lane 2, ila buffer out-of-range check (see <a href="#">Section 11.7.5.7</a> )
			1	<b>no action</b> lane 2 ila buffer out-of-range_error activates reinitialization
5	REINIT_ILA_L_LN1	R/W	0	logical lane 1, ila buffer out-of-range check (see <a href="#">Section 11.7.5.7</a> )
			1	<b>no action</b> lane 1 ila buffer out-of-range_error activates reinitialization
4	REINIT_ILA_L_LN0	R/W	0	logical lane 0, ila buffer out-of-range check (see <a href="#">Section 11.7.5.7</a> )
			1	<b>no action</b> lane 0 ila buffer out-of-range_error activates reinitialization
3	RESYNC_OLINK_P_LN3	R/W	0	physical lane 3, resynchronization over link (see <a href="#">Section 11.7.5.10</a> )
			1	<b>no action</b> lane 3 lane controller checks for K28.5 /K/ symbols
2	RESYNC_OLINK_P_LN2	R/W	0	physical lane 2, resynchronization over link (see <a href="#">Section 11.7.5.10</a> )
			1	<b>no action</b> lane 2 lane controller checks for K28.5 /K/ symbols

**Table 121. Reinitialization control register ...continued**

Default settings are shown highlighted.

REINIT_CTRL (address 00DCh)				
Bit	Symbol	Access	Value	Description
1	RESYNC_OLINK_P_LN1	R/W		physical lane 1, resynchronization over link (see <a href="#">Section 11.7.5.10</a> )
			0	<b>no action</b>
			1	lane 1 lane controller checks for K28.5 /K/ symbols
			0	<b>no action</b>
0	RESYNC_OLINK_P_LN0	R/W		physical lane 0, resynchronization over link (see <a href="#">Section 11.7.5.10</a> )
			0	<b>no action</b>
			1	lane 0 controller checks for K28.5 /K/ symbols

**Table 122. Miscellaneous control register**

MISC_CTRL (address 00DDh)				
Bit	Symbol	Access	Value	Description
7	DLP-STROBE	R/W		captures 16-bit data inside the DLP for each lane (see <a href="#">Section 11.7.6.4</a> )
			0	no action
			1	update DLP samples
			00	reserved to 00
1 to 0	RESERVED[1:0]	R/W	00	reserved to 00

**Table 123. LMF control register**

LMF_CTRL register (address 00DEh)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.9</a> )
7 to 5	L[2:0]	R/W	-	number of lanes [1, 2, 4]
4 to 3	M[1:0]	R/W	-	number of converters [1]
2 to 0	F[2:0]	R/W	-	number of octets/frame [1, 2, 4]

### 11.11.8 RX digital lane processing monitoring block

This block of registers enables the monitoring of the digital lane processing, ensuring the data is decoded correctly. The validity of the link can also be tested by using simple Bit Error Rate testing and be monitored through various available flags and counters registers.

#### 11.11.8.1 RX digital lane processing monitoring block register allocation map description

[Table 124](#) shows an overview of all the RX digital lane processing monitoring registers.

**Table 124. RX digital lane processing monitoring block register allocation map**

Register name		R/W	Bit definition								Default <sup>(1)</sup>	
			b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
00E0h	ILA_MON_L_LN_1_0	R	ILA_MON_L_LN1[3:0]				ILA_MON_L_LN0[3:0]				uuuu	uuh
00E1h	ILA_MON_L_LN_3_2	R	ILA_MON_L_LN3[3:0]				ILA_MON_L_LN2[3:0]				uuuu	uuh
00E2h	ILA_BUFF_ERR	R	-	-	-	-	ILA_BUFF_ERR_L_LN3	ILA_BUFF_ERR_L_LN2	ILA_BUFF_ERR_L_LN1	ILA_BUFF_ERR_L_LN0	uuuu	uuh
00E4h	DEC_FLAGS	R	DEC_NIT_ERR_P_LN3	DEC_NIT_ERR_P_LN2	DEC_NIT_ERR_P_LN1	DEC_NIT_ERR_P_LN0	DEC_DISP_ERR_P_LN3	DEC_DISP_ERR_P_LN2	DEC_DISP_ERR_P_LN1	DEC_DISP_ERR_P_LN0	uuuu	uuh
00E5h	KOUT_FLAG	R	-	-	-	-	DEC_KOUT_L_LN3	DEC_KOUT_L_LN2	DEC_KOUT_L_LN1	DEC_KOUT_L_LN0	uuuu	uuh
00E6h	K28_P_LN0_FLAG	R	-	-	-	K28_7_P_LN0	K28_5_P_LN0	K28_4_P_LN0	K28_3_P_LN0	K28_0_P_LN0	uuuu	uuh
00E7h	K28_P_LN1_FLAG	R	-	-	-	K28_7_P_LN1	K28_5_P_LN1	K28_4_P_LN1	K28_3_P_LN1	K28_0_P_LN1	uuuu	uuh
00E8h	K28_P_LN2_FLAG	R	-	-	-	K28_7_P_LN2	K28_5_P_LN2	K28_4_P_LN2	K28_3_P_LN2	K28_0_P_LN2	uuuu	uuh
00E9h	K28_P_LN3_FLAG	R	-	-	-	K28_7_P_LN3	K28_5_P_LN3	K28_4_P_LN3	K28_3_P_LN3	K28_0_P_LN3	uuuu	uuh
00EAh	KOUT_UNEXP_FLAG	R	-	-	-	-	DEC_KOUT_UNEXP_L_LN3	DEC_KOUT_UNEXP_L_LN2	DEC_KOUT_UNEXP_L_LN1	DEC_KOUT_UNEXP_L_LN0	uuuu	uuh
00EBh	LOCK_CNT_MON_LN01	R	LOCK_CNT_MON_P_LN1[3:0]				LOCK_CNT_MON_P_LN0[3:0]				uuuu	uuh
00ECh	LOCK_CNT_MON_LN23	R	LOCK_CNT_MON_P_LN3[3:0]				LOCK_CNT_MON_P_LN2[3:0]				uuuu	uuh

**Table 124. RX digital lane processing monitoring block register allocation map ...continued**

Register name		R/W	Bit definition								Default <sup>[1]</sup>		
			b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex	
00EDh	CS_STATE_LNX	R	CS_STATE_P_LN3[1:0]		CS_STATE_P_LN2[1:0]		CS_STATE_P_LN1[1:0]		CS_STATE_P_LN0[1:0]		uuuu uuuu	uuh	
00EEh	MISC_FLAG_CTRL	R/W	RST_BUFF_ERR_FLAGS	AUTO_RST_FLAG_CNTRS	HOLD_FLAG_CNT_EN	RESERVED[4:0]						0000 0000	00h
00EFh	INTR_MISC_EN	R/W	INTR_BUFF_EN_CS_INIT_P_LN3	INTR_EN_CS_INIT_P_LN2	INTR_EN_CS_INIT_P_LN1	INTR_EN_CS_INIT_P_LN0	INTR_EN_BUFF_ERR_L_LN3	INTR_EN_BUFF_ERR_L_LN2	INTR_EN_BUFF_ERR_L_LN1	INTR_EN_BUFF_ERR_L_LN0	0000 0000	00h	
00F0h	FLAG_CNT_LN0_LSB	R	FLAG_CNT_LN0[7:0]								uuuu uuuu	uuh	
00F1h	FLAG_CNT_LN0_MSB	R	FLAG_CNT_LN0[15:8]								uuuu uuuu	uuh	
00F2h	FLAG_CNT_LN1_LSB	R	FLAG_CNT_LN1[7:0]								uuuu uuuu	uuh	
00F3h	FLAG_CNT_LN1_MSB	R	FLAG_CNT_LN1[15:8]								uuuu uuuu	uuh	
00F4h	FLAG_CNT_LN2_LSB	R	FLAG_CNT_LN2[7:0]								uuuu uuuu	uuh	
00F5h	FLAG_CNT_LN2_MSB	R	FLAG_CNT_LN2[15:8]								uuuu uuuu	uuh	
00F6h	FLAG_CNT_LN3_LSB	R	FLAG_CNT_LN3[7:0]								uuuu uuuu	uuh	
00F7h	FLAG_CNT_LN3_MSB	R	FLAG_CNT_LN3[15:8]								uuuu uuuu	uuh	
00F8h	SER_LVL_LSB	R/W	SER_LVL[7:0]								0000 0000	00h	
00F9h	SER_LVL_MSB	R/W	SER_LVL[15:8]								0000 0000	00h	
00FAh	INTR_EN	R/W	INTR_EN_NIT	INTR_EN_DISP	INTR_EN_KOUT	INTR_EN_KOUT_UNEXP	INTR_EN_K28_7	INTR_EN_K28_5	INTR_EN_K28_3	INTR_EN_MISC	0000 0000	00h	
00FBh	CTRL_FLAG_CNT_LN10	R/W	RST_CTRL_FLAG_CNT_LN1	SEL_CTRL_FLAG_CNT_LN1[2:0]			RST_CTRL_FLAG_CNT_LN0	SEL_CTRL_FLAG_CNT_LN0[2:0]			0101 0101	55h	

Table 124. RX digital lane processing monitoring block register allocation map ...continued

Register name		R/W	Bit definition								Default <sup>[1]</sup>	
			b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
00FCh	CTRL_FLAG_CNT_LN32	R/W	RST_CTRL_FLAG_CNT_LN3	SEL_CTRL_FLAG_CNT_LN3[2:0]			RST_CTRL_FLAG_CNT_LN2	SEL_CTRL_FLAG_CNT_LN2[2:0]			0101 0101	55h
00FDh	RST_MON_FLAGS	R/W	RST_NIT_ERR_FLAGS	RST_DISP_ERR_FLAGS	RST_KOUT_FLAGS	RST_KOUT_UNEXP_FLAGS	RST_K28_LN3_FLAGS	RST_K28_LN2_FLAGS	RST_K28_LN1_FLAGS	RST_K28_LN0_FLAGS	0000 0000	00h
00FEh	DBG_CTRL	R/W	SER_MOD	INTR_CLR	INTR_MOD[2:0]			DBG_MOD[2:0]			0000 0000	00h

[1] u = undefined at power-up or after reset.

### 11.11.8.2 RX digital lane processing monitoring block bit definition detailed description

The tables in this section contain detailed descriptions of the RX digital lane processing monitoring registers.

**Table 125. Inter-lane alignment monitor registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.7</a> )
00E0h	ILA_MON_L_LN_1_0	7 to 4	ILA_MON_L_LN1[3:0]	R	-	ila_buf_l_ln1 pointer
		3 to 0	ILA_MON_L_LN0[3:0]		-	ila_buf_l_ln0 pointer
00E1h	ILA_MON_L_LN_3_2	7 to 4	ILA_MON_L_LN3[3:0]	R	-	ila_buf_l_ln3 pointer
		3 to 0	ILA_MON_L_LN2[3:0]		-	ila_buf_l_ln2 pointer

**Table 126. Inter-lane alignment buffer error register**

Default settings are shown highlighted.

ILA_BUFF_ERR (address 00E2h)						
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.7</a> )		
3	ILA_BUFF_ERR_L_LN3	R		logical lane 3 ila buffer error		
			0	ila_buf_l_ln3 pointer is in range		
			1	ila_buf_l_ln3 pointer is out of range		
2	ILA_BUFF_ERR_L_LN2	R		logical lane 2 ila buffer error		
			0	ila_buf_l_ln2 pointer is in range		
			1	ila_buf_l_ln2 pointer is out of range		
1	ILA_BUFF_ERR_L_LN1	R		logical lane 1 ila buffer error		
			0	ila_buf_l_ln1 pointer is in range		
			1	ila_buf_l_ln1 pointer is out of range		
0	ILA_BUFF_ERR_L_LN0	R		logical lane 0 ila buffer error		
			0	ila_buf_l_ln0 pointer is in range		
			1	ila_buf_l_ln0 pointer is out of range		

Table 127. Decoder flags register

DEC_FLAGS (address 00E4h)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.11</a> )
7	DEC_NIT_ERR_P_LN3	R	-	decoder not-in-table error flag physical lane 3
6	DEC_NIT_ERR_P_LN2	R	-	decoder not-in-table error flag physical lane 2
5	DEC_NIT_ERR_P_LN1	R	-	decoder not-in-table error flag physical lane 1
4	DEC_NIT_ERR_P_LN0	R	-	decoder not-in-table error flag physical lane 0
3	DEC_DISP_ERR_P_LN3	R	-	decoder disparity error flag physical lane 3
2	DEC_DISP_ERR_P_LN2	R	-	decoder disparity error flag physical lane 2
1	DEC_DISP_ERR_P_LN1	R	-	decoder disparity error flag physical lane 1
0	DEC_DISP_ERR_P_LN0	R	-	decoder disparity error flag physical lane 0

Table 128. Decoder /K/ symbols flag register

KOUT_FLAG (address 00E5h)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.11</a> )
3	DEC_KOUT_L_LN3	R	-	decoder: /K/ symbols found in physical lane 3
2	DEC_KOUT_L_LN2	R	-	decoder: /K/ symbols found in physical lane 2
1	DEC_KOUT_L_LN1	R	-	decoder: /K/ symbols found in physical lane 1
0	DEC_KOUT_L_LN0	R	-	decoder: /K/ symbols found in physical lane 0

Table 129. K28 flag registers

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.11</a> )
00E6h	K28_P_LN0_P_FLAG	4	K28_7_P_LN0	R	-	K28_7 /F/ symbols found in physical lane 0
		3	K28_5_P_LN0		-	K28_5 /K/ symbols found in physical lane 0
		2	K28_4_P_LN0		-	K28_4 /Q/ symbols found in physical lane 0
		1	K28_3_P_LN0		-	K28_3 /A/ symbols found in physical lane 0
		0	K28_0_P_LN0		-	K28_0 /R/ symbols found in physical lane 0
00E7h	K28_P_LN1_P_FLAG	4	K28_7_P_LN1	R	-	K28_7 /F/ symbols found in physical lane 1
		3	K28_5_P_LN1		-	K28_5 /K/ symbols found in physical lane 1
		2	K28_4_P_LN1		-	K28_4 /Q/ symbols found in physical lane 1
		1	K28_3_P_LN1		-	K28_3 /A/ symbols found in physical lane 1
		0	K28_0_P_LN1		-	K28_0 /R/ symbols found in physical lane 1

**Table 129. K28 flag registers ...continued**  
 Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.11</a> )
00E8h	K28_P_LN2_P_FLAG	4	K28_7_P_LN2	R	-	K28_7 /F/ symbols found in physical lane 2
		3	K28_5_P_LN2		-	K28_5 /K/ symbols found in physical lane 2
		2	K28_4_P_LN2		-	K28_4 /Q/ symbols found in physical lane 2
		1	K28_3_P_LN2		-	K28_3 /A/ symbols found in physical lane 2
		0	K28_0_P_LN2		-	K28_0 /R/ symbols found in physical lane 2
00E9h	K28_P_LN3_P_FLAG	4	K28_7_P_LN3	R	-	K28_7 /F/ symbols found in physical lane 3
		3	K28_5_P_LN3		-	K28_5 /K/ symbols found in physical lane 3
		2	K28_4_P_LN3		-	K28_4 /Q/ symbols found in physical lane 3
		1	K28_3_P_LN3		-	K28_3 /A/ symbols found in physical lane 3
		0	K28_0_P_LN3		-	K28_0 /R/ symbols found in physical lane 3

**Table 130. Decoder unexpected /K/ symbols flag register**

KOUT_UNEXP_FLAG (address 00EAh)					
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.11</a> )	
3	DEC_KOUT_UNEXP_L_LN3	R	-	decoder: unexpected /K/ symbols found in logical lane 3	
2	DEC_KOUT_UNEXP_L_LN2	R	-	decoder: unexpected /K/ symbols found in logical lane 2	
1	DEC_KOUT_UNEXP_L_LN1	R	-	decoder: unexpected /K/ symbols found in logical lane 1	
0	DEC_KOUT_UNEXP_L_LN0	R	-	decoder: unexpected /K/ symbols found in logical lane 0	

**Table 131. Lock counter monitor registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.6</a> )
0Bh	LOCK_CNT_MON_P_LN01	7 to 4	LOCK_CNT_MON_P_LN1[3:0]	R	-	lock_state monitor synchronization word alignment physical lane 1
		3 to 0	LOCK_CNT_MON_P_LN0[3:0]		-	lock_state monitor synchronization word alignment physical lane 0
0Ch	LOCK_CNT_MON_P_LN23	7 to 4	LOCK_CNT_MON_P_LN3[3:0]	R	-	lock_state monitor synchronization word alignment physical lane 3
		3 to 0	LOCK_CNT_MON_P_LN2[3:0]		-	lock_state monitor synchronization word alignment physical lane 2

**Table 132. Lane code synchronization state register**

Default settings are shown highlighted.

CS_STATE_LNX (address 00EDh)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.5</a> )
7 to 6	CS_STATE_P_LN3[1:0]	R	-	monitor cs_state fsm physical lane 3
5 to 4	CS_STATE_P_LN2[1:0]	R	-	monitor cs_state fsm physical lane 2
3 to 2	CS_STATE_P_LN1[1:0]	R	-	monitor cs_state fsm physical lane 1
1 to 0	CS_STATE_P_LN0[1:0]	R	-	monitor cs_state fsm physical lane 0

**Table 133. Reset buffer error flags register**

Default settings are shown highlighted.

RST_BUF_ERR_FLAGS (address 00EEh)				
Bit	Symbol	Access	Value	Description
7	RST_BUF_ERR_FLAGS	R/W	0	reset ILA_BUF_ERR_LN <sub>x</sub> flags (see <a href="#">Section 11.7.5.7</a> )
6	AUTO_RST_FLAG_CNTS	R/W	0	FLAGS counters are reset when DLP is reset (see <a href="#">Section 11.7.6.1</a> )
5	HOLD_FLAG_CNT_EN	R/W	0	see <a href="#">Section 11.7.6.1</a>

**Table 134. Miscellaneous interrupt enable register**

Default settings are shown highlighted.

INTR_MISC_EN (address 00EFh)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.3</a> )
7	INTR_EN_CS_INIT_P_LN3	R/W	0	<b>no action</b>
			1	intr_misc in case cs_state_p_l <sub>n3</sub> = cs_init
6	INTR_EN_CS_INIT_P_LN2	R/W	0	<b>no action</b>
			1	intr_misc in case cs_state_p_l <sub>n2</sub> = cs_init
5	INTR_EN_CS_INIT_P_LN1	R/W	0	<b>no action</b>
			1	intr_misc in case cs_state_p_l <sub>n1</sub> = cs_init

**Table 134. Miscellaneous interrupt enable register ...continued**

Default settings are shown highlighted.

INTR_MISC_EN (address 00EFh)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.3</a> )
4	INTR_EN_CS_INIT_P_LN0	R/W	0	<b>no action</b>
			1	intr_misc in case cs_state_p_ln0 = cs_init
3	INTR_EN_BUFF_ERR_L_LN3	R/W	0	<b>no action</b>
			1	generate interrupt if ILA_BUF_ERR_L_LN3 = 1
2	INTR_EN_BUFF_ERR_L_LN2	R/W	0	<b>no action</b>
			1	generate interrupt if ILA_BUF_ERR_L_LN2 = 1
1	INTR_EN_BUFF_ERR_L_LN1	R/W	0	<b>no action</b>
			1	generate interrupt if ILA_BUF_ERR_L_LN1 = 1
0	INTR_EN_BUFF_ERR_L_LN0	R/W	0	<b>no action</b>
			1	generate interrupt if ILA_BUF_ERR_L_LN0 = 1

**Table 135. LSB/MSB of flag\_counter lane registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.6.1</a> )
00F0h	FLAG_CNT_LN0_LSB	7 to 0	FLAG_CNT_LN0[7:0]	R	-	8 least significant bits of flag counter lane 0
00F1h	FLAG_CNT_LN0_MSB	7 to 0	FLAG_CNT_LN0[15:8]	R	-	8 most significant bits of flag_counter lane 0
00F2h	FLAG_CNT_LN1_LSB	7 to 0	FLAG_CNT_LN1[7:0]	R	-	8 least significant bits of flag counter lane 1
00F3h	FLAG_CNT_LN1_MSB	7 to 0	FLAG_CNT_LN1[15:8]	R	-	8 most significant bits of flag_counter lane 1
00F4h	FLAG_CNT_LN2_LSB	7 to 0	FLAG_CNT_LN2[7:0]	R	-	8 least significant bits of flag counter lane 2
00F5h	FLAG_CNT_LN2_MSB	7 to 0	FLAG_CNT_LN2[15:8]	R	-	8 most significant bits of flag_counter lane 2
00F6h	FLAG_CNT_LN3_LSB	7 to 0	FLAG_CNT_LN3[7:0]	R	-	8 least significant bits of flag counter lane 3
00F7h	FLAG_CNT_LN3_MSB	7 to 0	FLAG_CNT_LN3[15:8]	R	-	8 most significant bits of flag_counter lane 3

**Table 136. LSB/MSB SER measurement registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.6.2</a> )
00F8h	SER_LVL_LSB	7 to 0	SER_LVL[7:0]	R/W	00h	8 least significant bits used for simple (DC) SER measurement
00F9h	SER_LVL_MSB	7 to 0	SER_LVL[15:8]	R/W	00h	8 most significant bits for simple (DC) SER measurement

Table 137. Interrupt enable register

INTR_EN (address 00FAh)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.4</a> )
7	INTR_EN_NIT	R/W		not-in-table interrupt
			0	<b>no action</b>
			1	nit_error impacts global interrupt as per INTR_MODE configuration (bit 1E)
			0	<b>no action</b>
6	INTR_EN_DISP	R/W		disparity-error interrupt
			0	<b>no action</b>
			1	disparity-error in ln<x> affects i_ln<x>
			0	<b>no action</b>
5	INTR_EN_KOUT	R/W		K-character interrupt
			0	<b>no action</b>
			1	detection k-control character in ln<x> affects i_ln<x>
			0	<b>no action</b>
4	INTR_EN_KOUT_UNEXP	R/W		unexpected K-character interrupt
			0	<b>no action</b>
			1	detection unexpected K-character in ln<x> affects i_ln<x>
			0	<b>no action</b>
3	INTR_EN_K28_7	R/W		K28_7 interrupt
			0	<b>no action</b>
			1	detection K28_7 in ln<x> affects i_ln<x>
			0	<b>no action</b>
2	INTR_EN_K28_5	R/W		K28_5 interrupt
			0	<b>no action</b>
			1	detection K28_5 in ln<x> affects i_ln<x>
			0	<b>no action</b>
1	INTR_EN_K28_3	R/W		K28_3 interrupt
			0	<b>no action</b>
			1	detection K28_3 in ln<x> affects i_ln<x>
			0	<b>no action</b>
0	INTR_EN_MISC	R/W		miscellaneous interrupt intr_misc (see reg x0F)
			0	<b>no action</b>
			1	detection depends on intr_misc_ena (see <a href="#">Table 134</a> )

Table 138. Flag counter control registers

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.6.1</a> )
00FBh	CTRL_FLAG_CNT_LN10	7	RST_CTRL_FLAG_CNT_LN1	R/W	0	reset FLAG_CNT_LN1
		6 to 4	SEL_CTRL_FLAG_CNT_LN1[2:0]		5h	select FLAG_CNT_LN1 source
		3	RST_CTRL_FLAG_CNT_LN0		0	reset FLAG_CNT_LN0
		2 to 0	SEL_CTRL_FLAG_CNT_LN0[2:0]		5h	select FLAG_CNT_LN0 source

**Table 138. Flag counter control registers ...continued**  
 Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.6.1</a> )
00FCh	CTRL_FLAG_CNT_LN32	7	RST_CTRL_FLAG_CNT_LN3	R/W	0	reset FLAG_CNT_LN3
		6 to 4	SEL_CTRL_FLAG_CNT_LN3[2:0]		5h	select FLAG_CNT_LN3 source
		3	RST_CTRL_FLAG_CNT_LN2		0	reset FLAG_CNT_LN2
		2 to 0	SEL_CTRL_FLAG_CNT_LN2[2:0]		5h	select FLAG_CNT_LN2 source

**Table 139. Reset flags monitor register**

MON_FLAGS_RST (address 00FDh)					
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.5.11</a> )	
7	RST_NIT_ERR_FLAGS	R/W	0	reset not-in-table error monitor flags	
6	RST_DISP_ERR_FLAGS	R/W	0	reset disparity monitor flags	
5	RST_KOUT_FLAGS	R/W	0	reset /K/ symbols monitor flags	
4	RST_KOUT_UNEXP_FLAGS	R/W	0	reset unexpected /K/ symbols monitor flags	
3	RST_K28_LN3_FLAGS	R/W	0	reset K28_x monitor flags for lane 3	
2	RST_K28_LN2_FLAGS	R/W	0	reset K28_x monitor flags for lane 2	
1	RST_K28_LN1_FLAGS	R/W	0	reset K28_x monitor flags for lane 1	
0	RST_K28_LN0_FLAGS	R/W	0	reset K28_x monitor flags for lane 0	

**Table 140. Sample error rate interrupts control register**

SER_INTR_CTRL (address 00FEh)					
Bit	Symbol	Access	Value	Description	
7	SER_MOD	R/W		simple BER-measurement	
			0	<b>no action</b>	
			1	simple BER measurement enabled	
6	INTR_RST	R/W		interrupts clear	
			0	<b>no action</b>	
			1	clear interrupts (to '1')	
5 to 3	INTR_MOD[2:0]	R/W		interrupt settings	
			000	<b>DLP interrupt depends on lane 0</b>	
			001	DLP interrupt depends on lane 1	
			010	DLP interrupt depends on lane 2	
			011	DLP interrupt depends on lane 3	
			100	DLP interrupt depends on lane 0 or lane 2	
			101	DLP interrupt depends on lane 0 or lane 1 or lane 2 or lane 3	
			110	Hold_flagcnt (see <a href="#">Section 11.7.6.1</a> )	
111	no interrupt				

### 11.11.9 JESD204 receiver monitoring

This block of registers enables the monitoring of the JESD receiver.

#### 11.11.9.1 JESD204 receiver monitoring block register allocation map description

[Table 141](#) shows an overview of all the JESD204 receiver monitoring registers.

**Table 141. JESD204 receiver monitoring register allocation map**

Register name		R/W	Bit definition								Default <sup>[1]</sup>	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0100h	SER_CTRL_0	R/W	GEN_JTSPAT	GEN_PRBS31	CHCK_PRBS31	RD_SEL	SR_SER_CNT_LN3	SR_SER_CNT_LN2	SR_SER_CNT_LN1	SR_SER_CNT_LN0	0000 0000	00h
0101h	SER_CTRL_1	R/W	-	START_WIN_JTSPAT[6:0]						0000 0000	00h	
0102h	SER_CTRL_2	R/W	-	STOP_WIN_JTSPAT[6:0]						0111 0101	75h	
0104h	SER_CNT_LN0_ LSB	R	SER_CNT_LN0[7:0]						uuuu uuuu	uuh		
0105h	SER_CNT_LN0_ MSB	R	SER_CNT_LN0[15:8]						uuuu uuuu	uuh		
0106h	SER_CNT_LN1_ LSB	R	SER_CNT_LN1[7:0]						uuuu uuuu	uuh		
0107h	SER_CNT_LN1_ MSB	R	SER_CNT_LN1[15:8]						uuuu uuuu	uuh		
0108h	SER_CNT_LN2_ LSB	R	SER_CNT_LN2[7:0]						uuuu uuuu	uuh		
0109h	SER_CNT_LN2_ MSB	R	SER_CNT_LN2[15:8]						uuuu uuuu	uuh		
010Ah	SER_CNT_LN3_ LSB	R	SER_CNT_LN3[7:0]						uuuu uuuu	uuh		
010Bh	SER_CNT_LN3_ MSB	R	SER_CNT_LN3[15:8]						uuuu uuuu	uuh		
010Ch	FRST_SER_JTSPAT_LN0	R	-	FRST_SER_JTSPAT_LN0[6:0]						uuuu uuuu	uuh	
010Dh	FRST_SER_JTSPAT_LN1	R	-	FRST_SER_JTSPAT_LN1[6:0]						uuuu uuuu	uuh	
010Eh	FRST_SER_JTSPAT_LN2	R	-	FRST_SER_JTSPAT_LN2[6:0]						uuuu uuuu	uuh	

**Table 141. JESD204 receiver monitoring register allocation map ...continued**

Register name			R/W	Bit definition							Default <sup>[1]</sup>	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin
010Fh	FRST_SER_JTSPAT_LN3	R	-	FRST_SER_JTSPAT_LN3[6:0]							uuuu uuuu	uuh
0110h	FRST_SER_PAT_LSB_LN0	R	FRST_SER_PAT_LN0[7:0]							uuuu uuuu	uuh	
0111h	FRST_SER_PAT_MSB_LN0	R	-	-	-	-	-	-	FRST_SER_PAT_LN0[9:8]	uuuu uuuu	uuh	
0112h	FRST_SER_PAT_LSB_LN1	R	FRST_SER_PAT_LN1[7:0]							uuuu uuuu	uuh	
0113h	FRST_SER_PAT_MSB_LN1	R	-	-	-	-	-	-	FRST_SER_PAT_LN1[9:8]	uuuu uuuu	uuh	
0114h	FRST_SER_PAT_LSB_LN2	R	FRST_SER_PAT_LN2[7:0]							uuuu uuuu	uuh	
0115h	FRST_SER_PAT_MSB_LN2	R	-	-	-	-	-	-	FRST_SER_PAT_LN2[9:8]	uuuu uuuu	uuh	
0116h	FRST_SER_PAT_LSB_LN3	R	FRST_SER_PAT_LN3[7:0]							uuuu uuuu	uuh	
0117h	FRST_SER_PAT_MSB_LN3	R	-	-	-	-	-	-	FRST_SER_PAT_LN3[9:8]	uuuu uuuu	uuh	
0118h	SER_LVL_LSB	R/W	SER_LVL[7:0]							0000 0000	00h	
0119h	SER_LVL_MSB	R/W	SER_LVL[15:8]							0000 0000	00h	
011Ah	MAN_MFB_LN0	R/W	-	MAN_MFB_LN0[6:0]							00100 000	20h
011Bh	MAN_MFB_LN1	R/W	-	MAN_MFB_LN1[6:0]							0010 0000	20h
011Ch	MAN_MFB_LN2	R/W	-	MAN_MFB_LN2[6:0]							0010 0000	20h
011Dh	MAN_MFB_LN3	R/W	-	MAN_MFB_LN3[6:0]							0010 0000	20h
011Eh	FORCE_MFB_LNX	R/W	-	-	-	-	FORCE_MFB_LN3	FORCE_MFB_LN2	FORCE_MFB_LN1	FORCE_MFB_LN0	0000 0000	00h

[1] u = undefined at power-up or after reset.

### 11.11.9.2 JESD204 receiver monitoring block bit definition detailed description

The tables in this section contain detailed descriptions of the JESD204x receiver monitoring registers.

**Table 142. Sample rate error control registers**

*Default settings are shown highlighted.*

Address	Register	Bit	Symbol	Access	Value	Description
0100h	SER_CTRL_0	7	GEN_JTSPAT	R/W		jtspat generation
					0	normal operation
		1	jtspat generation active			
		6	GEN_PRBS31	R/W		prbs31 generation
					0	normal operation
		1	prbs31 generation active			
		5	CHCK_PRBS31	R/W		prbs31 sequence
					0	synchronization to prbs31 sequence
		1	check prbs31 sequence			
		4	RD_SEL	R/W		read back selection
					0	normal operation (readback WR0x01..0x02)
		1	debug mode (read ca_flags at 0x01..0x02)			
3	SR_SER_CNT_LN3	R/W		soft reset sample error rate counter lane 3		
			0	no action		
1	soft reset sample error rate counter lane 3					
2	SR_SER_CNT_LN2	R/W		soft reset sample error rate counter lane 2		
			0	no action		
1	soft reset sample error rate counter lane 2					
1	SR_SER_CNT_LN1	R/W		soft reset sample error rate counter lane 1		
			0	no action		
1	soft reset sample error rate counter lane 1					
0	SR_SER_CNT_LN0	R/W		soft reset sample error rate counter lane 0		
			0	no action		
1	soft reset sample error rate counter lane 0					
0101h	SER_CTRL_1	6 to 0	START_WIN_JTSPAT[6:0]	R/W	0000 000	start win jtspat generation (read depends on RD_SEL)
0102h	SER_CTRL_2	6 to 0	STOP_WIN_JTSPAT[6:0]	R/W	111 0101	stop window jtspat generation (read depends on RD_SEL)

**Table 143. LSB/MSB of sample error rate counter registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0104h	SER_CNT_LN0_LSB	7 to 0	SER_CNT_LN0[7:0]	R	-	8 least significant bits of sample error rate counter lane 0
0105h	SER_CNT_LN0_MSB	7 to 0	SER_CNT_LN0[15:8]	R	-	8 most significant bits of sample error rate counter lane 0
0106h	SER_CNT_LN1_LSB	7 to 0	SER_CNT_LN1[7:0]	R	-	8 least significant bits of sample error rate counter lane 1
0107h	SER_CNT_LN1_MSB	7 to 0	SER_CNT_LN1[15:8]	R	-	8 most significant bits of sample error rate counter lane 1
0108h	SER_CNT_LN2_LSB	7 to 0	SER_CNT_LN2[7:0]	R	-	8 least significant bits of sample error rate counter lane 2
0109h	SER_CNT_LN2_MSB	7 to 0	SER_CNT_LN2[15:8]	R	-	8 most significant bits of sample error rate counter lane 2
010Ah	SER_CNT_LN3_LSB	7 to 0	SER_CNT_LN3[7:0]	R	-	8 least significant bits of sample error rate counter lane 3
010Bh	SER_CNT_LN3_MSB	7 to 0	SER_CNT_LN3[15:8]	R	-	8 most significant bits of sample error counter lane 3

**Table 144. First JTSPAT with sample error rate registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
010Ch	FRST_SER_JTSPAT_LN0	6 to 0	FRST_SER_JTSPAT_LN0[6:0]	R	-	indication of first jtspat with sample error rate for lane 0
010Dh	FRST_SER_JTSPAT_LN1	6 to 0	FRST_SER_JTSPAT_LN1[6:0]	R	-	indication of first jtspat with sample error rate for lane 1
010Eh	FRST_SER_JTSPAT_LN2	6 to 0	FRST_SER_JTSPAT_LN2[6:0]	R	-	indication of first jtspat with sample error rate for lane 2
010Fh	FRST_SER_JTSPAT_LN3	6 to 0	FRST_SER_JTSPAT_LN3[6:0]	R	-	indication of first jtspat with sample error rate for lane 3

**Table 145. LSB/MSB of first sample error rate pattern registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0110h	FRST_SER_PAT_LN0_LSB	7 to 0	FRST_SER_PAT_LN0[7:0]	R	-	8 least significant bits of first sample error rate pattern lane 0
0111h	FRST_SER_PAT_LN0_MSB	1 to 0	FRST_SER_PAT_LN0[9:8]	R	-	2 most significant bits first sample error rate pattern lane 0
0112h	FRST_SER_PAT_LN1_LSB	7 to 0	FRST_SER_PAT_LN1[9:8]	R	-	8 least significant bits of first sample error rate pattern lane 1
0113h	FRST_SER_PAT_LN1_MSB	1 to 0	FRST_SER_PAT_LN1[9:8]	R	-	2 most significant bits first sample error rate pattern lane 1
0114h	FRST_SER_PAT_LSB_LN2	7 to 0	FRST_SER_PAT_LN2[7:0]	R	-	8 least significant bits of first sample error rate pattern lane 2

**Table 145. LSB/MSB of first sample error rate pattern registers ...continued**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0115h	FRST_SER_PAT_LN2_MSB	1 to 0	FRST_SER_PAT_LN2[9:8]	R	-	2 most significant bits first sample error rate pattern lane 2
0116h	FRST_SER_PAT_L3_LSB	7 to 0	FRST_SER_PAT_LN3[7:0]	R	-	8 least significant bits of first sample error rate pattern lane 3
0117h	FRST_SER_PAT_LN3_MSB	1 to 0	FRST_SER_PAT_LN3[9:8]	R	-	2 most significant bits first sample error rate pattern lane 3

**Table 146. LSB/MSB of sample error rate level registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0118h	SER_LVL_LSB	7 to 0	SER_LVL[7:0]	R/W	0000 0000	8 least significant bits of level used for simple (DC) sample error rate measurement
0119h	SER_LVL_MSB	7 to 0	SER_LVL[15:8]	R/W	0000 0000	8 most significant bits of level used for simple (DC) sample error rate measurement

**Table 147. Multi-frame bytes registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
011Ah	MAN_MFB_LN0	6 to 0	MAN_MFB_LN0[6:0]	R/W	010 0000	number of multi-frame bytes instead of force_mfb_In0 is '1
011Bh	MAN_MFB_LN1	6 to 0	MAN_MFB_LN1[6:0]	R/W	010 0000	number of multi-frame bytes instead of force_mfb_In1 is '1
011Ch	MAN_MFB_LN2	6 to 0	MAN_MFB_LN2[6:0]	R/W	010 0000	number of multi-frame bytes instead of force_mfb_In2 is '1
011Dh	MAN_MFB_LN3	6 to 0	MAN_MFB_LN3[6:0]	R/W	010 0000	number of multi-frame bytes instead of force_mfb_In3 is '1

**Table 148. Force multi-frame bytes register**

FORCE_MFB (address 011Eh)						
Bit	Symbol	Access	Value	Description		
3	FORCE_MFB_LN3	R/W		force multi-frame bytes for lane_3		
			0	no action		
			1	force man_mfb_In3 to ILA_CTRL		
2	FORCE_MFB_LN2	R/W		force multi-frame bytes for lane_2		
			0	no action		
			1	force man_mfb_In2 to ILA_CTRL		
1	FORCE_MFB_LN1	R/W		force multi-frame bytes for lane_1		
			0	no action		
			1	force man_mfb_In1 to ILA_CTRL		

Table 148. Force multi-frame bytes register ...continued

FORCE_MFB (address 011Eh)				
Bit	Symbol	Access	Value	Description
0	FORCE_MFB_LN0	R/W		force multi-frame bytes for lane_0
			0	no action
			1	force man_mfb_ln0 to ILA_CTRL

**11.11.10 JESD204 read configuration block**

These blocks of registers reproduce the values of the configuration data transmitted from the TX in the second multi-frame of the inter-lane alignment sequence and decoded in the DAC165xD.

[Table 149](#) show an overview of the generic parts of the register addresses.

**Table 149. Overview of generic parts of register addresses**

	<b>DAC AB</b>
lane 0	nnn = 012
lane 1	nnn = 013
lane 2	nnn = 014
lane 3	nnn = 015

### 11.11.10.1 JESD204 read configuration block lane register allocation map

[Table 150](#) shows an overview of all the JESD204 read configuration lane registers.

**Table 150. JESD204 read configuration block DAC X/Y lane 0/lane 1 register allocation map**

Register name		R/W	Bit definition							Default <sup>[1]</sup>		
			b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
nnn0h	P_LN_CFG_0	R	P_LN_DID[7:0]							uuuu	uuu	
nnn1h	P_LN_CFG_1	R	P_LN_ADJCNT[3:0]				P_LN_BID[3:0]			uuuu	uuu	
nnn2h	P_LN_CFG_2	R	-	P_LN_ADJDIR	P_LN_PHADJ	P_LN_LID[4:0]				uuuu	uuu	
nnn3h	P_LN_CFG_3	R	P_LN_SCR	-	-	P_LN_L[4:0]				uuuu	uuu	
nnn4h	P_LN_CFG_4	R	P_LN_F[7:0]							uuuu	uuu	
nnn5h	P_LN_CFG_5	R	-	-	-	P_LN_K[4:0]				uuuu	uuu	
nnn6h	P_LN_CFG_6	R	P_LN_M[7:0]							uuuu	uuu	
nnn7h	P_LN_CFG_7	R	P_LN_CS[1:0]		-	P_LN_N[4:0]				uuuu	uuu	
nnn8h	P_LN_CFG_8	R	P_LN_SUBCLASSV[2:0]				P_LN_N[4:0]				uuuu	uuu
nnn9h	P_LN_CFG_9	R	P_LN_JESDV[2:0]				P_LN_S[4:0]				uuuu	uuu
nnnAh	P_LN_CFG_10	R	P_LN_HD	-	-	P_LN_CF[4:0]				uuuu	uuu	
nnnBh	P_LN_CFG_11	R	P_LN_RES1[7:0]							uuuu	uuu	
nnnCh	P_LN_CFG_12	R	P_LN_RES2[7:0]							uuuu	uuu	
nnnDh	P_LN_CFG_13	R	P_LN_FCHK[7:0]							uuuu	uuu	

[1] u = undefined at power-up or after reset.

## 11.11.10.2 JESD204 read configuration block lane bit definition detailed description

The tables in this section contain detailed descriptions of the JESD204 read configuration lane registers.

**Table 151. Lane configuration registers**

Default settings are shown highlighted. See [Table 149](#) for the generic information on the register addresses.

Address	Register	Bit	Symbol	Access	Value	Description
nnn0h	P_LN_CFG_0	7 to 0	P_LN_DID[7:0]	R	-	physical lane 0 device ID
nnn1h	P_LN_CFG_1	7 to 4	P_LN_ADJ_CNT[3:0]	R	-	physical lane 0 adjustable counter
		3 to 0	P_LN_BID[3:0]		-	physical lane 0 bank ID
nnn2h	P_LN_CFG_2	4 to 0	P_LN_LID[4:0]	R	-	physical lane 0 lane ID
nnn3h	P_LN_CFG_3	6	P_LN_ADJ_DIR	R	-	physical lane 0 adjustable direction
		5	P_LN_PH_ADJ		-	physical lane 0 adjustable phase
		4 to 0	P_LN_L[4:0]		-	number of physical lanes minus 1
nnn4h	P_LN_CFG_4	7 to 0	P_LN_F[7:0]	R	-	number of octets per frame minus 1
nnn5h	P_LN_CFG_5	4 to 0	P_LN_K[4:0]	R	-	number of frames per multi-frame minus 1
nnn6h	P_LN_CFG_6	7 to 0	P_LN_M[7:0]	R	-	number of converters per device minus 1
nnn7h	P_LN_CFG_7	7 to 6	P_LN_CS[1:0]	R	-	number of control bits
		4 to 0	P_LN_N[4:0]		-	converter resolution minus 1
nnn8h	P_LN_CFG_8	7 to 5	P_LN_SBCLSS_VS[2:0]	R	-	physical lane 0 JESD204B subclass version
					00	subclass 0
					01	subclass 1
					10	subclass 2
		4 to 0	P_LN_N'[4:0]	R	-	number of bits per sample minus 1
nnn9h	P_LN_CFG_9	7 to 5	P_LN_JESDV	R	-	physical lane 0 JESD204 version
					000	version A
					001	version B
		4 to 0	P_LN0_S[4:0]	R	-	number of samples per converter per frame cycle minus 1
nnnAh	P_LN_CFG_10	7	P_LN_HD	R	-	high density
		4 to 0	P_LN_CF[4:0]		-	number of control words per frame cycle
nnnBh	P_LN_CFG_11	7 to 0	P_LN_RSRVD1[7:0]	R	-	physical lane 0 reserved field
nnnCh	P_LN_CFG_12	7 to 0	P_LN_RSRVD2[7:0]	R	-	physical lane 0 reserved field
nnnDh	P_LN_CFG_13	7 to 0	P_LN_FCHK[7:0]	R	-	physical lane 0 checksum

### 11.11.10.3 JESD204 read configuration block sample measurement registers

[Table 152](#) shows an overview of all the JESD204 read configuration sample measurement registers.

**Table 152. JESD204 read configuration block sample measurement registers**

Register name		R/W	Bit definition							Default <sup>[1]</sup>	
			b7	b6	b5	b4	b3	b2	b1	b0	Bin
012Eh	P_LN10_SAMPLE_LSB	R	P_LN10_SAMPLE[7:0]							uuuu uuuu	uuh
012Fh	P_LN10_SAMPLE_MSB	R	P_LN10_SAMPLE[15:8]							uuuu uuuu	uuh
013Eh	P_LN10_SEL	W	P_LN10_SEL[7:0]							0000 0000	00h
014Eh	P_LN32_SAMPLE_LSB	R	P_LN32_SAMPLE[7:0]							uuuu uuuu	uuh
014Fh	P_LN32_SAMPLE_MSB	R	P_LN32_SAMPLE[15:8]								
015Eh	P_LN32_SEL	W	P_LN32_SEL[7:0]							0000 0000	00h

[1] u = undefined at power-up or after reset.

#### 11.11.10.4 JESD204 read configuration block sample measurement registers detailed description

[Table 153](#) shows an overview of all the JESD204 read configuration sample measurement registers.

**Table 153. Lane 1/lane 0 sample LSB/MSB registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.6.4</a> )
012Eh	P_LN10_SAMPLE_LSB	7 to 0	P_LN10_SAMPLE[7:0]	R	-	internal DLP data on physical lane 0 or physical lane 1 depending on the value of LN10_SELECT (bit 1E; LSB)  The data are strobed by DLP_STROBE
012Fh	P_LN10_SAMPLE_MSB	7 to 0	P_LN10_SAMPLE[15:8]	R	-	internal DLP data on physical lane 0 or physical lane 1 depending on the value of LN10_SELECT (bit 1E; MSB)  The data are strobed by DLP_STROBE

**Table 154. Physical lane 1/lane 0 selection register**

Default settings are shown highlighted.

LN10_SEL (address 013Eh)					
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.6.4</a> )	
7 to 0	P_LN10_SEL	W		specifies the lane affected by DLP_STROBE	
			0	physical lane 0	
			1	physical lane 1	

**Table 155. Lane 3/lane 2 sample LSB/MSB registers**

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.6.4</a> )
014Eh	P_LN32_SAMPLE_LSB	7 to 0	P_LN32_SAMPLE[7:0]	R	-	internal DLP data on lane 2 or lane 3 depending on the value of LN10_SELECT (bit 1E; LSB)  The data are strobed by DLP_STROBE
014Fh	P_LN32_SAMPLE_MSB	7 to 0	P_LN32_SAMPLE[15:8]	R	-	internal DLP data on lane 2 or lane 3 depending on the value of LN10_SELECT (bit 1E; MSB)  The data are strobed by DLP_STROBE

**Table 156. Physical lane 3/lane 2 selection register***Default settings are shown highlighted.*

P_LN32_SEL (address 015Eh)				
Bit	Symbol	Access	Value	Description (see <a href="#">Section 11.7.6.4</a> )
7 to 0	P_LN32_SEL	W		specifies the lane affected by DLP_STROBE
			0	physical lane 2
			1	physical lane 3

### 11.11.11 RX physical layer control block

This block of registers specifies the configuration of the physical layer of the deserializer. The control block the various features as the equalizer and the common-mode voltage or resistor termination. The RX physical layer monitor block monitors the status of the previous controls.

#### 11.11.11.1 RX physical layer block register allocation map

[Table 157](#) shows an overview of all the RX physical layer control registers.

**Table 157. RX physical layer control block register allocation map**

Register name		R/W	Bit definition							Default		
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0162h	HS_RX_CDR_DIV	R/W	HS_RX_CDR_LOW_SPEED_EN	HS_RX_CDR_DIVM[1:0]	HS_RX_CDR_DIVN[4:0]					0000 0010	02h	
0164h	HS_RX_CDR_LOOP	R/W	HS_RX_CDR_LOOP_RZ_TRACK[2:0]		HS_RX_CDR_LOOP_RZ_RUNIN[2:0]			HS_RX_CDR_LOOP_CAP[1:0]		0001 0111	17h	
0167h	HS_RX_EQ_CTRL	R/W	-	-	RESERVED	HS_RX_EQ_AUTO_ZERO_EN	HS_RX_3_EQ_EN	HS_RX_2_EQ_EN	HS_RX_1_EQ_EN	HS_RX_0_EQ_EN	0001 1111	1Fh
0168h	HS_RX_LN0_EQ_GAIN	R/W	-	-	-	-	-	HS_RX_LN0_EQ_IF_GAIN[2:0]		0000 0000	00h	
0169h	HS_RX_LN1_EQ_GAIN	R/W	-	-	-	-	-	HS_RX_LN1_EQ_IF_GAIN[2:0]		0000 0000	00h	
016Ah	HS_RX_LN2_EQ_GAIN	R/W	-	-	-	-	-	HS_RX_LN2_EQ_IF_GAIN[2:0]		0000 0000	00h	
016Bh	HS_RX_LN3_EQ_GAIN	R/W	-	-	-	-	-	HS_RX_LN3_EQ_IF_GAIN[2:0]		0000 0000	00h	
016Ch	HS_RX_LN0_EQ_OFFSET	R/W	-	HS_RX_LN0_EQ_INPUT_SHORT	HS_RX_LN0_EQ_OFFSETS[5:0]					0000 0000	00h	
016Dh	HS_RX_LN1_EQ_OFFSET	R/W	-	HS_RX_LN1_EQ_INPUT_SHORT	HS_RX_LN1_EQ_OFFSETS[5:0]					0000 0000	00h	

Table 157. RX physical layer control block register allocation map ...continued

Register name			R/W	Bit definition							Default		
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
016Eh	HS_RX_LN2_EQ_OFFSET	R/W	-	HS_RX_LN2_EQ_INPUT_SHORT	HS_RX_LN2_EQ_OFFSET[5:0]							0000	00h
016Fh	HS_RX_LN3_EQ_OFFS	R/W	-	HS_RX_LN3_EQ_INPUT_SHORT	HS_RX_LN3_EQ_OFFSET[5:0]							0000	00h
0170h	HS_RX_RT_VCM	R/W	-	-	HS_RX_RT_VCM_SEL	HS_RX_RT_VCM_REF[4:0]					0010	25h	
0171h	HS_RX_RT_CTRL	R/W	HS_RX_LN3_RT_HIZ_EN	HS_RX_LN2_RT_HIZ_EN	HS_RX_LN1_RT_HIZ_EN	HS_RX_LN0_RT_HIZ_EN	HS_RX_LN3_RT_EN	HS_RX_LN2_RT_EN	HS_RX_LN1_RT_EN	HS_RX_LN0_RT_EN	0000	0Fh	
0172h	HS_RX_LN0_RT_REF_SIZE	R/W	HS_RX_LN0_RT_REF_SIZE[8:1]							0101	50h		
0173h	HS_RX_LN1_RT_REF_SIZE	R/W	HS_RX_LN1_RT_REF_SIZE[8:1]							0101	50h		
0174h	HS_RX_LN2_RT_REF_SIZE	R/W	HS_RX_LN2_RT_REF_SIZE[8:1]							0101	50h		
0175h	HS_RX_LN3_RT_REF_SIZE	R/W	HS_RX_LN3_RT_REF_SIZE[8:1]							0101	50h		
0176h	HS_RX_LNX_RT_REF_SIZE	R/W	-	-	-	-	HS_RX_LN3_RT_REF_SIZE[0]	HS_RX_LN2_RT_REF_SIZE[0]	HS_RX_LN1_RT_REF_SIZE[0]	HS_RX_LN0_RT_REF_SIZE[0]	0000	00h	
017Dh	SYNC_CFG_CTRL	R/W	SYNC_EN	SYNC_SET_VCM[6:4]			SYNC_SET_LVL[3:0]				1000	80h	
017Eh	SYNC_SEL_CTRL	R/W	SYNC_TST_DATA_TX_EN	-	SYNC_TST_DATA_SEL[1:0]		-	-	-	-	0000	00h	

### 11.11.11.2 RX physical layer control block bit definition detailed description

The tables in this section contain detailed descriptions of the RX physical layer control registers.

**Table 158. High speed receiver clock data recovery divider register**

Default values are shown highlighted.

HS_RX_CDR_DIV (address 0162h)				
Bit	Symbol	Access	Value	Description
7	HS_RX_CDR_LOW_SPEED_EN	R/W	0	low speed receiver clock data recovery mode disabled
			1	enabled
6 to 5	HS_RX_CDR_DIVM[1:0]	R/W	-	divm ratio used to divide the reference clock (predivider) (see <a href="#">Figure 50</a> )
4 to 0	HS_RX_CDR_DIVN[4:0]	R/W	-	divn ratio used in clock data receiver reference loop (see <a href="#">Figure 50</a> )

**Table 159. High speed receiver clock data recovery loop register**

Default values are shown highlighted.

HS_RX_CDR_LOOP (address 0164h)				
Bit	Symbol	Access	Value	Description
7 to 5	HS_RX_CDR_LOOP_RZ_TRACK[2:0]	R/W	-	CDR loop resistance value in track mode
4 to 2	HS_RX_CDR_LOOP_RZ_RUNIN[2:0]	R/W	-	CDR loop resistance value in run-in mode
1 to 0	HS_RX_CDR_LOOP_CAP[1:0]	R/W	-	CDR loop capacitance value

**Table 160. High speed receiver equalizer control register**

Default values are shown highlighted.

HS_RX_EQ_CTRL (address 0167h)				
Bit	Symbol	Access	Value	Description
5	RESERVED	R/W	0	reserved to 0
4	HS_RX_EQ_AUTO_ZERO_EN	R/W	0	Equalizer auto zero mode disabled (for all lanes)
			1	enabled (for all lanes)
3	HS_RX_LN3_EQ_EN	R/W	0	Equalizer of receiver lane 3 disabled (power-down)
			1	enabled (active)
2	HS_RX_LN2_EQ_EN	R/W	0	Equalizer of receiver lane 2 disabled (power-down)
			1	enabled (active)
1	HS_RX_LN1_EQ_EN	R/W	0	Equalizer of receiver lane 1 disabled (power-down)
			1	enabled (active)
0	HS_RX_LN0_EQ_EN	R/W	0	Equalizer of receiver lane 0 disabled (power-down)
			1	enabled (active)

**Table 161. High speed equalizer gain registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0168h	HS_RX_LN0_EQ_GAIN	2 to 0	HS_RX_LN0_EQ_IF_GAIN[2:0]	R/W	-	sets if-gain for receiver lane 0 equalizer
0169h	HS_RX_LN1_EQ_GAIN	2 to 0	HS_RX_LN1_EQ_IF_GAIN[2:0]	R/W	-	sets if-gain for receiver lane 1 equalizer
016Ah	HS_RX_LN2_EQ_GAIN	2 to 0	HS_RX_LN2_EQ_IF_GAIN[2:0]	R/W	-	sets if-gain for receiver lane 2 equalizer
016Bh	HS_RX_LN3_EQ_GAIN	2 to 0	HS_RX_LN3_EQ_IF_GAIN[2:0]	R/W	-	sets if-gain for receiver lane 3 equalizer

**Table 162. High speed equalizer offset registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0Ch	HS_RX_LN0_EQ_OFFSET	6	HS_RX_LN0_EQ_INPUT_SHORT	R/W	-	receiver lane 0 input equalizer shorted to V <sub>DD</sub>
					0	no action
					1	receiver lane 0 equalizer input shorted to V <sub>DD</sub>
		5 to 0	HS_RX_LN0_EQ_OFFSET[5:0]	R/W	-	receiver lane 0 equalizer offset adjustment input
0Dh	HS_RX_LN1_EQ_OFFSET	6	HS_RX_LN1_EQ_INPUT_SHORT	R/W	-	receiver lane 1 input equalizer shorted to V <sub>DD</sub>
					0	no action
					1	receiver lane 1 equalizer input shorted to V <sub>DD</sub>
		5 to 0	HS_RX_LN1_EQ_OFFSET[5:0]	R/W	-	receiver lane 1 equalizer offset adjustment input
0Eh	HS_RX_LN2_EQ_OFFSET	6	HS_RX_LN2_EQ_INPUT_SHORT	R/W	-	receiver lane 2 input equalizer shorted to V <sub>DD</sub>
					0	no action
					1	receiver lane 2 equalizer input shorted to V <sub>DD</sub>
		5 to 0	HS_RX_LN2_EQ_OFFSET[5:0]	R/W	-	receiver lane 2 equalizer offset adjustment input
0Fh	HS_RX_LN3_EQ_OFFSET	6	HS_RX_LN3_EQ_INPUT_SHORT	R/W	-	receiver lane 3 input equalizer shorted to V <sub>DD</sub>
					0	no action
					1	receiver lane 3 equalizer input shorted to V <sub>DD</sub>
		5 to 0	HS_RX_LN3_EQ_OFFSET[5:0]	R/W	-	receiver lane 3 equalizer offset adjustment input

**Table 163. High speed receiver termination resistor voltage common-mode register**

Default values are shown highlighted.

HS_RX_RT_VCM (address 0170h)				
Bit	Symbol	Access	Value	Description
5	HS_RX_RT_VCM_SEL	R/W		rx_rt modules configuration
			0	do not use
			1	rx_rt_modules configured for RX-use (all lanes)
4 to 0	HS_RX_RT_VCM_REF[4:0]	R/W	-	sets common-mode reference for hs_rx_rt (all lanes)

**Table 164. High speed resistor termination control register**

Default values are shown highlighted.

HS_RX_RT_CTRL (address 0171h)				
Bit	Symbol	Access	Value	Description
7	HS_RX_LN3_RT_HIZ_EN	R/W		high speed receiver lane 3 input
			0	100 $\Omega$ (differential impedance)
			1	high ohmic
6	HS_RX_LN2_RT_HIZ_EN	R/W		high speed receiver lane 2 input
			0	100 $\Omega$ (differential impedance)
			1	high ohmic
5	HS_RX_LN1_RT_HIZ_EN	R/W		high speed receiver lane 1 input
			0	100 $\Omega$ (differential impedance)
			1	high ohmic
4	HS_RX_LN0_RT_HIZ_EN	R/W		high speed receiver lane 0 input
			0	100 $\Omega$ (differential impedance)
			1	high ohmic
3	HS_RX_LN3_RT_EN	R/W		high speed receiver lane 3 resistance termination
			0	disabled (power-down)
			1	enabled (active)
2	HS_RX_LN2_RT_EN	R/W		high speed receiver lane 2 resistance termination
			0	disabled (power-down)
			1	enabled (active)
1	HS_RX_LN1_RT_EN	R/W		high speed receiver lane 1 resistance termination
			0	disabled (power-down)
			1	enabled (active)
0	HS_RX_LN0_RT_EN	R/W		high speed receiver lane 0 resistance termination
			0	disabled (power-down)
			1	enabled (active)

**Table 165. Termination impedance fine-tuning (MSBs) registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0172h	HS_RX_LN0_RT_REF_SIZE	7 to 0	HS_RX_LN0_RT_REF_SIZE[8:1]	R/W	-	most significant 8 bits of resistor termination impedance fine-tuning lane 0
0173h	HS_RX_LN1_RT_REF_SIZE	7 to 0	HS_RX_LN1_RT_REF_SIZE[8:1]	R/W	-	most significant 8 bits of resistor termination impedance fine-tuning lane 1
0174h	HS_RX_LN2_RT_REF_SIZE	7 to 0	HS_RX_LN2_RT_REF_SIZE[8:1]	R/W	-	most significant 8 bits of resistor termination impedance fine-tuning lane 2
0175h	HS_RX_LN3_RT_REF_SIZE	7 to 0	HS_RX_LN3_RT_REF_SIZE[8:1]	R/W	-	most significant 8 bits of resistor termination impedance fine-tuning lane 3

**Table 166. High speed resistor termination reference size register**

Default values are shown highlighted.

HS_RX_LNX_RT_REF_SIZE (address 0176h)					
Bit	Symbol	Access	Value	Description	
3	HS_RX_LN3_RT_REF_SIZE	R/W	-	least significant bit of termination impedance fine-tuning lane 3	
2	HS_RX_LN2_RT_REF_SIZE	R/W	-	least significant bit of termination impedance finetuning lane 2	
1	HS_RX_LN1_RT_REF_SIZE	R/W	-	least significant bit of termination impedance fine-tuning lane 1	
0	HS_RX_LN0_RT_REF_SIZE	R/W	-	least significant bit of termination impedance fine-tuning lane 0	

**Table 167. Synchronization configuration control register**

Default values are shown highlighted.

SYNC_CFG_CTRL (address 017Dh)					
Bit	Symbol	Access	Value	Description	
7	SYNC_EN	R/W	0	disabled (power-down)	
			1	enabled (active)	
6 to 4	SYNC_SET_VCM[6:4]	R/W	-	sets common-mode output voltage of synchronization buffer	
3 to 0	SYNC_SET_LVL[3:0]	R/W	-	sets output levels (swing) of synchronization buffer	

**Table 168. Synchronization test data control register**

Default values are shown highlighted.

SYNC_SEL_CTRL (address 017Eh)					
Bit	Symbol	Access	Value	Description	
7	SYNC_TST_DATA_TX_EN	R/W	0	normal operation (JESD204x synchronization buffer)	
			1	test mode (synchronization output depends on SYNC_TST_DATA_SEL)	

**Table 168. Synchronization test data control register ...continued***Default values are shown highlighted.*

SYNC_SEL_CTRL (address 017Eh)				
Bit	Symbol	Access	Value	Description
5 to 4	SYNC_TST_DATA_SEL[1:0]	R/W		synchronization test data selection
			00	synchronization ← HS_RX_0_CLK_DX
			01	synchronization ← HS_RX_1_CLK_DX
			10	synchronization ← HS_RX_2_CLK_DX
			11	synchronization ← HS_RX_3_CLK_DX

11.11.11.3 RX physical layer monitor register allocation map

Table 169 shows an overview of all RX physical layer monitor registers.

Table 169. RX physical layer monitor register allocation map

Register name	R/W	Bit definition								Default	
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0184h I_HS_RX_CDR_LOOP_MON	R	I_HS_RX_CDR_LOOP_RZ_MON[2:0]			-	-	-	-	-	0001 0111	17h
0185h HS_RX_CDR_EN_MON_0	R	-	-	-	-	HS_RX_LN3_CDR_EN_MON	HS_RX_LN2_CDR_EN_MON	HS_RX_LN1_CDR_EN_MON	HS_RX_LN0_CDR_EN_MON	0000 1111	0Fh
0186h HS_RX_CDR_EN_MON_1	R	-	-	-	-	HS_RX_LN3_CDR_TRACK_DATA_EN_MON	HS_RX_LN2_CDR_TRACK_DATA_EN_MON	HS_RX_LN1_CDR_TRACK_DATA_EN_MON	HS_RX_LN0_CDR_TRACK_DATA_EN_MON	0000 0000	00h
0187h HS_RX_EQ_CTRL_MON	R	-	-	RESERVED	HS_RX_EQ_AUTO_ZERO_EN_MON	HS_RX_LN3_EQ_EN_MON	HS_RX_LN2_EQ_EN_MON	HS_RX_LN1_EQ_EN_MON	HS_RX_LN0_EQ_EN_MON	0001 1111	1Fh
018Ch HS_RX_LN0_EQ_OFFSET_MON	R	-	HS_RX_LN0_EQ_INPUT_SHORT_MON	HS_RX_LN0_EQ_OFFSET_MON[5:0]						0000 0000	00h
018Dh HS_RX_LN1_EQ_OFFSET_MON	R	-	HS_RX_LN1_EQ_INPUT_SHORT_MON	HS_RX1_LN1_EQ_OFFSET_MON[5:0]						0000 0000	00h
018Eh HS_RX_LN2_EQ_OFFSET_MON	R	-	HS_RX_LN2_EQ_INPUT_SHORT_MON	HS_RX_LN2_EQ_OFFSET_MON[5:0]						0000 0000	00h
018Fh HS_RX_LN3_EQ_OFFSET_MON	R	-	HS_RX_LN3_EQ_INPUT_SHORT_MON	HS_RX_LN3_EQ_OFFSET_MON[5:0]						0000 0000	00h

Table 169. RX physical layer monitor register allocation map ...continued

Register name			R/W	Bit definition							Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin
0191h	HS_RX_RT_CTRL_MON	R	-	-	-	-	HS_RX_LN3_RT_EN_MON	HS_RX_LN2_RT_EN_MON	HS_RX_LN1_RT_EN_MON	HS_RX_LN0_RT_EN_MON		
0199h	HS_RX_LN0_MON	R	-	-	-	RESERVED[1:0]		HS_RX_LN0_EQ_OFFSET_POL_MON	HS_RX_LN0_LOCK_REF_CLK_MON	-		
019Ah	HS_RX_LN1_MON	R	-	-	-	-	RESERVED	HS_RX_LN1_EQ_OFFSET_POL_MON	HS_RX_LN1_LOCK_REF_CLK_MON	-		
019Bh	HS_RX_LN2_MON	R	-	-	-	-	RESERVED	HS_RX_LN2_EQ_OFFSET_POL_MON	HS_RX_LN2_LOCK_REF_CLK	-		
019Ch	HS_RX_LN3_MON	R	-	-	-	-	RESERVED	HS_RX_LN3_EQ_OFFSET_POL_MON	HS_RX_LN3_LOCK_REF_CLK_MON	-		

#### 11.11.11.4 RX physical layer monitor block bit definition detailed description

The tables in this section contain detailed descriptions of the RX physical layer monitor registers.

**Table 170. Current high speed receiver clock data recovery loop register**

Default values are shown highlighted.

I_HS_RX_CDR_LOOP_MON (address 0184h)				
Bit	Symbol	Access	Value	Description
7 to 5	HS_RX_CDR_LOOP_RZ_MON[2:0]	R	-	actual clock data recovery loop resistance value

**Table 171. Current high speed RX equalizer control register**

Default values are shown highlighted.

I_HS_RX_EQ_CTRL (address 0187h)				
Bit	Symbol	Access	Value	Description
5	RESERVED	R		reserved to 0
4	HS_RX_EQ_AUTO_ZERO_EN_MON	R	0 1	Equalizer auto zero mode disabled (for all lanes) enabled (for all lanes)
3	HS_RX_LN3_EQ_EN_MON	R	0 1	Equalizer of receiver lane 3 disabled (power-down) enabled (active)
2	HS_RX_LN2_EQ_EN_MON	R	0 1	Equalizer of receiver lane 2 disabled (power-down) enabled (active)
1	HS_RX_LN1_EQ_EN_MON	R	0 1	Equalizer of receiver lane 1 disabled (power-down) enabled (active)
0	HS_RX_LN0_EQ_EN_MON	R	0 1	Equalizer of receiver lane 0 disabled (power-down) enabled (active)

**Table 172. Equalizer offset registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
018Ch	HS_RX_LN0_EQ_OFFSET_MON	6	HS_RX_LN0_EQ_INPUT_SHORT_MON	R		receiver lane 0 input equalizer shorted to $V_{DD}$
					0	no action
					1	receiver lane 0 equalizer input shorted to $V_{DD}$
		5 to 0	HS_RX_LN0_EQ_OFFSET_MON[5:0]	R	-	receiver lane 0 equalizer offset adjustment input

Table 172. Equalizer offset registers ...continued

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
018Dh	HS_RX_LN1_EQ_OFFSET_MON	6	HS_RX_LN1_EQ_INPUT_SHORT_MON	R	0	receiver lane 1 input equalizer shorted to V <sub>DD</sub>
					1	receiver lane 1 equalizer input shorted to V <sub>DD</sub>
		5 to 0	HS_RX_LN1_EQ_OFFSET_MON[5:0]	R	-	receiver lane 1 equalizer offset adjustment input
018Eh	HS_RX_LN2_EQ_OFFSET_MON	6	HS_RX_LN2_EQ_INPUT_SHORT_MON	R	0	receiver lane 2 input equalizer shorted to V <sub>DD</sub>
					1	receiver lane 2 equalizer input shorted to V <sub>DD</sub>
		5 to 0	HS_RX_LN2_EQ_OFFSET_MON[5:0]	R	-	receiver lane 2 equalizer offset adjustment input
018Fh	HS_RX_LN3_EQ_OFFSET_MON	6	HS_RX_LN3_EQ_INPUT_SHORT_MON	R	0	receiver lane 3 input equalizer shorted to V <sub>DD</sub>
					1	receiver lane 3 equalizer input shorted to V <sub>DD</sub>
		5 to 0	HS_RX_LN3_EQ_OFFSET_MON[5:0]	R	-	receiver lane 3 equalizer offset adjustment input

Table 173. High speed receiver resistor termination control register

Default values are shown highlighted.

HS_RX_RT_CTRL (address 0191h)				
Bit	Symbol	Access	Value	Description
7	HS_RX_LN3_RT_HIZ_EN_MON	R	0	high speed receiver lane 3 input 100 Ω (differential impedance)
			1	high ohmic
6	HS_RX_LN2_RT_HIZ_EN_MON	R	0	high speed receiver lane 2 input 100 Ω (differential impedance)
			1	high ohmic
5	HS_RX_LN1_RT_HIZ_EN_MON	R	0	high speed receiver lane 1 input 100 Ω (differential impedance)
			1	high ohmic
4	HS_RX_LN0_RT_HIZ_EN_MON	R	0	high speed receiver lane 0 input 100 Ω (differential impedance)
			1	high ohmic
3	HS_RX_LN3_RT_EN_MON	R	0	termination of receiver lane 3 disabled (power-down)
			1	enabled (active)

**Table 173. High speed receiver resistor termination control register ...continued**

Default values are shown highlighted.

HS_RX_RT_CTRL (address 0191h)				
Bit	Symbol	Access	Value	Description
2	HS_RX_LN2_RT_EN_MON	R	0	termination of receiver lane 2 disabled (power-down)
			1	enabled (active)
1	HS_RX_LN1_RT_EN_MON	R	0	termination of receiver lane 1 disabled (power-down)
			1	enabled (active)
0	HS_RX_LN1_RT_EN_MON	R	0	termination of receiver lane 0 disabled (power-down)
			1	enabled (active)

**Table 174. High speed receiver monitor registers**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0199h	HS_RX_0_MON	4 to 3	RESERVED	R	00	reserved to 00
		2	HS_RX_LN0_EQ_OFFSET_POL_MON	R	0	high speed receiver lane 0 equalizer offset negative
					1	positive
		1	HS_RX_LN0_LOCK_REF_CLK_MON	R	0	high speed receiver lane 0 lock to reference clock not locked to reference clock (pfd mode)
1	locked to reference clock (pfd mode)					
019Ah	HS_RX_1_MON	3	RESERVED	R	0	reserved to 0
		2	HS_RX_LN1_EQ_OFFSET_POL_MON	R	0	high speed receiver lane 1 equalizer offset negative
					1	positive
		1	HS_RX_LN1_LOCK_REF_CLK_MON	R	0	high speed receiver lane 1 lock to reference clock not locked to reference clock (pfd mode)
1	locked to reference clock (pfd mode)					

**Table 174. High speed receiver monitor registers ...continued**

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
019Bh	HS_RX_2_MON	3	RESERVED	R		reserved to 0
		2	HS_RX_LN2_EQ_OFFSET_POL_MON	R		high speed receiver lane 2 equalizer offset
					0	negative
			1	positive		
		1	HS_RX_LN2_LOCK_REF_CLK_MON	R		high speed receiver lane 2 lock to reference clock
					0	not locked to reference clock (pfd mode)
1	locked to reference clock (pfd mode)					
019Ch	HS_RX_3_MON	3	RESERVED	R		reserved to 0
		2	HS_RX_LN3_EQ_OFFSET_POL_MON	R		high speed receiver lane 3 equalizer offset
					0	negative
			1	positive		
		1	HS_RX_LN3_LOCK_REF_CLK_MON	R		high speed receiver lane 3 lock to reference clock
					0	not locked to reference clock (pfd mode)
1	locked to reference clock (pfd mode)					

12. Package outline

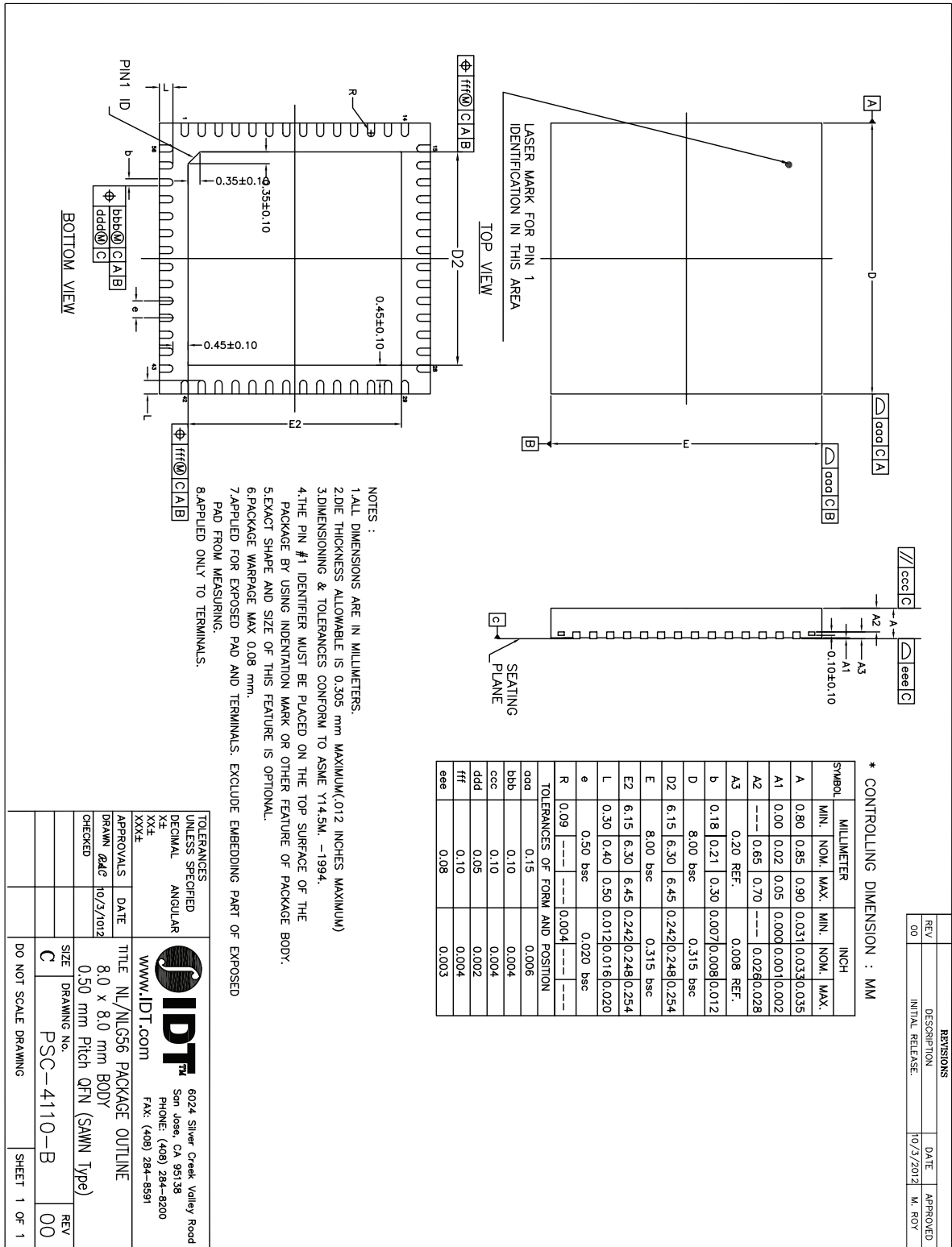


Fig 60. Package outline VFQFP-N 56

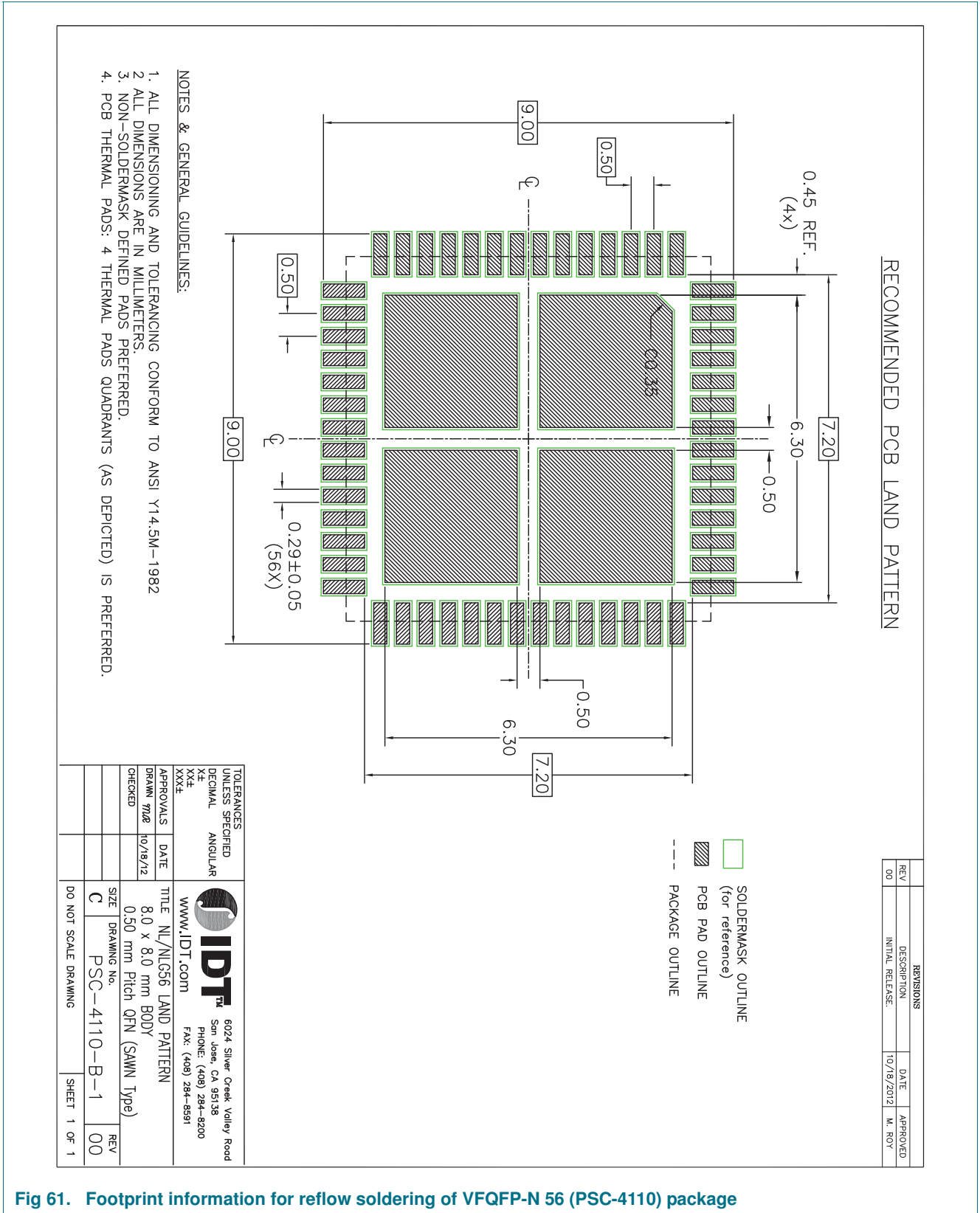


Fig 61. Footprint information for reflow soldering of VFQFP-N 56 (PSC-4110) package

## 13. Abbreviations

**Table 175. Abbreviations**

<b>Acronym</b>	<b>Description</b>
B	BandWidth
BWA	Broadband Wireless Access
CDI	Clock Domain Interface
CDMA	Code Division Multiple Access
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
EDGE	Enhanced Data rates for GSM Evolution
FIR	Finite Impulse Response
GSM	Global System for Mobile communications
IF	Intermediate Frequency
IMD3	Third Order InterModulation
LMDS	Local Multipoint Distribution Service
LO	Local Oscillator
LVDS	Low-Voltage Differential Signaling
NCO	Numerically Controlled Oscillator
NMOS	Negative Metal-Oxide Semiconductor
PLL	Phase-Locked Loop
SFDR	Spurious-Free Dynamic Range
SPI	Serial Peripheral Interface
WCDMA	Wide band Code Division Multiple Access
WLL	Wireless Local Loop

## 14. Glossary

### 14.1 Static parameters

**INL** — The deviation of the transfer function from a best fit straight line (linear regression computation).

**DNL** — The difference between the ideal and the measured output value between successive DAC codes.

### 14.2 Dynamic parameters

**Spurious-Free Dynamic Range (SFDR)** — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

**InterModulation Distortion (IMD)** — From a dual-tone digital input sine wave (these two frequencies being close together), the intermodulation distortion products IMD2 and IMD3 (second order and third order components) are defined below.

**IMD2** — The ratio between the RMS value of either tone and the RMS value of the worst second order intermodulation product.

**IMD3** — The ratio between the RMS value of either tone and the RMS value of the worst third order intermodulation product.

**Total Harmonic Distortion (THD)** — The ratio between the RMS value of the harmonics of the output frequency and the RMS value of the output sine wave. Usually, the calculation of THD is done on the first 5 harmonics.

**Signal-to-Noise Ratio (SNR)** — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise excluding the harmonics and the DC component.

**Restricted BandWidth Spurious-Free Dynamic Range (SFDR<sub>RBW</sub>)** — the ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise, including the harmonics, in a given bandwidth centered around  $f_{\text{offset}}$ .

## 15. Revision history

Table 176. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
DAC1653D; DAC1658D v.2	20121108	Advance data sheet	-	-

## Contact information



[www.IDT.com](http://www.IDT.com)

6024 Silver Creek Valley Road  
San Jose, California 95138

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