

ADC1113S125

Single 11-bit ADC; serial JESD204A interface

Rev. 02 — 2 July 2012

Product data sheet

1. General description

The ADC1113S125 is a single channel 11-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performance and low power at a sample rate of 125 Msps. Pipelined architecture and output error correction ensure the ADC1113S125 is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a 3 V source for analog and a 1.8 V source for the output driver, it outputs data in serial mode via a single differential lane, which complies with the JESD204A standard. The integration of Serial Peripheral Interface (SPI) allows the user to easily configure the ADCs and the serial output modes. The device also includes a programmable full-scale SPI to allow a flexible input voltage range from 1 V (p-p) to 2 V (p-p).

Excellent dynamic performance is maintained from the baseband to input frequencies of 170 MHz or more, making the ADC1113S125 ideal for use in communications, imaging, and medical applications.

2. Features and benefits

- SNR, 66.2 dBFS; SFDR, 87 dBc
- Sample rate: 125 Msps
- Single channel, 11-bit pipelined ADC core
- 3 V, 1.8 V power supplies
- Flexible input voltage range: 1 V (p-p) to 2 V (p-p)
- Serial output
- Compliant with JESD204A serial transmission standard
- Pin compatible with ADC1613S series, ADC1413S series, and ADC1213S series
- Input bandwidth, 600 MHz
- Power dissipation, 550 mW at 80 Msps
- SPI register programming
- Duty cycle stabilizer
- High Intermediate Frequency (IF) capability
- Offset binary, two's complement, gray code
- Power-down mode and Sleep mode
- HVQFN32 package

3. Applications

- Wireless and wired broadband communications
- Spectral analysis
- Ultrasound equipment
- Portable instrumentation
- Imaging systems



4. Ordering information

Table 1. Ordering information

| Type number | Sampling frequency (Msps) | Package | | |
|------------------|---------------------------|----------|--|-----------|
| | | Name | Description | Version |
| ADC1113S125HN-C1 | 125 | HVQFN32R | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; resin based; body 7 × 7 × 0.8 mm | SOT1152-1 |

5. Block diagram

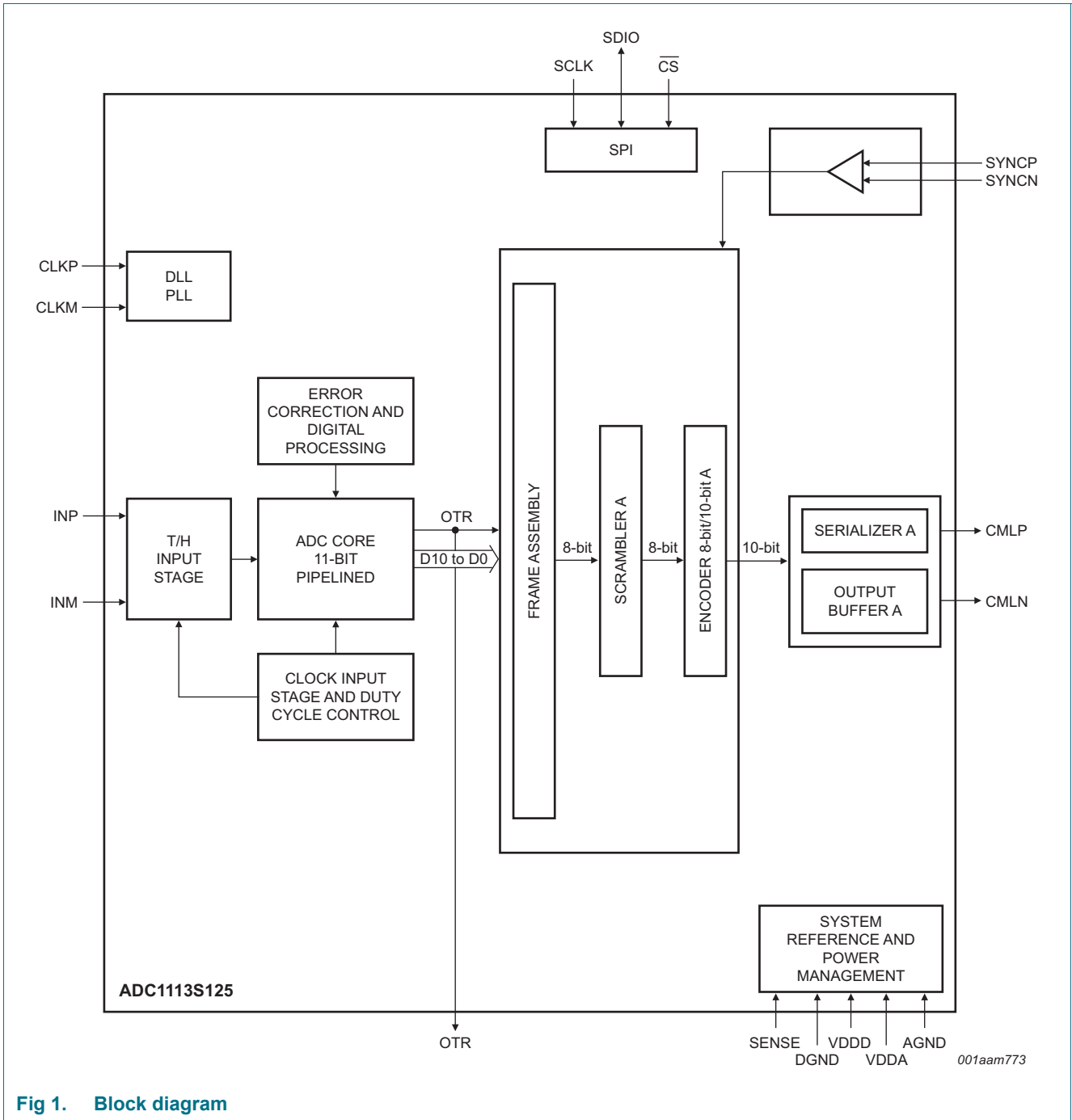


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

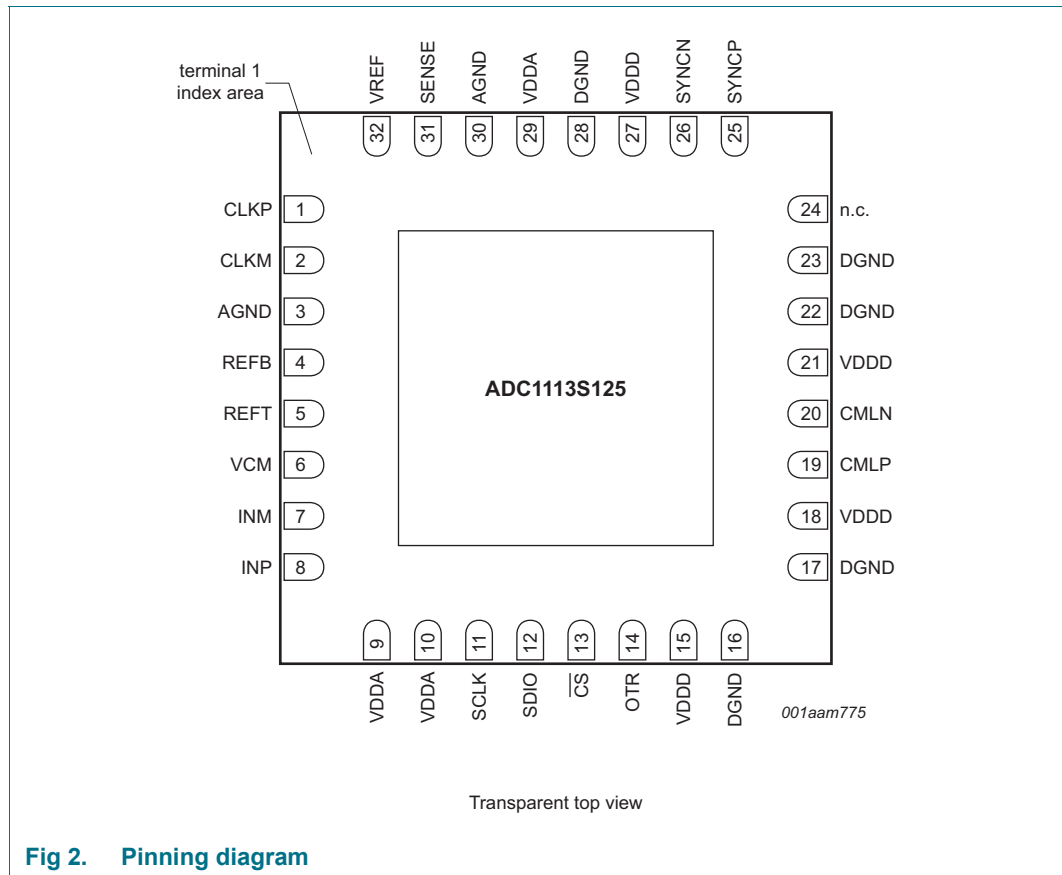


Fig 2. Pinning diagram

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type ^[1] | Description |
|--------|-----|---------------------|--------------------------------|
| CLKP | 1 | I | clock input |
| CLKM | 2 | I | complementary clock input |
| AGND | 3 | G | analog ground |
| REFB | 4 | O | ADC bottom reference |
| REFT | 5 | O | ADC top reference |
| VCM | 6 | O | ADC output common voltage |
| INM | 7 | I | ADC complementary analog input |
| INP | 8 | I | ADC analog input |
| VDDA | 9 | P | analog power supply 3 V |
| VDDA | 10 | P | analog power supply 3 V |
| SCLK | 11 | I | SPI clock |
| SDIO | 12 | I/O | SPI data input/output |

Table 2. Pin description ...continued

| Symbol | Pin | Type ^[1] | Description |
|--------|-----|---------------------|---|
| CS | 13 | I | chip select |
| OTR | 14 | O | out-of-range information |
| VDDD | 15 | P | digital power supply 1.8 V |
| DGND | 16 | G | digital ground |
| DGND | 17 | G | digital ground |
| VDDD | 18 | P | digital power supply 1.8 V |
| CMLP | 19 | O | serial output |
| CMLN | 20 | O | serial complementary output |
| VDDD | 21 | P | digital power supply 1.8 V |
| DGND | 22 | G | digital ground |
| DGND | 23 | G | digital ground |
| n.c. | 24 | - | not connected |
| SYNCP | 25 | I | positive synchronization signal from the receiver |
| SYNCP | 26 | I | negative synchronization signal from the receiver |
| VDDD | 27 | P | digital power supply 1.8 V |
| DGND | 28 | G | digital ground |
| VDDA | 29 | P | analog power supply 3 V |
| AGND | 30 | G | analog ground |
| SENSE | 31 | I | reference programming pin |
| VREF | 32 | I/O | voltage reference input/output |

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------|--------------------------------|------------|------|------|------|
| V _{DDA} | analog supply voltage | | -0.4 | +4.6 | V |
| V _{DDD(1V8)} | digital supply voltage (1.8 V) | | -0.4 | +2.5 | V |
| T _{stg} | storage temperature | | -55 | +125 | °C |
| T _{amb} | ambient temperature | | -40 | +85 | °C |
| T _j | junction temperature | | - | 125 | °C |

8. Thermal characteristics

Table 4. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|----------------------|---|------------|----------|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | | [1] 25.6 | K/W |
| R _{th(j-c)} | thermal resistance from junction to case | | [1] 8.6 | K/W |

[1] Value for six layers board in still air with a minimum of 25 thermal vias.

9. Static characteristics

Table 5. Static characteristics^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|----------------------------------|---|--------------|-----------|--------------|----------|
| Supplies | | | | | | |
| V_{DDA} | analog supply voltage | | 2.85 | 3.0 | 3.4 | V |
| $V_{DDD(1V8)}$ | digital supply voltage (1.8 V) | | 1.65 | 1.8 | 1.95 | V |
| I_{DDA} | analog supply current | $f_{clk} = 125$ Msps; $f_i = 70$ MHz | - | 185 | - | mA |
| $I_{DDD(1V8)}$ | digital supply current (1.8 V) | $f_{clk} = 125$ Msps; $f_i = 70$ MHz | - | 75 | - | mA |
| P_{tot} | total power dissipation | $f_{clk} = 125$ Msps | - | 690 | - | mW |
| | | $f_{clk} = 105$ Msps | - | 625 | - | mW |
| | | $f_{clk} = 80$ Msps | - | 550 | - | mW |
| | | $f_{clk} = 65$ Msps | - | 495 | - | mW |
| P | power dissipation | Power-down mode | - | 30 | - | mW |
| | | Standby mode | - | 150 | - | mW |
| Clock inputs: pins CLKP and CLKM (AC-coupled) | | | | | | |
| Low-Voltage Positive Emitter-Coupled Logic (LVPECL) | | | | | | |
| $V_{i(clk)dif}$ | differential clock input voltage | peak-to-peak | - | 1.6 | - | V |
| Sine | | | | | | |
| $V_{i(clk)dif}$ | differential clock input voltage | peak | ± 0.8 | ± 3.0 | - | V |
| Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) | | | | | | |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{DDA}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DDA}$ | - | - | V |
| SPI: pins CS, SDIO, SCLK | | | | | | |
| V_{IL} | LOW-level input voltage | | 0 | - | $0.3V_{DDA}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DDA}$ | - | V_{DDA} | V |
| I_{IL} | LOW-level input current | | -10 | - | +10 | μ A |
| I_{IH} | HIGH-level input current | | -50 | - | +50 | μ A |
| C_i | input capacitance | | - | 4 | - | pF |
| Analog inputs: pins INP and INM | | | | | | |
| I_i | input current | track mode | -5 | - | +5 | μ A |
| R_i | input resistance | track mode | - | 15 | - | Ω |
| C_i | input capacitance | track mode | - | 5 | - | pF |
| $V_{i(cm)}$ | common-mode input voltage | track mode | 1.1 | 1.5 | 2 | V |
| B_i | input bandwidth | | - | 600 | - | MHz |
| $V_{i(dif)}$ | differential input voltage | peak-to-peak | 1 | - | 2 | V |

Table 5. Static characteristics^[1] ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|----------------------------|-----------------------------|-------|--------------|-------|------|
| Voltage controlled regulator output: pin VCM | | | | | | |
| $V_{O(cm)}$ | common-mode output voltage | | - | $0.5V_{DDA}$ | - | V |
| $I_{O(cm)}$ | common-mode output current | | - | 4 | - | mA |
| Reference voltage input/output: pin VREF | | | | | | |
| V_{VREF} | voltage on pin VREF | output | 0.5 | - | 1 | V |
| | | input | 0.5 | - | 1 | V |
| Data outputs: pins CMLP, CMLN | | | | | | |
| Output levels, $V_{DD(1V8)} = 1.8\text{ V}$; $SWING_SEL[2:0] = 000$ | | | | | | |
| V_{OL} | LOW-level output voltage | DC-coupled; output | - | 1.5 | - | V |
| | | AC-coupled | - | 1.35 | - | V |
| V_{OH} | HIGH-level output voltage | DC-coupled; output | - | 1.8 | - | V |
| | | AC-coupled | - | 1.65 | - | V |
| Output levels, $V_{DD(1V8)} = 1.8\text{ V}$; $SWING_SEL[2:0] = 001$ | | | | | | |
| V_{OL} | LOW-level output voltage | DC-coupled; output | - | 1.45 | - | V |
| | | AC-coupled | - | 1.275 | - | V |
| V_{OH} | HIGH-level output voltage | DC-coupled; output | - | 1.8 | - | V |
| | | AC-coupled | - | 1.625 | - | V |
| Output levels, $V_{DD(1V8)} = 1.8\text{ V}$; $SWING_SEL[2:0] = 010$ | | | | | | |
| V_{OL} | LOW-level output voltage | DC-coupled; output | - | 1.4 | - | V |
| | | AC-coupled | - | 1.2 | - | V |
| V_{OH} | HIGH-level output voltage | DC-coupled; output | - | 1.8 | - | V |
| | | AC-coupled | - | 1.6 | - | V |
| Output levels, $V_{DD(1V8)} = 1.8\text{ V}$; $SWING_SEL[2:0] = 011$ | | | | | | |
| V_{OL} | LOW-level output voltage | DC-coupled; output | - | 1.35 | - | V |
| | | AC-coupled | - | 1.125 | - | V |
| V_{OH} | HIGH-level output voltage | DC-coupled; output | - | 1.8 | - | V |
| | | AC-coupled | - | 1.575 | - | V |
| Output levels, $V_{DD(1V8)} = 1.8\text{ V}$; $SWING_SEL[2:0] = 100$ | | | | | | |
| V_{OL} | LOW-level output voltage | DC-coupled; output | - | 1.3 | - | V |
| | | AC-coupled | - | 1.05 | - | V |
| V_{OH} | HIGH-level output voltage | DC-coupled; output | - | 1.8 | - | V |
| | | AC-coupled | - | 1.55 | - | V |
| Serial configuration: pins SYNCp, SYNCn | | | | | | |
| V_{IL} | LOW-level input voltage | differential; input | - | 0.95 | - | V |
| V_{IH} | HIGH-level input voltage | differential; input | - | 1.47 | - | V |
| Accuracy | | | | | | |
| INL | integral non-linearity | | -5 | - | +5 | LSB |
| DNL | differential non-linearity | guaranteed no missing codes | -0.95 | ± 0.5 | +0.95 | LSB |
| E_{offset} | offset error | | - | ± 2 | - | mV |

Table 5. Static characteristics^[1] ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|------------------------------|--------------------------------------|-----|-----------|-----|------|
| E_G | gain error | full-scale | - | ± 0.5 | - | % |
| Supply | | | | | | |
| PSRR | power supply rejection ratio | 200 mV (p-p) on pin VDDA; $f_i = DC$ | - | -54 | - | dB |

[1] Typical values measured at $V_{DDA} = 3\text{ V}$, $V_{DDD(1V8)} = 1.8\text{ V}$, $T_{amb} = 25\text{ }^\circ\text{C}$. Minimum and maximum values are across the full temperature range $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ at $V_{DDA} = 3\text{ V}$, $V_{DDD(1V8)} = 1.8\text{ V}$; $V_{i(INP)} - V_{i(INM)} = -1\text{ dBFS}$; internal reference mode; $100\text{ }\Omega$ differential applied to serial outputs; unless otherwise specified.

10. Dynamic characteristics

10.1 Dynamic characteristics

Table 6. Dynamic characteristics^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|-----------------------------|------------------------|-----|------|-----|------|
| α_{2H} | second harmonic level | $f_i = 3\text{ MHz}$ | - | 88 | - | dBc |
| | | $f_i = 30\text{ MHz}$ | - | 87 | - | dBc |
| | | $f_i = 70\text{ MHz}$ | - | 85 | - | dBc |
| | | $f_i = 170\text{ MHz}$ | - | 83 | - | dBc |
| α_{3H} | third harmonic level | $f_i = 3\text{ MHz}$ | - | 87 | - | dBc |
| | | $f_i = 30\text{ MHz}$ | - | 86 | - | dBc |
| | | $f_i = 70\text{ MHz}$ | - | 84 | - | dBc |
| | | $f_i = 170\text{ MHz}$ | - | 82 | - | dBc |
| THD | total harmonic distortion | $f_i = 3\text{ MHz}$ | - | 84 | - | dBc |
| | | $f_i = 30\text{ MHz}$ | - | 83 | - | dBc |
| | | $f_i = 70\text{ MHz}$ | - | 81 | - | dBc |
| | | $f_i = 170\text{ MHz}$ | - | 79 | - | dBc |
| ENOB | effective number of bits | $f_i = 3\text{ MHz}$ | - | 10.7 | - | bits |
| | | $f_i = 30\text{ MHz}$ | - | 10.7 | - | bits |
| | | $f_i = 70\text{ MHz}$ | - | 10.7 | - | bits |
| | | $f_i = 170\text{ MHz}$ | - | 10.6 | - | bits |
| SNR | signal-to-noise ratio | $f_i = 3\text{ MHz}$ | - | 66.2 | - | dBFS |
| | | $f_i = 30\text{ MHz}$ | - | 66.2 | - | dBFS |
| | | $f_i = 70\text{ MHz}$ | - | 66.0 | - | dBFS |
| | | $f_i = 170\text{ MHz}$ | - | 65.8 | - | dBFS |
| SFDR | spurious-free dynamic range | $f_i = 3\text{ MHz}$ | - | 87 | - | dBc |
| | | $f_i = 30\text{ MHz}$ | - | 86 | - | dBc |
| | | $f_i = 70\text{ MHz}$ | - | 84 | - | dBc |
| | | $f_i = 170\text{ MHz}$ | - | 82 | - | dBc |

Table 6. Dynamic characteristics^[1] ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|----------------------------|-------------------------|-----|-----|-----|------|
| IMD | intermodulation distortion | $f_i = 3 \text{ MHz}$ | - | 89 | - | dBc |
| | | $f_i = 30 \text{ MHz}$ | - | 88 | - | dBc |
| | | $f_i = 70 \text{ MHz}$ | - | 86 | - | dBc |
| | | $f_i = 170 \text{ MHz}$ | - | 84 | - | dBc |
| $\alpha_{ct(ch)}$ | channel crosstalk | $f_i = 70 \text{ MHz}$ | - | 100 | - | dBc |

[1] Typical values measured at $V_{DDA} = 3 \text{ V}$, $V_{DDD(1V8)} = 1.8 \text{ V}$, $T_{amb} = 25 \text{ }^\circ\text{C}$. Minimum and maximum values are across the full temperature range $T_{amb} = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$ at $V_{DDA} = 3 \text{ V}$, $V_{DDD(1V8)} = 1.8 \text{ V}$; $V_{i(INP)} - V_{i(INM)} = -1 \text{ dBFS}$; internal reference mode; $100 \text{ } \Omega$ differential applied to serial outputs; unless otherwise specified.

10.2 Clock and digital output timing

Table 7. Clock and digital output characteristics^[1]

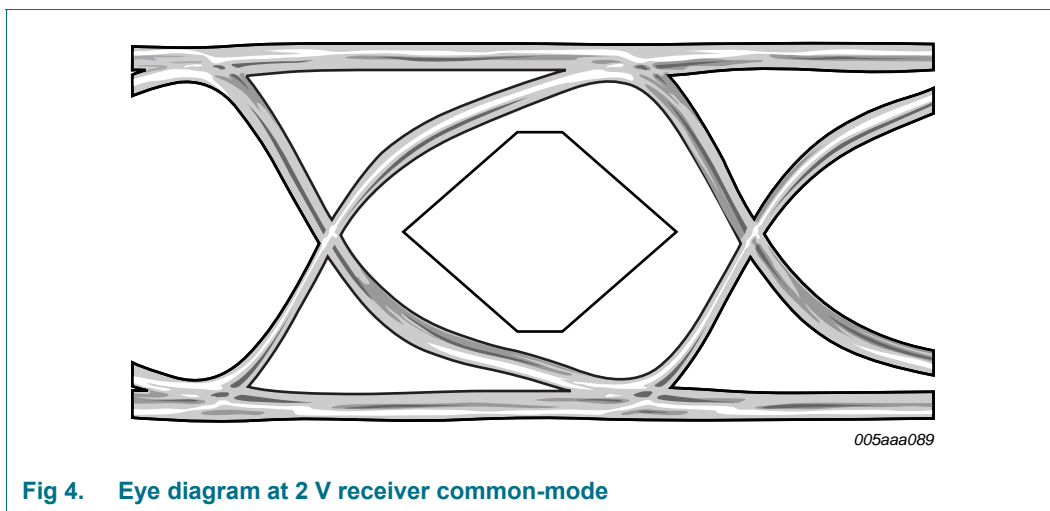
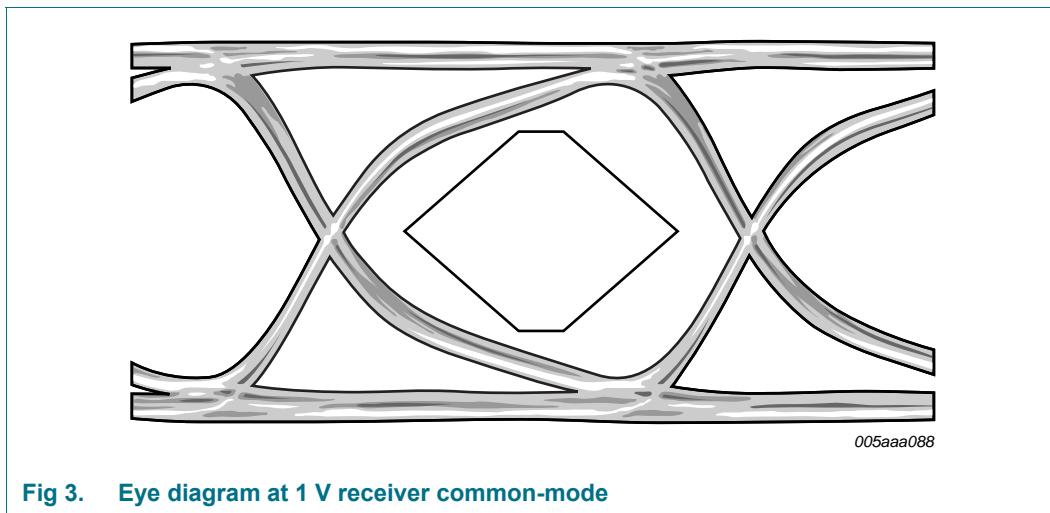
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|---------------------|------------------|-----|-----|-----|---------------|
| pins CLKP and CLKM | | | | | | |
| f_{clk} | clock frequency | | 100 | - | 125 | MspS |
| $t_{lat(data)}$ | data latency time | clock cycles | 160 | - | 170 | ns |
| δ_{clk} | clock duty cycle | DCS_EN = logic 1 | 30 | 50 | 70 | % |
| $t_{d(s)}$ | sampling delay time | | - | 0.8 | - | ns |
| t_{wake} | wake-up time | | - | 76 | - | μs |

[1] Typical values measured at $V_{DDA} = 3 \text{ V}$, $V_{DDD(1V8)} = 1.8 \text{ V}$, $T_{amb} = 25 \text{ }^\circ\text{C}$. Minimum and maximum values are across the full temperature range $T_{amb} = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$ at $V_{DDA} = 3 \text{ V}$, $V_{DDD(1V8)} = 1.8 \text{ V}$; $V_{i(INP)} - V_{i(INM)} = -1 \text{ dBFS}$; internal reference mode; $100 \text{ } \Omega$ differential applied to serial outputs; unless otherwise specified.

10.3 Serial output timing

The eye diagram of the serial output is shown in Figure 3 and Figure 4. Test conditions are:

- 3.125 Gbps data rate
- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- DC-coupling with two different receiver common-mode voltages



10.4 SPI timing

Table 8. SPI timing characteristics^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|-------------------------|---|-----|-----|-----|------|
| $t_{w(SCLK)}$ | SCLK pulse width | | - | 40 | - | ns |
| $t_{w(SCLKH)}$ | SCLK HIGH pulse width | | - | 16 | - | ns |
| $t_{w(SCLKL)}$ | SCLK LOW pulse width | | - | 16 | - | ns |
| t_{su} | set-up time | data to SCLK HIGH | - | 5 | - | ns |
| | | \overline{CS} to SCLK HIGH | - | 5 | - | ns |
| t_h | hold time | data to SCLK HIGH | - | 2 | - | ns |
| | | \overline{CS} to SCLK HIGH ² | - | 2 | - | ns |
| $f_{clk(max)}$ | maximum clock frequency | | - | 25 | - | MHz |

[1] Typical values measured at $V_{DDA} = 3\text{ V}$, $V_{DDD(1V8)} = 1.8\text{ V}$, $T_{amb} = 25\text{ }^\circ\text{C}$. Minimum and maximum values are across the full temperature range $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ at $V_{DDA} = 3\text{ V}$, $V_{DDD(1V8)} = 1.8\text{ V}$; $V_{i(INP)} - V_{i(INM)} = -1\text{ dBFS}$; internal reference mode; $100\text{ }\Omega$ differential applied to serial outputs; unless otherwise specified.

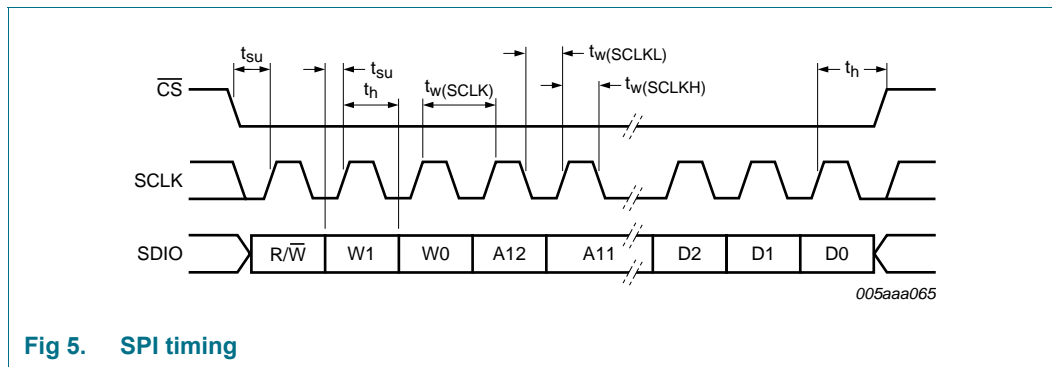


Fig 5. SPI timing

11. Application information

11.1 Analog inputs

11.1.1 Input stage description

The analog input of the ADC1113S supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM set to $0.5V_{DDA}$.

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see Section 11.2 and Table 21).

Figure 6 shows the equivalent circuit of the sample-and-hold input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics.

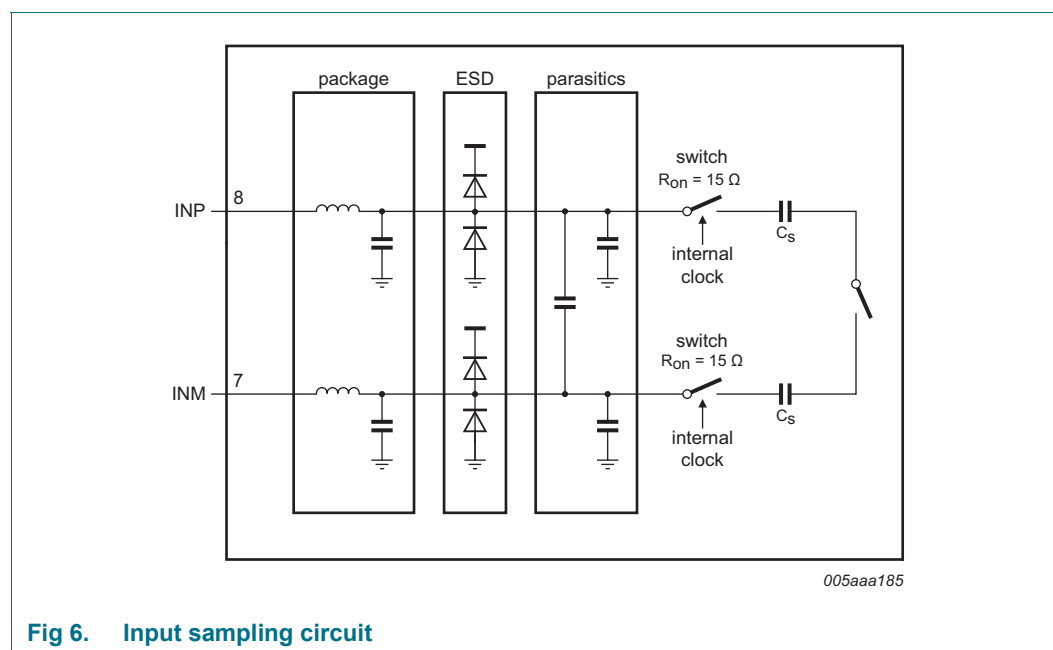


Fig 6. Input sampling circuit

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

11.1.2 Anti-kickback circuitry

Anti-kickback circuitry (RC filter in Figure 7) is needed to counteract the effects of a charge injection generated by the sampling capacitance.

The RC filter is also used to filter noise from the signal before it reaches the sampling stage. The value of the capacitor should be chosen to maximize noise attenuation without degrading the settling time excessively.

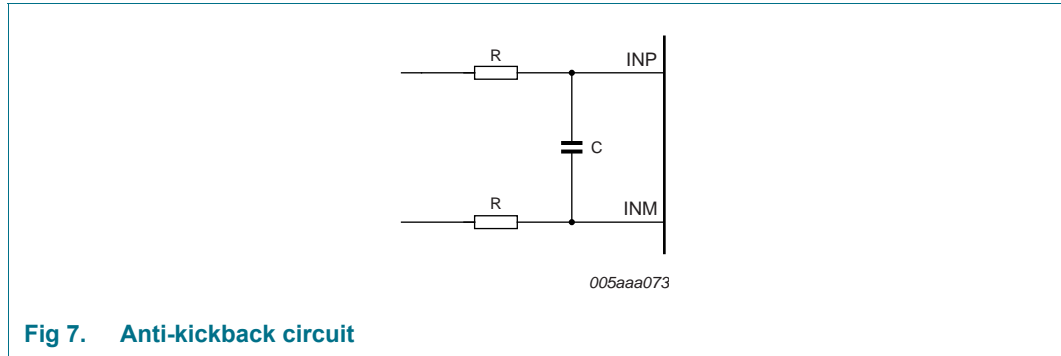


Fig 7. Anti-kickback circuit

The component values are determined by the input frequency and should be selected so as not to affect the input bandwidth.

Table 9. RC-coupling versus input frequency, typical values

| Input frequency (MHz) | Resistance (Ω) | Capacitance (pF) |
|-----------------------|-------------------------|------------------|
| 3 | 25 | 12 |
| 70 | 12 | 8 |
| 170 | 12 | 8 |

11.1.3 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in Figure 8 would be suitable for a baseband application.

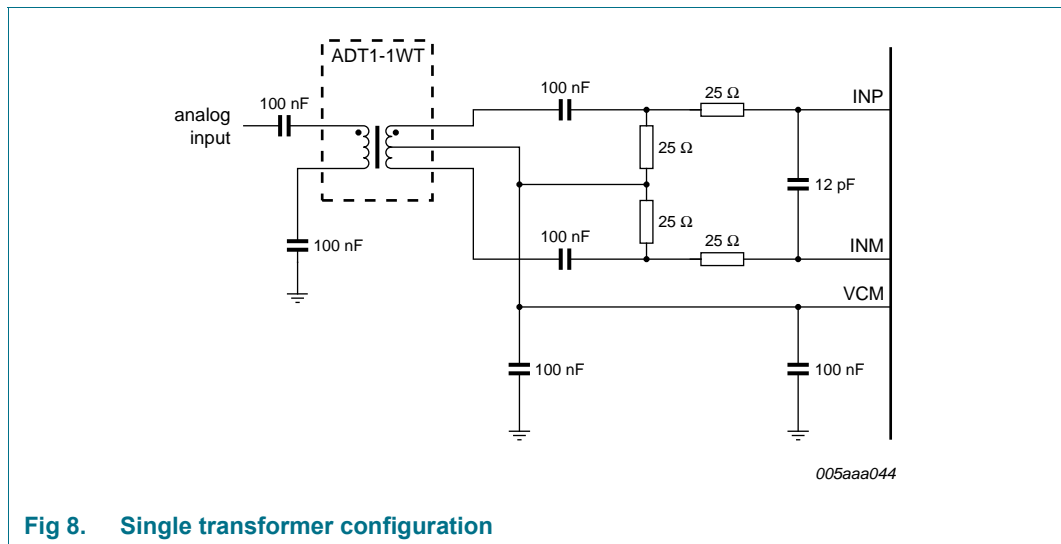


Fig 8. Single transformer configuration

The configuration shown in Figure 9 is recommended for high frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

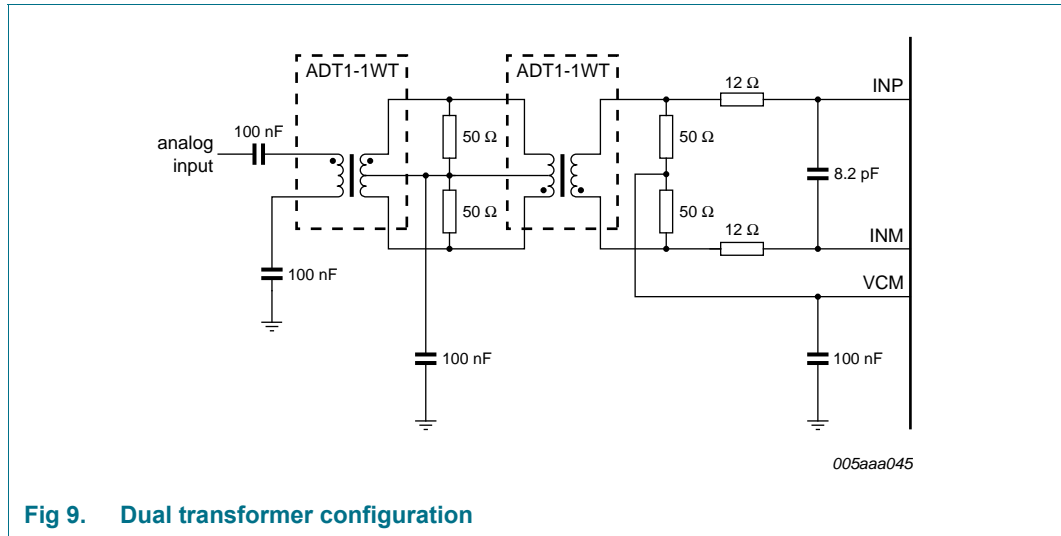


Fig 9. Dual transformer configuration

11.2 System reference and power management

11.2.1 Internal/external reference

The ADC1113S has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF and SENSE (see Figure 11 to Figure 14), in 1 dB steps between 0 dB and -6 dB, via SPI control bits INTREF[2:0] (when bit INTREF_EN = logic 1; see Table 21). The equivalent reference circuit is shown in Figure 10. An external reference is also possible by providing a voltage on pin VREF as described in Figure 14.

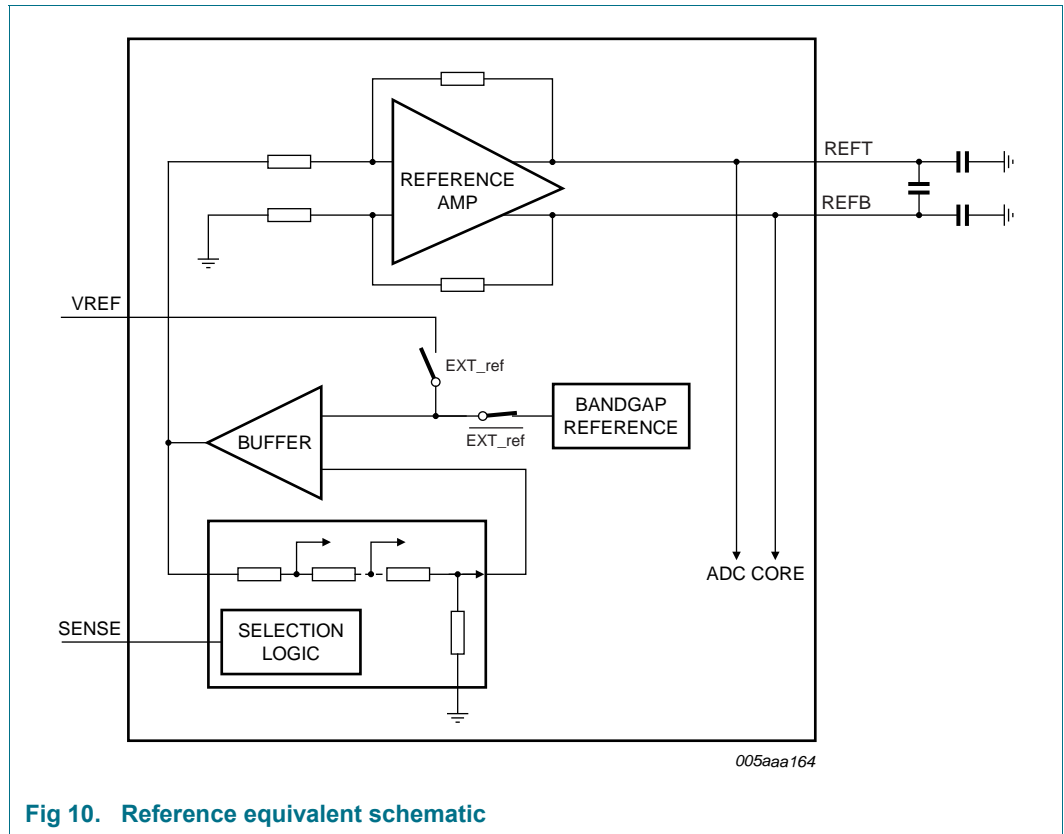


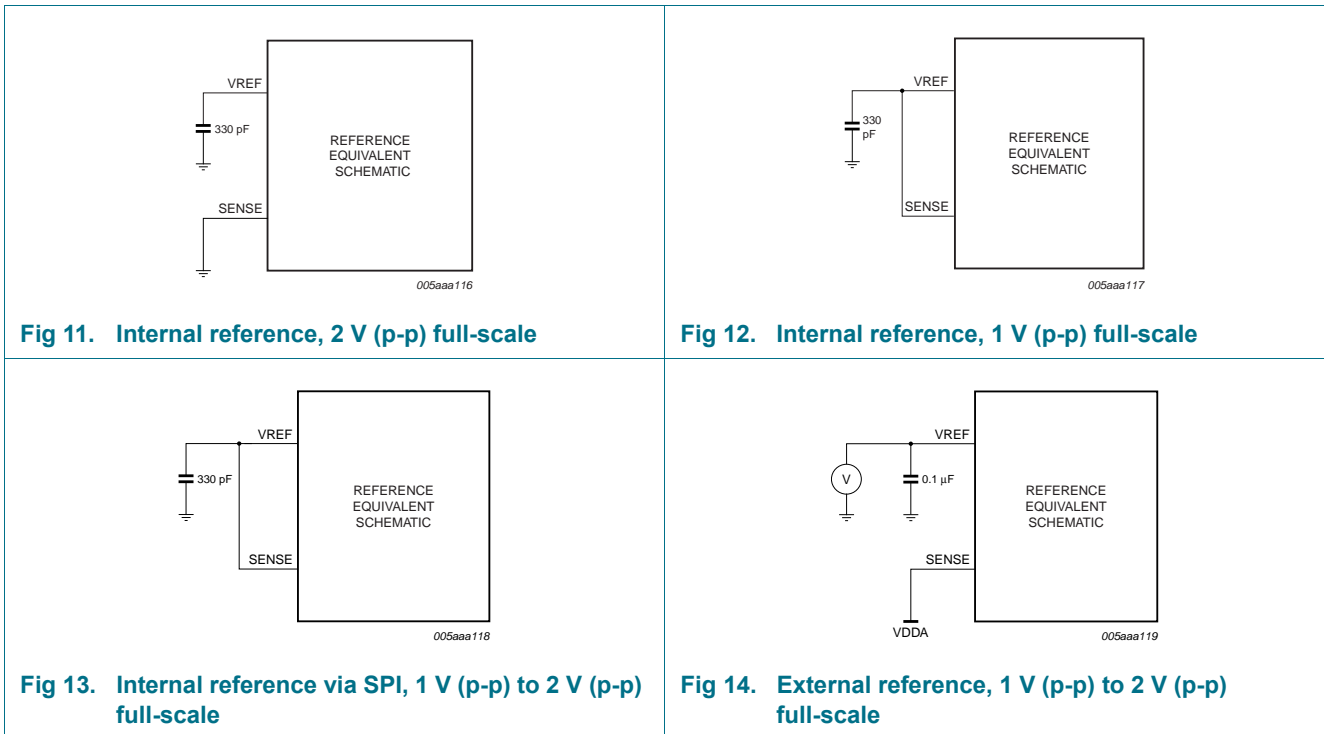
Fig 10. Reference equivalent schematic

If bit INTREF_EN is set to logic 0, the reference voltage is determined either internally or externally as detailed in Table 10.

Table 10. Reference modes

| Mode | SPI bit, "Internal reference" | SENSE pin | VREF pin | Full-scale (V (p-p)) |
|--------------------------------|-------------------------------|--|------------------------------------|----------------------|
| Internal (Figure 11) | 0 | GND | 330 pF capacitor to GND | 2 |
| Internal (Figure 12) | 0 | VREF pin = SENSE pin and 330 pF capacitor to GND | | 1 |
| Internal, SPI mode (Figure 12) | 1 | VREF pin = SENSE pin and 330 pF capacitor to GND | | 1 to 2 |
| External (Figure 14) | 0 | V _{DDA} | external voltage from 0.5 V to 1 V | 1 to 2 |

Figure 11 to Figure 14 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.



11.2.2 Programmable full-scale

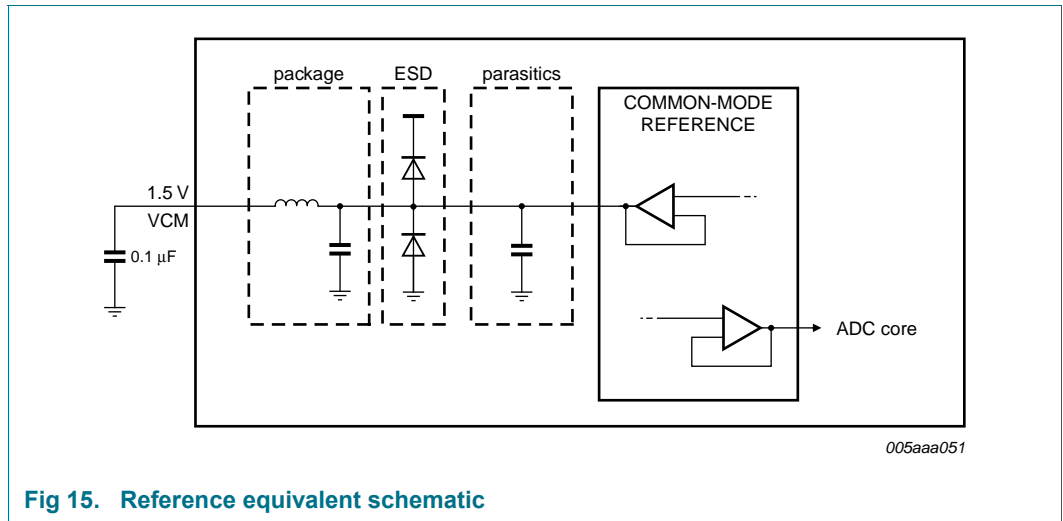
The full-scale is programmable between 1 V (p-p) to 2 V (p-p) (see Table 11).

Table 11. Reference SPI gain control

| INTREF[2:0] | Level (dB) | Full-scale (V (p-p)) |
|-------------|------------|----------------------|
| 000 | 0 | 2 |
| 001 | -1 | 1.78 |
| 010 | -2 | 1.59 |
| 011 | -3 | 1.42 |
| 100 | -4 | 1.26 |
| 101 | -5 | 1.12 |
| 110 | -6 | 1 |
| 111 | not used | x |

11.2.3 Common-mode output voltage ($V_{O(cm)}$)

An 0.1 μF filter capacitor should be connected between pin VCM and ground to ensure a low-noise common-mode output voltage. When AC-coupled, this pin can be used to set the common-mode reference for the analog inputs, for instance via a transformer middle point.



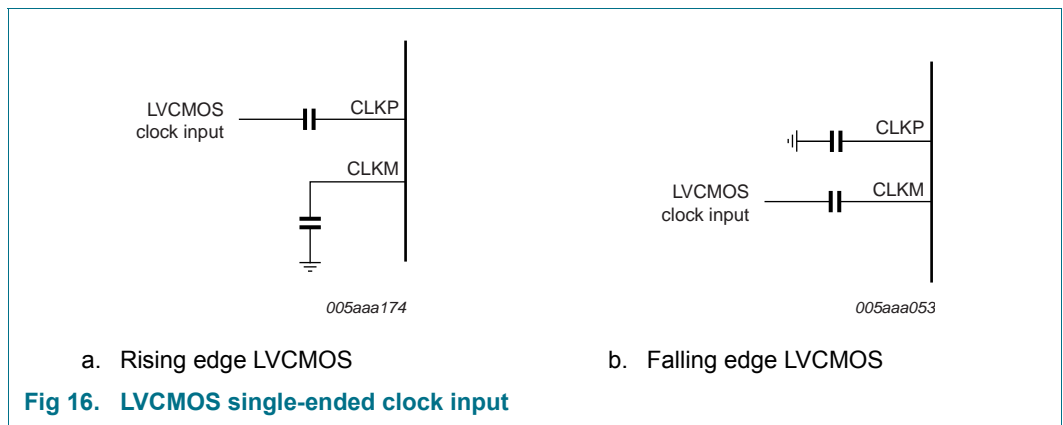
11.2.4 Biasing

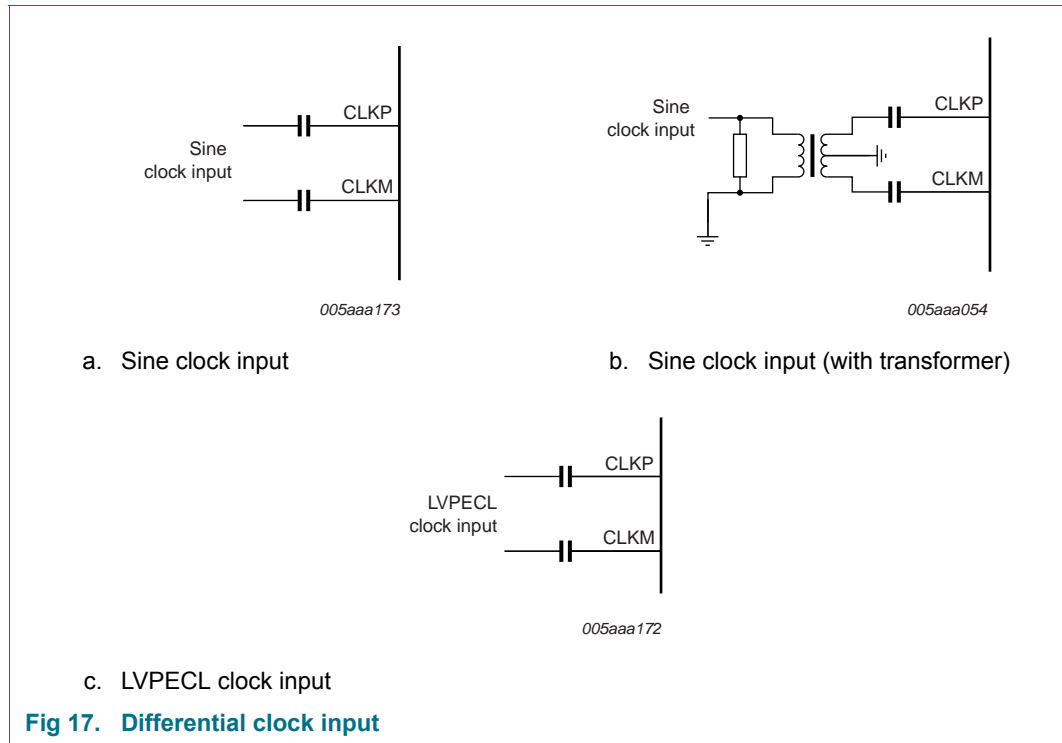
The common-mode input voltage ($V_{I(cm)}$) on pins INP and INM should be set externally to $0.5V_{DDA}$ for optimal performance and should always be between 0.9 V and 2 V.

11.3 Clock input

11.3.1 Drive modes

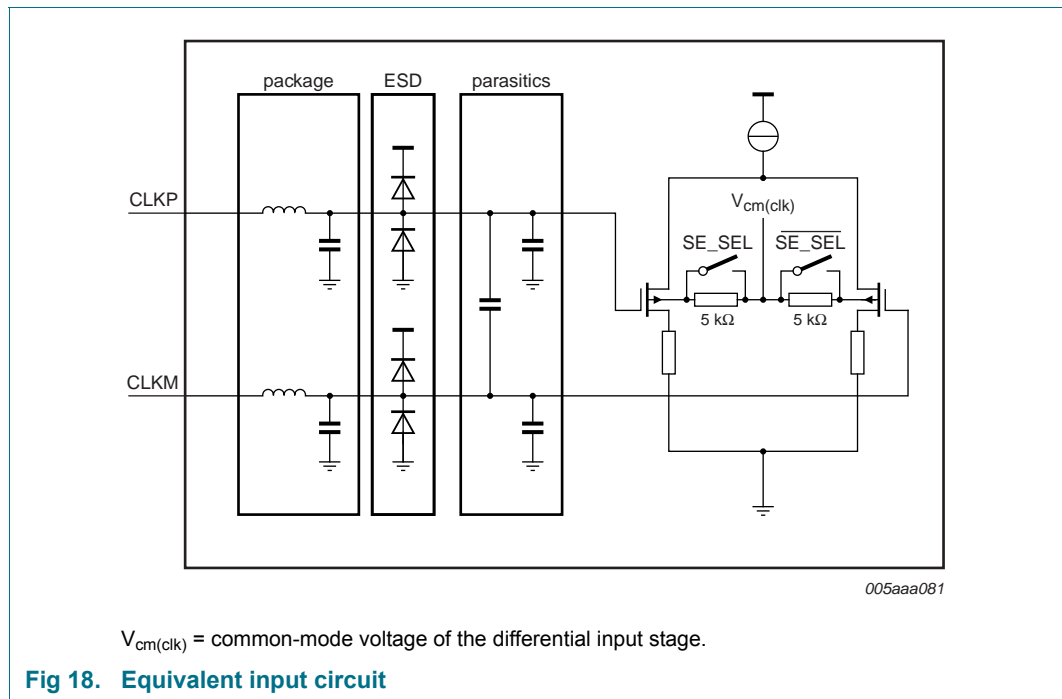
The ADC1113S125 can be driven differentially (LVPECL). It can also be driven by a single-ended LVCMOS signal connected to pin CLKP (CLKM should be connected to ground via a capacitor).





11.3.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 18. The common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.



Single-ended or differential clock inputs can be selected via the SPI (see Table 20). If single-ended is selected, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting bit SE_SEL accordingly, the unused pin should be connected to ground via a capacitor.

11.3.3 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performance of the ADC by compensating the input clock signal duty cycle. When the duty cycle stabilizer is active (bit DCS_EN = logic 1; see Table 20), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = logic 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

Table 12. Duty cycle stabilizer

| Bit DCS_EN | Description |
|------------|-------------------------------|
| 0 | duty cycle stabilizer disable |
| 1 | duty cycle stabilizer enable |

11.3.4 Clock input divider

The ADC1113S contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV2_SEL = logic 1; see Table 20). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

11.4 Digital outputs

11.4.1 Serial output equivalent circuit

The JESD204A standard specifies that if the receiver and the transmitter are DC-coupled, both must be fed from the same supply.

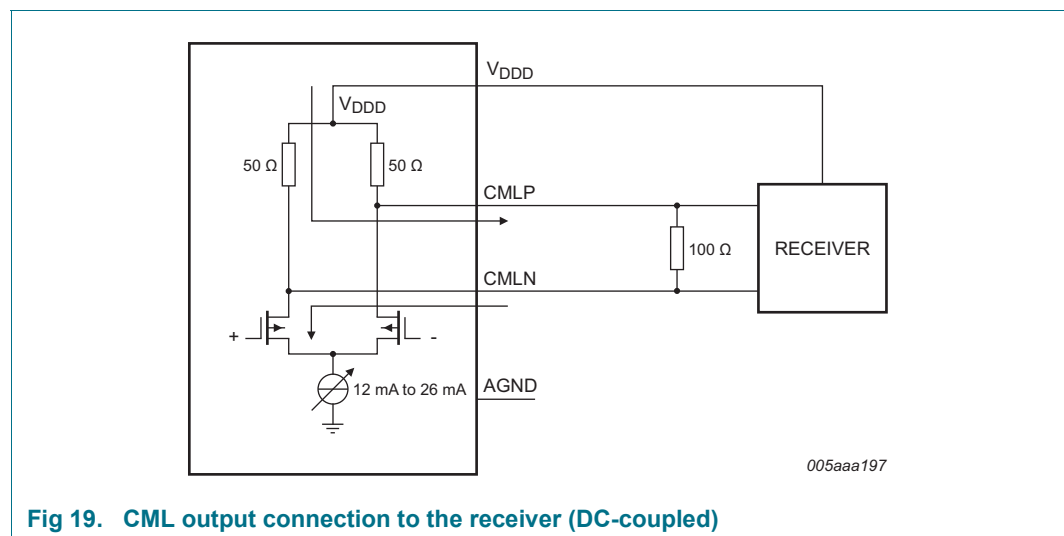


Fig 19. CML output connection to the receiver (DC-coupled)

The output should be terminated when 100 Ω (typical) is reached at the receiver side.

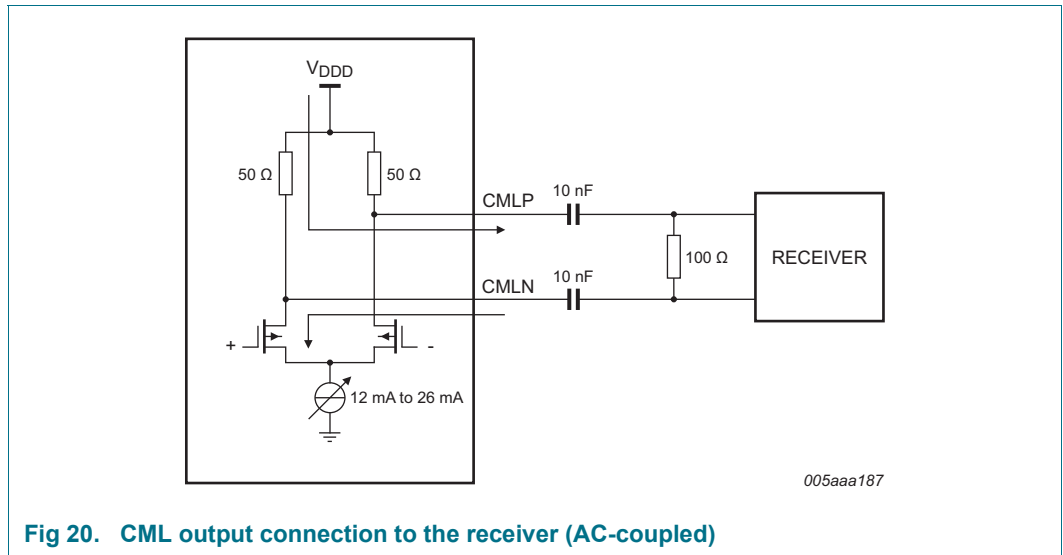


Fig 20. CML output connection to the receiver (AC-coupled)

11.5 JESD204A serializer

For more information about the JESD204A standard refer to the JEDEC web site.

11.5.1 Digital JESD204A formatter

The block placed after the ADC core is used to implement all functions of the JESD204A standard. This ensures signal integrity and guarantees the clock and the data recovery at the receiver side.

The block is highly parameterized and can be configured in various ways depending on the sampling frequency and the number of lanes used.

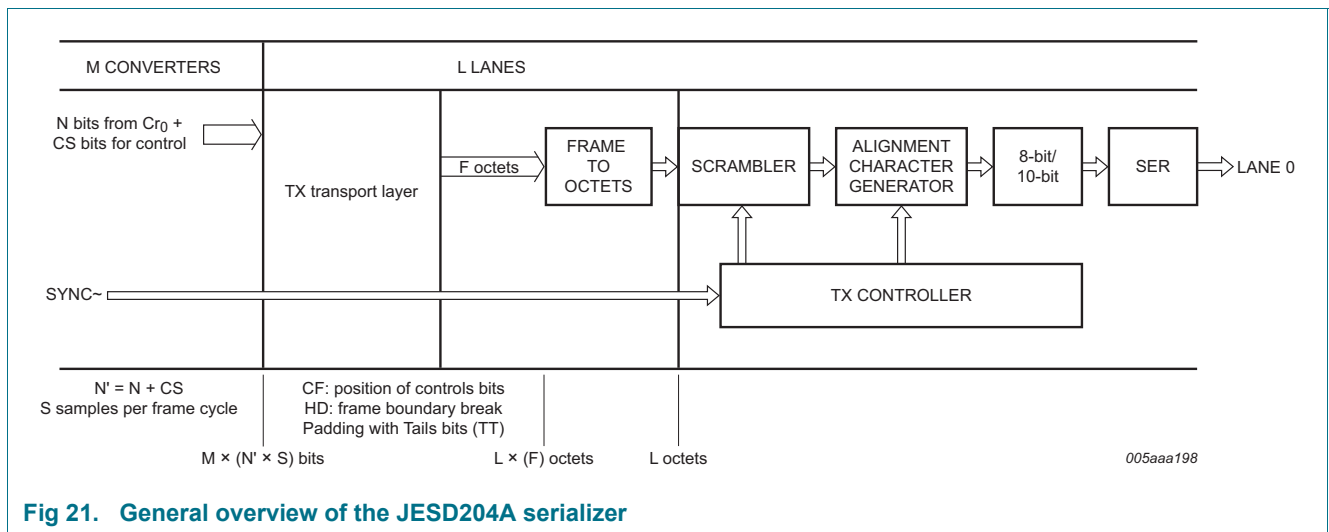


Fig 21. General overview of the JESD204A serializer

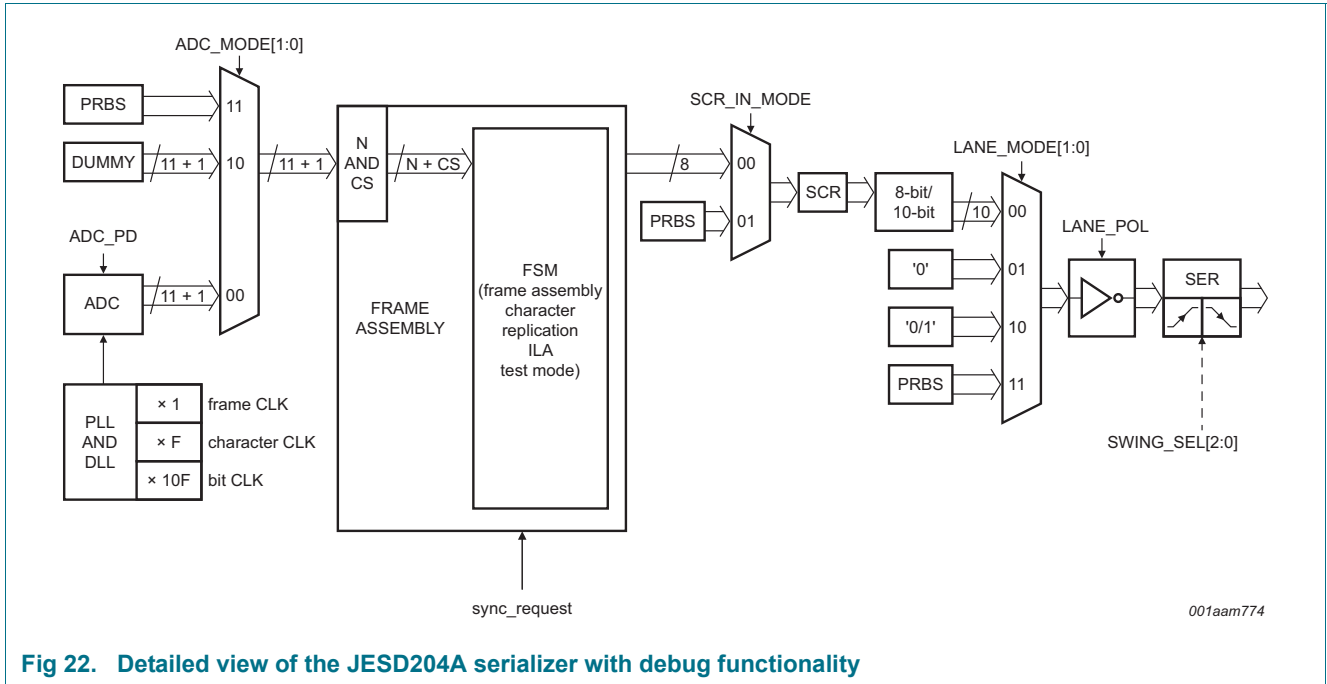


Fig 22. Detailed view of the JESD204A serializer with debug functionality

11.5.2 ADC core output codes versus input voltage

Table 13 shows the data output codes for a given analog input voltage.

Table 13. Output codes versus input voltage

| INP – INM (V) | Offset binary | Two's complement | OTR |
|---------------|---------------|------------------|-----|
| < -1 | 000 0000 0000 | 100 0000 0000 | 1 |
| -1.0000000 | 000 0000 0000 | 100 0000 0000 | 0 |
| -0.9990234 | 000 0000 0001 | 100 0000 0001 | 0 |
| -0.9980469 | 000 0000 0010 | 100 0000 0010 | 0 |
| -0.9970703 | 000 0000 0011 | 100 0000 0011 | 0 |
| -0.996093 | 000 0000 0100 | 100 0000 0100 | 0 |
| | | | 0 |
| -0.0019531 | 011 1111 1110 | 111 1111 1110 | 0 |
| -0.0009766 | 011 1111 1111 | 111 1111 1111 | 0 |
| 0.0000000 | 100 0000 0000 | 000 0000 0000 | 0 |
| +0.0009766 | 100 0000 0001 | 000 0000 0001 | 0 |
| +0.0019531 | 100 0000 0010 | 000 0000 0010 | 0 |
| | | | 0 |
| +0.9970703 | 111 1111 1011 | 011 1111 1011 | 0 |
| +0.99990845 | 111 1111 1100 | 011 1111 1100 | 0 |
| +0.9980469 | 111 1111 1101 | 011 1111 1101 | 0 |
| +0.9990234 | 111 1111 1110 | 011 1111 1110 | 0 |
| +1.0000000 | 111 1111 1111 | 011 1111 1111 | 0 |
| > +1 | 111 1111 1111 | 011 1111 1111 | 1 |

11.6 Serial Peripheral Interface (SPI)

11.6.1 Register description

The ADC1113S serial interface is a synchronous serial communications port allowing for easy interfacing with many industry microprocessors. It provides access to the registers that control the operation of the chip in both read and write modes.

This interface is configured as a 3-wire type (SDIO as bidirectional pin).

Pin SCLK acts as the serial clock and pin $\overline{\text{CS}}$ acts as the serial chip select.

Each read/write operation is sequenced by the $\overline{\text{CS}}$ signal and enabled by a LOW level to drive the chip with N bytes, depending on the content of the instruction byte (see Table 14).

Table 14. SPI instruction bytes

| | MSB | | | | | | | LSB |
|-------------|--------------------|----|----|-----|-----|-----|----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Description | R/W ^[1] | W1 | W0 | A12 | A11 | A10 | A9 | A8 |
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

[1] R/W indicates whether a read (logic 1) or write (logic 0) transfer occurs after the instruction byte.

Table 15. Read or Write mode access description

| R/W ^[1] | Description |
|--------------------|----------------------|
| 0 | Write mode operation |
| 1 | Read mode operation |

[1] Bits W1 and W0 indicate the number of bytes transferred.

Table 16. Number of bytes to be transferred

| W1 | W0 | Number of bytes transferred |
|----|----|-----------------------------|
| 0 | 0 | 1 byte |
| 0 | 1 | 2 bytes |
| 1 | 0 | 3 bytes |
| 1 | 1 | 4 or more bytes |

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is incremented to access subsequent addresses.

The steps involved in a data transfer are as follows:

1. The falling edge on pin $\overline{\text{CS}}$ in combination with a rising edge on pin SCLK determine the start of communications.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data which can vary in length but is always a multiple of 8 bits. The Most Significant Bit (MSB) is always sent first (for instruction and data bytes)
4. A rising edge on pin $\overline{\text{CS}}$ indicates the end of data transmission.

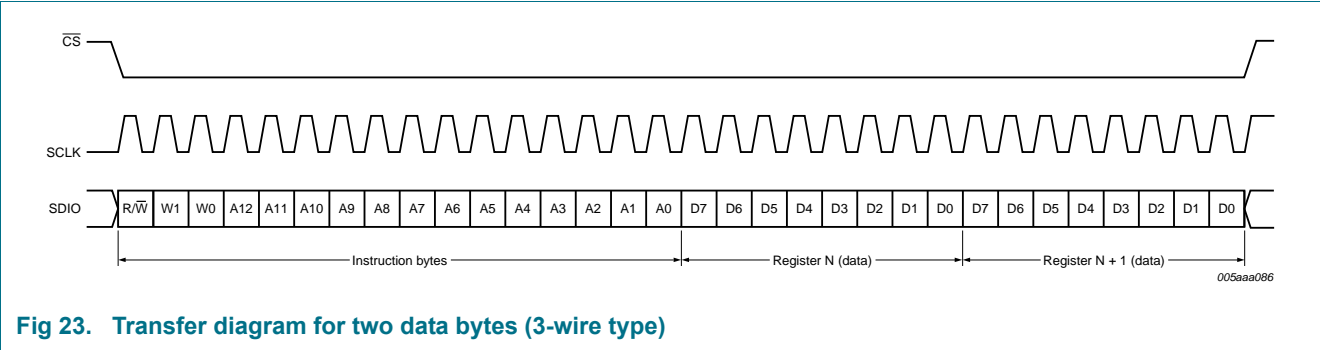


Fig 23. Transfer diagram for two data bytes (3-wire type)

11.6.2 Channel control

Table 17. Register allocation map

| Address (hex) | Register name | Access ^[1] | Bit definition | | | | | | | | Default ^[2] (bin) |
|-----------------------------|----------------------------|-----------------------|-----------------|---------------|-----------------|-------------------|------------|----------------|-------------|------------|---------------------------------|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| ADC control register | | | | | | | | | | | |
| 0003 | SPI control | R/W | - | - | - | - | - | - | ENABLE | - | 1111 1111 |
| 0005 | Reset and Power-down modes | R/W | SW_RST | - | - | - | - | - | PD[1:0] | | 0000 0000 |
| 0006 | Clock | R/W | - | - | - | SE_SEL | DIFF_SE | - | CLKDIV2_SEL | DCS_EN | 0000 000* |
| 0008 | Vref | R/W | - | - | - | - | INTREF_EN | INTREF[2:0] | | 0000 0000 | |
| 0013 | Offset | R/W | - | - | DIG_OFFSET[5:0] | | | | | 0000 0000 | |
| 0014 | Test pattern 1 | R/W | - | - | - | - | - | TESTPAT_1[2:0] | | 0000 0000 | |
| 0015 | Test pattern 2 | R/W | TESTPAT_2[10:3] | | | | | | | 0000 0000 | |
| 0016 | Test pattern 3 | R/W | TESTPAT_3[2:0] | | | - | - | - | - | - | 0000 0000 |
| JESD204A control | | | | | | | | | | | |
| 0801 | Ser_Status | R | RXSYNC_ERROR | RESERVED[2:0] | | | 0 | 0 | POR_TST | RESERVED | 0001 0000 |
| 0802 | Ser_Reset | R/W | SW_RST | 0 | 0 | 0 | FSM_SW_RST | 0 | 0 | 0 | 0000 0000 |
| 0805 | Ser_Control1 | R/W | 0 | RESERVED | SYNC_POL | SYNC_SINGLE_ENDED | 1 | REV_SCR | REV_ENCODER | REV_SERIAL | 0100 1001 |
| 0808 | Ser_Analog_Ctrl | R/W | 0 | 0 | 0 | 0 | 0 | SWING_SEL[2:0] | | 0000 0011 | |
| 0809 | Ser_ScramblerA | R/W | 0 | LSB_INIT[6:0] | | | | | | | 0000 0000 |

Table 17. Register allocation map ...continued

| Address (hex) | Register name | Access ^[1] | Bit definition | | | | | | | | Default ^[2] (bin) |
|------------------|----------------|-----------------------|----------------|--------------|----------------|----------|----------|-----------|----------------|-----------|---------------------------------|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 080A | Ser_ScramblerB | R/W | MSB_INIT[7:0] | | | | | | | | 1111 1111 |
| 080B | Ser_PRBS_Ctrl | R/W | 0 | 0 | 0 | 0 | 0 | 0 | PRBS_TYPE[1:0] | | 0000 0000 |
| 0820 | Cfg_0_DID | R | DID[7:0] | | | | | | | | 1110 1101 |
| 0821 | Cfg_1_BID | R/W* | 0 | 0 | 0 | 0 | BID[3:0] | | | 0000 1010 | |
| 0822 | Cfg_3_SCR_L | R/W* | SCR | 0 | 0 | 0 | 0 | 0 | 0 | L | 0000 0000 |
| 0823 | Cfg_4_F | R/W* | 0 | 0 | 0 | 0 | 0 | F[2:0] | | 0000 0*** | |
| 0824 | Cfg_5_K | R/W* | 0 | 0 | 0 | K[4:0] | | | | 000* **** | |
| 0825 | Cfg_6_M | R/W* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | M | 0000 000* |
| 0826 | Cfg_7_CS_N | R/W* | 0 | CS[0] | 0 | 0 | N[3:0] | | | 0100 0001 | |
| 0827 | Cfg_8_Np | R/W | 0 | 0 | 0 | NP[4:0] | | | | 0000 1111 | |
| 0828 | Cfg_9_S | R/W* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | S | 0000 0000 |
| 0829 | Cfg_10_HD_CF | R/W* | HD | 0 | 0 | 0 | 0 | 0 | CF[1:0] | | *000 0000 |
| 082D | Cfg_02_2_LID | R/W* | 0 | 0 | 0 | LID[4:0] | | | | 0001 1100 | |
| 084D | Cfg02_13_FCHK | R | FCHK[7:0] | | | | | | | | **** **** |
| 0871 | Lane_0_Ctrl | R/W | 0 | SCR_IN_ MODE | LANE_MODE[1:0] | | 0 | LANE_ POL | RESERVED | LANE_PD | 0000 0000 |
| 0891 | ADC_0_Ctrl | R/W | 0 | 0 | ADC_MODE[1:0] | | 0 | 0 | 0 | ADC_PD | 0000 0000 |

[1] An "*" in the R/W column means that this register is subject to control access conditions in Write mode.

[2] An "*" in the Default column replaces a bit whose value depends on the binary level of external pins.

11.6.3 Register description

11.6.3.1 ADC control registers

Table 18. Register SPI control (address 0003h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|--------|---------------------------------------|
| 7 to 2 | - | - | 111111 | not used |
| 1 | ENABLE | R/W | | ADC SPI control enable: |
| | | | 0 | ADC does not get the next SPI command |
| | | | 1 | ADC gets the next SPI command |
| 0 | - | - | 1 | not used |

Table 19. Register Reset and Power-down mode (address 0005h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------|--------|-------|--------------------------------------|
| 7 | SW_RST | R/W | | reset digital part: |
| | | | 0 | no reset |
| | | | 1 | performs a reset of the digital part |
| 6 to 2 | - | - | 00000 | not used |
| 1 to 0 | PD[1:0] | R/W | | Power-down mode: |
| | | | 00 | normal (power-up) |
| | | | 01 | full power-down |
| | | | 10 | sleep |
| | | | 11 | normal (power-up) |

Table 20. Register Clock (address 0006h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|---|
| 7 to 5 | - | - | 000 | not used |
| 4 | SE_SEL | R/W | | select SE clock input pin: |
| | | | 0 | select CLKM input |
| | | | 1 | select CLKP input |
| 3 | DIFF_SE | R/W | | differential/single-ended clock input select: |
| | | | 0 | fully differential |
| | | | 1 | single-ended |
| 2 | - | - | 0 | not used |
| 1 | CLKDIV2_SEL | R/W | | select clock input divider by 2: |
| | | | 0 | disable |
| | | | 1 | enable |
| 0 | DCS_EN | R/W | | duty cycle stabilizer enable: |
| | | | 0 | disable |
| | | | 1 | enable |

Table 21. Register Vref (address 0008h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|------------|---|
| 7 to 4 | - | - | 0000 | not used |
| 3 | INTREF_EN | R/W | | enable internal programmable VREF mode: |
| | | | 0 | disable |
| | | | 1 | enable |
| 2 to 0 | INTREF[2:0] | R/W | | programmable internal reference: |
| | | | 000 | 0 dB (FS = 2 V) |
| | | | 001 | -1 dB (FS = 1.78 V) |
| | | | 010 | -2 dB (FS = 1.59 V) |
| | | | 011 | -3 dB (FS = 1.42 V) |
| | | | 100 | -4 dB (FS = 1.26 V) |
| | | | 101 | -5 dB (FS = 1.12 V) |
| | | | 110 | -6 dB (FS = 1 V) |
| | | | 111 | not used |

Table 22. Digital offset adjustment (address 0013h)

Default values are highlighted.

| Register offset | | |
|-----------------|-----------------|---------|
| Decimal | DIG_OFFSET[5:0] | |
| +31 | 011111 | +31 LSB |
| ... | ... | ... |
| 0 | 000000 | 0 |
| ... | ... | ... |
| -32 | 100000 | -32 LSB |

Table 23. Register Test pattern 1 (address 0014h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|------------|--|
| 7 to 3 | - | - | 00000 | not used |
| 2 to 0 | TESTPAT_1[2:0] | R/W | | digital test pattern: |
| | | | 000 | off |
| | | | 001 | mid-scale |
| | | | 010 | - FS |
| | | | 011 | + FS |
| | | | 100 | toggle '1111..1111'/'0000..0000' |
| | | | 101 | custom test pattern, to be written in register 0015h and 0016h |
| | | | 110 | '010101...' |
| | | | 111 | '101010...' |

Table 24. Register Test pattern 2 (address 0015h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------|--------|-----------------|---|
| 7 to 0 | TESTPAT_2[10:3] | R/W | 00000000 | custom digital test pattern (bit 10 to 3) |

Table 25. Register Test pattern 3 (address 0016h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|------------|--|
| 7 to 5 | TESTPAT_3[2:0] | R/W | 000 | custom digital test pattern (bit 2 to 0) |
| 4 to 0 | - | - | 00000 | not used |

11.6.4 JESD204A digital control registers

Table 26. Ser_Status (address 0801h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|----------|--|
| 7 | RXSYNC_ERROR | R | 0 | set to 1 when a synchronization error occurs |
| 6 to 4 | RESERVED[2:0] | - | 001 | reserved |
| 3 to 2 | - | - | 00 | not used |
| 1 | POR_TST | R | 0 | power-on-reset |
| 0 | RESERVED | - | 0 | reserved |

Table 27. Ser_Reset (address 0802h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|----------|--|
| 7 | SW_RST | R/W | 0 | initiates a software reset of the JESD204A unit |
| 6 to 4 | - | - | 000 | not used |
| 3 | FSM_SW_RST | R/W | 0 | initiates a software reset of the internal state machine of JESD204A unit |
| 2 to 0 | - | - | 000 | not used |

Table 28. Ser_Control1 (address 0805h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-------------------|--------|----------|---|
| 7 | - | - | 0 | not used |
| 6 | RESERVED | - | 1 | reserved |
| 5 | SYNC_POL | R/W | | defines the synchronization signal polarity: |
| | | | 0 | synchronization signal is active LOW |
| | | | 1 | synchronization signal is active HIGH |
| 4 | SYNC_SINGLE_ENDED | R/W | | defines the input mode of the synchronization signal: |
| | | | 0 | synchronization input mode is set in Differential mode |
| | | | 1 | synchronization input mode is set in Single-ended mode |
| 3 | - | - | 1 | not used |
| 2 | REV_SCR | - | | LSBs are swapped with MSBs at the scrambler input: |
| | | | 0 | disable |
| | | | 1 | enable |

Table 28. Ser_Control1 (address 0805h) ...continued

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-------------|--------|----------|---|
| 1 | REV_ENCODER | - | | LSBs are swapped with MSBs at the 8-bit/10-bit encoder input: |
| | | | 0 | disable |
| | | | 1 | enable |
| 0 | REV_SERIAL | - | | LSBs are swapped with MSBs at the lane input: |
| | | | 0 | disable |
| | | | 1 | enable |

Table 29. Ser_Analog_Ctrl (address 0808h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|------------|---|
| 7 to 3 | - | - | 00000 | not used |
| 2 to 0 | SWING_SEL[2:0] | R/W | 011 | defines the swing output for the lane pads |

Table 30. Ser_ScramblerA (address 0809h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|----------------|---|
| 7 | - | - | 0 | not used |
| 6 to 0 | LSB_INIT[6:0] | R/W | 0000000 | defines the initialization vector for the scrambler polynomial (lower) |

Table 31. Ser_ScramblerB (address 080Ah)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-----------------|---|
| 7 to 0 | MSB_INIT[7:0] | R/W | 11111111 | defines the initialization vector for the scrambler polynomial (upper) |

Table 32. Ser_PRBS_Ctrl (address 080Bh)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-------------------|--|
| 7 to 2 | - | - | 000000 | not used |
| 1 to 0 | PRBS_TYPE[1:0] | R/W | | defines the type of Pseudo-Random Binary Sequence (PRBS) generator to be used: |
| | | | 00 (reset) | PRBS-7 |
| | | | 01 | PRBS-7 |
| | | | 10 | PRBS-23 |
| | | | 11 | PRBS-31 |

Table 33. Cfg_0_DID (address 0820h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------|--------|-----------------|--|
| 7 to 0 | DID[7:0] | R | 11101101 | defines the device (= link) identification number |

Table 34. Cfg_1_BID (address 0821h)*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|----------|--------|-------------|---|
| 7 to 4 | - | - | 0000 | not used |
| 3 to 0 | BID[3:0] | R/W | 1010 | defines the bank ID – extension to DID |

Table 35. Cfg_3_SCR_L (address 0822h)*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|--------|---|
| 7 | SCR | R/W | 0 | scrambling enabled |
| 6 to 1 | - | - | 000000 | not used |
| 0 | L | R/W | 0 | defines the number of lanes per converter device, minus 1 |

Table 36. Cfg_4_F (address 0823h)*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|------------|---|
| 7 to 3 | - | - | 00000 | not used |
| 2 to 0 | F[2:0] | R/W | *** | defines the number of octets per frame, minus 1 |

Table 37. Cfg_5_K (address 0824h)*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|--------------|--|
| 7 to 5 | - | - | 000 | not used |
| 4 to 0 | K[4:0] | R/W | ***** | defines the number of frames per multiframe, minus 1 |

Table 38. Cfg_6_M (address 0825h)*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|----------|--|
| 7 to 1 | - | - | 0000000 | not used |
| 0 | M | R/W | * | defines the number of converters per device, minus 1 |

Table 39. Cfg_7_CS_N (address 0826h)*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|-------|--|
| 7 | - | - | 0 | not used |
| 6 | CS[0] | R/W | 1 | defines the number of control bits per sample, minus 1 |
| 5 to 4 | - | - | 00 | not used |
| 3 to 0 | N[3:0] | R/W | 0001 | defines the converter resolution |

Table 40. Cfg_8_Np (address 0827h)*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------|--------|-------|--|
| 7 to 5 | - | - | 000 | not used |
| 4 to 0 | NP[4:0] | R/W | 01111 | defines the total number of bits per sample, minus 1 |

Table 41. Cfg_9_S (address 0828h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|----------|--|
| 7 to 1 | - | - | 0000000 | not used |
| 0 | S | R/W | 0 | defines number of samples per converter per frame cycle |

Table 42. Cfg_10_HD_CF (address 0829h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------|--------|-------|---|
| 7 | HD | R/W | * | defines high density format |
| 6 to 2 | - | - | 00000 | not used |
| 1 to 0 | CF[1:0] | R/W | 00 | defines number of control words per frame clock cycle per link. |

Table 43. Cfg_02_2_LID (address 082Dh)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------|--------|--------------|---|
| 7 to 5 | - | - | 000 | not used |
| 4 to 0 | LID[4:0] | R/W | 11100 | defines lane identification number |

Table 44. Cfg02_13_FCHK (address 084Dh)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|---|
| 7 to 0 | FCHK[7:0] | R | ***** | defines the checksum value for lane checksum corresponds to the sum of all the link configuration parameters module 256 (as defined in JEDEC Standard No.204A) |

Table 45. Lane_0_Ctrl (address 0871h)

Default values are highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-------------------|--|
| 7 | - | - | 0 | not used |
| 6 | SCR_IN_MODE | R/W | 0 (reset) | defines the input type for scrambler and 8-bit/10-bit units (normal mode) = input of the scrambler and 8-bit/10-bit units is the output of the frame assembly unit. |
| | | | 1 | input of the scrambler and 8-bit/10-bit units is the PRBS generator (PRBS type is defined with "PRBS_TYPE[1:0]" (Ser_PRBS_Ctrl register) |
| 5 to 4 | LANE_MODE[1:0] | R/W | 00 (reset) | defines output type of lane output unit: normal mode: lane output is the 8-bit/10-bit output unit |
| | | | 01 | constant mode: lane output is set to a constant (0 × 0) |
| | | | 10 | toggle mode: lane output is toggling between 0 × 0 and 0 × 1 |
| | | | 11 | PRBS mode: lane output is the PRBS generator (PRBS type is defined with "PRBS_TYPE[1:0]" (Ser_PRBS_Ctrl register) |
| 3 | - | - | 0 | not used |

Table 45. Lane_0_Ctrl (address 0871h) ...continued*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|----------|--------------------------------|
| 2 | LANE_POL | R/W | | defines lane polarity: |
| | | | 0 | lane polarity is normal |
| | | | 1 | lane polarity is inverted |
| 1 | RESERVED | R/W | 0 | reserved |
| 0 | LANE_PD | R/W | | lane power-down control: |
| | | | 0 | lane is operational |
| | | | 1 | lane is in Power-down mode |

Table 46. ADC_0_Ctrl (address 0891h)*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------------------|--|
| 7 to 6 | - | - | 00 | not used |
| 5 to 4 | ADC_MODE[1:0] | R/W | | defines input type of JESD204A unit |
| | | | 00 (reset) | ADC output is connected to the JESD204A input |
| | | | 01 | not used |
| | | | 10 | JESD204A input is fed with a dummy constant, set to: OTR = 0 and ADC[13:0] = "10011011101010" |
| | | | 11 | JESD204A is fed with a PRBS generator (PRBS type is defined with "PRBS_TYPE[1:0]" (Ser_PRBS_Ctrl register) |
| 3 to 1 | - | - | 000 | not used |
| 0 | ADC_PD | R/W | | ADC power-down control: |
| | | | 0 | ADC is operational |
| | | | 1 | ADC is in Power-down mode |

12. Package outline

HVQFN32R: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; resin based; body 7 x 7 x 0.8 mm

SOT1152-1

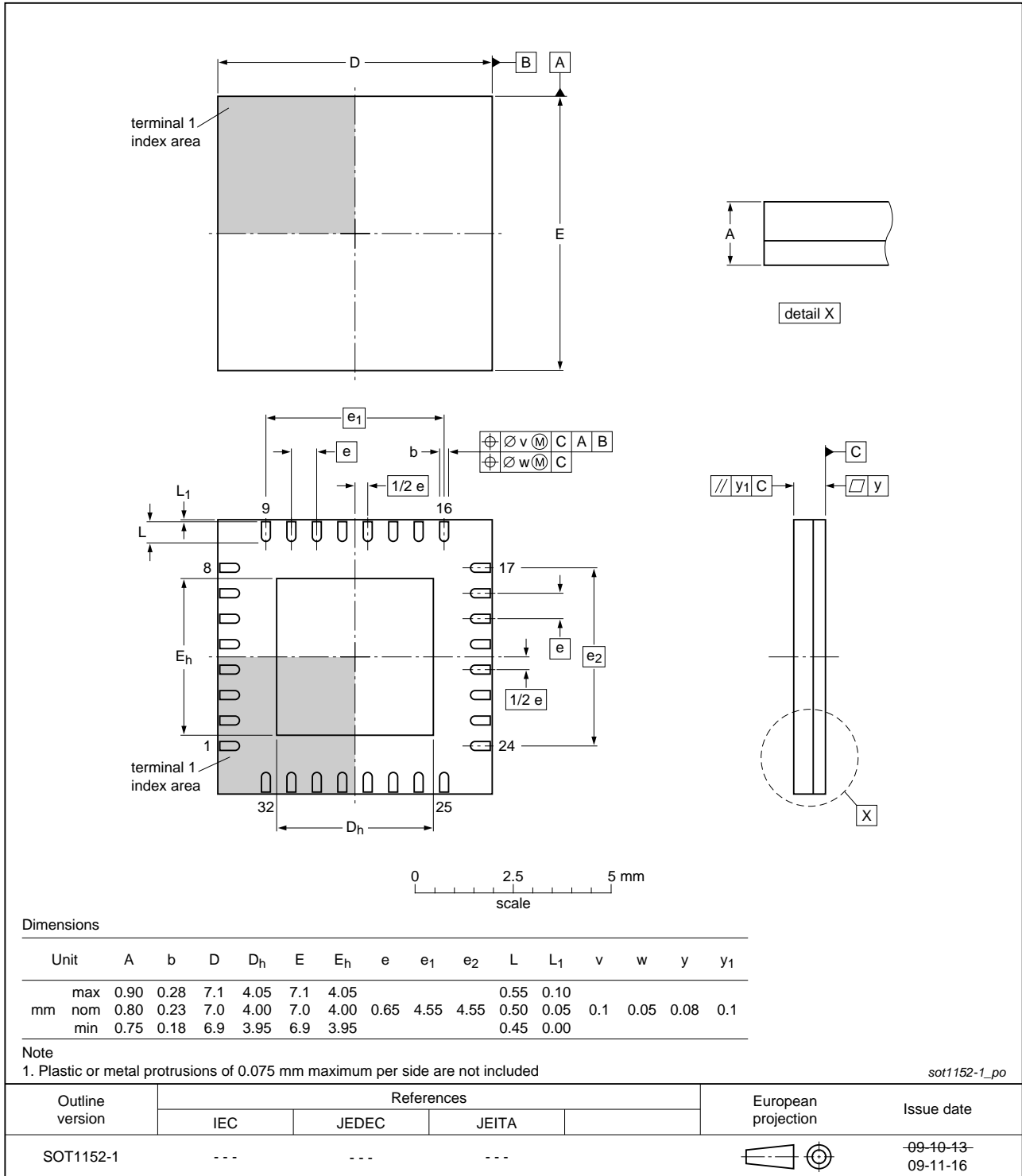


Fig 24. Package outline SOT1152-1 (HVQFN32)

13. Abbreviations

Table 47. Abbreviations

| Acronym | Description |
|---------|---|
| ADC | Analog-to-Digital Converter |
| DCS | Duty Cycle Stabilizer |
| ESD | ElectroStatic Discharge |
| IF | Intermediate Frequency |
| IMD | InterModulation Distortion |
| LSB | Least Significant Bit |
| LVCMOS | Low-Voltage Complementary Metal-Oxide Semiconductor |
| LVPECL | Low-Voltage Positive Emitter-Coupled Logic |
| MSB | Most Significant Bit |
| OTR | Out-of-Range |
| PRBS | Pseudo-Random Binary Sequence |
| SFDR | Spurious-Free Dynamic Range |
| SNR | Signal-to-Noise Ratio |
| SPI | Serial Peripheral Interface |
| TX | Transmitter |

14. Revision history

Table 48. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|-----------------|
| ADC1113S125 v.2 | 20120702 | Product data sheet | - | ADC1113S125 v.1 |
| ADC1113S125 v.1 | 20110315 | Product data sheet | - | - |

15. Contact information

For more information or sales office addresses, please visit: <http://www.idt.com>

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