FAST CMOS 16-BIT TRANSPARENT LATCH
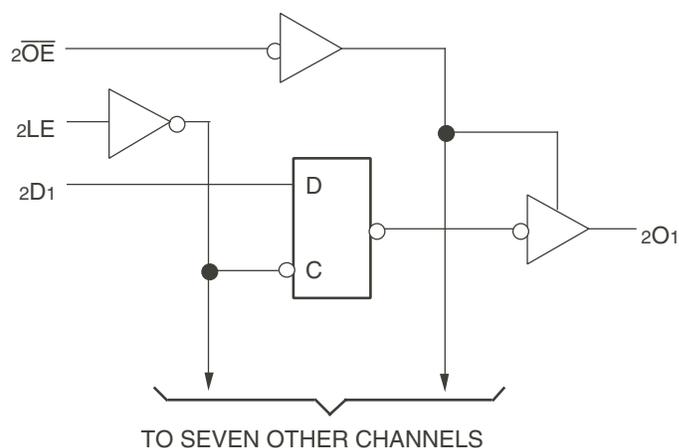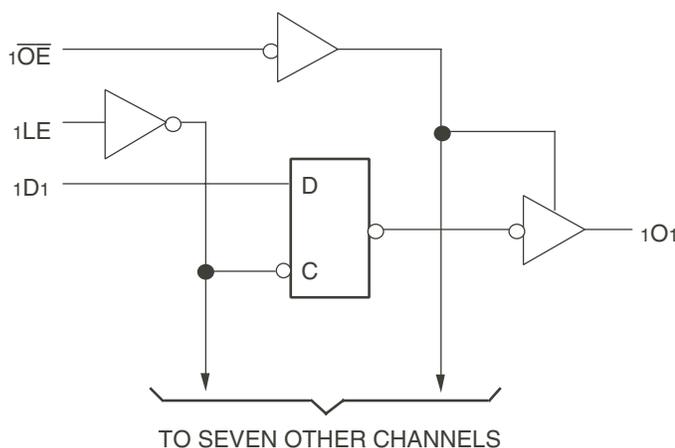
IDT74FCT162373AT/CT/ET

FEATURES:

- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- Low input and output leakage ≤1µA (max.)
- V_{CC} = 5V ±10%
- Balanced Output Drivers: ±24mA
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
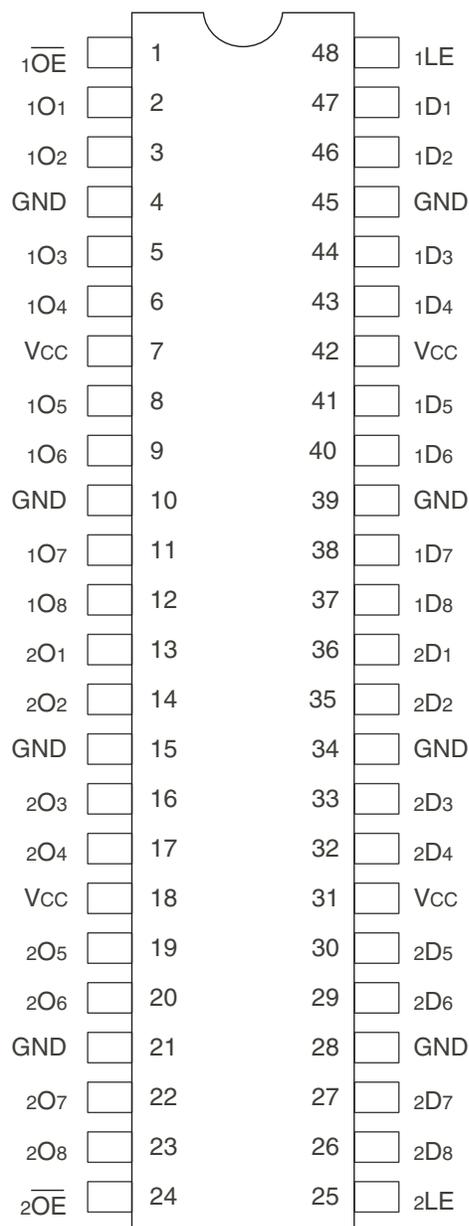- Available in SSOP and TSSOP packages

DESCRIPTION:

The FCT162373T 16-bit transparent D-type latch is built using advanced dual metal CMOS technology. This high-speed, low-power latch is ideal for temporary storage of data. It can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches, or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162373T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162373T is a plug-in replacement for the FCT16373T and ABT16373 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM

TO SEVEN OTHER CHANNELS

TO SEVEN OTHER CHANNELS

INDUSTRIAL TEMPERATURE RANGE

SEPTEMBER 2009

DSC-5455/6

PIN CONFIGURATION

1$\overline{OE}$	1	48	1LE
1O1	2	47	1D1
1O2	3	46	1D2
GND	4	45	GND
1O3	5	44	1D3
1O4	6	43	1D4
VCC	7	42	VCC
1O5	8	41	1D5
1O6	9	40	1D6
GND	10	39	GND
1O7	11	38	1D7
1O8	12	37	1D8
2O1	13	36	2D1
2O2	14	35	2D2
GND	15	34	GND
2O3	16	33	2D3
2O4	17	32	2D4
VCC	18	31	VCC
2O5	19	30	2D5
2O6	20	29	2D6
GND	21	28	GND
2O7	22	27	2D7
2O8	23	26	2D8
2$\overline{OE}$	24	25	2LE

SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to VCC+0.5	V
T_{STG}	Storage Temperature	−65 to +150	°C
I_{OUT}	DC Output Current	−60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Output and I/O terminals terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active HIGH)
x$\overline{OE}$	Outputs Enable Input (Active LOW)
xOx	3-State Outputs

FUNCTION TABLE[1]

Inputs			Outputs
xDx	xLE	x$\overline{OE}$	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	µA
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	5	500	µA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24mA	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.55	V

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Togging 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Togging	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
		$x\overline{OE}$ = GND xLE = V_{CC} Sixteen Bits Togging	V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
 f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol	Parameter	Condition[1]	74FCT162373AT Min.[2]	Max.	74FCT162373CT Min.[2]	Max.	74FCT162373ET Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xDx to xOx	$C_L = 50pF$ $R_L = 500\Omega$	1.5	5.2	1.5	4.2	1.5	3.4	ns
t_{PLH} t_{PHL}	Propagation Delay xLE to xOx		2	8.5	2	5.5	1.5	3.7	ns
t_{PZL} t_{PZH}	Output Enable Time		1.5	6.5	1.5	5.5	1.5	4.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.5	1.5	5	1.5	3.6	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xLE		2	—	2	—	1	—	ns
t_H	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1	—	ns
t_W	xLE Pulse Width HIGH		5	—	5	—	3[4]	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
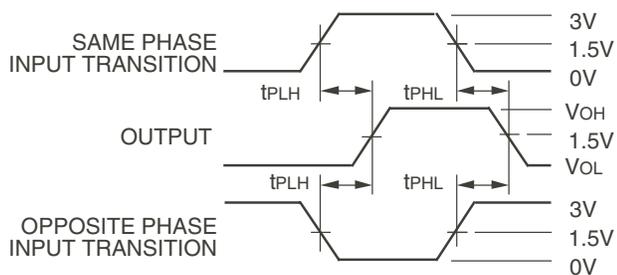4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS
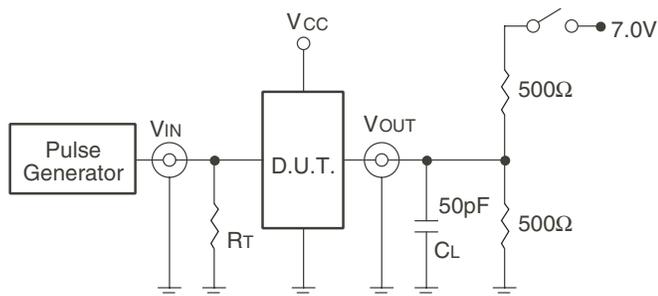
Test Circuits for All Outputs
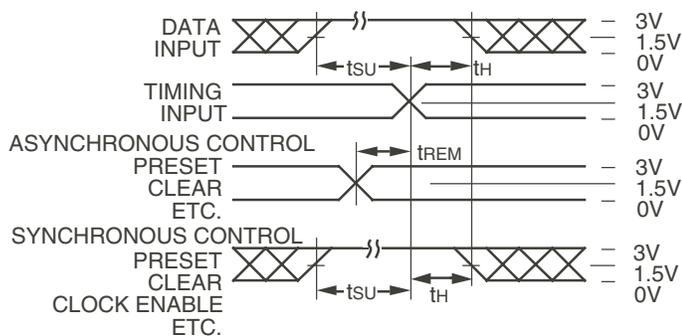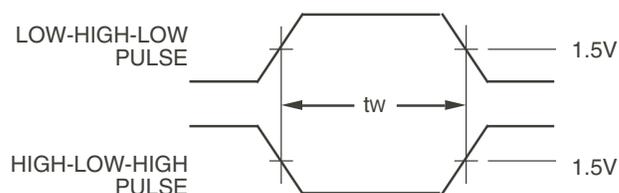

Set-up, Hold, and Release Times
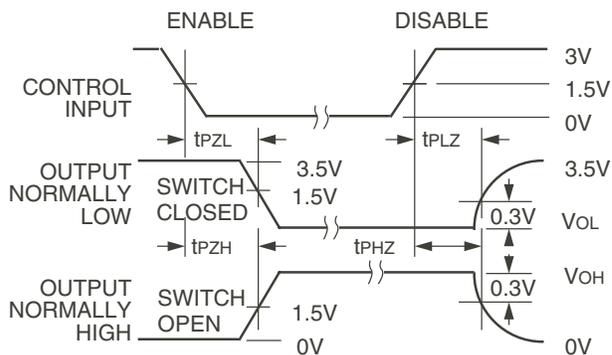

Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
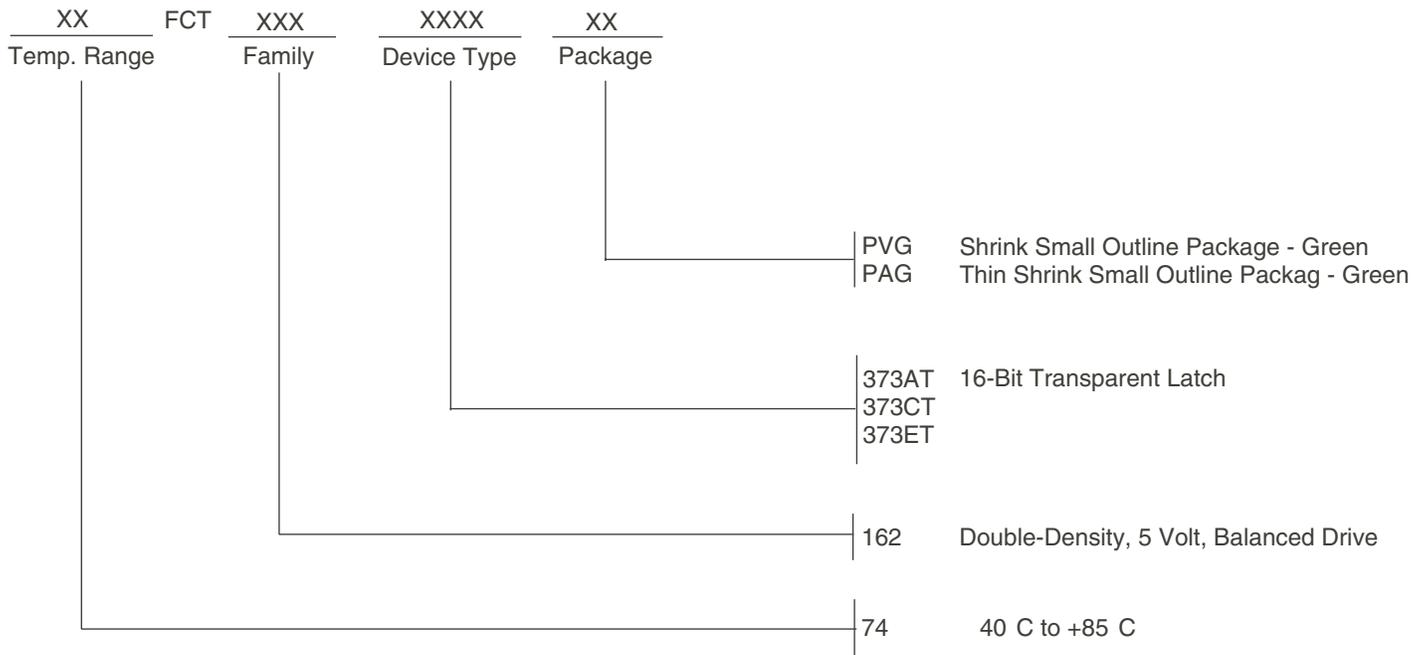

Pulse Width

Enable and Disable Times

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq$ 1.0MHz; $t_F \leq$ 2.5ns; $t_R \leq$ 2.5ns.

ORDERING INFORMATION

| XX | FCT | XXX | XXXX | XX |
| Temp. Range | | Family | Device Type | Package |

PVG   Shrink Small Outline Package - Green
PAG   Thin Shrink Small Outline Packag - Green

373AT   16-Bit Transparent Latch
373CT
373ET

162   Double-Density, 5 Volt, Balanced Drive

74   40 C to +85 C

Datasheet Document History

09/06/09 Pg.6   Updated the ordering information by removing the "IDT" notation and non RoHS part.