Local Temperature Sensor

TS3001GB2A0
Data Sheet

Description

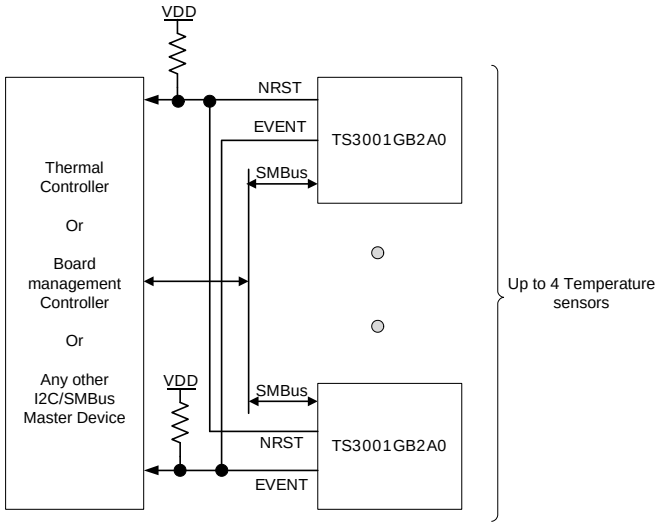
The TS3001GB2A0 digital temperature sensor with accuracy up to ±0.5°C was designed to target applications demanding highest level of temperature readout.

The digital temperature sensor comes with several user-programmable registers to provide maximum flexibility for temperature-sensing applications. The registers allow specifying critical, upper, and lower temperature limits as well as hysteresis settings. Both the limits and hysteresis values are used for communicating temperature events from the chip to the system. This communication is done using $\overline{\text{Event}}$ pin, which has an open-drain configuration. The user has the option of setting the $\overline{\text{Event}}$ pin polarity as either an active-low or active-high comparator output for thermostat operation, or as a temperature event interrupt output for microprocessor-based systems.

An additional output open-drain pin, NRST is also sensitive to temperature thresholds and releases a low pulse after TCRIT temperature limit has been exceeded followed by TLOW limit crossing.

The sensor uses an industry standard 2-wire, I^2C/SMBus serial interface, and allows up to four devices to be controlled on the bus.

Typical Applications



Features

- Temperature Sensor
- Single Supply: 3.3V *± 5%*
- Accurate timeout support
  - Meets strict SMBus spec of 25ms (min) 35ms (max)
- Timeout supported in all Modes
  - *Active mode*
  - *Shutdown mode*
- Schmitt trigger and noise filtering on bus inputs
- 2-wire Serial Interface: 10-400 kHz I^2C™ /SMBus™
- Package: TDFN-8

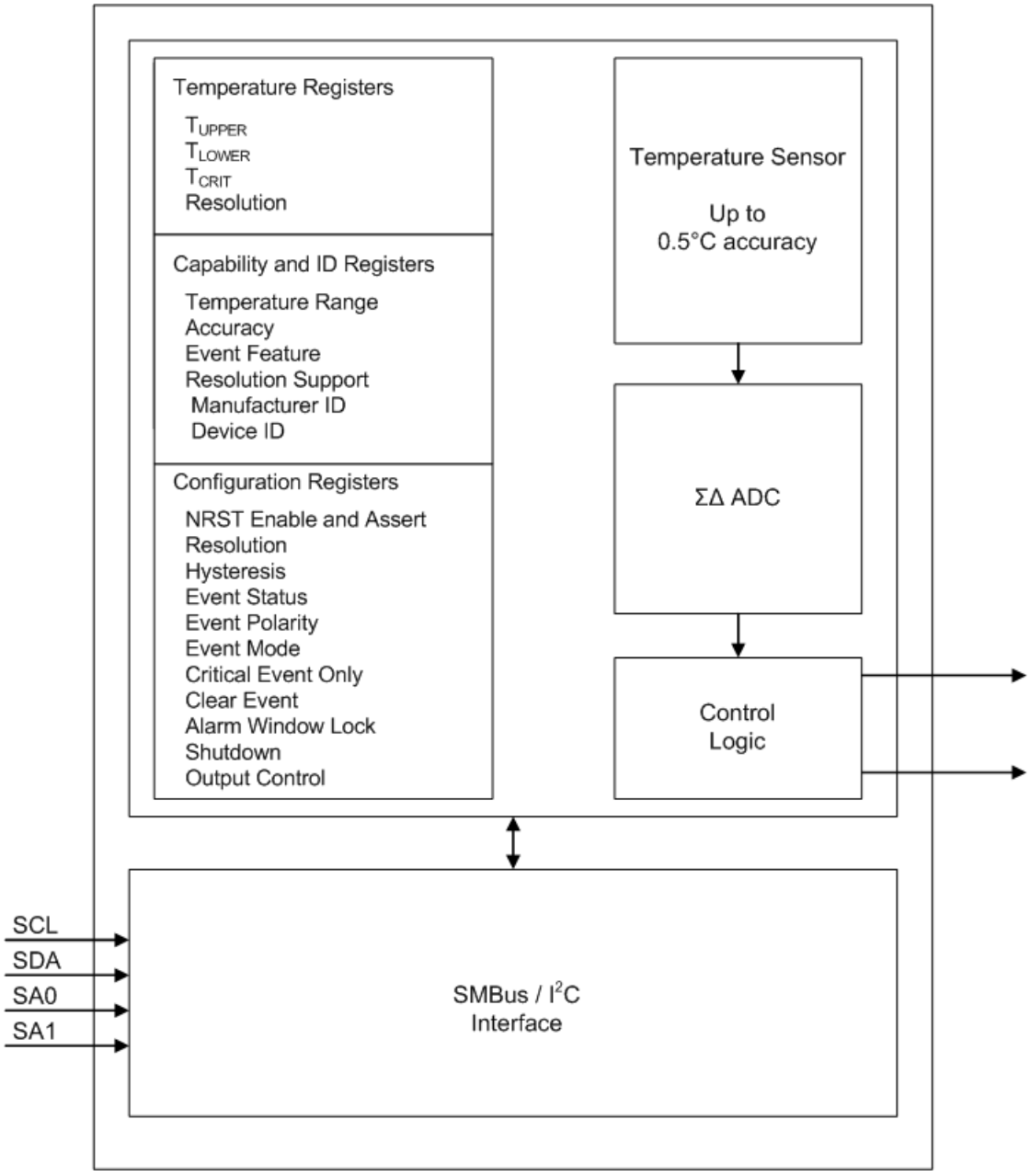
Temperature Sensor Features

- Temperature Converted to Digital Data
- Sampling Rate of 100ms (max)
- EVENT and NRST outputs based on temperature threshold events
- Selectable 0, 1.5°C, 3°C, 6°C Hysteresis
- Programmable Resolution from 0.0625°C to 0.5°C
- Accuracy:
  - *±0.5°C/ ±1.0°C (typ/max)from +75°C to +95°C*
  - *±1.0°C/±2.0°C (typ/max) from +40°C to +125°C*
  - *±2.0°C/ ±3.0°C (typ/max) from -20°C to +125°C*

Typical Applications

- Electric Power Module
- Servers, Laptops, Ultra-portables, PC Boards
- High end audio / video equipment
- Portable devices
- Hard Disk Drives and Other PC Peripherals

Block Diagram: Temperature Sensor



Maximum Ratings

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
T_{STG}	Storage Temperature	-65	150	°C
V_{IO}	Input or output range, SA0	-0.50	10	V
	Input or output range, other pins	-0.50	4.3	V
V_{DD}	Supply Voltage	-0.5	4.3	V

DC and AC Parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters. DC Characteristics

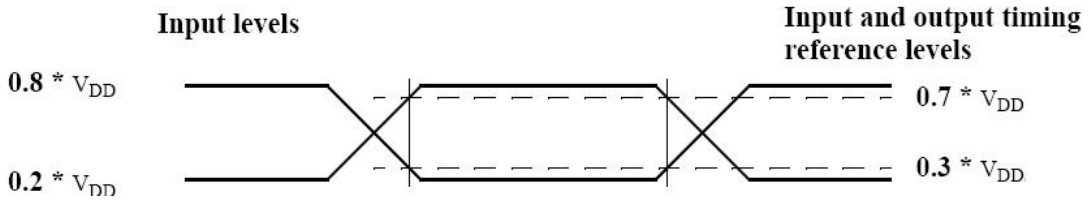
Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Ambient operating temperature	-20	125	°C

AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Units
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input levels	$0.2*V_{DD}$ to $0.8*V_{DD}$		V
	Input and output timing reference levels	$0.3*V_{DD}$to $0.7*V_{DD}$		V

AC Measurement I/O Waveform



Input Parameters for the TS3001GB2A0

Symbol	Parameter[1,2]	Test Condition	Min.	Max.	Units
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input rise and fall times			6	ns
Z_{EIL}	Ei (SA0,SA1) input impedance	V_{IN}< 0.3* V_{DD}	30		kΩ
Z_{EIH}	Ei (SA0,SA1) input impedance	V_{IN}> 0.7* V_{DD}	800		kΩ
t_{SP}	Pulse width ignored (input filter on SCL and SDA)	Single glitch, f ≤ 100 KHz		100	ns
		Single glitch, f> 100 KHz		50	

1.T_A=25°C, f=400 kHz

2.Verified by design and characterization not necessarily tested on all devices

DC Characteristics

Parameter	Symbol	Conditions	Min.	Max.	Units
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ or V_{DD}		±1	µA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ or V_{DD}, SDA in Hi-Z		±1	µA
Supply Current, temp sensor active	I_{DD}	V_{DDSPD} = 3.3 V, f_C = 100 kHz (rise/fall time < 30 ns)		500	µA
Standby Supply Current	I_{DD1}	$V_{IN} = V_{SS}$ or V_{DD}, VDD= 3.465 V		40	µA
Input Low Voltage (SCL, SDA)	V_{IL}		-0.5	$0.3*V_{DD}$	V
Input High Voltage (SCL, SDA)	V_{IH}		$0.7* V_{DD}$	V_{DD} +1	V
SA0 High Voltage	V_{HV}	$V_{HV} - V_{DD} \geq 4.8$ V	7	10	V
Output Low Voltage (SDA,EVENT,NRST)	V_{OL}	I_{OL} = 2.1 mA, 3.135 V =≤ V_{DD} =≤ 3.465 V		0.4	V
		I_{OL} = 0.7 mA, V_{DD} = 3.135- 3.465 V		0.2	V
Input hysteresis	V_{HYST}		$0.05*V_{DD}$	—	V

AC Characteristics

Parameter[3,6]	Symbol	Min.	Max.	Units
Clock Frequency	f_{SCL}	10	400	kHz
Clock Pulse Width High Time	t_{HIGH}	600		ns
Clock Pulse Width Low Time	t_{LOW}[4]	1300		ns
Detect clock low timeout, Capabilities Register bit 6 =1	$t_{TIMEOUT}$[5]	25	35	ms
SDA Rise Time	t_R[2]	20	300	ns
SDA Fall Time	t_F[2]	20	300	ns
Data In Setup Time	$t_{SU:DAT}$	100		ns
Data In Hold Time	$t_{HD:DI}$	0		ns
Data Out Hold Time	$t_{HD:DAT}$	200	900	ns
Start Condition Setup Time	$t_{SU:STA}$[1]	600		ns
Start Condition Hold Time	$t_{HD:STA}$	600		ns
Stop Condition Setup Time	$t_{SU:STO}$	600		ns
Time Between Stop Condition and Next Start Condition	t_{BUF}	1300		ns
NRST reset (active low) Pulse Duration		160	200	ms

1. For a RESTART condition, or following a write cycle.
2. Guaranteed by design and characterization, not necessarily tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between falling edge of SCL and the falling or rising edge of SDA.
4. The TS3001GB2A0 does not initiate clock stretching which is an optional I^2C bus feature
5. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller and embedded controller and most devices that can master the SMBus. Some devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds SCL low for $t_{TIMEOUT,MAX}$ or longer.
6. The temperature sensor family of devices are not required to support the SMBus ALERT function.

Temperature-to-Digital Conversion Performance

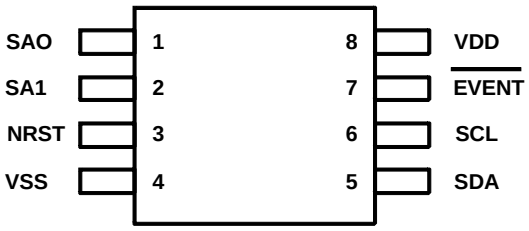
Parameter	Typ	Max	Unit	Test Conditions[1]
Temperature Sensor Accuracy	±0.5	±1.0	°C	$75°C \leq T_A \leq 95°C$
	±1.0	±2.0	°C	$40°C \leq T_A \leq 125°C$
	±2.0	±3.0	°C	$-20°C \leq T_A \leq 125°C$

1. $V_{DDSPDMIN} \leq V_{DDSPD} \leq V_{DDSPDMAX}$

Temperature Conversion Time

Resolution	ADC Setting	t_{CONV} (typ)	t_{CONV} (Max)	Unit
0.5°C	9 bit		100	ms
0.25°C (POR default)	10 bit		100	ms
0.125°C	11 bit		100	ms
0.0625°C	12 bit		100	ms

Pin Assignment



Pin Description

Pin #	Pin Name	Definition
1	SA0	Select Address 0
2	SA1	Select Address 1
3	NRST	Reset (active low)
4	V_{SS}	Ground
5	SDA	Serial Data In
6	SCL	Serial Clock In
7	$\overline{EVENT}$	Temperature Event Out
8	V_{DD}	Supply Voltage

Pin Functional Descriptions

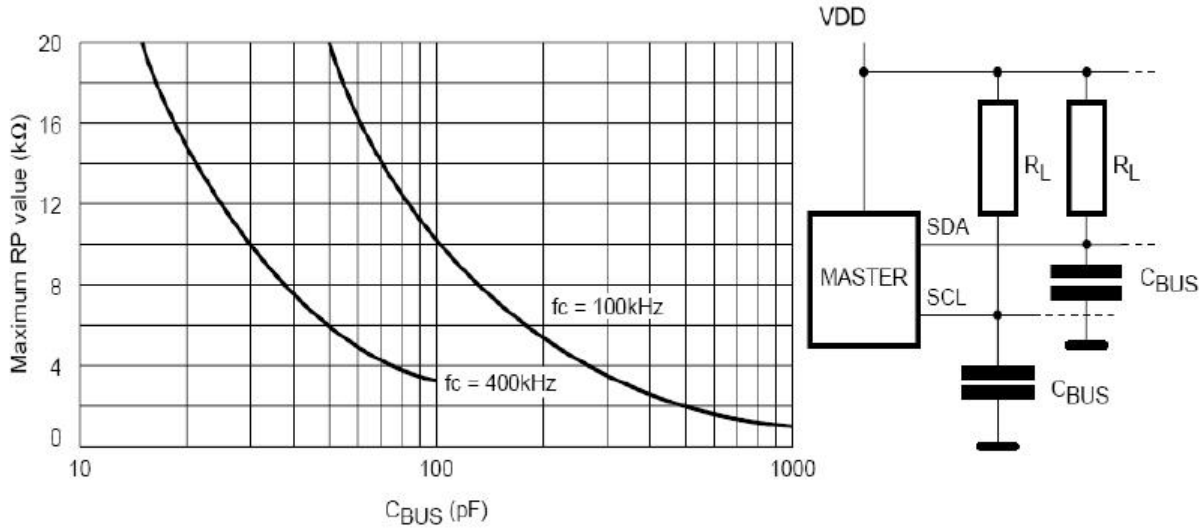
Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{DD}. (refer to the Maximum R_L Value vs. Bus Capacitance figure on how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive V_{DD} in the I^2C chain. (refer to the Maximum R_L Value vs. Bus Capacitance figure on how the value of the pull-up resistor can be calculated).

Maximum R_L Value vs. Bus Capacitance (C_{BUS}) for an I^2C Bus



Select Address (SA0, SA1)

These input signals are used to set the value that is to be looked for on two bits (b2, b1) of the 7-bit Slave Address. In the end application, SA0, SA1 and SA1 must be directly (not through a pull-up or pull-down resistor) connected to V_{DD} or V_{SS} to establish the Slave Address. When these inputs are not connected, an internal pull-down circuitry makes (SA0, SA1) = (0, 0).

NRST

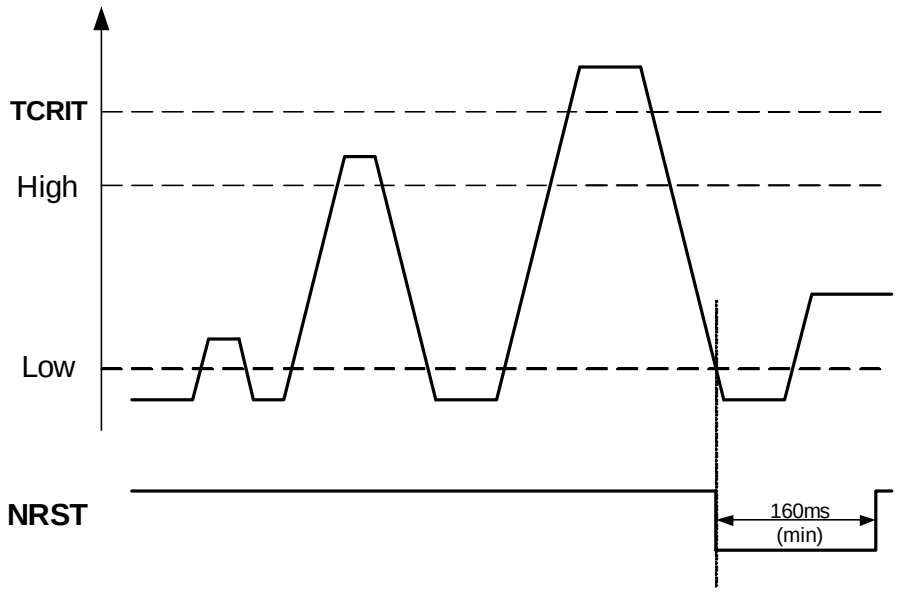
NRST pin is an open drain output without internal pull-up resistor that requires a pull-up to VDD on the system motherboard or integrated into the master controller. It generates and sends out a reset pulse for a minimum of 160ms. The reset pulse is generated only when the temperature first exceeds TCRIT temp limit and then goes down below low temp limit. (TCRIT Limit -> Low Limit -> Reset Pulse). NRST pin polarity is active low. Similarly, if the temperature is above TCRIT limit at power-up, NRST gets generated as soon as the temperature drops below low temp limit.

NRST pin functionality is independent of mode of operation (TCRIT, Interrupt, Comparator).

The default state of NRST is Hi-z at power-on.

NRST function is enabled via configuration register bit NRST_EN. The status bit NRST_ASSERTED indicates whether NRST event took place. This status bit can be cleared via I2C interface with NRST_CLR bit and it needs to be cleared during device initialization. If NRST function gets disabled via NRST_EN=0 setting, NRST_ASSERTED bit stays unchanged at its last value when NRST_EN was still set to 1.

NRST Functionality



$\overline{\text{EVENT}}$

The TS3001GB2A0 $\overline{\text{EVENT}}$ pin is an open drain output that requires a pull-up to V_{DD} on the system motherboard or integrated into the master controller. The TS3001GB2A0 $\overline{\text{EVENT}}$ pin has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt, Comparator, or TCRIT Only.

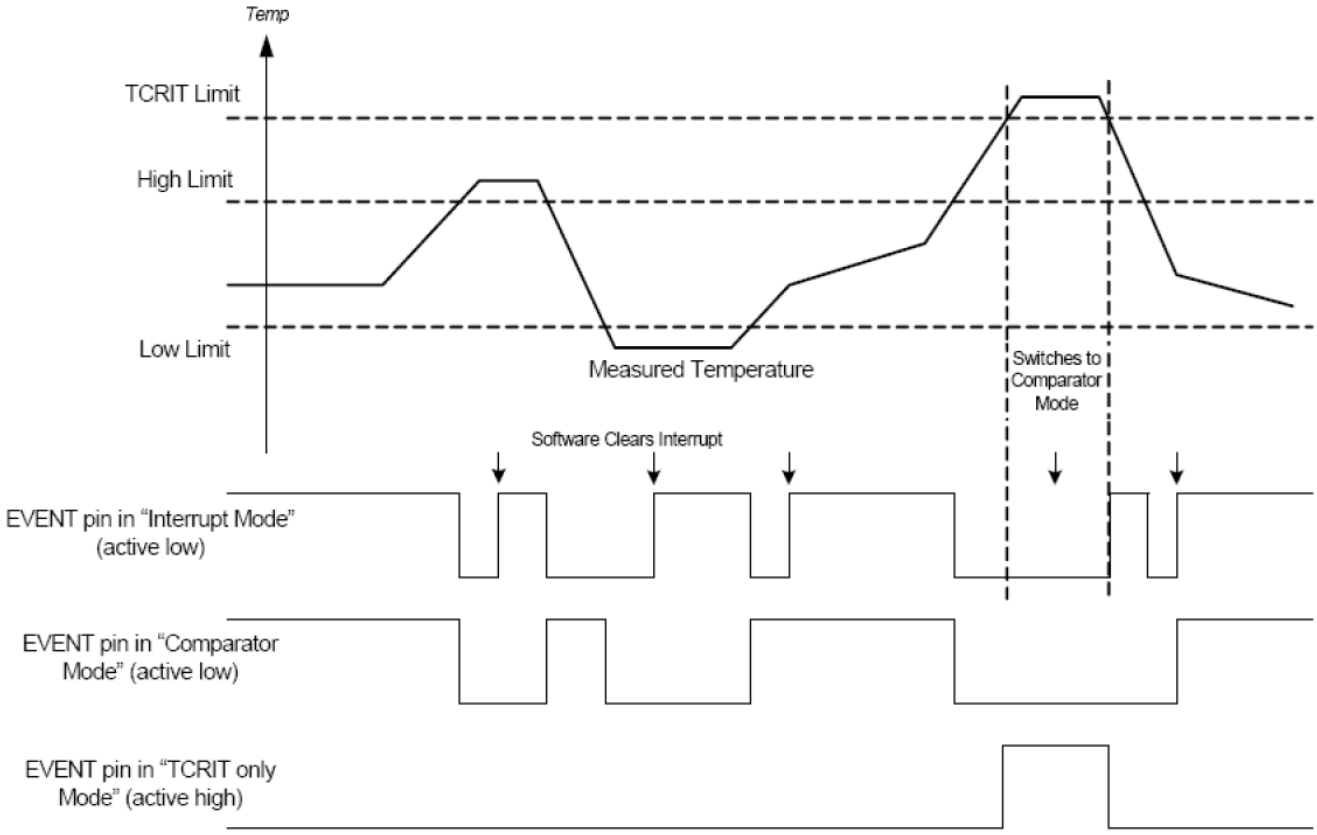
In Interrupt Mode the $\overline{\text{EVENT}}$ pin will remain asserted until it is released by writing a '1' to the “Clear Event” bit in the Status Register. The value to write is independent of the $\overline{\text{EVENT}}$ polarity bit.

In Comparator Mode the $\overline{\text{EVENT}}$ pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

Finally, in the TCRIT Only Mode the $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis. The next figure illustrates the operation of the different modes over time and temperature.

Systems that use the active high mode for $\overline{\text{EVENT}}$ must be wired point to point between the TS3001GB2A0 and the sensing controller. Wire-OR configurations should not be used with active high $\overline{\text{EVENT}}$ since any device pulling the $\overline{\text{EVENT}}$ signal low will mask the other devices on the bus. Also note that the normal state of $\overline{\text{EVENT}}$ in active high mode is a 0 which will continually draw power through the pull-up resistor.

EVENT Pin Mode Functionality

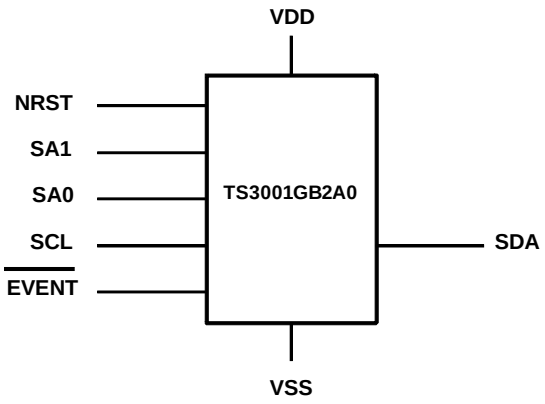


Serial Communications

The TS3001GB2A0 temperature sensor circuitry continuously monitors the temperature and updates the temperature data minimum of eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

Internal registers are used to configure both the TS performance and response to over-temperature conditions. The device contains programmable high, low, and critical temperature limits. Finally, the device $\overline{\text{EVENT}}$ pin can be configured as active high or active low and can be configured to operate as an interrupt or as a comparator output.

Device Diagram



SMBus/I^{2}C Communications

The data registers in this device are selected by the Pointer Register. At power-up the Pointer Register is set to “00”, the location for the Capability Register. The Pointer Register latches the last location it was set to. Each data register falls into one of three types of user accessibility:

1. Read only
2. Write only
3. Write/Read same address

A Write to this device will always include the address byte and the pointer byte. A write to any register, other than the pointer register, requires two data bytes.

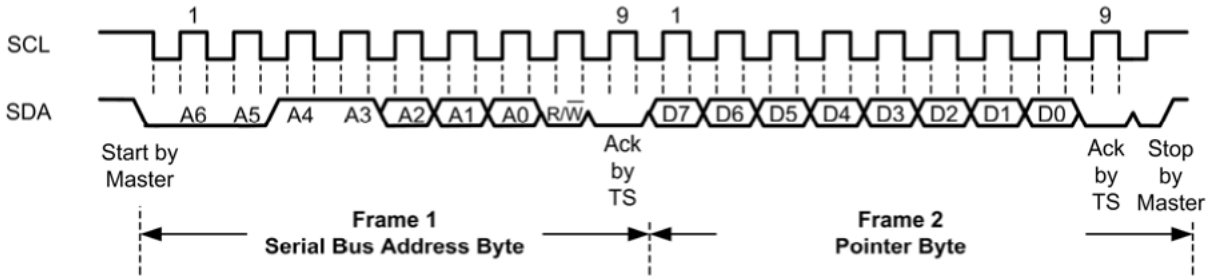
Reading this device can take place either of two ways:

If the location latched in the Pointer Register is correct (most of the time it is expected that the Pointer Register will point to one of the Read Temperature Registers because that will be the data most frequently read), then the read can simply consist of an address byte, followed by retrieving the two data bytes.

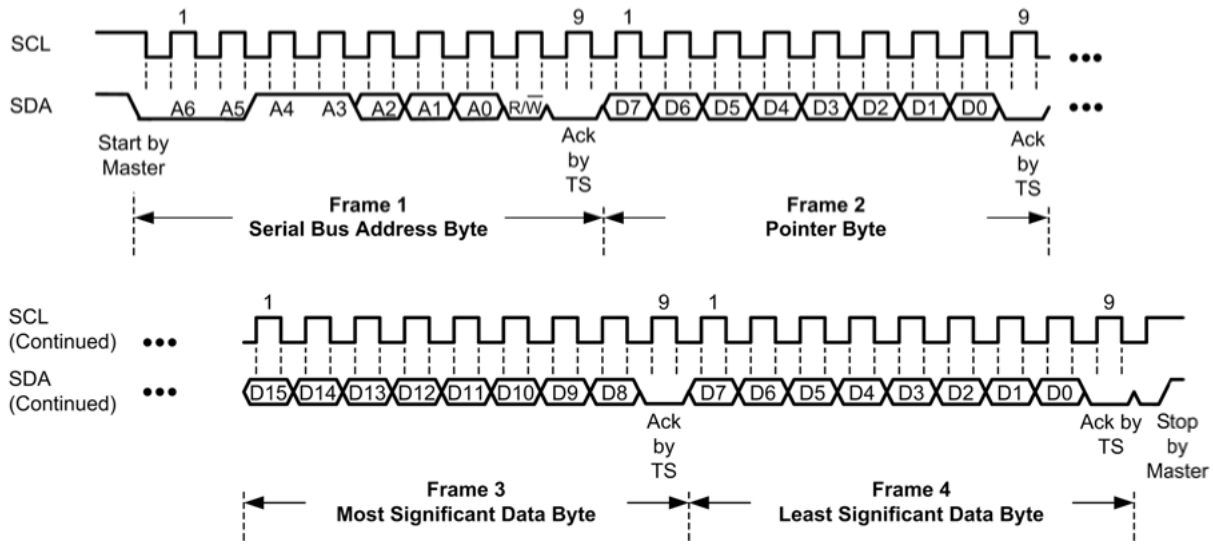
If the Pointer Register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (Ack) or No Acknowledge (No Ack) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

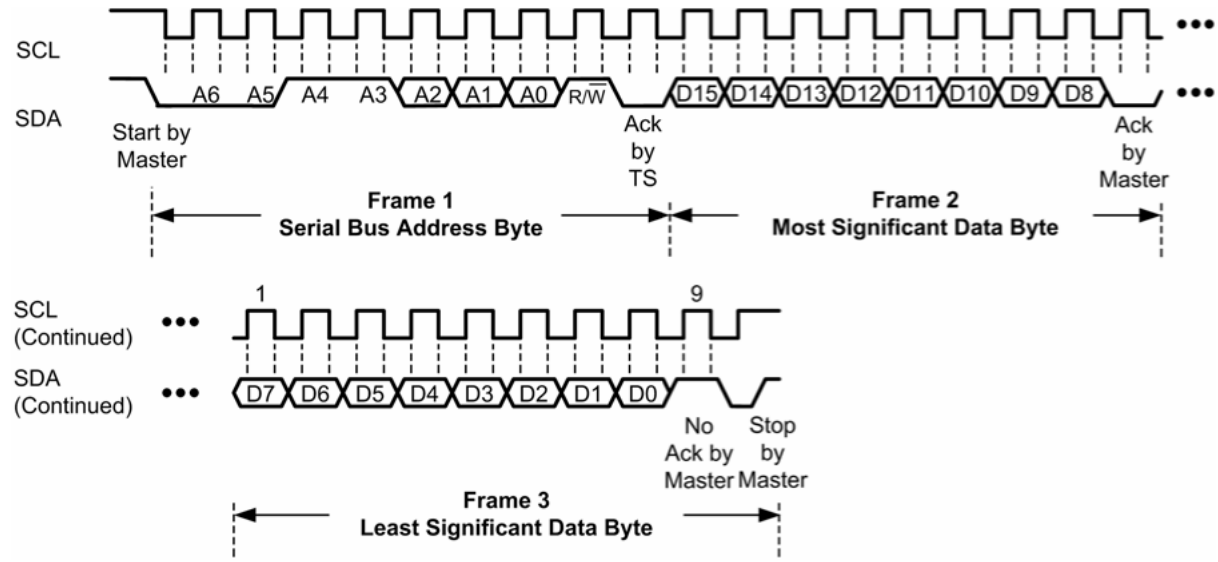
SMBus/I²C write to the pointer register



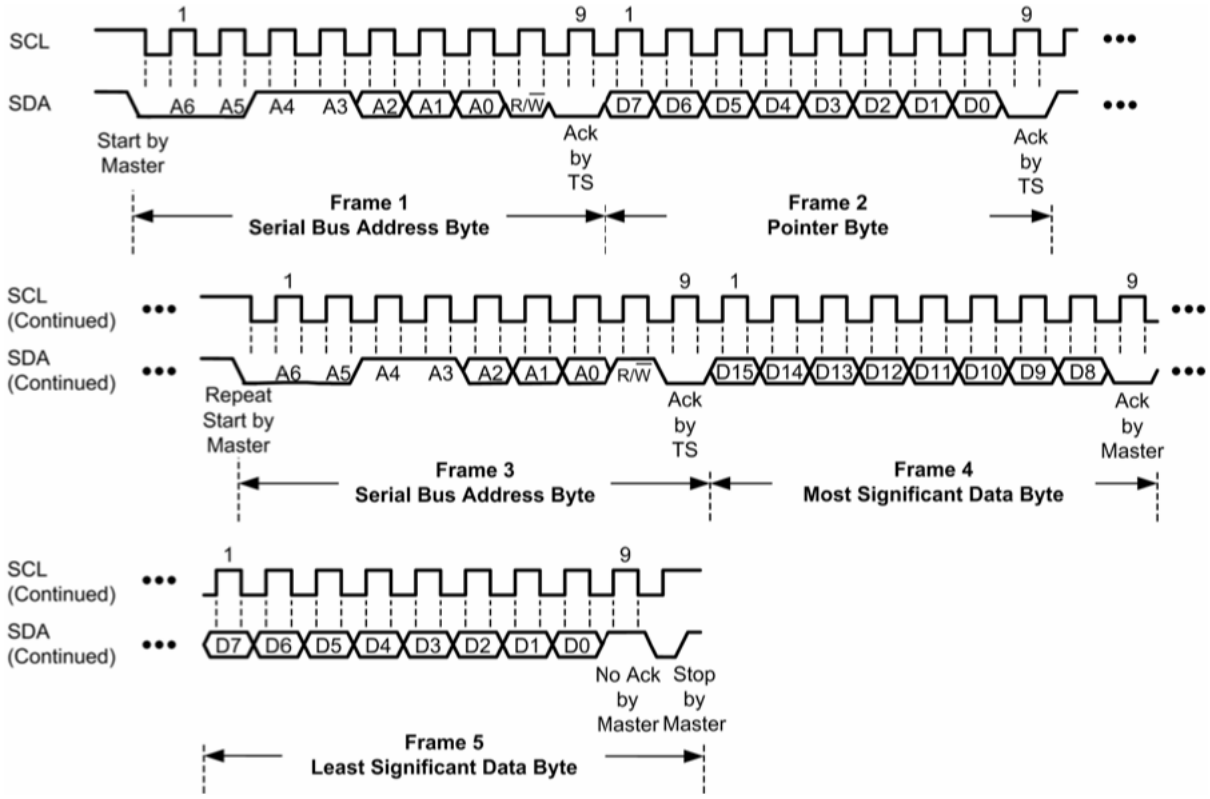
SMBus/I²C write to the pointer register followed by a write data word



SMBus/I²C word read from register with a preset pointer



SMBus/I²C write to pointer register followed by a repeat start and an immediate data word read



SMBus/I²C Slave Sub-Address Decoding

The physical address for TS is different than that used by current SPD devices. The physical address for thermal sensor is “0 0 1 1 A2 A1 A0 RW” in binary, where A1, A0 are two slave sub-address pins, and the least significant bit “RW” is the Read/Write flag.

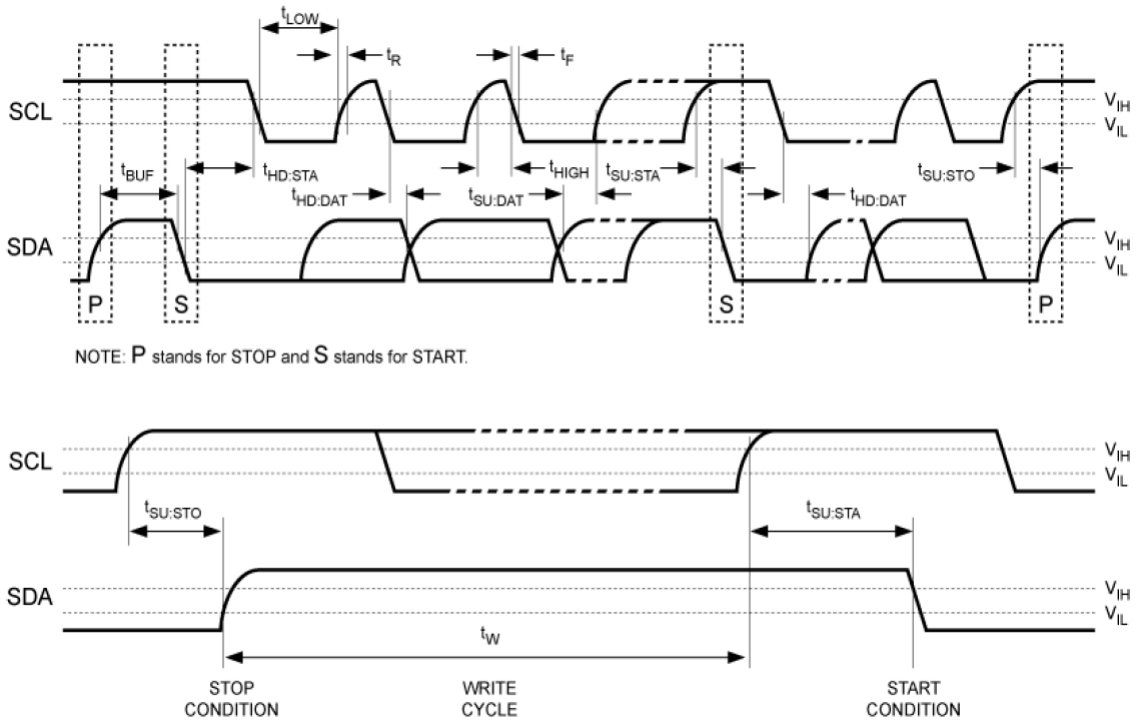
Slave Address Decoding

Slave Address	A2	A1	A0
x0	0	0	0
x2	0	0	1
x4	0	1	0
x6	0	1	1

The meaning of the A0/A1pin states is as follows:; 0= Pull-down to Thermal Sensor Vss, 1=Pull-up to Thermal Sensor VDD.

SMBus/I2 AC Timing Consideration

In order for this device to be both SMBus and I^2C compliant, the device complies with a subset of each specification. This requires a few minor considerations to ensure interoperability. The time out requirements of SMBus are optional for this device. The minimum clock frequency of SMBus is a required feature. Note that the minimum data hold time (THD:DAT) of 200 ns is smaller than the 300 ns of the SMBus specification. With these minor considerations, this device is capable of co-existing with devices on either an SMBus or an I^2C bus.



TS Register Set Definition

The register set address are shown in the Acknowledge When Writing Data or Defining Write Protection table. These values are used in the I^2C operations as the “REG_PTR” as shown in previous figures.

Temperature Register Addresses

ADDR	R/W	Name	Function	Default
N/A	W	Address Pointer	Address storage for subsequent operations	00
00	R	Capabilities	Indicates the functions and capabilities of the temperature sensor	006F
01	R/W	Configuration	Controls the operation of the temperature monitor	0001
02	R/W	High Limit	Temperature High Limit	0000
03	R/W	Low Limit	Temperature Low Limit	0000
04	R/W	TCRIT Limit	Critical Temperature	0000
05	R	Ambient Temperature	Current Ambient temperature	N/A
06	R	Manufacturer ID	PCI-SIG manufacturer ID	00B3
07	R	Device/Revision	Device ID and Revision number	3001
08	R/W	Resolution Register	Allows changing temperature sensor resolution	0008

Capabilities Register

The Capabilities Register indicates the supported features of the temperature sensor.

Capabilities Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
00	R	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	006F
		EVSD	TMOUT	X	TRES[1:0]		RANGE	ACC	$\overline{\text{EVENT}}$	

Bits 15 - Bit 8 – RFU; Reserved for future use. These bits will always read '0' and writing to them will have no affect.

Bit 7- EVSD-EVENT with Shutdown action.

‘0’ - (default) The $\overline{\text{EVENT}}$ output freezes in its current state when entering shutdown. Upon exiting shutdown, the $\overline{\text{EVENT}}$ output remains in the previous state until the next thermal sample is taken, or possibly sooner if $\overline{\text{EVENT}}$ is programmed for comparator mode.

‘1’ The $\overline{\text{EVENT}}$ output is deasserted (not driven) when entering shutdown and remains deasserted upon exit from shutdown until the next thermal sample is taken, or possibly sooner if $\overline{\text{EVENT}}$ is programmed for comparator mode.

Bit 6 - TMOUT – Bus timeout period for thermal sensor access during normal operation. Note that the TS3001GB2A0 supports timeout in both active and shutdown mode.

‘0’ - Parameter $t_{TIMEOUT}$ is supported within the range of 10 to 60 ms.

‘1’ - (default) Parameter $t_{TIMEOUT}$ is supported within the range of 25 to 35 ms (SMBus compatible).

Bit 5 - X – May be 0 or 1; applications must accept either code. (Default =1)

Bits 4 - 3 – TRES[1:0]; Indicates the resolution of the temperature monitor as shown in the TRES Bit Decode table. (Default =01)

TRES Bit Decode

TRES[1:0]		Temperature Resolution
1	0	
0	0	0.5°C (9-bit)
0	1	0.25°C (10-bit) (default)
1	0	0.125°C (11-bit)
1	1	0.0625°C (12-bit)

Note: Refer to section Resolution Register on page 22.

Bit 2 - RANGE; Indicates the supported temperature range.

'0' - The temperature monitor clamps values lower than 0 °C.

'1' (default) - The temperature monitor can read temperatures below 0 °C and sets the sign bit appropriately.

Bit 1 - ACC; Indicates the supported temperature accuracy.

'0' - The temperature monitor has ±2 °C accuracy of the active range (75 °C to 95 °C) and 3 °C accuracy over the entire operating range.

'1' (default) - Bgrade. The temperature monitor has ±1 ℃ accuracy

Bit 0 - $\overline{\text{EVENT}}$; Indicates whether the temperature monitor supports interrupt capabilities

'0'.-The device does not support interrupt capabilities.

'1' (default); The device supports interrupt capabilities.

Configuration Register

Configuration Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
01	R/W	RFU	RFU	NRST_ CLEAR	NRST_ ASSERTED	NRST_EN	HYST[1:0]		SHDN	0001
		TCRIT_ LOCK	EVENT_ LOCK	CLEAR	EVENT_ STS	EVENT_ CTRL	TCRIT_ ONLY	EVENT_ POL	EVENT_ MODE	

The Configuration Register holds the control and status bits of the EVENT pin as well as general hysteresis on all limits.

Bits 15 - 11 – RFU; Reserved for future use. These bits will always read '0' and writing to them will have no affect. For future compatibility, all RFU bits must be programmed as '0'.

Bit 13 - NRST_CLEAR: Clear the NRST_ASSERTED register bit. This bit is write only and will always read '0'

'0': Does nothing

'1': Clear the NRST_ASSERTED bit. This bit is self clearing

Bit 12 - NRST_ASSERTED: status bit indicating if NRST reset pulse took place. This bit gets asserted as soon as NRST pin transitions low. This status bit can be cleared via I2C interface and it needs to be cleared during device initialization. Default=0

'0': NRST has not yet been asserted (Default)

'1': NRST was asserted. When 1 is written by software through I2C to bit 13, NRST_ASSERTED gets cleared

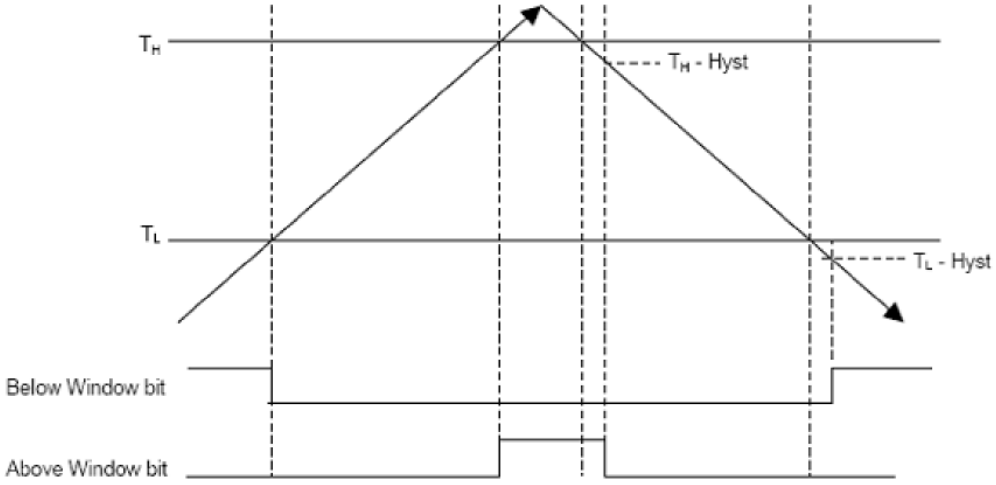
Bit 11 - NRST_EN: enables NRST function when set to 1 (default = 0)

'0': Disable NRST feature. Do not generate the reset pulse. Output state is Hi-z. (Default)

'1': Enable NRST feature.

Bits 10 - 9 – HYST[1:0]; Control the hysteresis that is applied to all limits as shown in the HYST Bit Decode table that follows. This hysteresis applies to all limits when the temperature is dropping below the threshold so that once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. Note that hysteresis is also applied to $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits is set, these bits cannot be altered. For NRST operation described in NRST pin description section, HYST[1:0] bits have to be kept at default (no hysteresis).

Hysteresis



	Below Alarm Window Bit		Above Alarm Window Bit	
	Temperature slope	Threshold Temperature	Temperature Slope	Temperature
Sets	Falling	T_L -Hyst	Rising	T_H
Clears	Rising	T_L	Falling	T_H -Hyst

T_U= Value stored in Alarm Temperature Upper Boundary Trip Register

T_L=Value stored in Alarm Temperature Lower Boundary Trip Register

Hyst= Absolute value of selected hysteresis

HYST Bit Decode

HYST[1:0]		Hysteresis
1	0	
0	0	Disable hysteresis (default)
0	1	1.5°C
1	0	3°C
1	1	6°C

Bit 8 – SHDN-Shutdown. The thermal sensing device and A/D converters are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However it can be cleared at any time. When in shutdown mode, the TS3001GB2A0 still responds to commands normally, however bus timeout may or may not be supported in this mode.

'0' (default); The temperature monitor is active and converting

'1'; The temperature monitor is disabled and will not generate interrupts or update the temperature data.

Bit 7 – TCRIT_LOCK; Locks the TCRIT Limit Register from being updated.

'0' (default; The TCRIT Limit Register can be updated normally.

'1'; The TCRIT Limit Register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit 6 – EVENT_LOCK; Locks the High and Low Limit Registers from being updated.

'0' (default); The High and Low Limit Registers can be updated normally.

'1'; The High and Low Limit Registers are locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit 5 – CLEAR; Clears the EVENT pin when it has been asserted. This bit is write only and will always read '0'.

'0'; does nothing

'1'; The $\overline{\text{EVENT}}$ pin is released and will not be asserted until a new interrupt condition occurs. This bit is ignored if the device is operating in Comparator Mode. This bit is self clearing.

Bit 4 – EVENT_STS; Indicates if the $\overline{\text{EVENT}}$ pin is asserted. This bit is read only.

‘0' (default); The EVENT pin is not asserted.

'1'; The $\overline{\text{EVENT}}$ pin is being asserted by the device.

Bit 3 – EVENT_CTRL; Masks the $\overline{\text{EVENT}}$ pin from generating an interrupt. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

'0' (default); The $\overline{\text{EVENT}}$ pin is disabled and will not generate interrupts.

'1'; The $\overline{\text{EVENT}}$ pin is enabled.

Bit 2 – TCRIT_ONLY; Controls whether the $\overline{\text{EVENT}}$ pin will be asserted from a high / low out-of-limit condition. When the EVENT_LOCK bit is set, this bit cannot be altered.

'0' (default); The $\overline{\text{EVENT}}$ pin will be asserted if the measured temperature is above the High Limit or below the Low Limit in addition to if the temperature is above the TCRIT Limit.

'1'; The $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature is above the TCRIT Limit.

Bit 1 – EVENT_POL; Controls the “active” state of the $\overline{\text{EVENT}}$ pin. The $\overline{\text{EVENT}}$ pin is driven to this state when it is asserted.

'0' (default); The $\overline{\text{EVENT}}$ pin is active low. The “active” state of the pin will be logical '0'.

'1'; The $\overline{\text{EVENT}}$ pin is active high. The “active” state of the pin will be logical '1'.

Bit 0 – EVENT_MODE; Controls the behavior of the $\overline{\text{EVENT}}$ pin. The $\overline{\text{EVENT}}$ pin may function in either comparator or interrupt mode.

'0'; The $\overline{\text{EVENT}}$ pin will function in comparator mode.

'1' (default); The $\overline{\text{EVENT}}$ pin will function in interrupt mode.

Temperature Register Value Definitions

Temperatures in the High Limit Register, Low Limit Register, TCRIT Register, and Temperature Data Register are expressed in two's complement format. Bits B 12 through B2 for each of these registers are defined for all device resolutions as defined in the TRES field of the Capabilities Register, hence a 0.25°C minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits:

Temperature Register Coding Examples		
B15~B0 (binary)	**Value**	**Units**
xxx0 0000 0010 11xx	+2.75	°C
xxx0 0000 0001 00xx	+1.00	°C
xxx0 0000 0000 01xx	+0.25	°C
xxx0 0000 0000 00xx	0	°C
xxx1 1111 1111 11xx	-0.25	°C
xxx1 1111 1111 00xx	-1.00	°C
xxx1 1111 1101 01xx	-2.75	°C

The TRES field of the Capabilities Register optionally defines higher resolution devices. For compatibility and simplicity, this additional resolution affects only the Temperature Data Register but none of the Limit Registers. When higher resolution devices generate status or $\overline{\text{EVENT}}$ changes, only bits B12 through B2 are used in the comparison; however, all 11 bits (TRES[1-0] = 10) or all 12 bits (TRES[1-0] = 11) are visible in reads from the Temperature Data Register.

When a lower resolution device is indicated in the Capabilities Register (TRES[1-0] = 00), the finest resolution supported is 0.5°C. When this is detected, bit 2 of all Limit Registers should be programmed to 0 to assure correct operation of the temperature comparators.

High Limit Register

The temperature limit registers (High, Low, and TCRIT) define the temperatures to be used by various on-chip comparators to determine device temperature status and thermal EVENTs. For future compatibility, unused bits "-" must be programmed as 0.

High Limit Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
02	R/W	–	–	–	Sign	128	64	32	16	0000
		8	4	2	1	0.5	0.25	–	–	

The High Limit Register holds the High Limit for the nominal operating window. When the temperature rises above the High Limit, or drops below or equal to the High Limit, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). If the EVENT_LOCK bit is set as shown in the Configuration Register table), then this register becomes read-only.

Low Limit Register

Low Limit Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
03	R/W	–	–	–	Sign	128	64	32	16	0000
		8	4	2	1	0.5	0.25	–	–	

The Low Limit Register holds the lower limit for the nominal operating window. When the temperature drops below the Low Limit or rises up to meet or exceed the Low Limit, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). If the EVENT_LOCK bit is set as shown in the Configuration Register, then this register becomes read-only.

TCRIT Limit Register

TCRIT Limit Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
04	R/W	–	–	–	Sign	128	64	32	16	0000
		8	4	2	1	0.5	0.25	–	–	

The TCRIT Limit Register holds the TCRIT Limit. If the temperature exceeds the limit, the $\overline{\text{EVENT}}$ pin will be asserted. It will remain asserted until the temperature drops below or equal to the limit minus hysteresis. If the TCRIT_LOCK bit is set as shown in the Configuration Register table, then this register becomes read-only.

Temperature Data Register

Temperature Data Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
05	R	TCRIT	HIGH	LOW	Sign	128	64	32	16	N/A (0000)
		8	4	2	1	0.5	0.25*	0.125*	0.0625*	

* Resolution defined based on value of TRES field of the Capabilities Register. Unused/unsupported bits will read as 0.

The Temperature Data Register holds the 10-bit + sign data for the internal temperature measurement as well as the status bits indicating which error conditions, if any, are active. The encoding of bits B 12 through B0 is the same as for the temperature limit registers.

Bit 15 – TCRIT; When set, the temperature is above the TCRIT Limit. This bit will remain set so long as the temperature is above TCRIT and will automatically clear once the temperature has dropped below the limit minus the hysteresis.

Bit 14 – HIGH; When set, the temperature is above the High Limit. This bit will remain set so long as the temperature is above the HIGH limit. Once set, it will only be cleared when the temperature drops below or equal to the HIGH Limit minus the hysteresis.

Bit 13 – LOW; When set, the temperature is below the Low Limit. This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis. Once set, it will only be cleared when the temperature meets or exceeds the Low Limit.

Manufacturer ID Register

Manufacturer ID Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
06	R/W	0	0	0	0	0	0	0	0	00B3
		1	0	1	1	0	0	1	1	

The Manufacturer ID Register holds the PCI SIG number assigned to the specific manufacturer.

Device ID/Revision Register

Device ID/Revision Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
07	R/W	0	0	1	1	0	0	0	0	3001
		0	0	0	0	0	0	0	1	

The upper byte of the Device ID / Revision Register stores a unique number indicating the TS3001GB2A0 from other devices. The lower byte holds the revision value.

Resolution Register

This register allows the user to change the resolution of the temperature sensor. The POR default resolution is 0.25°C. The resolution implemented via this register is also reflected in the capability register.

Resolution Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
08h	R/W	0	0	0	0	0	0	0	0	0008
		0	0	0	TRES[1]	TRES[0]	0	0	0	

Legend:

Resolution bits 4-3 TRES[4:3]

00 = LSB = 0.5℃ (register value = 0007)

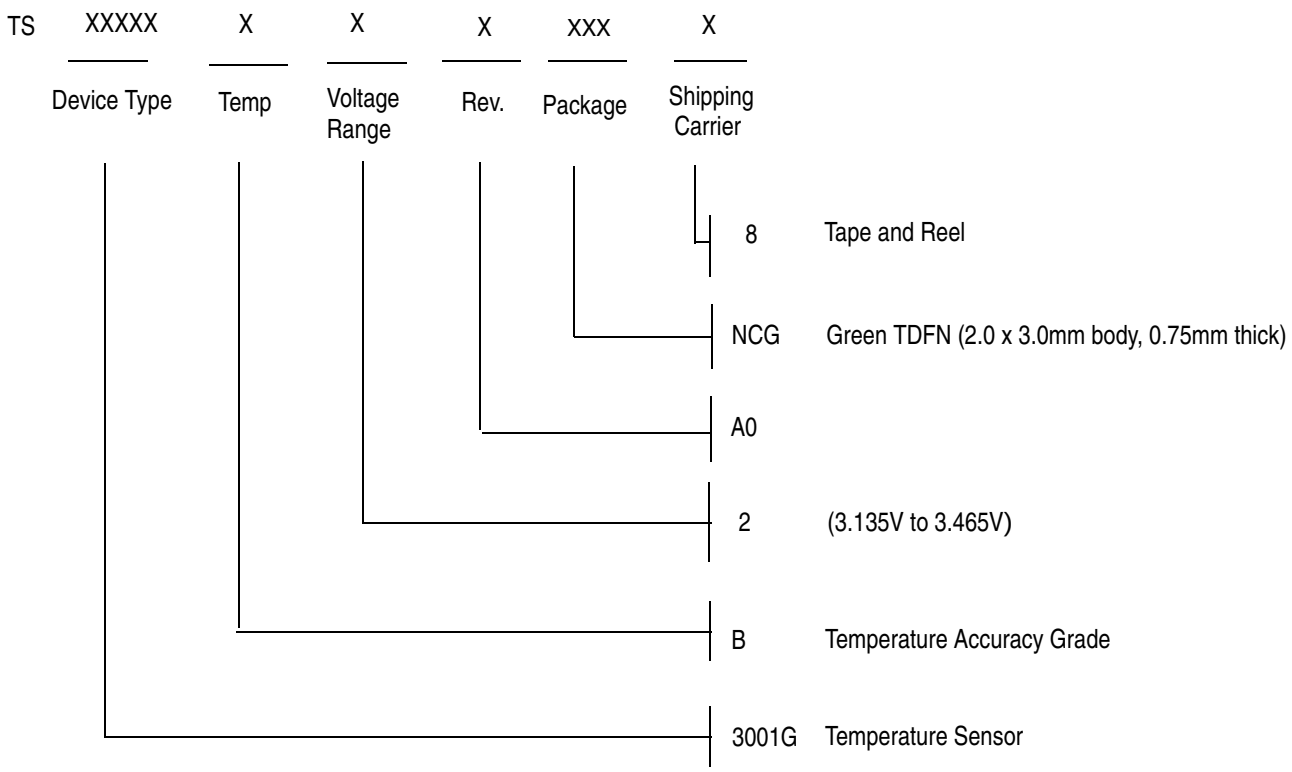
01 = LSB = 0.25℃ (register value = 000F)

10 = LSB = 0.125℃ (register value = 0017)

11 = LSB = 0.0625℃ (register value = 001F)

Conversion times for each resolution are less than 100ms (worst case).

Ordering Information



Example: TS3001GB2A0 NCG8

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