AvnetCore: Datasheet

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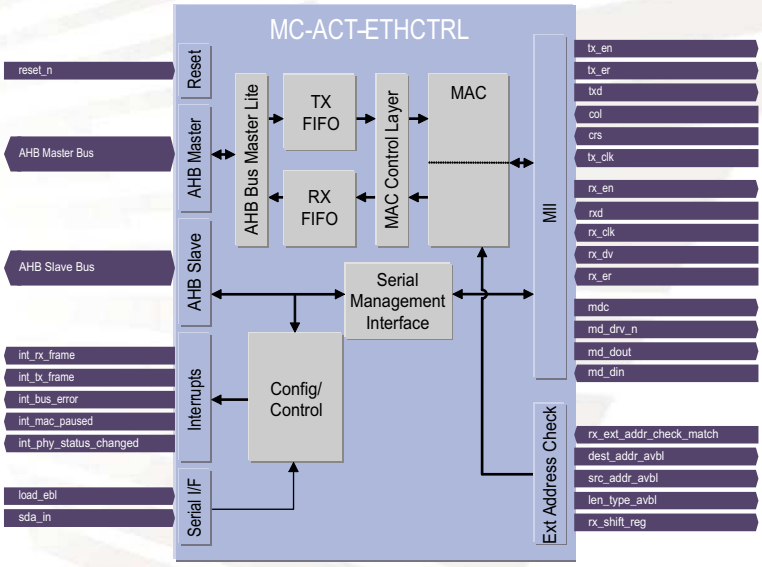
G704-E1 Framer



Block Diagram

The MC-ACT-G704E1 Framer core is designed to handle synchronous frame structures (Recommendation G.704) running on an E1 carrier. Transmitter and receiver part are two completely independent blocks both capable of handling basic and multi frames. Both perform functions such as overhead bit insertion / detection, CRC4 computation and check. A very flexible synchronization unit (Recommendation G.706) synchronizes automatically or by means of an external frame sync signal. The frame builder unit can be configured which of the overhead bits are to be inserted or not.

Avnet Memec cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. Avnet Memec cores contain resources present in only the sequential and combinatorial array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, run through a global buffer, and then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core in order to complete it.

Intended Use:

- ISDN Terminal Equipment
- E2 Interface (multi G704 on chip)
- E1-ATM Interface

Features:

- G704 framing de-framing on E1 carriers
- Basic & multi frame alignment
- Alarm bit processing
- Customizable error counters
- Selectable conditions for loss of sync
- CRC4 error checking and monitoring
- Fully synchronous

Targeted Devices:

- SX-A Family
- Axcelerator® Family
- ProASIC PLUS® Family

Core Deliverables:

- Netlist Version
  - > Netlist compatible with the Actel Designer place and route tool
- RTL Version
  - > VHDL Source Code
  - > Test Bench
- All
  - > User Guide

Synthesis and Simulation Support:

- Synthesis: Synplicity®
- Simulation: ModelSim®
- Other tools supported upon request

Verification:

- Test Bench

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Functional Description

TRANSMITTER
The transmitter part consists of the multi frame overhead handler and the frame builder itself.

Multi Frame Overhead Handler
This block is responsible for providing the overhead bits according to the current frame type. These bits are then forwarded to the frame builder unit that inserts them into the outgoing data stream.

Frame Builder
The frame builder performs all the tasks necessary to output a valid frame that complies with the E1 carrier system.

Basic Frame Synchronizer Generator
This block synchronizes the incoming data and provides a basic frame reference signal that identifies every bit within a basic frame.

Multi Frame Generator
The multi frame generator builds a multi frame reference signal based on the basic frame reference and provides the associated interrupts.

TS0 Bit Insertion
This unit automatically inserts all the special bits on the fly into time slot 0. It uses the frame reference signal to insert the corresponding bits. It inserts the basic frame alignment, the CRC4 multi frame alignment signal, the computed CRC4 value plus the configured special bits.

CRC4 Calculation
This block computes the CRC4 value on the outgoing data stream and feeds it back to the TS0 bit insertion block.

RECEIVER
The receiver part comprises the synchronizer block and the analyzer block.

Snychronizer
The synchronizer samples the incoming data frame and generates the corresponding frame reference signal and the necessary interrupts.

Basic Frame Aligner
This block synchronizes the incoming data and provides a basic frame reference signal that identifies every bit within a basic frame.

Multi Frame Aligner
The multi frame aligner detects multi frame structures and builds a multi frame reference signal based on the basic frame reference and provides the associated interrupts.

CRC4 Checker
This unit computes the CRC4 on the incoming frame and compares it with the received CRC bits and provides the corresponding status signals.

Analyzer
This unit uses the frame reference signal to analyze the incoming frame.

Alarm Detector
This unit samples the alarm bits of the incoming frame. It registers them and outputs an alarm history. Plus it marks the reception of the alarm indication signal.

Monitor Counter
The monitor counter holds error counters that keep track on the CRC4, FAS and E-bit errors that have been detected on the incoming frames.

TS0 Signal Capture
This block samples the bits in time slot 0 and stores them into a register bank for further processing. The register bank can hold the TS0 bits of 8 consecutive frames within a multi frame structure.

AISLOS Detector
This unit detects the alarm indication signal (AIS) and the 2Mbit loss condition.

Family	Device	Utilization			Performance
		COMB	SEQ	Total	
SX-A	SX32A-3	760 (42%)	510 (48%)	1270 (44%)	77 MHz
ProASIC^{PLUS}	APA150-STD	n/a	n/a	2212 (36%)	42 MHz
Axcelerator	AX500-3	695 (13%)	507 (19%)	1202 (15%)	79 MHz

Verification and Compliance

Complete functional and timing simulation has been performed on the G704-E1 Framer using ModelSim 5.5d. This core has also been used successfully in customer designs.

Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Direction	Description
ClkSys	Input	System clock: This is the only clock source for the whole G704-E1 core
resn	Input	Asynchronous System Reset: active low
CfgFSync.SyncMode[1:0]	Input	Configuration of Frame Synchronizer: “00”: transparent (no FSync generated) “01”: free run (generate dummy FSync) “10”: use external FSync “11”: fully automatic sync (G.706)
CfgFSync.ForceResync	Input	User controlled resync: When toggled form ‘0’ to ‘1’, a resync is initialized
CfgFSync.AutoResync	Input	Automatic resync after loss of sync: ‘1’: Automatic resync ON (‘0’: OFF)
CfgFSync.FAImprove_411	Input	‘0’: Improved BasicFrame alignment disabled ‘1’: Use improved BasicFrame alignment procedure as in $4.1.1 of G.704/Note 1 (check FA bit 2 of nFAS frames)
CfgFSync.MF_Mode		‘0’: MultiFrame alignment search disabled (only Basic-Frame search) ‘1’: MultiFrame alignment search enabled
CfgFSync.MF_SyncMode	Input	‘0’: use parallel BFA search (G.706) ‘1’: reuse primary BFA search (PTT simplified search path)
CfgFSync.MFA_Check	Input	‘0’: MultiFrame alignment loss checking process disabled ‘1’: MultiFrame alignment checking process enabled (if 3 consecutive MFA not found while MFSyncState = InSync, then MFSyncState <= Hunt)
CfgFSync.CRC4_Mode	Input	‘0’: CRC4 Error limit of <= 915 disabled ‘1’: CRC4 Error limit checking enabled
CfgFan.CRC_CountEbl	Input	‘0’: CRC4 Error counter enabled ‘1’: CRC4 Error counter disabled
CfgFan.FAS_Count_Ebl	Input	‘0’: FAS Error counter enabled ‘1’: FAS Error counter disabled
CfgFan.E_Count_Ebl	Input	‘0’: E-Bit counter enabled ‘1’: E-Bit counter disabled
CfgOverhead.Si_E1	Input	E1 / Si of FAS frame
CfgOverhead.Si_E2	Input	E2 / Si of non FAS frame
CfgOverhead.A-Bit	Input	A-Bit
CfgOverhead.InsertEbl[4:0]	Input	Insert enable pattern related to Sa bits
CfgOverhead.saBitsMF[1:8][4:0]	Input	Sa4...Sa8 bits Note: When FrameRef.MF.MFSyncState NOT = InSync, then only SaBitsMF(1) will be inserted.
CfgFBuild.CRC4_MFMode	Input	‘0’: CRC4 MultiFrame Mode disabled ‘1’: CRC4 MultiFrame Mode enabled
CfgFBuild.BuildMode[1:0]		“0x”: transparent, “10”: synchronize BFA phase, “11”: generate BFA phase (Note: when NOT transparent, a new MultiFrame is generated)
IntSrc_FSync.BFA.Sync	Output	Pulse @ ‘1’ when entering state InSync
IntSrc_FSync.BFA.SyncLoss	Output	Pulse @ ‘1’ when leaving state InSync
IntSrc_FSync.MFA.SyncEntry	Output	Pulse @ ‘1’ when entering state InSync
IntSrc_FSync.MFA.MFSync	Output	Pulse @ ‘1’ at begin of each MultiFrame

IntSrc_FSync.MFA.SyncLoss	Output	Pulse @ ‘1’ when leaving state InSync
IntSrc_Fan.AlarmByteCaptured	Output	Pulse @ ‘1’ when 8 A-bits have been captured (only when BFSyncState = InSync and MFSyncState /= InSync)
IntSrc_Fan.A_Bit_detected	Output	Pulse @ ‘1’ when A-Bit sequence “001” has been received
IntSrc_FSync.BFB.Sync	Output	Pulse @ ‘1’ when entering state InSync
IntSrc_FSync.BFB.SyncLoss	Output	Pulse @ ‘1’ when leaving state InSync
IntSrc_FSync.MFB.SyncEntry	Output	Pulse @ ‘1’ when entering state InSync
IntSrc_FSync.MFB.MFSync	Output	Pulse @ ‘1’ at begin of each MultiFrame
Status_FAn.LOS_2M	Output	2MBit Loss detection
Status_FAn.AIS	Output	AIS detection result
Status_FAn.TS0Data	Output	TS0 Data, OTHERS => ‘0’ when not InSync
Status_FAn.AlarmHistory	Output	Sampled history of last 8 A-bits
Status_FAn.ErrorCountCRC[7:0]	Output	Sampled state of CRC error counter
Status_FAn.ErrorCountFAS[7:0]	Output	Sampled state of FAS/nFAS error counter
Status_FAn.ErrorCountE[7:0]	Output	Sampled state of E-Bit counter
SampleCmds.SampleCRC	Input	Active ‘1’ during one clock cycle, when up write access has been detected to the read-only port of the related counter
SampleCmds.SampleFAS	Input	Active ‘1’ during one clock cycle, when up write access has been detected to the read-only port of the related counter
SampleCmds.SampleE	Input	Active ‘1’ during one clock cycle, when up write access has been detected to the read-only port of the related counter
Data_in_FSC.Data	Input	Binary NRZ data
Data_in_FSC.DataEbl	Input	Data enable
Data_in_FSC.FSync	Input	(FSC) Frame Sync pulse
DiFramed.Data	Output	Binary NRZ Data, synchronized to local clock domain
DiFramed.DataEbl	Output	Data enable
DiFrameRef.BF.BitNr[2:0]	Output	Frame reference pointer identifying every bit in a frame: Bit number within time slot 1 .. 8
DiFrameRef.BF.TSNr[4:0]	Output	Time slot number 0 .. 31
DiFrameRef.BF.BFNr	Output	Basic frame number
DiFrameRef.BF.BFSyncState[1:0]	Output	Basic Frame synchronization state: “01”: Hunt, “00”: Recover, “10”: InSync, “11”: OutOFSync
DiFrameRef.BF.TSInd	Output	Time slot indicator ‘1’ when bit number = 7
DiFrameRef.BF.TS0Ind_BF1	Output	Time slot 0 indicator of basic frame 1
DiFrameRef.BF.TS0Ind_BF2	Output	Time slot 0 indicator of basic frame 2
DiFrameRef.BF.FSync	Output	‘1’ when 1st bit of a frame when BFSyncState = InSync
DiFrameRef.MF.FrameNr[3:0]	Output	Multi frame synchronization state: “00”: Hunt, “01”: Recover, “10”: ParRecover, “11”: InSync
DiFrameRef.MF.SMFInd	Output	Sub multi frame indicator ‘1’ at last bit of previous sub multi frame
DiFrameRef.MF.MFInd	Output	Multi frame indicator
DiFrameRef.MF.SMFSync	Output	‘1’ at 1st bit of sub multi frame when MFSyncState = InSync
DiFrameRef.MF.next_MFSync	Output	‘1’ one bit before MFSync
DiFrameRef.MF.MFSync	Output	‘1’ at 1st bit of multi frame when MFSyncState = InSync
Do_FSC.Data	Input	Binary NRZ data
Do_FSC.DataEbl	Input	Data enable
Do_FSC.FSync	Input	(FSC) Frame Sync pulse
DataOut_FSC.Data	Output	Binary NRZ Data, synchronized to local clock domain
DataOut_FSC.DataEbl	Output	Data enable
DataOut_FrameRef[24:0]	Output	Frame reference pointer (see DiFrameRef)

Table 2: Core I/O Signals

Recommended Design Experience

For the source version, users should be familiar with HDL entry and Actel design flows. Users should be familiar with Actel Libero v2.2 Integrated Design Environment (IDE) and preferably with Synplify and Model*Sim*.

Ordering Information

The CORE is provided under license from Avnet Memec for use in Actel programmable logic devices. Please contact Avnet Memec for pricing and more information.

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Ordering Information:

Part Number	Hardware	Resale
MC-ACT-G704E1-NET	Actel Core Netlist	Contact for pricing
MC-ACT-G704E1-VHD	Actel Core VHDL	Contact for pricing

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