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Product Summary

Intended Use

- Automotive Industry
- Engine Control Unit
- Sensors

Key Features

- CAN 2.0B, 1Mbit/s
- Very small footprint
- Fully Synchronous Design
- AMBA (APB) compliant interface
- TX message FIFO
- 16 RX message trays with individual filtering

Targeted Devices

- Axcelerator Family
- ProASIC^{PLUS} Family

General Description

The MC-ACT-XCANMF is an APB compliant full CAN controller with a very small 'footprint'. It provides a TX FIFO and 16 RX message trays with individual message filtering. The core comes with an AMBA (APB) interface. The APB protocol is very simple and the interface can be easily used as a generic interface.

The MC-ACT-XCANMF has two independent clock inputs, one for the APB interface and one for the XCAN core. This makes the core very flexible, connecting it to a fast APB bus while the XCAN runs on a clock > 8MHz

Core Deliverables

- Netlist Version
  - Netlist compatible with the Actel Designer place and route tool
- RTL Version
  - VHDL Source Code
  - Test Bench
- All
  - User Guide

Synthesis and Simulation Support

- Synthesis: Synplicity
- Simulation: ModelSim
- Other tools supported upon request

Verification

- Test Bench

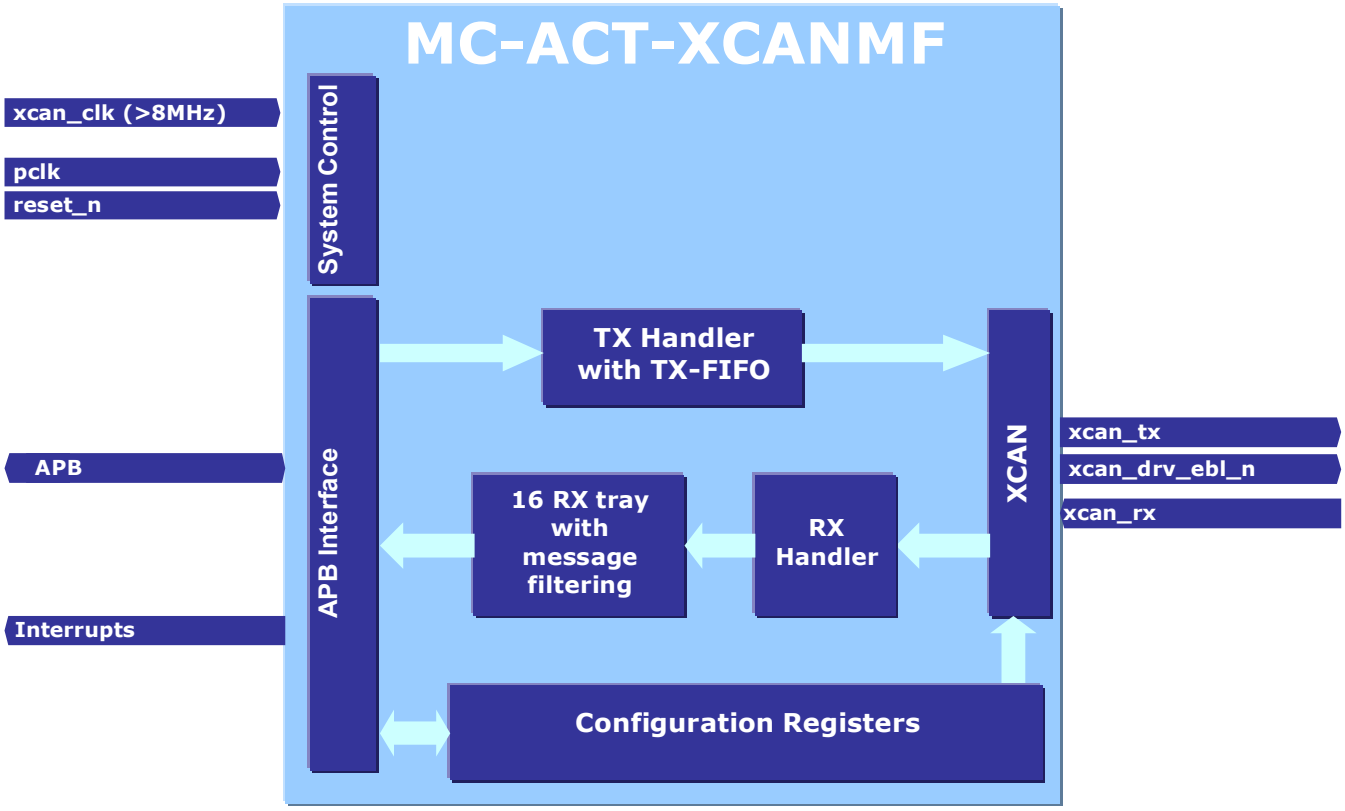


Figure 1: Logic Symbol

Functional Description (XCAN)

The XCAN core contains the complete data link layer, including the framer, transmit and receive control, error handling, error reporting and synchronization.

The core is designed to provide a bus bit rate up to 1Mbit/s with a minimum core clock frequency of 8 MHz.

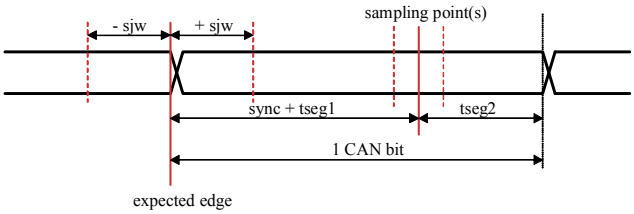
CAN Configuration

Bit rate, sub-bit segments (timing segment 1 & 2) and the synchronization jump width (sjw) for resynchronization can be configured to meet the required timing to the connected CAN bus.

The edge for resynchronization on the incoming message is defined in the edge-mode. Either the R-D edge or both (R-D and D-R) are used for resynchronization.

The XCAN provides two different sampling modes: Direct Sampling or three point sampling with majority decision.

The following diagram shows the bit timing:

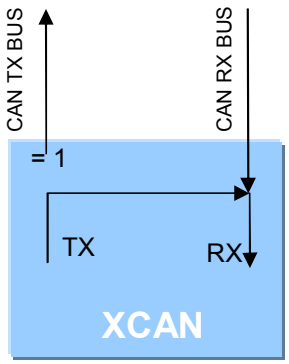


Start/Stop Controlling

The XCAN can be set in stop or start mode by user command.

Silent Mode

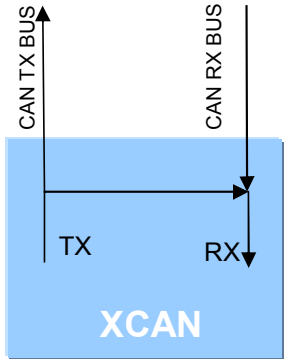
In silent mode the XCAN receives valid data and remote frames but sends only recessive bits on the CAN bus. In this mode the bus traffic can be analyzed without affecting it by sending dominant bits. The tx bus of the core is internally routed to the rx bus to receive acknowledges generated by this core.



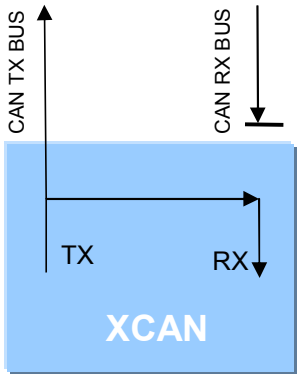
Loop Back Mode

In loop back mode the XCAN receives also messages which are sent by the core itself. Two different loop back mode can be configured.

Mode a: The core receives also messages sent by itself.



Mode b: The CAN receives only messages sent by itself and ignores messages and acknowledges from CAN rx bus.



Silent mode combined with loop back mode

Loop back and silent mode can be used together. In this configuration the XCAN can be tested without affecting a running CAN system.

Functional Description (MC-ACT-XCANMF)

Clock Configuration

The MC-ACT-XCANF has two independent clock inputs, one for the APB interface and one for the XCAN core. This makes the core very flexible, connecting it to a fast APB bus while the XCAN runs on a clock > 8MHz. Of course these two clocks can also be fed from the same source.

APB Interface

The core comes with an AMBA (APB) compliant interface. The APB protocol is very simple and the interface can be easy used as a generic interface.

Message handling, configuration of the core and read out of status information is done via this interface. For more information about the registers and address offsets please refer the user guide.

TX Handler

For transmission the MC-ACT-XCANMF provides a FIFO for storing the outgoing messages. Writing a TX message to the FIFO is like accessing a memory. The ID, DLC and IDE and RTR, data 1-4, data 5-8 can be written in any order. Committing the TX message to the FIFO takes place when writing an arbitrary value to TX start register. This also increments the TX FIFO fill level by 1.

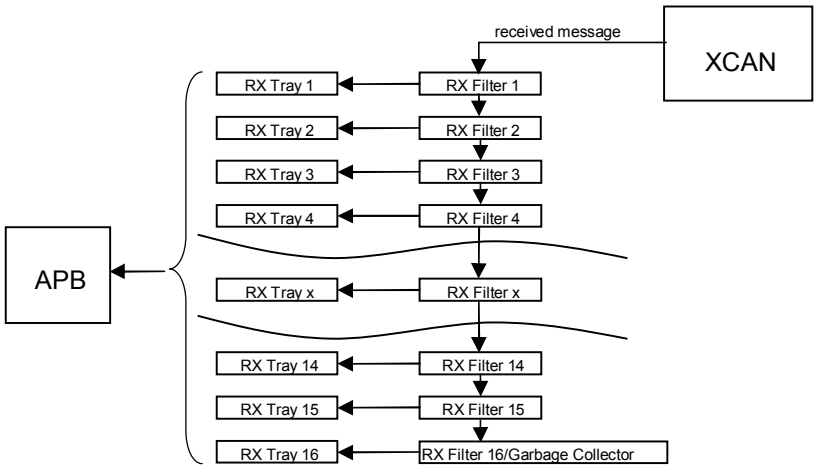
As soon as there is one or more TX messages in the TX FIFO the TX handler automatically feeds the messages to the XCAN, which in turn sends the messages onto the CAN network. When a message has been completely transmitted then the TX interrupt flag is set, and the next TX message, if there is any, is sent.

The TX FIFO is full when ‘TX FIFO size’ – 1 messages have been committed. If another commit takes place before at least 1 message has been sent by the CAN the TX overflow flag is set. Write accesses to the TX FIFO after an overflow have now effect, i.e. the messages in the FIFO remain valid.

RX Handler

The RX path of the MC-ACT-XCANMF contains sixteen RX trays. For each tray an individual filter value can be set. The filter value contains the ID, IDE and RTR bits. It defines which messages have to be received by a tray. The RX handler compares the configured filter values against the identifier bits of the incoming message. The message will be stored to each matching tray. Tray 16 can be configured as a garbage collector. In this mode the tray ignores its configured filter value and stores all the messages which don’t match to another tray.

Filter values can be reprogrammed at any time. But it is possible that incoming messages of the new or old identifier are lost.



Behavior of a tray

As soon as a message is received and stored in a tray a corresponding 'rx valid' flag is set. Before the message can be read it has to be requested first. The 'rx valid' flag is reset and the message can be read. The actual message remains valid until a newly received message is requested by the user. (A newly received message is indicated with an active 'rx valid' flag). An active overflow flag for each tray indicates that another message has been received although the tray contained an old unrequested message. In this case the old message is overwritten by the new one.

Interrupts

The MC-ACT-XCANMF provides 3 interrupts for efficient message and CAN error handling. One flag marks the reception of a new RX message, one marks that a message has been completely sent and the third flag signals that either the RX or the TX error counter or both have become bigger than 96.

Device Requirements

Family	Device	Utilization				Performance
		COMB*	SEQ*	Total*	RAM Blocks	pclk/xcan_clk
ProASIC^{PLUS}	APA075-STD	n/a	n/a	2607 (84%) [2162 (70%)]	8	39/16 MHz
Axcelerator	AX125-STD	1270 (95%) [1063 (80%)]	429 (64%) [346 (52%)]	1699 (85%) [1409 (70%)]	3	103/20 MHz

* max [min] values. (Minimum values are with reduced features.)

Table 1: Device Utilization and Performance

Verification and Compliance

Functional and timing simulation has been performed on the MC-ACT-XCANMF using VHDL Test Benches. Simulation vectors used for verification are provided with the core. This core has also been used successfully in customer designs.

Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Direction	Description
reset_n	in	asynchronous system reset, active low
xcan_clk	in	Clock source for the XCAN, > 8MHz
pclk	in	APB clock
paddr[31:0]	in	APB Address input, bits [5:2] used only
psel	in	APB Select signal
penable	in	APB Enable signal
pwrite	in	APB Write signal
pwdata[31:0]	in	APB Write data
prdata[31:0]	out	APB Read data
pdata_byte_ebl[3:0]	in	Data byte enable
xcan_int_tx	out	Transmit interrupt
xcan_int_rx	out	Receive interrupt
xcan_int_err	out	Error interrupt
xcan_rx_bus	in	Receiver pin of CAN bus
xcan_tx_bus	out	Transmitter pin of CAN bus
xcan_bus_ebl_n	out	Can bus driver enable; '0': active, '1': passive

Table 2: Core I/O Signals

Recommended Design Experience

For the source version, users should be familiar with HDL entry and Actel design flows. Users should be familiar with Actel Libero v2.2 Integrated Design Environment (IDE) and preferably with Synplify and ModelSim.

Ordering Information

Part Number	Description
MC-ACT-XCANMF-NET	Core Netlist
MC-ACT-XCANMF-VHD	Core VHDL

Table 3: Core Part Numbers

The CORE is provided under license from Memec Design for use in Actel programmable logic devices. Please contact Memec Design for pricing and more information.

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Datasheet Revision History

Version	Date	Description
Datasheet 0.1	March 5, 2003	Preliminary Release
Datasheet 1.0	May 9, 2003	Initial Release