



## Functional Description

This core conforms to the appropriate standard(s). In general, standards do not define the internal user interface, only the external interfaces and protocols. Therefore, Avnet Memec has created a simple FIFO interface to this core for easy user connectivity. This document describes this Avnet Memec created interface. Please consult the appropriate standards document for all external signaling.

### TOP\_PHY

This is the top level of the core. Its only purpose is to serve as a container to instantiate the transmit (TX) & receive (RX) modules. TOP\_LINK is also where the generics are located that configure the core. These parameters are then passed down to the TX & RX modules. This is an optional module as the TOP\_TX\_PHY, and the TOP\_RX\_PHY modules may be instantiated separately (even in different FPGAs).

### TOP\_TX\_PHY & TOP\_RX\_PHY

These modules comprise the transmit & receive portions of the interface. They were developed so that they may be instantiated either separately in different FPGAs or together in one FPGA. They use common sub-modules FIFO\_16 for simplicity and reliability.

### TX\_POSPHY3\_PHY

The TX PHY is responsible for replying to polls from the LINK in order to receive packets.

### RX\_POSPHY3\_PHY

The RX PHY is responsible for sending packets to the LINK.

### PACKET\_COUNTER

The packet counter module (one per PHY port) is responsible for generating the packet available flags for the core. Every time an EOP (End of Packet) is written the packet count goes up and when a EOP is read the packet count goes down. This allows the core to send data when there is an EOP in the FIFO even if the FIFO low watermark hasn't been reached.

### FIFO\_16

The FIFO module contains one FIFO per PHY port (i.e. this module is instantiated N times, where N = number of PHY ports). The FIFOs are created by utilizing the available embedded memory resources in the FPGA. The FIFO may be operated in synchronous (same clock for read & write) and asynchronous (different clocks for read & write) systems.

The user provides wr\_data and wr\_stats to the FIFO interface. This is concatenated into a single bus and written into the FIFO. For example, if the data\_size is 8, then the wr\_data would be 8 bits wide and the wr\_stats would be 8 bits wide. These two buses are concatenated together and written into the FIFO, which is 16 bits wide. This way there doesn't have to be a single FIFO for the stats and a single FIFO for the data, which would nearly double the size of the core. In the opposite direction the reverse takes place.

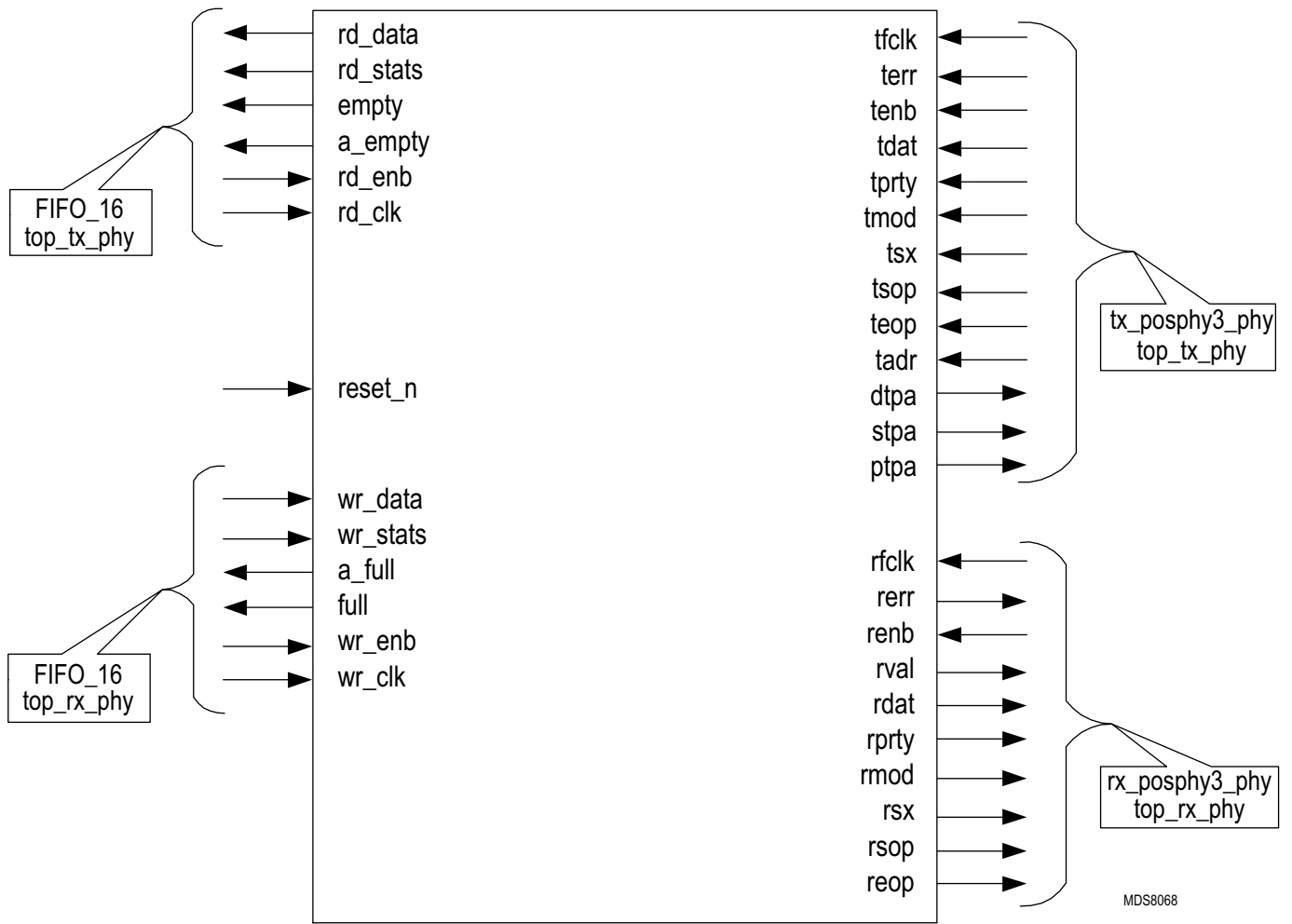


Figure 1: Logic Symbol

### Device Requirements

Family	Device	Utilization			Performance
		COMB	SEQ	Tiles	
Axcelerator	AX250	19%	26%	n/a	119 MHz

Table 1: Device Utilization and Performance\*

\*Note: These numbers obtained with 2 PHY's and 16-bit data size.

### Verification and Compliance

The testbench is self-checking, which means that if there is an error detected in the start word, end word, or payload the testbench will assert one or both of two error signals. The test checks for errors at two stages in the testbench: when the cells (packets) are looped back through the PHY device (SIG\_LOOP\_ERROR\_OUT), and upon reading out of the link device (SIG\_ERROR\_OUT). This core has also been used successfully in customer designs.

## Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Width	Direction	Description
RD_DATA	DATA_SIZE	Output	Read data bus for the FIFOs.
RD_STATS	8	Output	Statistics for the link. Includes SOP, EOP, ERR, MOD, & PARITY.
A_EMPTY	1	Output	Indicates when FIFO is almost empty.
EMPTY	1	Output	Indicates when FIFO is empty.
RD_ENB	1	Input	Read enable signal for the FIFO.
RD_CLK	1	Input	Read clock for the FIFO.
RESET_N	1	Input	Reset signal from user logic.
WR_DATA	DATA_SIZE * NUM_PHYS	Input	Write data bus for FIFO.
WR_STATS	8	Input	Statistics for the link. Includes SOP, EOP, ERR, MOD, & PARITY.
A_FULL	NUM_PHYS	Output	Almost full for FIFOs indicates that the FIFO does not have enough room for an additional cell.
FULL	NUM_PHYS	Output	Indicates that the FIFO is full.
WR_ENB	NUM_PHYS	Input	Write enable signal for FIFO.
WR_CLK	1	Input	System clock for all registers in this block.
RFCLK	1	Input	104 MHz Clock for all registers in this block.
RERR	1	Output	POS-PHY Error signal used to flag an errored packet.
RENB	1	Input	POS-PHY Enable signal used for throttle control.
RVAL	1	Output	POS-PHY Valid signal used to indicate valid data on RDAT
RDAT	8, 16, 32	Output	POS-PHY Data Bus. 8-bit or 32-bit selectable.
RPRTY	1	Output	POS-PHY Parity used for odd parity on rdat.
RMOD	2	Output	POS-PHY signal used to indicate which bytes are valid in the last word of the packet.
RSX	1	Output	POS-PHY Select signal used to indicate the address on the rdat lines for selection.
RSOP	1	Output	POS-PHY Start of Packet signal used to flag the first byte/word in the packet.
REOP	1	Output	POS-PHY End of Packet signal used to flag the last byte/word in the packet.
TFCLK	1	Input	104 MHz Clock for all registers in this block.
TERR	1	Input	POS-PHY Error signal used to flag an errored packet.
TENB	1	Input	POS-PHY Enable signal used for throttle control.
TDAT	8, 16, 32	Input	POS-PHY Data Bus. 8-bit or 32-bit selectable.
TPRTY	1	Input	POS-PHY Parity used for odd parity on TDAT.
TMOD	2	Input	POS-PHY signal used to indicate which bytes are valid in the last word of the packet.
TSX	1	Input	POS-PHY Select signal used to indicate the address on the TDAT lines for selection.
TSOP	1	Input	POS-PHY Start of Packet signal used to flag the first byte/word in the packet.
TEOP	1	Input	POS-PHY End of Packet signal used to flag the last byte/word in the packet.
TADR	5	Input	POS-PHY Address Bus used for polling.
DTPA	4	Output	POS-PHY Packet Available signal used to indicate that the PHY has room for a cell when direct.
STPA	1	Output	POS-PHY Packet Available signal used to indicate that the selected PHY has room for a cell.
PTPA	1	Output	POS-PHY Packet Available signal used to indicate that the PHY has room for a cell when polled.

Table 2: Core I/O Signals

## Timing

Since the ATM Forum specification fully defines the line side of the POS-PHY Level 3 interface, timing for that is not replicated here. Instead, only user (FIFO) interface timing information is presented here. The figure below shows the functional timing for FIFO reads and writes.

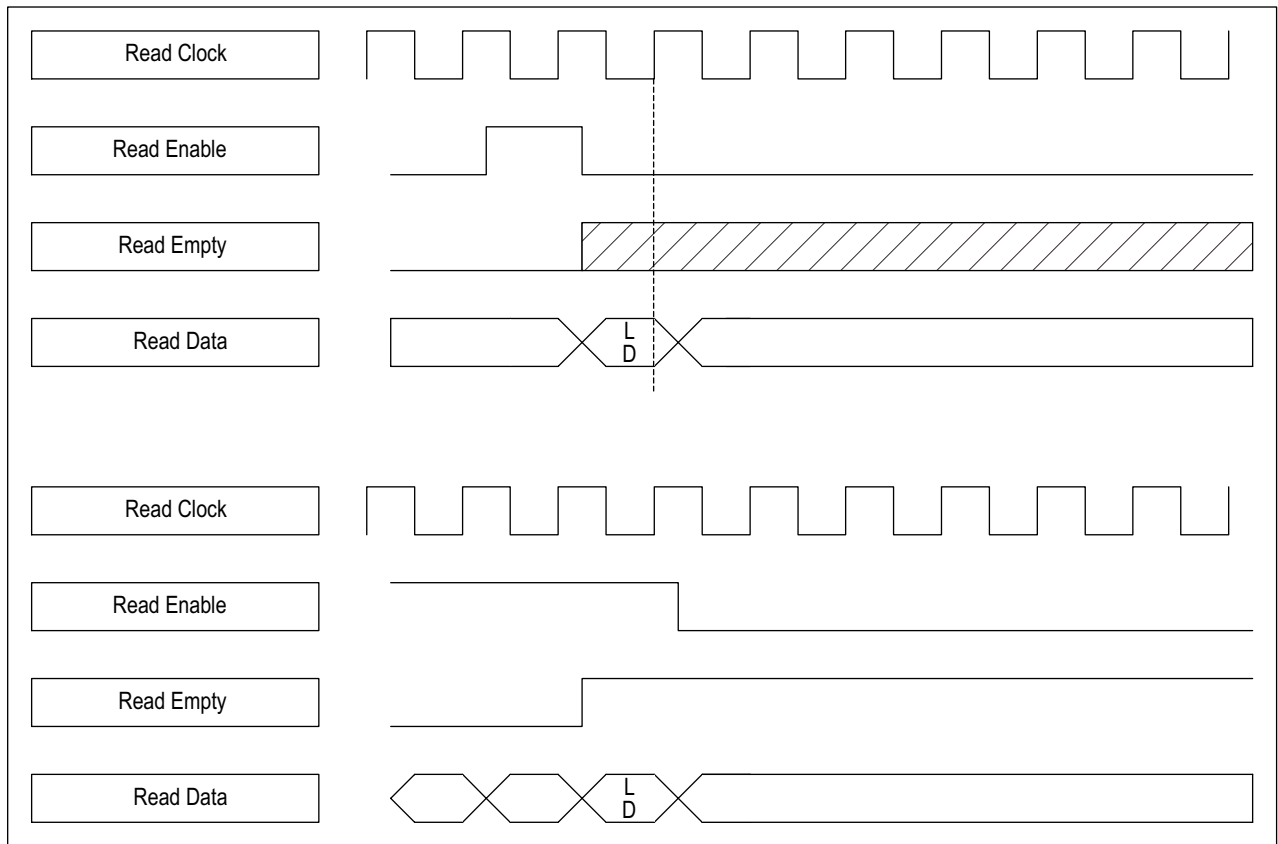


Figure 2: FIFO Timing

The top example shows where the last valid data word (LD) is clocked out relative to the deassertion of read enable. The bottom example shows read enable responding to the assertion of read empty.

## Recommended Design Experience

For the source version, users should be familiar with HDL entry and Actel design flows. Users should be familiar with Actel Libero Integrated Design Environment (IDE) and preferably with Synplify and ModelSim.

## Ordering Information

The CORE is provided under license from Avnet Memec for use in Actel programmable logic devices. Please contact Avnet Memec for pricing and more information.

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### Ordering Information:

#### Part Number

MC-ACT-PL3PHY-NET

MC-ACT-PL3PHY-VHDL

#### Hardware

Actel PL3PHY Netlist

Actel PL3PHY VHDL

#### Resale

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