JPEG-C

Baseline JPEG Codec Core

Implements a high-performance, half-duplex image or video encoder/decoder (codec) that complies with the baseline ISO/IEC 10918-1 JPEG standard.

One of the fastest available JPEG cores, the JPEG-C provides a high-performance solution for a variety of image and video decompression applications. It can, for example, encode or decode over 30 frames/sec of 4:3 HDTV, 1440x1152, 4:2:0, even in FPGA devices. In a typical 0.09µ process ASIC, the core requires just 95,000 gates and operates at 330 MHz.

In addition to processing baseline JPEG streams, the core can compress or decompress non-standard motion JPEG streams. It also has two options. Encoding can be enhanced with an optional add-on bit-rate control block, which may benefit applications that have tight bandwidth constraints. Decoding may be enhanced with an optional IDCT block that enables down-scaling in the frequency domain, a feature that allows decompression at various resolutions from the same compressed stream.

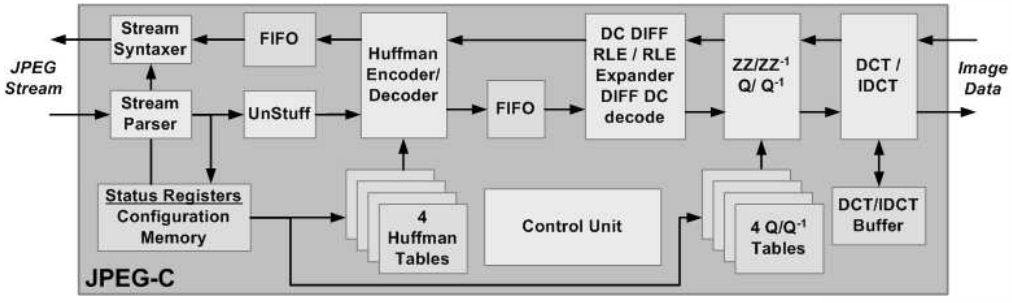
The core includes FIFO-like pixel and stream input/output interfaces, and other standard interfaces (e.g. AMBA) are also available. The core is designed for reliability and ease of integration, and has been proven in a number of ASIC and FPGA designs. The deliverables include a software bit-accurate model that facilitates system-on-chip verification.

Applications

The JPEG-C can be utilized for a variety of multimedia applications including:

- Office automation equipment (Multifunction printers, scanners, digital copiers etc)
- Digital cameras & camcorders
- Video production, video conference
- Display-projection systems
- Surveillance systems

Block Diagram



Features

Baseline ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC) and
- Programmable quantization tables (four)
- Up to 4 color components (optionally extendable to 255 components)
- Supports all possible scan configurations and all JPEG formats for input/output data
- Any image size up to 64k x 64k
- Supports DNL and restart markers

Additional Image Processing Capabilities

- Motion JPEG encoding/decoding
- One-pass compression ratio regulation (optional)
- Decompressing at various resolution via downscaling in the frequency domain (optional)

Designed for Easy Integration

- Encoding Mode
  - Single clock per input sample
  - Fully programmable through standard JPEG stream marker segments
  - Automatic headers generation
  - Automatic program-once encode-many operation
- Decoding Mode
  - Stand-alone operation
  - Automatic self-programming by JPEG stream headers parsing
  - Header errors catching
  - Broadcasting of decoded image parameters for controlling peripherals such as a raster to block converter

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Scan-ready design architecture

September 2005

Functional Description

For encoding, the JPEG-C is automatically configured by feeding it with JPEG headers, which contain table specification, image format, and encoding options data. The core's configuration can be modified after the encoding of one or multiple frames. Image samples in any color space format are input to the JPEG-C in a MCU block by MCU block, raster scan order.

Consuming a single clock cycle per image sample while encoding, the JPEG-C can address the most demanding frame-based video compression applications. The JPEG-C outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled if the optional rate-control block is used.

The JPEG-C's decoding path is highly autonomous, since it is self-configured (with table, image format and encoding options) by parsing the incoming JPEG stream's headers. The core parses and checks all JPEG marker segments and signals in case it detects an error. Decoded image parameters are made available for controlling peripherals such as a block-to-raster converter.

Designed for continuous data flow decoding, the JPEG-C can address the most demanding frame-based video decompression applications. Optional decoding at various resolutions from the same JPEG data-stream without the need for any extra buffering is enabled when the IDCT block is configured during synthesis to support downscaling in the frequency domain.

Implementation Results

JPEG-C reference designs have been evaluated in a variety of technologies. The following are sample Actel results.

Actel Device	Cells	Seq	Comb	Frequency	Special Features
Axcelerator AX2000-2	24,112	7,511	16,601	66 MHz	12 RAM
Axcelerator RTAX2000S-1	24,310	7,698	16,612	42 MHz	12 RAM
Proasic Plus APA1000-STD	45,791	8,049	37,742	28 MHz	26 RAM
Proasic3E A3P3000-2	44,299	11,759	32,540	49 MHz	13 RAM

Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. Being embedded in numerous of products, the core is silicon proven in both FPGA and ASIC technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Actel version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide
- Software (C++) Bit-Accurate Model

CAST
info@cast-inc.com
www.cast-inc.com

CAST, Inc. 11 Stonewall Court
Woodcliff Lake, NJ 07677 USA
tel 201-391-8300 fax 201-391-8694

Alma Technologies
This core developed by the multimedia experts at Alma Technologies S.A.