CAN

Bus Controller Core

General Description

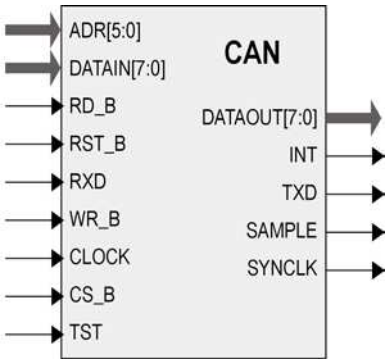
The development of increasingly complex microsystems requires the usage of a powerful field bus systems for distributed real-time networks. The CAN protocol has a wide acceptance in the field of serial communication.

The CAN bus controller core is described at the RTL system level which allow easy targeting of various technologies.

The CAN bus core is founded on the basic CAN principle and meets all constraints of the CAN-specification 2.0B. For buffering of received or transmitted messages three 13-byte buffers are used. In practice no overload frames will be generated.

Developed for easy reuse in Actel FPGA applications, the CAN is available optimized for several device families with competitive utilization and performance characteristics.

Symbol



Features

- Implementation of the Basic CAN specification
- No generated Overload Frames
- Receiving and transmitting of both identifiers (CAN specification 2.0B)
- Programmable data rate up to 1 mbps
- Programmable baud rate prescaler (up to 1/30)
- Application specific interface to the host-controller
- Link to commercial bus drivers (for instance PCA82C250T by Philips)
- Certified by Bosch reference model

Applications

- Automotive systems
- Industrial and manufacturing control systems

Performance

The CAN is a technology-independent design that can be implemented in a variety of process technologies. Results with representative Actel devices are shown in Table 1.

Family	Device (-speed grade)	Utilization (Cells or Tiles)		
		Sequential	Combinatorial	Total
ProASIC^{PLUS}	APA750-STD	625 Tiles	3265 Tiles	12%
Axcelerator	AX1000-3	699	1797	14%
SXA	A54SX72A-STD	658	1738	40%
RTSX-S	RT54SX72S-STD	658	1738	40%

Table 1: Utilization Table for CAN Core implemented in Actel Devices

Verification Methods

The CAN controller has been implemented into Fraunhofer-IMS' 1.0 micron double metal CMOS technology library and has been tested successfully. sThe core has also been certified by a Bosch reference model.

Deliverables

- Post-synthesis EDIF netlist (source code versions are also available; contact CAST)
- Extensive testbench and expected results
- Simulation vectors and expected results
- Place and route scripts
- Detailed user's documentation

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