Revision 5

Radiation-Tolerant ProASIC3 Low Power Spaceflight Flash FPGAs with Flash*Freeze Technology

Features and Benefits

MIL-STD-883 Class B Qualified Packaging

- Ceramic Column Grid Array with Six Sigma Copper-Wrapped Lead-Tin Columns
- Land Grid Array
- Ceramic Quad Flat Pack

Low Power

- Dramatic Reduction in Dynamic and Static Power
- 1.2 V to 1.5 V Core and I/O Voltage Support for Low Power
- Low Power Consumption in Flash*Freeze Mode

Radiation Performance

- 25 Krad to 30 Krad with 10% Propagation Delay Increase (TM 1019 Cond. A, Dose Rate 5 Krad/min)
- Up to 40 Krad with 10% Propagation Delay Increase, Dose Rate < 1 Krad/min
- Up to 55 Krad with 15% Propagation Delay Increase, Dose Rate < 1 Krad/min
- Wafer-Lot-Specific TID Reports

High Capacity

- 600 k to 3 M System Gates
- Up to 504 kbits of True Dual-Port SRAM
- Up to 620 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

High Performance

- 350 MHz (1.5 V) and 250 MHz (1.2 V) System Performance
- 3.3 V, 66 MHz, 66-Bit PCI (1.5 V); 66 MHz, 32-Bit PCI (1.2 V)

In-System Programming (ISP) and Security

- ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock® Designed to Secure FPGA Contents

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced and Pro (Professional) I/Os

- 700 Mbps DDR, LVDS-Capable I/Os
- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, and 3.3 V PCI / 3.3 V PCI-X
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II (RT3PE3000L only)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay (RT3PE3000L only)
- Schmitt Trigger Option on Single-Ended Inputs (RT3PE3000L)
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the Radiation-Tolerant (RT) ProASIC®3 Family

Clock Conditioning Circuit (CCC) and PLL

- Six CCC Blocks, All with Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range 1.5 MHz to 250 MHz (1.2 V systems) and 350 MHz (1.5 V systems)

SRAMs and FIFOs

- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- 24 SRAM and FIFO Blocks with Synchronous Operation:
  – 250 MHz: For 1.2 V Systems
  – 350 MHz: For 1.5 V Systems

Table I-1 • Radiation-Tolerant (RT) ProASIC3 Low Power Spaceflight FPGAs

RT ProASIC3 Devices	**RT3PE600L**	**RT3PE3000L**
System Gates	600,000	3,000,000
VersaTiles (D-flip-flops)	13,824	75,264
RAM kbits (1,024 bits)	108	504
4,608-Bit Blocks	24	112
FlashROM Kbits	1	1
Secure (AES) ISP	Yes	Yes
Integrated PLL in CCCs	6	6
VersaNet Globals	18	18
I/O Banks	8	8
Maximum User I/Os	270	620
Package Pins		
CCGA/LGA	CG/LG484	CG/LG484, CG/LG896
CQFP	CQ256	CQ256

I/Os Per Package [1]

RT ProASIC3 Low Power Devices	RT3PE600L		RT3PE3000L	
Package	**Single-Ended I/Os[2]**	**Differential I/O Pairs**	**Single-Ended I/Os[2]**	**Differential I/O Pairs**
CG/LG484	270	135	341	168
CG/LG896	–	–	620	310
CQ256	166	82	166	82

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the packaging section of the datasheet to ensure you are complying with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *For RT3PE3000L devices, the usage of certain I/O standards is limited as follows:*
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V / GTL 2.5 V: up to 72 I/Os per north or south bank
4. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

RT ProASIC3 Device Status

RT ProASIC3 Devices	Status
RT3PE600L	Production
RT3PE3000L	Production

RT ProASIC3 Ordering Information

RT3PE3000L – 1 CG 484 Y B

Application (Screening Level)
B = MIL-STD-883 Class B
E = Extended Flow
PROTO = Protoype Unit; Not for Space-Flight or Qualification of Space-Flight Hardware

Security Feature
Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

Package Lead Count

Package Type
CG = Ceramic Column Grid Array (1.0 mm pitch)
LG = Land Grid Array (1.0 mm pitch)
CQ = Ceramic Quad Flat Pack

Speed Grade
Blank = Standard
1 = 15% Faster than Standard

Part Number

RT ProASIC3 Spaceflight FPGAs

RT3PE600L = 600,000 System Gates
RT3PE3000L = 3,000,000 System Gates

Screening Levels

Package	RT3PE600L	RT3PE3000L
CG/LG484	B, E, PROTO	B, E, PROTO
CG/LG896	–	B, E, PROTO
CQ256	B, E, PROTO	B, E, PROTO

Note: *B = MIL-STD-883 Class B screening*
E = Extended flow
PROTO = Prototype unit; not for space-flight or qualification of space-flight hardware.

Speed Grade Offerings

Speed Grade	RT3PE600L	RT3PE3000L
Std.	✓	✓
–1	✓	✓

Notes:

1. *Data applies to B, E, and PROTO flow devices.*
2. *Contact your local Microsemi SoC Products Group representative for availability.*

MIL-STD-883 Class B Product Flow

Table 2 • MIL-STD-883 Class B Product Flow for RT ProASIC3 Devices*

Step	Screen	Method	Requirement
1	Internal Visual	2010, Condition B	100%
2	Serialization		100%
3	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
4	Constant Acceleration	2001, Y1 Orientation Only Condition B for CQ256, CQ352, LG624, LG1152 Condition D for CQ208 Condition A for LG1272, LGD1272, CQ352	100%
5	Particle Impact Noise Detection	2020, Condition A	100%
6	Seal (Fine & Gross Leak Test)	1014	100%
7	Pre-Burn-In Electrical Parameters	In accordance with applicable Microsemi device specification	100%
8	Dynamic Burn-In	1015, Condition D, 160 hours at 125°C or 80 hours at 150°C minimum	100%
9	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Microsemi device specification	100%
10	Percent Defective Allowable (PDA) Calculation	5%	All Lots
11	Final Electrical Test a. Static Tests (1) 25°C (2) –55°C and +125°C b. Functional Tests (1) 25°C (2) –55°C and +125°C c. Switching Tests at 25°C	In accordance with applicable Microsemi device specification, which includes a, b, and c: 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b 5005, Table 1, Subgroup 9	100%
12	External Visual	2009	100%

*Note: *For CCGA devices, all Assembly, Screening, and TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.*

Extended Flow (E Flow)

Table 3 • Extended Flow for RT ProASIC3 Devices[1,2]

Step	Screen	Method	Requirement
1	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
2	Internal Visual	2010, Condition A	100%
3	Serialization		100%
4	Temperature Cycling	1010, Condition C	100%
5	Constant Acceleration	2001, Condition B or D, Y1 Orientation Only	100%
6	Particle Impact Noise Detection	2020, Condition A	100%
7	Radiographic (X-Ray)	2012, One View (Y1 Orientation) Only	100%
8	Pre-Burn-In Test	In accordance with applicable Microsemi device specification	100%
9	Dynamic Burn-In	1015, Condition D, 240 hours at 125℃ or 120 hours at 150℃ minimum	100%
10	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Microsemi device specification	100%
11	Static Burn-In	1015, Condition C, 72 hours at 150℃ or 144 hours at 125℃ minimum	100%
12	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Microsemi device specification	100%
13	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters at 25℃	All Lots
14	Final Electrical Test	In accordance with Microsemi applicable device specification which includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25℃ (Subgroup 1, Table1)	5005	
	(2) –55℃ and +125℃ (Subgroups 2, 3, Table 1)	5005	
	b. Functional Tests		100%
	(1) 25℃ (Subgroup 7, Table 15)	5005	
	(2) –55℃ and +125℃ (Subgroups 8A and B, Table 1)	5005	
	c. Switching Tests at 25℃ (Subgroup 9, Table 1)	5005	100%
15	Seal a. Fine b. Gross	1014	100%
16	External Visual	2009	100%

Notes:

1. *Microsemi offers Extended Flow for users requiring additional screening beyond MIL-STD-883, Class B requirement. Microsemi offers this Extended Flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Method 5004 are shown in notes 2 and 4 below.*
2. *For CCGA devices, all Assembly/Screening/TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.*
3. *Method 5004 requires a 100 percent, nondestructive bond-pull to Method 2003. Microsemi substitutes a destructive bond-pull to Method 2011 Condition D on a sample basis only.*
4. *MIL-STD-883, Method 5004, requires a 100 percent radiation latch-up testing to Method 1020. Microsemi will NOT perform any radiation testing, and this requirement must be waived in its entirety.*
5. *Wafer lot acceptance complies to commercial standards only (requirement per Method 5007 is not performed).*

Table of Contents

Radiation-Tolerant ProASIC3 Low Power Spaceflight FPGA Overview

Radiation-Tolerant ProASIC3 Low Power Spaceflight Flash FPGAs DC and Switching Characteristics

Pin Descriptions

Package Pin Assignments

Datasheet Information

1 – Radiation-Tolerant ProASIC3 Low Power Spaceflight FPGA Overview

General Description

The radiation-tolerant (RT) ProASIC3 family of Microsemi flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50%. These power savings are coupled with performance, density, true single chip, 1.2 V to 1.5 V core and I/O operation, reprogrammability, and advanced features. The RT ProASIC3 FPGA is based on the ProASIC3EL family of low power FPGAs.

Microsemi's proven Flash*Freeze technology enables RT ProASIC3 device users to shut off dynamic power instantaneously and switch the device to static mode without the need to switch off clocks or power supplies, and retaining internal states of the device. This greatly simplifies power management. In addition, optimized software tools using power-driven layout provide instant push-button power reduction.

Nonvolatile flash technology gives RT ProASIC3 devices the advantage of being a secure, low power, single-chip solution that is live at power-up (LAPU). RT ProASIC3 devices offer dramatic dynamic power savings, giving FPGA users flexibility to combine low power with high performance.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

RT ProASIC3 devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry (CCC) based on an integrated phase-locked loop (PLL). RT ProASIC3 devices support devices from 600 k system gates to 3 million system gates with up to 504 kbits of true dual-port SRAM and 620 user I/Os.

Flash*Freeze Technology

RT ProASIC3 devices offer the proven Flash*Freeze technology, which allows instantaneous switching from an active state to a static state. When Flash*Freeze mode is activated, RT ProASIC3 devices enter a static state while retaining the contents of registers and SRAM. Power is conserved without the need for additional external components to turn off I/Os or clocks. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of RT ProASIC3 devices to support a 1.2 V core voltage allows for an even greater reduction in power consumption, which enables low total system power.

When the RT ProASIC3 device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low power modes, combined with a reprogrammable, single-chip, single-voltage solution, make RT ProASIC3 devices suitable for low power data transfer and manipulation in military-temperature applications where available power may be limited (e.g., in battery-powered equipment); or where heat dissipation may be limited (e.g., in enclosures with no forced cooling).

Flash Advantages

Low Power

The RT ProASIC3 family of flash-based FPGAs provides a low power advantage, and when coupled with high performance, enables designers to make power-smart choices using a single-chip, reprogrammable, and live-at-power-up device.

RT ProASIC3 devices offer 40% dynamic power and 50% static power savings by reducing the core operating voltage to 1.2 V. In addition, the power-driven layout (PDL) feature in Libero® System-on-Chip (SoC) software offers up to 30% additional power reduction. With Flash*Freeze technology, an RT ProASIC3 device is able to retain device SRAM and logic while dynamic power is reduced to a minimum, without the need to stop clock or power supplies. Combining these features provides a low power, feature-rich, and high-performance solution.

Security

Nonvolatile, flash-based RT ProASIC3 devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. RT ProASIC3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

RT ProASIC3 devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in RT ProASIC3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. RT ProASIC3 devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. RT ProASIC3 devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the RT ProASIC3 family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The RT ProASIC3 family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An RT ProASIC3 device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based RT ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

Flash-based RT ProASIC3 devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based RT ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based RT ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based RT ProASIC3 devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms are designed to prevent access to all the programming information and enable the highest level of security available for remote updates of the FPGA logic. Designers can perform remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property is protected and very unlikely to be compromised or copied. ISP can be performed using the industry-standard AES algorithm. The RT ProASIC3 family device architecture mitigates the need for ASIC migration at higher volumes. This makes the RT ProASIC3 family a cost-effective ASIC replacement.

Advanced Flash Technology

The RT ProASIC3 family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary RT ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The RT ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the RT ProASIC3 core tile, as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable, allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of RT ProASIC3 devices via an IEEE 1532 JTAG interface.

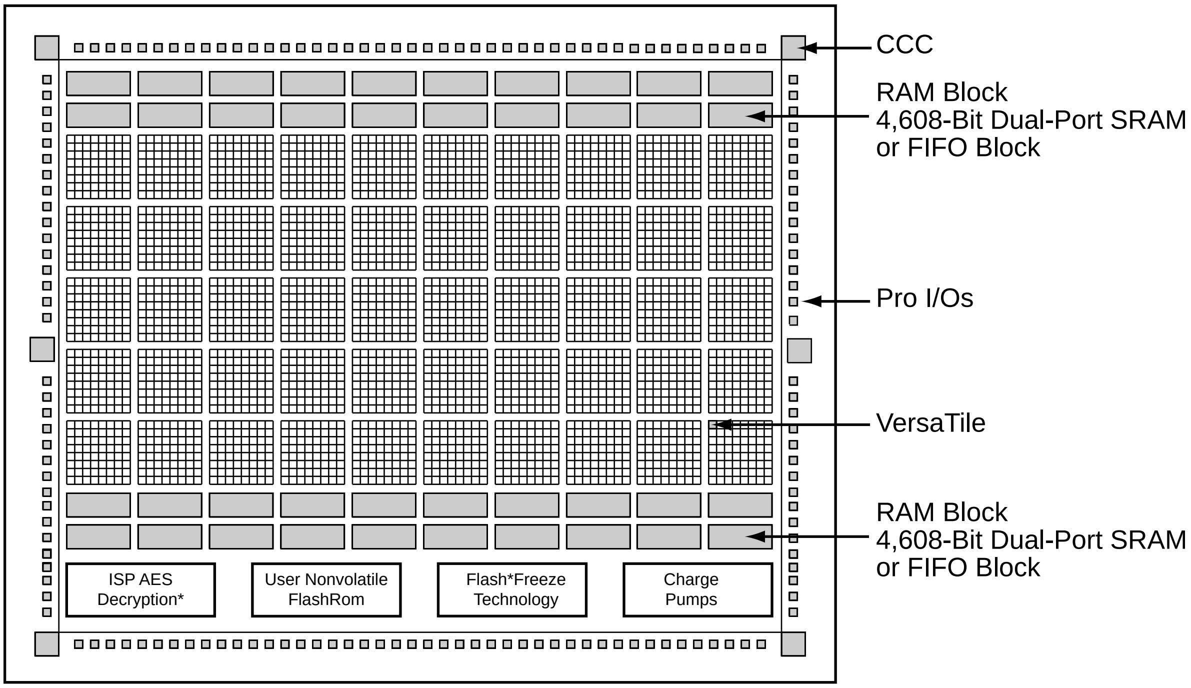


Figure 1-1 • **RT ProASIC3 Device Architecture Overview**

Flash*Freeze Technology

RT ProASIC3 devices offer proven Flash*Freeze technology, which enables designers to instantaneously shut off dynamic power consumption while retaining all SRAM and register information. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze (FF) pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption; clocks can still be driven or can be toggling without impact on power consumption; all core registers and SRAM cells retain their states. I/Os are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLLs. Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The FF pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the FF pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static and dynamic capabilities of the RT ProASIC3 device. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode.

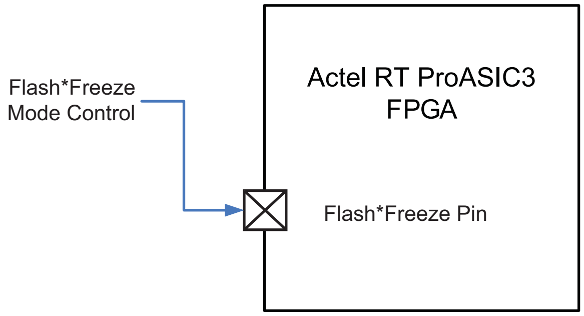


Figure 1-2 • **RT ProASIC3 Flash*Freeze Mode**

VersaTiles

The RT ProASIC3 core consists of VersaTiles, which have been enhanced beyond the ProASIC$^{\text{PLUS}®}$ core tiles. The RT ProASIC3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-3 for VersaTile configurations.

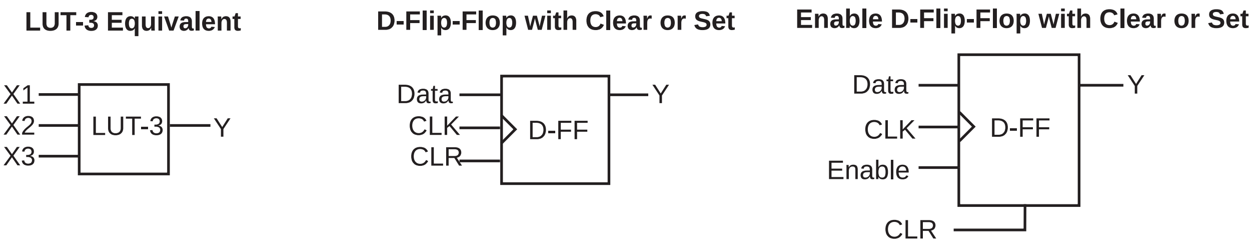


Figure 1-3 • **VersaTile Configurations**

User Nonvolatile FlashROM

RT ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

FlashROM is written using the standard RT ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to provide a high level of security when loading data over public networks, as in security keys stored in the FlashROM for a user design.

FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The RT ProASIC3 development software solution, Libero SoC, has extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

RT ProASIC3 devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

RT ProASIC3 space-flight FPGAs provide designers with flexible clock conditioning circuit (CCC) capabilities. Each member of the RT ProASIC3 family contains six CCCs, located at the four corners and the centers of the east and west sides. All six CCC blocks are equipped with a PLL. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 µs
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC}

Global Clocking

RT ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The RT ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). In addition, 1.2 V I/O operation is supported for RT ProASIC3 devices. RT ProASIC3 FPGAs support different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device. The configuration of these banks determines the I/O standards supported. For RT ProASIC3, each I/O bank is subdivided into V_{REF} minibanks, which are used by voltage-referenced I/Os. V_{REF} minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common V_{REF} line. Therefore, if any I/O in a given V_{REF} minibank is configured as a V_{REF} pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-data-rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-data-rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

RT ProASIC3 banks support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

2 – Radiation-Tolerant ProASIC3 Low Power Spaceflight Flash FPGAs DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI and VMV[2]	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG}	Storage temperature	–65 to +150	°C
T_J	Junction temperature	+150	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-7.*
2. *VMV pins must be connected to the corresponding VCCI pins. Refer to the "Pin Descriptions" section on page 3-1 for further information.*
3. *For recommended operating limits, refer to Table 2-2 on page 2-2.*

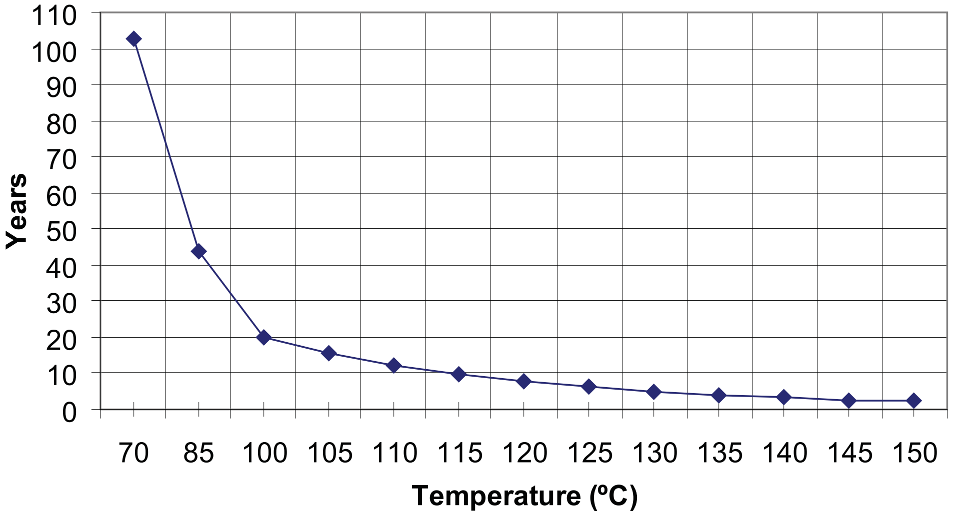
Table 2-2 • **Recommended Operating Conditions[1,2]**

Symbol	Parameter		Military	Units
T_A	Ambient temperature		–55 to 125	°C
T_J	Junction temperature		–55 to 125	°C
VCC[6]	1.5 V DC core supply voltage[3]		1.425 to 1.575	V
	1.2 – 1.5 V Wide Range DC core supply voltage[4]		1.14 to 1.575	V
VJTAG[6]	JTAG DC voltage		1.4 to 3.6	V
VPUMP[5,6]	Programming voltage	Programming mode	3.15 to 3.45	V
		Operation	0	V
VCCPLL[6]	Analog power supply (PLL)	1.5 V DC core supply voltage[3]	1.425 to 1.575	V
		1.2 – 1.5 V DC core supply voltage[4]	1.14 to 1.575	V
VCCI and VMV[6]	1.2 V DC supply voltage[4]		1.14 to 1.26	V
	1.2 V Wide Range DC supply voltage[4]		1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	V
	3.0 V DC supply voltage[7]		2.7 to 3.6	
	3.3 V DC supply voltage		3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.*
3. *For RT ProASIC3 devices operating at VCC = 1.5 V core voltage.*
4. *For RT ProASIC3 devices operating at VCC = 1.2 V core voltage and VCCI ≥ VCC.*
5. *VPUMP should be tied to 0 V to optimize total ionizing dose performance during operation in spaceflight applications.*
6. *See the "Pin Descriptions" section on page 3-1 for instructions and recommendations on tie-off and supply grouping.*
7. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*
8. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-18 on page 2-20.*

Tj (°C)	HTR Lifetime (yrs)
70	102.7
85	43.8
100	20.0
105	15.6
110	12.3
115	9.7
120	7.7
125	6.2
130	5.0
135	4.0
140	3.3
145	2.7
150	2.2



Note: HTR time is the period during which you would not expect a verify failure due to flash cell leakage.

Figure 2-1 • **High-Temperature Data Retention (HTR)**

Table 2-3 • **Overshoot and Undershoot Limits**

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle	Maximum Overshoot/Undershoot (125ºC)
2.7 V or less	10%	0.72 V
	5%	0.82 V
3 V	10%	0.72 V
	5%	0.81 V
3.3 V	10%	0.69 V
	5%	0.70 V
3.6 V	10%	N/A
	5%	N/A

Notes:

1. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
2. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-2 on page 2-5 and Figure 2-3 on page 2-6.

There are five regions to consider during power-up.

RT ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-2 on page 2-5 and Figure 2-3 on page 2-6).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic, at least until VCC and VCCPLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-2 and Figure 2-3 on page 2-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the V_{CC} brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *Radiation-Tolerant ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

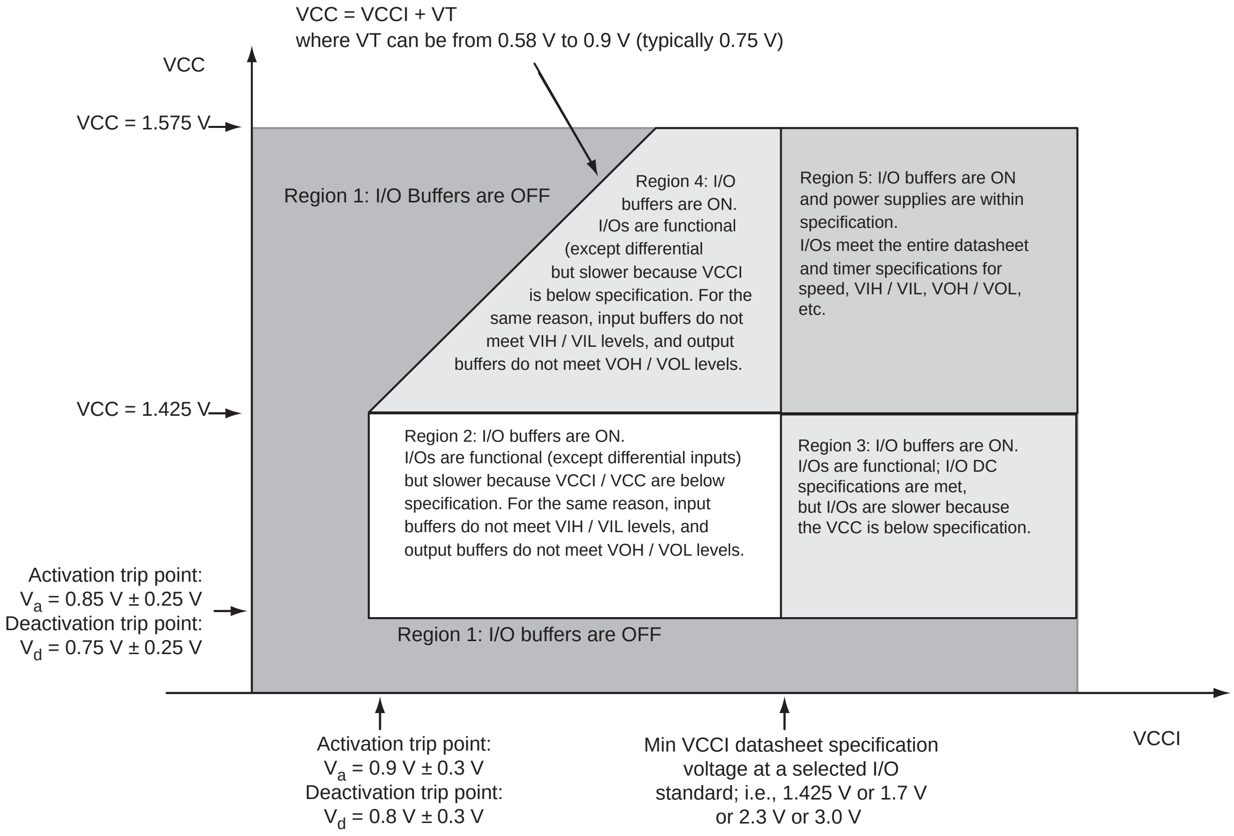


Figure 2-2 • **Devices Operating at 1.5 V Core Voltage – I/O State as a Function of VCCI and VCC Voltage Levels**

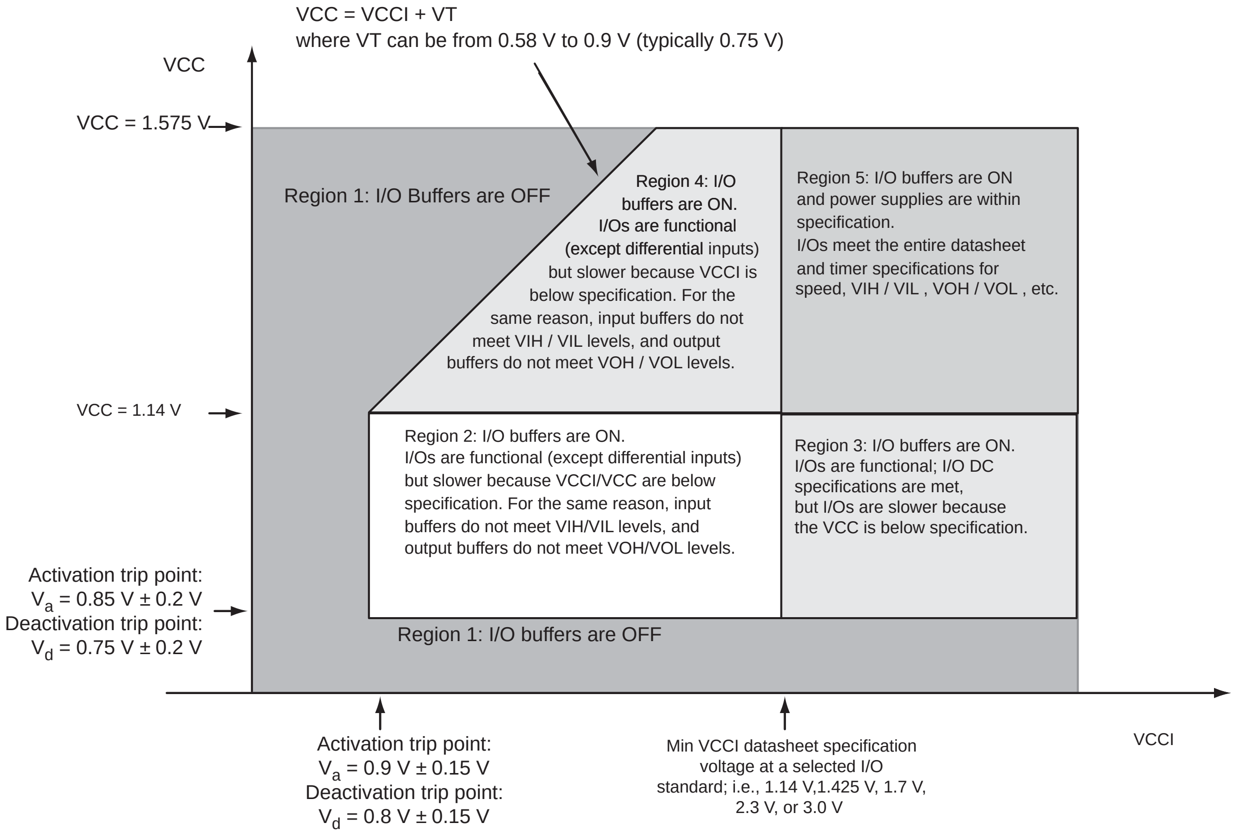


Figure 2-3 • **Devices Operating at 1.2 V Core Voltage – I/O State as a Function of VCCI and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Libero SoC software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \text{EQ 1}$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-4.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The recommended maximum junction temperature is 125°C. EQ 2 shows a sample calculation of the recommended maximum power dissipation allowed for a 484-pin CCGA package with the junction at 125°C and with the case temperature maintained at 70°C.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°\text{C}) - \text{Max. case temp. } (°\text{C})}{\theta_{jc}(°\text{C/W})} \qquad \text{EQ 2}$$

Table 2-4 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jb}	θ_{jc}	θ_{ja}			Units
					Still Air	200 ft./min.	500 ft./min.	
Ceramic Column Grid Array (CCGA)	RT3PE600L	484	TBD	TBD	TBD	TBD	TBD	C/W
	RT3PE3000L	484	TBD	TBD	TBD	TBD	TBD	C/W
	RT3PE3000L	896	3.5	2.8	11.9	TBD	TBD	C/W

Temperature and Voltage Derating Factors

Table 2-5 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 125°C, VCC = 1.14 V)**

	Junction Temperature						
Array Voltage VCC (V)	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
1.14	0.86	0.87	0.90	0.92	0.96	0.97	1.00
1.2	0.82	0.83	0.86	0.88	0.92	0.93	0.96
1.26	0.79	0.80	0.83	0.84	0.88	0.89	0.92
1.3	0.77	0.77	0.80	0.82	0.86	0.87	0.90
1.35	0.74	0.75	0.77	0.79	0.83	0.84	0.86
1.4	0.71	0.72	0.74	0.76	0.79	0.80	0.83
1.425	0.70	0.70	0.73	0.75	0.78	0.79	0.82
1.5	0.66	0.67	0.69	0.71	0.74	0.75	0.77
1.575	0.63	0.64	0.67	0.68	0.71	0.72	0.74

Calculating Power Dissipation

Quiescent Supply Current

Table 2-6 • **Power Supply State per Mode**

Modes/Power Supplies	**Power Supply Configurations[1]**				
	VCC	**VCCPLL**	**VCCI**	**VJTAG**	**VPUMP[2]**
Flash*Freeze[3]	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
Static and Active[3]	On	On	On	On	On/off/floating

Notes:

1. *Off: Power Supply level = 0 V.*
2. *VPUMP should be tied to 0 V to optimize total ionizing dose performance during operation in spaceflight applications.*
3. *Even though the power supply configuration in Flash*Freeze and Static and Active mode is the same, the device's clocks and inputs are shut off in Flash*Freeze mode.*

Table 2-7 • **Quiescent Supply Current (IDD) Characteristics, Flash*Freeze Mode***

	Core Voltage	**RT3PE600L**	**RT3PE3000L**	**Units**
Nominal (25°C)	1.2 V	0.55	2.75	mA
	1.5 V	0.83	4.2	mA
Typical maximum (25°C)	1.2 V	9	17	mA
	1.5 V	12	20	mA
Military maximum (125°C)	1.2 V	65	165	mA
	1.5 V	85	185	mA

*Note: *IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents. Under Flash*Freeze conditions, VCCI, VPUMP. and VCCPLL currents are negligible. Values do not include I/O static contribution (PDC6 and PDC7).*

Table 2-8 • **Quiescent Supply Current (IDD) Characteristics, Sleep Mode (VCC = 0 V)***

	Core Voltage	**RT3PE600L**	**RT3PE3000L**	**Units**
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	µA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	µA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	µA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	µA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	µA

Note: IDD = N_{BANKS} × ICCI. Values do not include I/O static contribution (PDC6 and PDC7), which is shown in Table 2-15 on page 2-13.

Table 2-9 • Quiescent Supply Current (IDD) Characteristics Shutdown Mode

	Core Voltage	RT3PE600L	RT3PE3000L	Units
Nominal (25℃)	1.2 V / 1.5 V	0		µA
Military (125ºC)	1.2 V / 1.5 V	0		µA

Table 2-10 • Quiescent Supply Current (IDD), Static Mode and Active Mode[1]

	Core Voltage	RT3PE600L	RT3PE3000L	Units
ICCA Current[2]				
Nominal (25℃)	1.2 V	0.55	2.75	mA
	1.5 V	0.83	4.2	mA
Typical maximum (25℃)	1.2 V	9	17	mA
	1.5 V	12	20	mA
Military maximum (125℃)	1.2 V	65	165	mA
	1.5 V	85	185	mA
ICCI or IJTAG Current[3]				
VCCI / VJTAG = 1.2 V (per bank) Typical (25℃)	1.2 V	1.7	1.7	µA
VCCI / VJTAG = 1.5 V (per bank) Typical (25℃)	1.2 V / 1.5 V	1.8	1.8	µA
VCCI / VJTAG = 1.8 V (per bank) Typical (25℃)	1.2 V / 1.5 V	1.9	1.9	µA
VCCI / VJTAG = 2.5 V (per bank) Typical (25℃)	1.2 V / 1.5 V	2.2	2.2	µA
VCCI / VJTAG = 3.3 V (per bank) Typical (25℃)	1.2 V / 1.5 V	2.5	2.5	µA

Notes:

1. *IDD = NBANKS × ICCI + ICCA. JTAG counts as one bank when powered.*
2. *Includes VCC , VCCPLL, and VPUMP currents. VPUMP and VCCPLL currents are negligible.*
3. *Values do not include I/O static contribution (PDC6 and PDC7).*

Power per I/O Pin

Table 2-11 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
3.3 V LVCMOS Wide Range	3.3	–	16.34
3.3 V LVCMOS – Schmitt trigger Wide Range	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS[3]	1.2	–	0.60
1.2 V LVCMOS (JESD8-11) – Schmitt trigger[3]	1.2	–	0.53
1.2 V LVCMOS Wide Range[3]	1.2	–	0.60
1.2 V LVCMOS Schmitt trigger Wide Range[3]	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.14
2.5 V GTL	2.5	2.13	3.54
3.3 V GTL+	3.3	2.81	2.91
2.5 V GTL+	2.5	2.57	2.61
HSTL (I)	1.5	0.17	0.79
HSTL (II)	1.5	0.17	0.79
SSTL2 (I)	2.5	1.38	3.26
SSTL2 (II)	2.5	1.38	3.26
SSTL3 (I)	3.3	3.21	7.97
SSTL3 (II)	3.3	3.21	7.97
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.71	1.94

Notes:

1. *PDC6 is the static power measured on VCCI for voltage referenced and differential I/O standards. Single-ended I/O standards do not have the PDC6 static component. Refer to the "Power Calculation Methodology" section on page 2-13 for details on how to calculate total static and dynamic power.*
2. *PAC9 is the total dynamic power measured on VCCI.*
3. *Applicable to RT ProASIC3 devices operating at VCC = 1.2 V and VCCI ≥ VCC.*

Table 2-12 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings**[1]

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	5	3.3	–	148.00
3.3 V LVCMOS Wide Range	5	3.3	–	148.00
2.5 V LVCMOS	5	2.5	–	83.23
1.8 V LVCMOS	5	1.8	–	54.58
1.5 V LVCMOS (JESD8-11)	5	1.5	–	37.05
1.2 V LVCMOS	5	1.2	–	17.94
1.2 V LVCMOS Wide Range	5	1.2	–	17.94
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.18
SSTL2 (I)	30	2.5	16.69	105.65
SSTL2 (II)	30	2.5	25.91	116.48
SSTL3 (I)	30	3.3	26.02	114.67
SSTL3 (II)	30	3.3	42.21	131.69
Differential				
LVDS	–	2.5	7.70	89.58
LVPECL	–	3.3	19.42	167.86

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC7 is the static power measured on VCCI for voltage referenced and differential I/O standards. Single-ended I/O standards do not have the PDC7 static component. Refer to the "Power Calculation Methodology" section on page 2-13 for details on how to calculate total static and dynamic power.*
3. *PAC10 is the total dynamic power measured on VCCI.*

Power Consumption of Various Internal Resources

Table 2-13 • **Different Components Contributing to Dynamic Power Consumption in Devices Operating at 1.2 V VCC**

Parameter	Definition	Device-Specific Dynamic Power (µW/MHz)	
		RT3PE3000L	RT3PE600L
PAC1	Clock contribution of a Global Rib	8.34	3.99
PAC2	Clock contribution of a Global Spine	4.28	2.22
PAC3	Clock contribution of a VersaTile row	0.94	0.94
PAC4	Clock contribution of a VersaTile used as a sequential module	0.08	0.08
PAC5	First contribution of a VersaTile used as a sequential module	0.05	
PAC6	Second contribution of a VersaTile used as a sequential module	0.19	
PAC7	Contribution of a VersaTile used as a combinatorial module	0.11	
PAC8	Average contribution of a routing net	0.45	
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-11 on page 2-10.	
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-12 on page 2-11.	
PAC11	Average contribution of a RAM block during a read operation	25.00	
PAC12	Average contribution of a RAM block during a write operation	30.00	
PAC13	Dynamic contribution for PLL	1.74	

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in the Libero SoC software.

Table 2-14 • **Different Components Contributing to Dynamic Power Consumption in RT ProASIC3 Devices at 1.5 V VCC**

Parameter	Definition	Device-Specific Dynamic Power (µW/MHz)	
		RT3PE3000L	RT3PE600L
PAC1	Clock contribution of a Global Rib	13.03	6.24
PAC2	Clock contribution of a Global Spine	6.69	3.47
PAC3	Clock contribution of a VersaTile row	1.46	1.46
PAC4	Clock contribution of a VersaTile used as a sequential module	0.13	0.13
PAC5	First contribution of a VersaTile used as a sequential module	0.07	
PAC6	Second contribution of a VersaTile used as a sequential module	0.29	
PAC7	Contribution of a VersaTile used as a combinatorial module	0.29	
PAC8	Average contribution of a routing net	0.70	
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-11 on page 2-10.	
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-12 on page 2-11.	
PAC11	Average contribution of a RAM block during a read operation	25.00	
PAC12	Average contribution of a RAM block during a write operation	30.00	
PAC13	Dynamic contribution for PLL	2.60	

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in the Libero SoC software.

Table 2-15 • Different Components Contributing to the Static Power Consumption in RT ProASIC3 Devices

Parameter	Definition	Device-Specific Dynamic Power (µW)
PDC0	Array static power in Sleep mode	0 mW
PDC1	Array static power in Active mode	See Table 2-10 on page 2-9.
PDC2	Array static power in Static (Idle) mode	See Table 2-10 on page 2-9.
PDC3	Array static power in Flash*Freeze mode	See Table 2-7 on page 2-8.
PDC4	Static PLL contribution at 1.2 V operating core voltage	1.42 mW
	Static PLL contribution 1.5 V operating core voltage	2.55 mW
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-7 on page 2-8, Table 2-8 on page 2-8, Table 2-10 on page 2-9.
PDC6	I/O input pin static power (standard-dependent)	See Table 2-11 on page 2-10.
PDC7	I/O output pin static power (standard-dependent)	See Table 2-12 on page 2-11.

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-16 on page 2-15.
- Enable rates of output buffers—guidelinesare provided for typical applications in Table 2-17 on page 2-15.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-17 on page 2-15. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

P_{STAT} = (PDC0 or PDC1 or PDC2 or PDC3) + N_{BANKS} * PDC5 + N_{INPUTS}* PDC6 + $N_{OUTPUTS}$* PDC7

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *RT ProASIC3 FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in "Spine Architecture" section of the Global Resources chapter in the *RT ProASIC3 FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-16 on page 2-15.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-16 on page 2-15.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-16 on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-16 on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-16 on page 2-15.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-17 on page 2-15.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-17 on page 2-15.

PLL Contribution—P_{PLL}

$P_{PLL} = PDC4 + PAC1_3 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-16 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-17 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

---

[1] *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

User I/O Characteristics

Timing Model

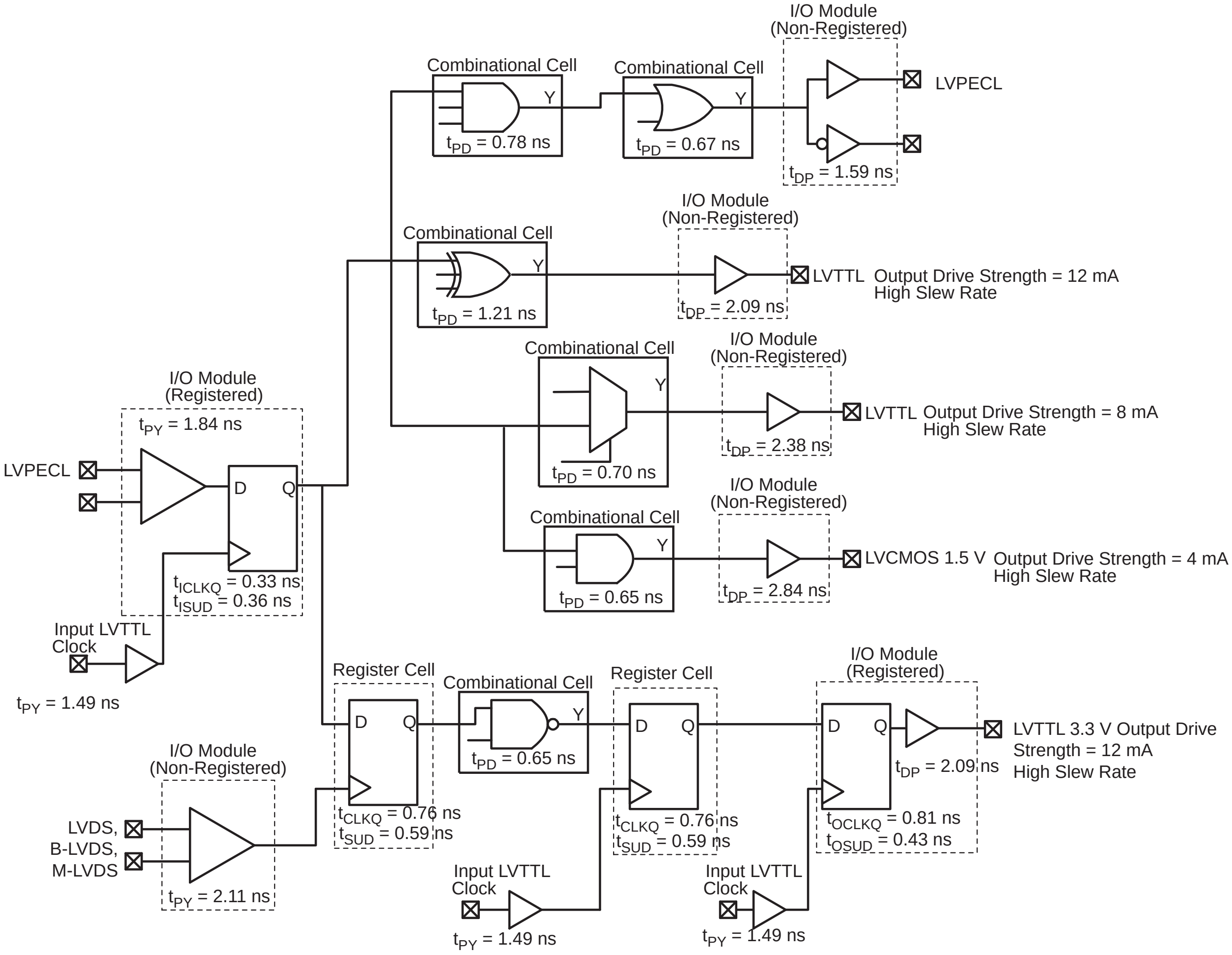


Figure 2-4 • **Timing Model**
Operating Conditions: –1 Speed, Military Temperature Range (T_J = 125°C), Worst-Case VCC = 1.14 V (example for RT3PE3000L and RT3PE600L)

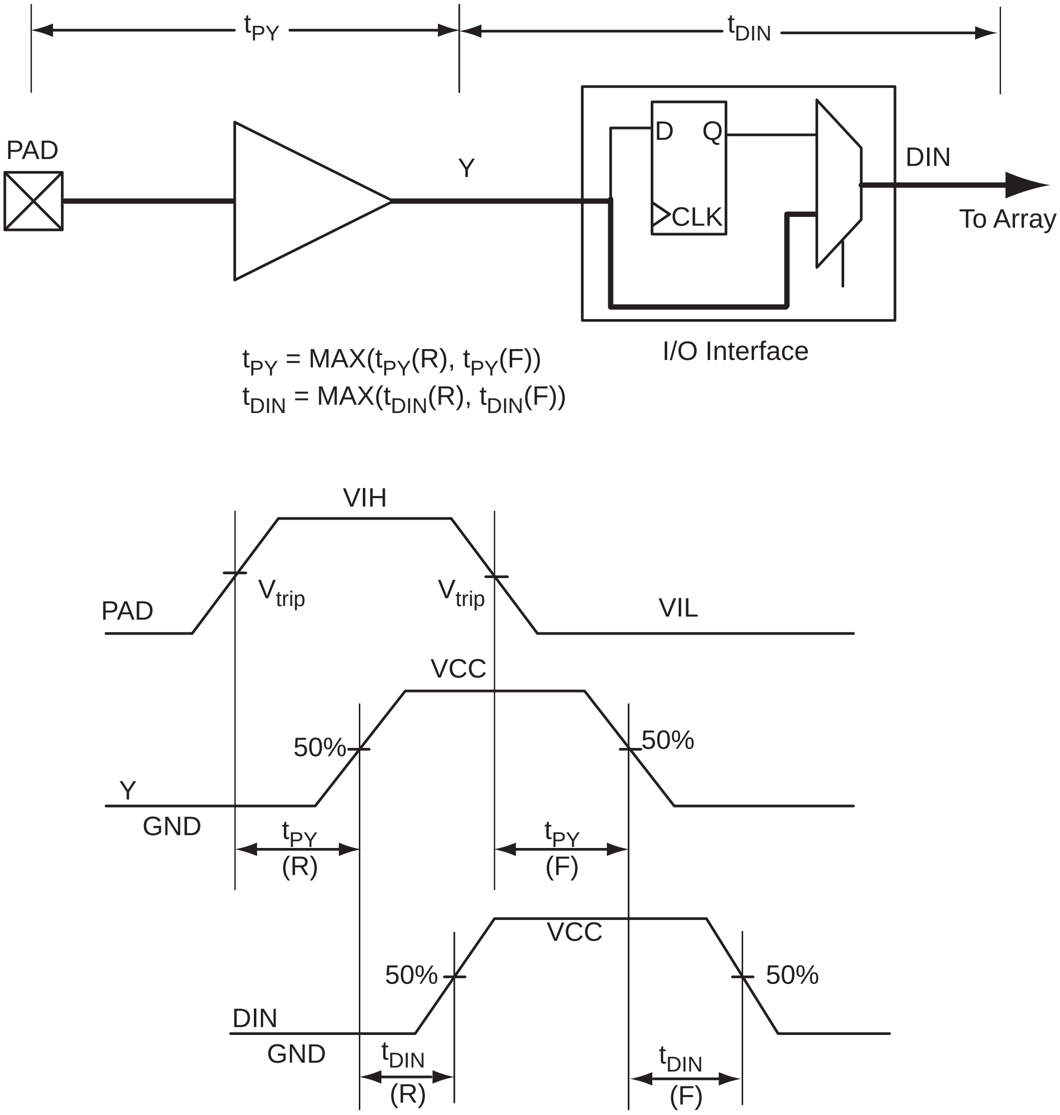


Figure 2-5 • **Input Buffer Timing Model and Delays (example)**

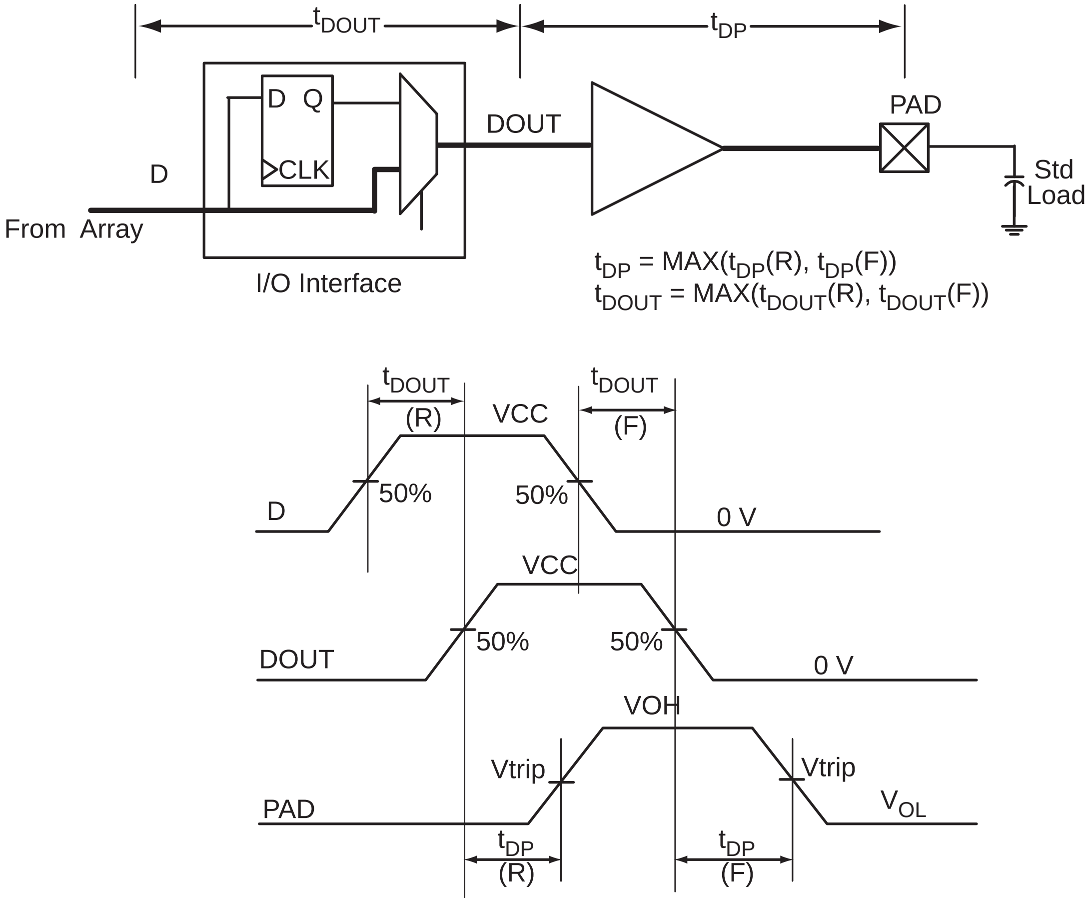


Figure 2-6 • **Output Buffer Model and Delays (example)**

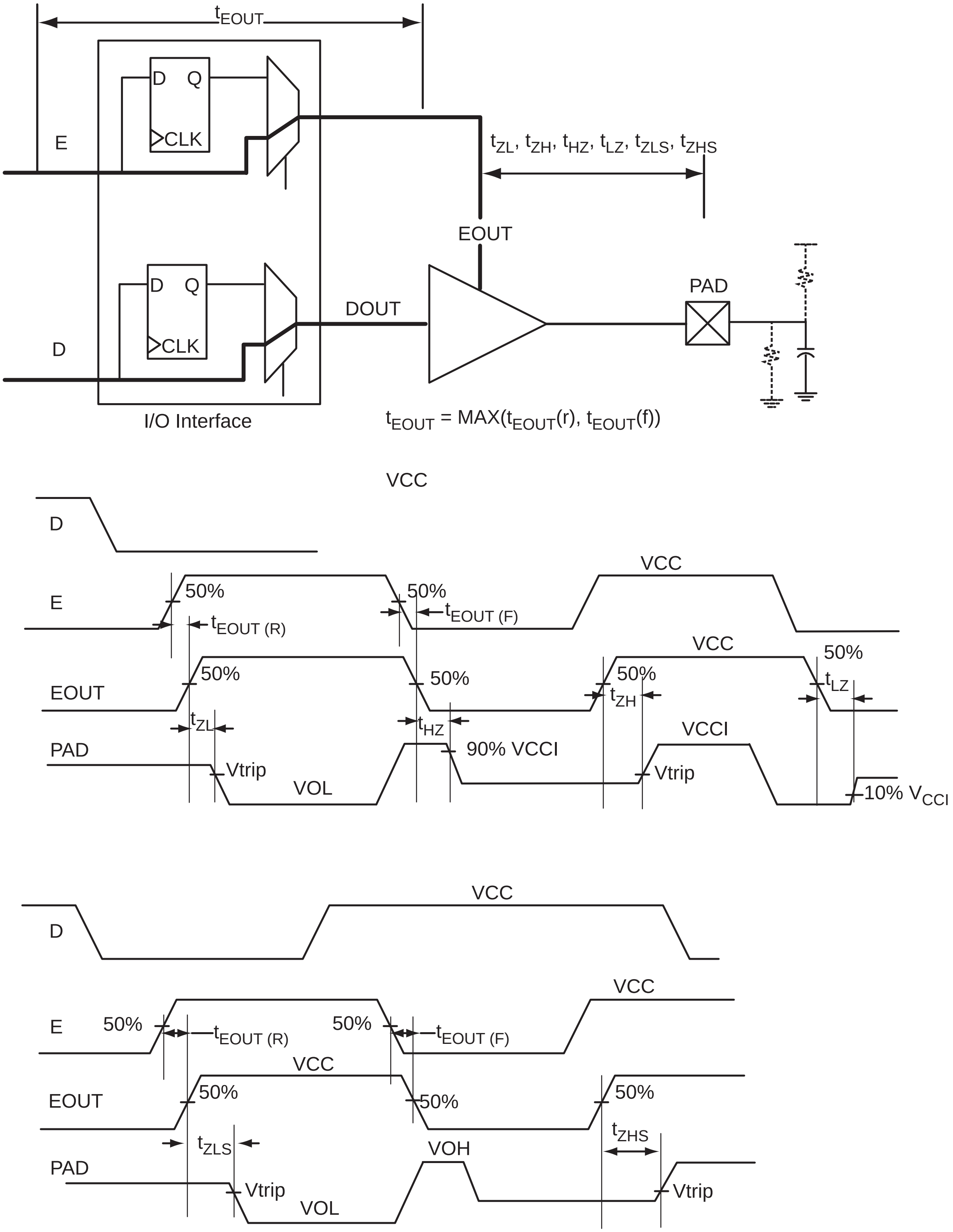


Figure 2-7 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-18 • Summary of Maximum and Minimum DC Output Levels Software Default Settings

I/O Standard	Drive Strgth.	Equiv. Software Default Drive Strength Option[1] (mA)	Slew Rate	VOL		VOH		IOL	IOH
				Max. V		Min. V		mA	mA
				–55 ≤ T_J ≤ 100 (℃)	100 < T_J ≤ 125 (℃)	–55 ≤ T_J ≤ 100 (℃)	100 < T_J ≤ 125 (℃)	–55 ≤ T_J ≤ 125 (℃)	
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12	High	0.4	0.4	2.4	2.4	12	12
3.3 V LVCMOS Wide Range[1,2]	100 µA	12	High	0.2	0.2	VCCI – 0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12	High	0.7	0.7	1.7	1.7	12	12
1.8 V LVCMOS	12 mA	12	High	0.45	0.45	VCCI – 0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12	High	0.25 * VCCI	0.25 * VCCI	0.75 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS[3,4]	2 mA	2	High	0.25 * VCCI	0.25 * VCCI	0.75 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[1,3,4]	100 µA	2	High	0.1	0.1	VCCI – 0.1	VCCI – 0.1	0.1	0.1
3.3 V PCI	Per PCI Specification								
3.3 V PCI-X	Per PCI-X Specification								
3.3 V GTL	20[5]	20[5]	High	0.4	0.5	–	–	20	20
2.5 V GTL	20[5]	20[5]	High	0.4	0.5	–	–	20	20
3.3 V GTL+	35	35	High	0.6	0.75	–	–	35	35
2.5 V GTL+	33	33	High	0.6	0.75	–	–	33	33
HSTL (I)	8	8	High	0.4	0.4	VCCI – 0.4	VCCI – 0.4	8	8
HSTL (II)	15[5]	15[5]	High	0.4	0.5	VCCI – 0.4	VCCI – 0.5	15	15
SSTL2 (I)	15	15	High	0.54	0.54	VCCI – 0.62	VCCI – 0.62	15	15
SSTL2 (II)	18	18	High	0.35	0.44	VCCI – 0.43	VCCI – 0.43	18	18
SSTL3 (I)	14	14	High	0.7	0.7	VCCI – 1.1	VCCI – 1.1	14	14
SSTL3 (II)	21	21	High	0.5	0.625	VCCI – 0.9	VCCI – 0.9	21	21

Notes:

1. *The minimum drive strength for any 1.2 V LVCMOS or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *Applicable to RT ProASIC3 devices operating at VCC = 1.2 V and VCCI ≥ VCC.*
4. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
5. *Output drive strength is below JEDEC specification.*
6. *Output slew rate can be extracted using the IBIS models.*

Table 2-19 • **Summary of Maximum and Minimum DC Input Levels
Software Default Settings**

	VIL		**VIH**		**IIL**[1]	**IIH**[2]
I/O Standard	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**µA**	**µA**
	$-55 \le T_J \le 125$ (℃)		$-55 \le T_J \le 125$ (℃)		$-55 \le T_J \le 125$ (℃)	
3.3 V LVTTL / 3.3 V LVCMOS	–0.3	0.8	2	3.6	15	15
3.3 V LVCMOS Wide Range	–0.3	0.8	2	3.6	15	15
2.5 V LVCMOS	–0.3	0.7	1.7	3.6	15	15
1.8 V LVCMOS	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	15	15
1.5 V LVCMOS	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	15	15
1.2 V LVCMOS[3]	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	15	15
1.2 V LVCMOS Wide Range[3]	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	15	15
3.3 V PCI	Per PCI Specification					
3.3 V PCI-X	Per PCI-X Specification					
3.3 V GTL	–0.3	VREF – 0.05	VREF + 0.05	3.6	15	15
2.5 V GTL	–0.3	VREF – 0.05	VREF + 0.05	3.6	15	15
3.3 V GTL+	–0.3	VREF – 0.1	VREF + 0.1	3.6	15	15
2.5 V GTL+	–0.3	VREF – 0.1	VREF + 0.1	3.6	15	15
HSTL (I)	–0.3	VREF – 0.1	VREF + 0.1	3.6	15	15
HSTL (II)	–0.3	VREF – 0.1	VREF + 0.1	3.6	15	15
SSTL2 (I)	–0.3	VREF – 0.2	VREF + 0.2	3.6	15	15
SSTL2 (II)	–0.3	VREF – 0.2	VREF + 0.2	3.6	15	15
SSTL3 (I)	–0.3	VREF – 0.2	VREF + 0.2	3.6	15	15
SSTL3 (II)	–0.3	VREF – 0.2	VREF + 0.2	3.6	15	15

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Applicable to RT ProASIC3 devices operating at VCC = 1.2 V core voltage and VCCI ≥ VCC.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-20 • **Summary of AC Measuring Points***

Standard	Input/Output Supply Voltage	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	3.3 V	–	–	1.4 V
3.3 V LVCMOS Wide Range	3.3 V	–		1.4 V
2.5 V LVCMOS	2.5 V	–	–	1.2 V
1.8 V LVCMOS	1.8 V	–	–	0.90 V
1.5 V LVCMOS	1.5 V	–	–	0.75 V
1.2 V LVCMOS*	1.2 V	–	–	0.6V
1.2 V LVCMOS – Wide Range*	1.2 V	–	–	0.6 V
3.3 V PCI	3.3 V	–	–	0.285 * VCCI (RR)
		–	–	0.615 * VCCI (FF))
3.3 V PCI-X	3.3 V	–	–	0.285 * VCCI (RR)
		–	–	0.615 * VCCI (FF)
3.3 V GTL	3.3 V	0.8 V	1.2 V	VREF
2.5 V GTL	2.5 V	0.8 V	1.2 V	VREF
3.3 V GTL+	3.3 V	1.0 V	1.5 V	VREF
2.5 V GTL+	2.5 V	1.0 V	1.5 V	VREF
HSTL (I)	1.5 V	0.75 V	0.75 V	VREF
HSTL (II)	1.5 V	0.75 V	0.75 V	VREF
SSTL2 (I)	2.5 V	1.25 V	1.25 V	VREF
SSTL2 (II)	2.5 V	1.25 V	1.25 V	VREF
SSTL3 (I)	3.3 V	1.5 V	1.485 V	VREF
SSTL3 (II)	3.3 V	1.5 V	1.485 V	VREF
LVDS	2.5 V	–	–	Cross point
LVPECL	3.3 V	–	–	Cross point

*Note: *Applicable to RT ProASIC3 devices operating at 1.2 V core voltage only*

Table 2-21 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

1.2 V Core Operating Voltage

Table 2-22 • **Summary of I/O Timing Characteristics—Software Default Settings**
–1 Speed Grade, Military-Case Conditions: T_J = 125°C, Worst Case VCC = 1.14 V, Worst Case VCCI

Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.09	0.05	1.49	2.03	0.44	2.12	1.56	2.76	3.06	3.99	3.43
3.3 V LVCMOS Wide Range[2]	100 µA	12 mA	High	5	–	0.68	3.01	0.05	1.86	2.69	0.44	3.01	2.22	4.03	4.42	4.89	4.09
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.12	0.05	1.73	2.17	0.44	2.15	1.74	2.84	2.95	4.03	3.62
1.8 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.36	0.05	1.70	2.40	0.44	2.40	1.94	3.16	3.58	4.27	3.81
1.5 V LVCMOS	12 mA	12 mA	High	5	–	0.68	2.71	0.05	1.86	2.61	0.44	2.76	2.24	3.34	3.69	4.63	4.12
1.2 V LVCMOS	2 mA	2 mA	High	5	–	0.68	4.39	0.05	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61
1.2 V LVCMOS Wide Range[3]	100 µA	2 mA	High	5	–	0.68	4.39	0.05	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61
3.3 V PCI	Per PCI spec	–	High	10	25[4]	0.68	2.37	0.05	2.31	3.13	0.44	2.40	1.68	2.77	3.06	4.28	3.56
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[4]	0.68	2.37	0.05	2.31	3.13	0.44	2.40	1.68	2.77	3.06	4.28	3.56
3.3 V GTL	20 mA[5]	20 mA[5]	High	10	25	0.68	1.75	0.05	1.99	–	0.44	1.71	1.75	–	–	3.59	3.62
2.5 V GTL	20 mA[5]	20 mA[5]	High	10	25	0.68	1.79	0.05	1.93	–	0.44	1.82	1.79	–	–	3.70	3.67
3.3 V GTL+	35 mA	35 mA	High	10	25	0.68	1.74	0.05	1.99	–	0.44	1.76	1.73	–	–	3.64	3.61
2.5 V GTL+	33 mA	33 mA	High	10	25	0.68	1.86	0.05	1.93	–	0.44	1.89	1.77	–	–	3.77	3.64
HSTL (I)	8 mA	8 mA	High	20	25	0.68	2.68	0.05	2.34	–	0.44	2.73	2.65	–	–	4.60	4.52
HSTL (II)	15 mA[5]	15 mA[5]	High	20	50	0.68	2.55	0.05	2.34	–	0.44	2.59	2.28	–	–	4.47	4.16
SSTL2 (I)	15 mA	15 mA	High	30	25	0.68	1.80	0.05	1.78	–	0.44	1.82	1.55	–	–	1.82	1.55
SSTL2 (II)	18 mA	18 mA	High	30	50	0.68	1.83	0.05	1.78	–	0.44	1.86	1.49	–	–	1.86	1.49
SSTL3 (I)	14 mA	14 mA	High	30	25	0.68	1.95	0.05	1.71	–	0.44	1.98	1.55	–	–	1.98	1.55
SSTL3 (II)	21 mA	21 mA	High	30	50	0.68	1.75	0.05	1.71	–	0.44	1.77	1.41	–	–	1.77	1.41
LVDS	24 mA	–	High	–	–	0.68	1.59	0.05	2.11	–	–	–	–	–	–	–	–
LVPECL	24 mA	–	High	–	–	0.68	1.51	0.05	1.84	–	–	–	–	–	–	–	–

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-13 on page 2-48 for connectivity. This resistor is not required during normal operation.*
5. *Output drive strength is below JEDEC specification.*
6. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.5 V Core Voltage

Table 2-23 • **Summary of I/O Timing Characteristics—Software Default Settings**
–1 Speed Grade, Military-Case Conditions: T_J = 125℃, VCC = 1.425 V, Worst Case VCCI

Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	0.52	1.97	0.03	1.23	1.78	0.34	1.99	1.46	2.63	2.89	3.23	2.71
3.3 V LVCMOS Wide Range[2]	100 µA	12 mA	High	5	–	0.52	2.89	0.03	1.61	2.44	0.34	2.88	2.12	3.89	4.25	4.12	3.36
2.5 V LVCMOS	12 mA	12 mA	High	5	–	0.52	2.01	0.03	1.49	1.93	0.34	2.02	1.65	2.71	2.78	3.27	2.89
1.8 V LVCMOS	12 mA	12 mA	High	5	–	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08
1.5 V LVCMOS	12 mA	12 mA	High	5	–	0.52	2.60	0.03	1.60	2.35	0.34	2.62	2.14	3.21	3.52	3.87	3.39
3.3 V PCI	Per PCI spec	–	High	10	25[3]	0.52	2.25	0.03	2.03	2.88	0.34	2.27	1.58	2.64	2.89	3.52	2.83
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[3]	0.52	2.25	0.03	2.03	2.88	0.34	2.27	1.58	2.64	2.89	3.52	2.83
3.3 V GTL	20 mA[4]	20 mA[4]	High	10	25	0.52	1.68	0.03	1.79	–	0.34	1.58	1.68	–	–	2.83	2.92
2.5 V GTL	20 mA[4]	20 mA[4]	High	10	25	0.52	1.72	0.03	1.73	–	0.34	1.69	1.72	–	–	2.93	2.97
3.3 V GTL+	35 mA	35 mA	High	10	25	0.52	1.66	0.03	1.79	–	0.34	1.63	1.66	–	–	2.88	2.90
2.5 V GTL+	33 mA	33 mA	High	10	25	0.52	1.75	0.03	1.73	–	0.34	1.76	1.69	–	–	3.00	2.94
HSTL (I)	8 mA	8 mA	High	20	25	0.52	2.57	0.03	2.14	–	0.34	2.59	2.55	–	–	3.84	3.79
HSTL (II)	15 mA[4]	15 mA[4]	High	20	50	0.52	2.44	0.03	2.14	–	0.34	2.46	2.19	–	–	3.71	3.43
SSTL2 (I)	15 mA	15 mA	High	30	25	0.52	1.68	0.03	1.58	–	0.34	1.69	1.46	–	–	1.69	1.46
SSTL2 (II)	18 mA	18 mA	High	30	50	0.52	1.72	0.03	1.58	–	0.34	1.73	1.39	–	–	1.73	1.39
SSTL3 (I)	14 mA	14 mA	High	30	25	0.52	1.83	0.03	1.51	–	0.34	1.84	1.45	–	–	1.84	1.45
SSTL3 (II)	21 mA	21 mA	High	30	50	0.52	1.63	0.03	1.51	–	0.34	1.64	1.31	–	–	1.64	1.31
LVDS	24 mA	–	High	–	–	0.52	1.75	0.04	2.18	–	–	–	–	–	–	–	–
LVPECL	24 mA	–	High	–	–	0.52	1.65	0.04	1.89	–	–	–	–	–	–	–	–

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-13 on page 2-48 for connectivity. This resistor is not required during normal operation.*
4. *Output drive strength is below JEDEC specification.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

Detailed I/O DC Characteristics

Table 2-24 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 2-25 • **I/O Output Buffer Maximum Resistances**[1]

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS[4]	2 mA	158	158
1.2 V LVCMOS Wide Range[4]	100 µA	158	158
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA[5]	11	–
2.5 V GTL	20 mA[5]	14	–
3.3 V GTL+	35 mA	12	–

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models posted at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)}$ *= (VOLspec) / IOLspec*
3. $R_{(PULL\text{-}UP\text{-}MAX)}$ *= (VCCImax – VOHspec) / IOHspec*
4. *Applicable to RT ProASIC3 devices operating at 1.2 V core voltage only.*
5. *Output drive strength is below JEDEC specification.*

Table 2-25 • I/O Output Buffer Maximum Resistances[1] (continued)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA[5]	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models posted at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)}$ *= (VOLspec) / IOLspec*
3. $R_{(PULL\text{-}UP\text{-}MAX)}$ *= (VCCImax – VOHspec) / IOHspec*
4. *Applicable to RT ProASIC3 devices operating at 1.2 V core voltage only.*
5. *Output drive strength is below JEDEC specification.*

Table 2-26 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	95 k	13 k	45 k
3.3 V (wide range I/Os)	10 k	95 k	13 k	45 k
2.5 V	11 k	100 k	17 k	74 k
1.8 V	19 k	85 k	23 k	110 k
1.5 V	20 k	120 k	17 k	156 k
1.2 V	30 k	450 k	25 k	300 k
1.2 V (wide range I/Os)	20 k	450 k	17 k	300 k

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)}$ *= (VCCImax – VOHspec) /* $I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)}$ *= VOLspec /* $I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

Table 2-27 • I/O Short Currents IOSH/IOSL

	Drive Strength	IOSH (mA)[1]	IOSL (mA)[1]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	TBD	TBD
1. V LVCMOS Wide Range	100 µA	TBD	TBD
3.3 V PCI/PCIX	Per PCI/PCI-X Specification	Per PCI Curves	
3.3 V GTL	20 mA[2]	268	181
2.5 V GTL	20 mA[2]	169	124
3.3 V GTL+	35 mA	268	181
2.5 V GTL+	33 mA	169	124
HSTL (I)	8 mA	32	39
HSTL (II)	15 mA	66	55
SSTL2 (I)	15 mA	83	87
SSTL2 (II)	18 mA[2]	169	124
SSTL3 (I)	14 mA	51	54
SSTL3 (II)	21 mA	103	109

Notes:

1. *T_J = 100°C*
2. *Output drive strength is below JEDEC specification.*

Table 2-28 • **Schmitt Trigger Input Hysteresis, Hysteresis Voltage Value (typical) for Schmitt Mode Input Buffers Applicable**

Input Buffer Configuration	Hysteresis Value (typical)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110℃, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-29 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–55ºC	> 20 years
–40℃	> 20 years
0℃	> 20 years
25℃	> 20 years
70℃	5 years
85℃	2 years
100℃	6 months
110℃	3 months
125℃	1 month

Table 2-30 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110℃)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100℃)

Note: **The maximum input rise/fall time is related to the noise induced in the input buffer trace. If the noise is low, the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-31 • Minimum and Maximum DC Output Levels 3.3 V LVTTL / 3.3 V LVCMOS

Drive Strgth.	VOL		VOH		IOL	IOH	IOSH	IOSL
	Max. V		Min. V		mA	mA	Max. mA	Max. mA
	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 100$ (ºC)	
4 mA	0.4	0.4	2.4	2.4	4	4	25	27
8 mA	0.4	0.4	2.4	2.4	8	8	51	54
12 mA	0.4	0.4	2.4	2.4	12	12	103	109
16 mA	0.4	0.5	2.4	2.4	16	16	132	127
24 mA	0.4	0.5	2.4	2.4	24	24	268	181

Note: Software default selection highlighted in gray.

Table 2-32 • Minimum and Maximum DC Input Levels 3.3 V LVTTL / 3.3 V LCMOS

VIL		VIH		IIL[1]	IIH[2]
Min. V	Max. V	Min. V	Max. V	µA	µA
$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)	
–0.3	0.8	2	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

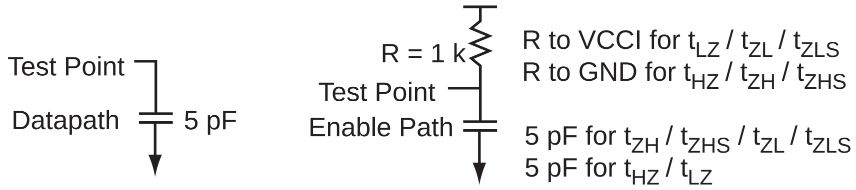


Figure 2-8 • AC Loading

Table 2-33 • 3.3 V LVTTL/LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	5

*Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-34 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	6.04	0.05	1.75	2.38	0.52	6.14	4.84	2.68	2.43	8.35	7.05	ns
	–1	0.68	5.13	0.05	1.49	2.03	0.44	5.22	4.12	2.28	2.07	7.10	6.00	ns
8 mA	Std.	0.80	4.93	0.05	1.75	2.38	0.52	5.02	4.14	3.02	3.05	7.22	6.34	ns
	–1	0.68	4.20	0.05	1.49	2.03	0.44	4.27	3.52	2.57	2.59	6.14	5.40	ns
12 mA	Std.	0.80	4.15	0.05	1.75	2.38	0.52	4.22	3.61	3.25	3.43	6.43	5.81	ns
	–1	0.68	3.53	0.05	1.49	2.03	0.44	3.59	3.07	2.76	2.92	5.47	4.95	ns
16 mA	Std.	0.80	3.93	0.05	1.75	2.38	0.52	3.99	3.49	3.29	3.54	6.20	5.70	ns
	–1	0.68	3.34	0.05	1.49	2.03	0.44	3.40	2.97	2.80	3.01	5.27	4.85	ns
24 mA	Std.	0.80	3.81	0.05	1.75	2.38	0.52	3.87	3.51	3.36	3.94	6.08	5.71	ns
	–1	0.68	3.24	0.05	1.49	2.03	0.44	3.30	2.98	2.86	3.35	5.17	4.86	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-35 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	3.40	0.05	1.75	2.38	0.52	3.45	2.60	2.68	2.58	5.66	4.81	ns
	–1	0.68	2.89	0.05	1.49	2.03	0.44	2.94	2.21	2.28	2.19	4.81	4.09	ns
8 mA	Std.	0.80	2.79	0.05	1.74	2.38	0.52	2.84	2.08	3.02	3.19	5.04	4.29	ns
	–1	0.68	2.38	0.05	1.49	2.03	0.44	2.41	1.77	2.57	2.72	4.29	3.65	ns
12 mA	Std.	0.80	2.45	0.05	1.75	2.38	0.52	2.49	1.83	3.25	3.59	4.70	4.04	ns
	–1	0.68	2.09	0.05	1.49	2.03	0.44	2.12	1.56	2.76	3.06	3.99	3.43	ns
16 mA	Std.	0.80	2.40	0.05	1.75	2.38	0.52	2.43	1.79	3.30	3.70	4.64	3.99	ns
	–1	0.68	2.04	0.05	1.49	2.03	0.44	2.07	1.52	2.81	3.15	3.95	3.40	ns
24 mA	Std.	0.80	2.42	0.05	1.75	2.38	0.52	2.46	1.72	3.37	4.10	4.66	3.93	ns
	–1	0.68	2.06	0.05	1.49	2.03	0.44	2.09	1.47	2.86	3.49	3.97	3.34	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.5 V DC Core Voltage

Table 2-36 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.61	5.90	0.04	1.45	2.09	0.40	5.98	4.73	2.52	2.24	7.45	6.19	ns
	–1	0.52	5.02	0.03	1.23	1.78	0.34	5.09	4.02	2.15	1.90	6.34	5.27	ns
8 mA	Std.	0.61	4.80	0.04	1.45	2.09	0.40	4.86	4.02	2.87	2.85	6.32	5.49	ns
	–1	0.52	4.08	0.03	1.23	1.78	0.34	4.13	3.42	2.44	2.43	5.38	4.67	ns
12 mA	Std.	0.61	4.02	0.04	1.45	2.09	0.40	4.06	3.49	3.09	3.23	5.53	4.96	ns
	–1	0.52	3.42	0.03	1.23	1.78	0.34	3.46	2.97	2.63	2.75	4.70	4.22	ns
16 mA	Std.	0.61	3.79	0.04	1.45	2.09	0.40	3.84	3.38	3.14	3.34	5.30	4.84	ns
	–1	0.52	3.23	0.03	1.23	1.78	0.34	3.26	2.87	2.67	2.84	4.51	4.12	ns
24 mA	Std.	0.61	3.67	0.04	1.45	2.09	0.40	3.72	3.39	3.20	3.74	5.18	4.86	ns
	–1	0.52	3.13	0.03	1.23	1.78	0.34	3.16	2.88	2.72	3.18	4.41	4.13	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-37 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.61	3.26	0.04	1.45	2.09	0.40	3.30	2.48	2.52	2.38	4.76	3.95	ns
	–1	0.52	2.77	0.03	1.23	1.78	0.34	2.80	2.11	2.15	2.03	4.05	3.36	ns
8 mA	Std.	0.61	2.66	0.04	1.45	2.09	0.40	2.68	1.97	2.87	3.00	4.15	3.43	ns
	–1	0.52	2.26	0.03	1.23	1.78	0.34	2.28	1.67	2.44	2.55	3.53	2.92	ns
12 mA	Std.	0.61	2.32	0.04	1.45	2.09	0.40	2.33	1.72	3.09	3.40	3.80	3.18	ns
	–1	0.52	1.97	0.03	1.23	1.78	0.34	1.99	1.46	2.63	2.89	3.23	2.71	ns
16 mA	Std.	0.61	2.26	0.04	1.45	2.09	0.40	2.28	1.67	3.15	3.51	3.74	3.14	ns
	–1	0.52	1.92	0.03	1.23	1.78	0.34	1.94	1.42	2.68	2.98	3.18	2.67	ns
24 mA	Std.	0.61	2.28	0.04	1.45	2.09	0.40	2.30	1.61	3.21	3.90	3.77	3.07	ns
	–1	0.52	1.94	0.03	1.23	1.78	0.34	1.96	1.37	2.73	3.32	3.20	2.61	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

3.3 V LVCMOS Wide Range

Table 2-38 • Minimum and Maximum DC Output Levels 3.3 V LVCMOS Wide Range

Drive Strength	Equiv. Software Default Drive Strength Option[1]	VOL	VOH	IOL	IOH	IOSH	IOSL
		Max. V	Min. V	µA	µA	Max. mA	Max. mA
		$-55 \le T_J \le 125$ (ºC)	$-55 \le T_J \le 125$ (ºC)	$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 100$ (ºC)	
100 µA	2 mA	0.2	VCCI – 0.2	100	100	25	27
100 µA	4 mA	0.2	VCCI – 0.2	100	100	25	27
100 µA	6 mA	0.2	VCCI – 0.2	100	100	51	54
100 µA	8 mA	0.2	VCCI – 0.2	100	100	51	54
100 µA	12 mA	0.2	VCCI – 0.2	100	100	103	109
100 µA	16 mA	0.2	VCCI – 0.2	100	100	132	127
100 µA	24 mA	0.2	VCCI – 0.2	100	100	268	181

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-A specification.*
3. *Software default selection highlighted in gray.*

Table 2-39 • Minimum and Maximum DC Input and Output Levels 3.3 V LVCMOS Wide Range

VIL		VIH		I_{IL}[1]	I_{IH}[2]
Min. V	Max. V	Min. V	Max. V	µA	µA
$-55 \le T_J \le 125$		$-55 \le T_J \le 125$		$-55 \le T_J \le 125$	
–0.3	0.8	2	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

Table 2-40 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	5

Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-41 • **3.3 V LVCMOS Wide Range Low Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.80	9.08	0.05	2.18	3.16	0.52	9.08	7.17	3.85	3.40	11.28	9.38	ns
		–1	0.68	7.72	0.05	1.86	2.69	0.44	7.72	6.10	3.28	2.89	9.60	7.98	ns
100 µA	8 mA	Std.	0.80	7.37	0.05	2.18	3.16	0.52	7.37	6.10	4.38	4.35	9.58	8.31	ns
		–1	0.68	6.27	0.05	1.86	2.69	0.44	6.27	5.19	3.73	3.70	8.15	7.07	ns
100 µA	12 mA	Std.	0.80	6.17	0.05	2.18	3.16	0.52	6.17	5.30	4.73	4.94	8.37	7.51	ns
		–1	0.68	5.24	0.05	1.86	2.69	0.44	5.24	4.51	4.03	4.20	7.12	6.38	ns
100 µA	16 mA	Std.	0.80	5.82	0.05	2.18	3.16	0.52	5.82	5.12	4.80	5.11	8.03	7.33	ns
		–1	0.68	4.95	0.05	1.86	2.69	0.44	4.95	4.36	4.09	4.34	6.83	6.23	ns
100 µA	24 mA	Std.	0.80	5.64	0.05	2.18	3.16	0.52	5.64	5.14	4.90	5.72	7.85	7.35	ns
		–1	0.68	4.80	0.05	1.86	2.69	0.44	4.80	4.38	4.17	4.87	6.67	6.25	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

Table 2-42 • **3.3 V LVCMOS Wide Range High Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.80	5.00	0.05	2.18	3.16	0.52	5.00	3.77	3.85	3.62	7.21	5.97	ns
		–1	0.68	4.25	0.05	1.86	2.69	0.44	4.25	3.21	3.28	3.08	6.13	5.08	ns
100 µA	8 mA	Std.	0.80	4.07	0.05	2.18	3.16	0.52	4.07	2.98	4.38	4.57	6.27	5.19	ns
		–1	0.68	3.46	0.05	1.86	2.69	0.44	3.46	2.54	3.73	3.89	5.33	4.41	ns
100 µA	12 mA	Std.	0.80	3.54	0.05	2.18	3.16	0.52	3.54	2.60	4.73	5.19	5.74	4.81	ns
		–1	0.68	3.01	0.05	1.86	2.69	0.44	3.01	2.22	4.03	4.42	4.89	4.09	ns
100 µA	16 mA	Std.	0.80	3.45	0.05	2.18	3.16	0.52	3.45	2.54	4.82	5.36	5.66	4.74	ns
		–1	0.68	2.94	0.05	1.86	2.69	0.44	2.94	2.16	4.10	4.56	4.81	4.03	ns
100 µA	24 mA	Std.	0.80	3.49	0.05	2.18	3.16	0.52	3.49	2.44	4.91	5.98	5.69	4.64	ns
		–1	0.68	2.97	0.05	1.86	2.69	0.44	2.97	2.07	4.18	5.08	4.84	3.95	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to the Table 2-5 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

1.5 V DC Core Voltage

Table 2-43 • 3.3 V LVCMOS Wide Range Low Slew
Military-Case Conditions: T_J = 125℃, Worst-Case VCC = 1. 425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.61	8.94	0.04	1.89	2.86	0.40	8.92	7.06	3.69	3.20	10.39	8.53	ns
		–1	0.52	7.61	0.03	1.61	2.43	0.34	7.59	6.00	3.14	2.72	8.84	7.25	ns
100 µA	8 mA	Std.	0.61	7.23	0.04	1.89	2.86	0.40	7.21	5.99	4.22	4.15	8.68	7.45	ns
		–1	0.52	6.15	0.03	1.61	2.43	0.34	6.14	5.09	3.59	3.53	7.39	6.34	ns
100 µA	12 mA	Std.	0.61	6.03	0.04	1.89	2.86	0.40	6.01	5.18	4.57	4.74	7.47	6.65	ns
		–1	0.52	5.13	0.03	1.61	2.43	0.34	5.11	4.41	3.89	4.03	6.36	5.66	ns
100 µA	16 mA	Std.	0.61	5.68	0.04	1.89	2.86	0.0	5.66	5.01	4.64	4.91	7.13	6.47	ns
		–1	0.52	4.83	0.03	1.61	2.43	0.34	4.82	4.26	3.95	4.18	6.06	5.51	ns
100 µA	24 mA	Std.	0.61	5.50	0.04	1.89	2.86	0.40	5.48	5.03	4.74	5.52	6.95	6.49	ns
		–1	0.52	4.68	0.03	1.61	2.43	0.34	4.66	4.28	4.03	4.70	5.91	5.52	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

Table 2-44 • 3.3 V LVCMOS Wide Range High Slew
Military-Case Conditions: T_J = 125℃, Worst-Case VCC = 1. 425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.61	4.86	0.04	1.89	2.86	0.40	4.84	3.65	3.69	3.42	6.29	5.12	ns
		–1	0.52	4.14	0.03	1.61	2.43	0.34	4.12	3.11	3.14	2.91	5.35	4.35	ns
100 µA	8 mA	Std.	0.61	3.93	0.04	1.89	2.86	0.40	3.91	2.86	4.22	4.38	5.36	4.33	ns
		–1	0.52	3.34	0.03	1.61	2.43	0.34	3.32	2.44	3.59	3.72	4.56	3.68	ns
100 µA	12 mA	Std.	0.61	3.40	0.04	1.89	2.86	0.40	3.38	2.49	4.57	4.99	4.83	3.95	ns
		–1	0.52	2.89	0.03	1.61	2.43	0.34	2.88	2.12	3.89	4.25	4.11	3.36	ns
100 µA	16 mA	Std.	0.61	3.31	0.04	1.89	2.86	0.40	3.29	2.42	4.66	5.16	4.75	3.89	ns
		–1	0.52	2.82	0.03	1.61	2.43	0.34	2.80	2.06	3.96	4.39	4.04	3.31	ns
100 µA	24 mA	Std.	0.61	3.35	0.04	1.89	2.86	0.40	3.33	2.32	4.76	5.78	4.78	3.79	ns
		–1	0.52	2.85	0.03	1.61	2.43	0.34	2.83	1.98	4.05	4.91	4.07	3.22	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-45 • **Minimum and Maximum DC Output Levels 2.5 V LVCMOS**

	VOL	VOH	IOL	IOH	IOSH	IOSL
Drive Strength	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA**	**Max. mA**
	$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 100$ (°C)	
4 mA	0.7	1.7	4	4	16	18
8 mA	0.7	1.7	8	8	32	37
12 mA	0.7	1.7	12	12	65	74
16 mA	0.7	1.7	16	16	83	87
24 mA	0.7	1.7	24	24	169	124

Note: Software default selection highlighted in gray.

Table 2-46 • **Minimum and Maximum DC Input Levels 2.5 V LVCMOS**

VIL		VIH		I_{IL}[1]	I_{IH}[2]
Min. V	**Max. V**	**Min. V**	**Max. V**	**µA**	**µA**
$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)	
–0.3	0.7	1.7	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

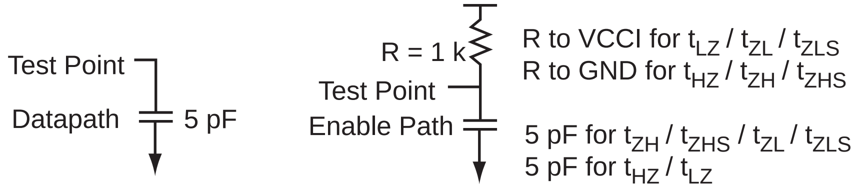


Figure 2-9 • **AC Loading**

Table 2-47 • **2.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	5

*Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-48 • **2.5 V LVCMOS Low Slew**
Military-Case Conditions: T_J = 125℃, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	6.87	0.05	2.04	2.56	0.52	6.99	5.83	2.70	2.19	9.20	8.03	ns
	–1	0.68	5.84	0.05	1.73	2.17	0.44	5.95	4.96	2.29	1.86	7.82	6.83	ns
8 mA	Std.	0.80	5.62	0.05	2.04	2.56	0.52	5.72	4.84	3.08	2.90	7.92	7.14	ns
	–1	0.68	4.78	0.05	1.73	2.17	0.44	4.86	4.20	2.62	2.47	6.74	6.08	ns
12 mA	Std.	0.80	4.73	0.05	2.04	2.56	0.52	4.81	4.30	3.34	3.38	7.01	6.50	ns
	–1	0.68	4.02	0.05	1.73	2.17	0.44	4.09	3.65	2.84	2.87	5.97	5.53	ns
16 mA	Std.	0.80	4.46	0.05	2.04	2.56	0.52	4.53	4.16	3.39	3.50	6.74	6.36	ns
	–1	0.68	3.79	0.05	1.73	2.17	0.44	3.86	3.54	2.89	2.98	5.73	5.41	ns
24 mA	Std.	0.80	4.34	0.05	2.04	2.56	0.52	4.41	4.17	3.47	3.96	6.62	6.38	ns
	–1	0.68	3.69	0.05	1.73	2.17	0.4	3.75	3.55	2.95	3.36	5.63	5.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-49 • **2.5 V LVCMOS High Slew**
Military-Case Conditions: T_J = 125℃, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	3.51	0.05	2.04	2.56	0.52	3.56	3.13	2.70	2.27	5.77	5.33	ns
	–1	0.68	2.98	0.05	1.73	2.17	0.44	3.03	2.66	2.29	1.93	4.91	4.53	ns
8 mA	Std.	0.80	2.87	0.05	2.04	2.56	0.52	2.92	2.40	3.08	3.01	5.12	4.61	ns
	–1	0.68	2.44	0.05	1.73	2.17	0.44	2.48	2.05	2.62	2.56	4.36	3.92	ns
12 mA	Std.	0.80	2.50	0.05	2.04	2.56	0.52	2.53	2.05	3.34	3.47	4.74	4.25	ns
	–1	0.68	2.12	0.05	1.73	2.17	0.44	2.15	1.74	2.84	2.95	4.03	3.62	ns
16 mA	Std.	0.80	2.43	0.05	2.04	2.56	0.52	2.47	1.98	3.39	3.59	4.67	4.19	ns
	–1	0.68	2.07	0.05	1.73	2.17	0.44	2.10	1.69	2.89	3.06	3.97	3.56	ns
24 mA	Std.	0.80	2.44	0.05	2.04	2.56	0.52	2.48	1.90	3.47	4.08	4.68	4.10	ns
	–1	0.68	2.08	0.05	1.73	2.17	0.44	2.11	1.61	2.95	3.47	3.98	3.49	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.5 V DC Core Voltage

Table 2-50 • 2.5 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125℃, VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.61	6.73	0.04	1.75	2.26	0.40	6.83	5.71	2.54	1.99	8.30	7.18	ns
	–1	0.52	5.73	0.03	1.49	1.93	0.34	5.81	4.86	2.16	1.69	7.06	6.10	ns
8 mA	Std.	0.61	5.48	0.04	1.75	2.26	0.40	5.56	4.82	2.92	2.71	7.02	6.29	ns
	–1	0.52	4.66	0.03	1.49	1.93	0.34	4.73	4.10	2.48	2.30	5.98	5.35	ns
12 mA	Std.	0.61	4.59	0.04	1.75	2.26	0.40	4.65	4.18	3.18	3.18	6.12	5.65	ns
	–1	0.52	3.91	0.03	1.49	1.93	0.34	3.96	3.56	2.71	2.70	5.20	4.80	ns
16 mA	Std.	0.61	4.32	0.04	1.75	2.26	0.40	4.38	4.04	3.24	3.31	5.84	5.51	ns
	–1	0.52	3.68	0.03	1.49	1.93	0.34	3.72	3.44	2.75	2.81	4.97	4.69	ns
24 mA	Std.	0.61	4.20	0.04	1.75	2.26	0.40	4.26	4.06	3.31	3.76	5.72	5.52	ns
	–1	0.52	3.58	0.03	1.49	1.93	0.34	3.62	3.45	2.82	3.20	4.87	4.70	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-51 • 2.5 V LVCMOS High Slew
Military-Case Conditions: T_J = 125℃, VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.61	3.37	0.04	1.75	2.26	0.40	3.41	3.01	2.54	2.08	4.87	4.48	ns
	–1	0.52	2.87	0.03	1.49	1.93	0.34	2.90	2.56	2.16	1.77	4.14	3.81	ns
8 mA	Std.	0.61	2.74	0.04	1.75	2.26	0.40	2.76	2.29	2.92	2.82	4.23	3.75	ns
	–1	0.52	2.33	0.03	1.49	1.93	0.34	2.35	1.95	2.48	2.40	3.60	3.19	ns
12 mA	Std.	0.61	2.36	0.04	1.75	2.26	0.40	2.38	1.93	3.19	3.27	3.84	3.40	ns
	–1	0.52	2.01	0.03	1.49	1.93	0.34	2.02	1.65	2.71	2.78	3.27	2.89	ns
16 mA	Std.	0.61	2.29	0.04	1.75	2.26	0.40	2.31	1.87	3.24	3.40	3.77	3.33	ns
	–1	0.52	1.95	0.03	1.49	1.93	0.34	1.96	1.59	2.75	2.89	3.21	2.84	ns
24 mA	Std.	0.61	2.31	0.04	1.75	2.26	0.40	2.32	1.78	3.31	3.89	3.79	3.25	ns
	–1	0.52	1.96	0.03	1.49	1.93	0.34	1.98	1.52	2.82	3.31	3.22	2.76	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-52 • Minimum and Maximum DC Output Levels 1.8 V LVCMOS

	VOL	VOH	IOL	IOH	IOSH	IOSL
Drive Strength	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA**	**Max mA**[3]
	$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 100$ (°C)	
2 mA	0.45	VCCI – 0.45	2	2	9	11
4 mA	0.45	VCCI – 0.45	4	4	17	22
6 mA	0.45	VCCI – 0.45	6	6	35	44
8 mA	0.45	VCCI – 0.45	8	8	45	51
12 mA	0.45	VCCI – 0.45	12	12	91	74
16 mA	0.45	VCCI – 0.45	16	16	91	74

Note: Software default selection highlighted in gray.

Table 2-53 • Minimum and Maximum DC Input Levels 1.8 V LVCMOS

VIL		VIH		IIL[1]	IIH[2]
Min. V	**Max. V**	**Min. V**	**Max. V**	**μA**	**μA**
$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)	
–0.3	0.35 * VCCI	0.65 * VCCI	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

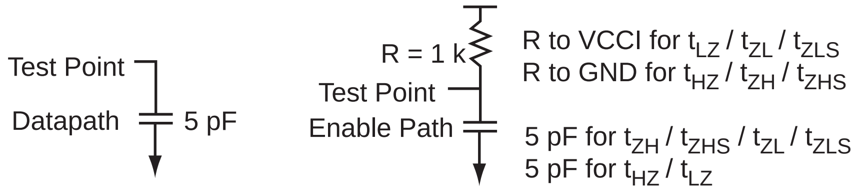


Figure 2-10 • AC Loading

Table 2-54 • 1.8 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	5

*Note: *Measuring point = Vtrip. See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-55 • **1.8 V LVCMOS Low Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	9.16	0.05	2.00	2.82	0.52	9.32	7.69	2.77	1.20	11.53	9.89	ns
	–1	0.68	7.79	0.05	1.70	2.40	0.44	7.93	6.54	2.36	1.02	9.81	8.42	ns
4 mA	Std.	0.80	7.55	0.05	2.00	2.82	0.52	7.68	6.48	3.23	2.76	9.88	8.68	ns
	–1	0.68	6.42	0.05	1.70	2.40	0.44	6.53	5.51	2.75	2.35	8.41	7.38	ns
6 mA	Std.	0.80	6.40	0.05	2.00	2.82	0.52	6.51	5.65	3.54	3.34	8.71	7.85	ns
	–1	0.68	5.44	0.05	1.70	2.40	0.44	5.54	4.80	3.01	2.84	7.41	6.68	ns
8 mA	Std.	0.80	6.01	0.05	2.00	2.82	0.52	6.12	5.48	3.61	3.50	8.32	7.69	ns
	–	0.68	5.11	0.05	1.70	2.40	0.44	5.20	4.66	3.07	2.98	7.08	6.54	ns
12 mA	Std.	0.80	5.90	0.05	2.00	2.82	0.52	6.00	5.49	3.71	4.08	8.21	7.70	ns
	–1	0.68	5.02	0.05	1.70	2.40	0.44	5.11	4.67	3.16	3.47	6.98	6.55	ns
16 mA	Std.	0.80	5.90	005	2.00	2.82	0.52	6.00	5.49	3.71	4.08	8.21	7.70	ns
	–1	0.68	5.02	0.05	1.70	2.40	0.44	5.11	4.67	3.16	3.47	6.98	6.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-56 • **1.8 V LVCMOS High Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	4.14	0.05	2.00	2.82	0.52	4.21	4.05	2.76	1.23	6.42	6.26	ns
	–1	0.68	3.52	0.05	1.70	2.40	0.44	3.58	3.45	2.35	1.04	5.46	5.32	ns
4 mA	Std.	0.80	3.36	0.05	2.00	2.82	0.52	3.41	3.01	3.22	2.85	5.62	5.21	ns
	–1	0.68	2.86	0.05	1.70	2.40	0.44	2.90	2.56	2.74	2.42	4.78	4.43	ns
6 mA	Std.	0.80	2.88	0.05	2.00	2.82	0.52	2.93	2.49	3.54	3.43	5.13	4.70	ns
	–1	0.68	2.45	0.05	1.70	2.40	0.44	2.49	2.12	3.01	2.92	4.36	3.99	ns
8 mA	Std.	0.80	2.79	0.05	2.00	2.82	0.52	2.83	2.40	3.60	3.59	5.04	4.60	ns
	–1	0.68	2.37	0.05	1.70	2.40	0.44	2.41	2.04	3.06	3.05	4.29	3.91	ns
12 mA	Std.	0.80	2.78	0.05	2.00	2.82	0.52	2.82	2.28	3.71	4.21	5.02	4.48	ns
	–1	0.68	2.36	0.05	1.70	2.40	0.44	2.40	1.94	3.16	3.58	4.27	3.81	ns
16 mA	Std.	0.80	2.78	0.05	2.00	2.82	0.52	2.82	2.28	3.71	4.21	5.02	4.48	ns
	–1	0.68	2.36	0.05	1.70	2.40	0.44	2.40	1.94	3.16	3.58	4.27	3.81	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.5 V DC Core Voltage

Table 2-57 • **1.8 V LVCMOS Low Slew**
Military-Case Conditions: T_J = 125℃, VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	9.02	0.04	1.69	2.52	0.40	9.17	7.57	2.61	1.01	10.63	9.04	ns
	–1	0.52	7.68	0.03	1.44	2.14	0.34	7.80	6.44	2.22	0.86	9.04	7.69	ns
4 mA	Std.	0.61	7.41	0.04	1.69	2.52	0.40	7.52	6.36	3.07	2.56	8.99	7.83	ns
	–1	0.52	6.30	0.03	1.44	2.14	0.34	6.40	5.41	2.62	2.18	7.64	6.66	ns
6 mA	Std.	0.61	6.26	0.04	1.69	2.52	0.40	6.35	5.53	3.38	3.14	7.82	7.00	ns
	–1	0.52	5.33	0.03	1.44	2.14	0.34	5.40	4.71	2.88	2.67	6.65	5.95	ns
8 mA	Std.	0.61	5.88	0.04	1.69	2.52	0.40	5.96	5.37	3.45	3.30	7.42	6.83	ns
	–1	0.52	5.00	0.03	1.44	2.14	0.34	5.07	4.57	2.94	2.81	6.32	5.81	ns
12 mA	Std.	0.61	5.76	0.04	1.69	2.52	0.40	5.85	5.38	3.55	3.88	7.31	6.84	ns
	–1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns
16 mA	Std.	0.61	5.76	0.04	1.69	2.52	040	5.85	5.38	3.55	3.88	7.31	6.84	ns
	–1	0.52	4.90	0.03	1.44	2.14	0.34	4.97	4.57	3.02	3.30	6.22	5.82	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-58 • **1.8 V LVCMOS High Slew**
Military-Case Conditions: T_J = 125℃, VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	4.01	0.04	1.69	2.52	0.40	4.06	3.94	2.60	1.03	5.52	5.40	ns
	–1	0.52	3.41	0.03	1.44	2.14	0.34	3.45	3.35	2.21	0.88	4.70	4.60	ns
4 mA	Std.	0.61	3.22	0.04	1.69	2.52	0.40	3.26	2.89	3.07	2.65	4.72	4.36	ns
	–1	0.52	2.74	0.03	1.44	2.14	0.34	2.77	2.46	2.61	2.26	4.02	3.71	ns
6 mA	Std.	0.61	2.74	0.04	1.69	2.52	0.40	2.77	2.38	3.38	3.23	4.23	3.84	ns
	–1	0.52	2.33	0.03	1.44	2.14	0.34	2.36	2.02	2.88	2.75	3.60	3.27	ns
8 mA	Std.	0.52	2.65	0.04	1.69	2.52	0.40	2.68	2.28	3.45	3.40	4.14	3.75	ns
	–1	0.51	2.26	0.03	1.44	2.14	0.34	2.28	1.94	2.93	2.89	3.52	3.19	ns
12 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	–1	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08	ns
16 mA	Std.	0.61	2.64	0.04	1.69	2.52	0.40	2.66	2.16	3.55	4.01	4.13	3.63	ns
	–1	0.52	2.24	0.03	1.44	2.14	0.34	2.26	1.84	3.02	3.41	3.51	3.08	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-59 • **Minimum and Maximum DC Output Levels 1.5 V LVCMOS**

Drive Strength	VOL	VOH	IOL	IOH	IOSH	IOSL
	Max. V	Min. V	mA	mA	Max. mA	Max. mA
	–55 ≤ T_J ≤ 125 (℃)		–55 ≤ T_J ≤ 125 (℃)		–55 ≤ T_J ≤ 100 (℃)	
2 mA	0.25 * VCCI	0.75 * VCCI	2	2	13	16
4 mA	0.25 * VCCI	0.75 * VCCI	4	4	25	33
6 mA	0.25 * VCCI	0.75 * VCCI	6	6	32	39
8 mA	0.25 * VCCI	0.75 * VCCI	8	8	66	55
12 mA	0.25 * VCCI	0.75 * VCCI	12	12	66	55

Note: Software default selection highlighted in gray.

Table 2-60 • **Minimum and Maximum DC Input Levels 1.5 V LVCMOS**

VIL		VIH		IIL[1]	IIH[2]
Min. V	Max. V	Min. V	Max. V	µA	µA
–55 ≤ T_J ≤ 125 (℃)		–55 ≤ T_J ≤ 125 (℃)		–55 ≤ T_J ≤ 125 (℃)	
–0.3	0.35 * VCCI	0.65 * VCCI	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

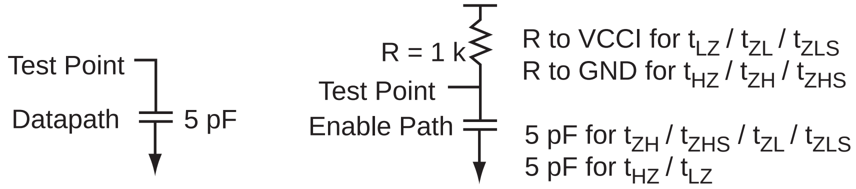


Figure 2-11 • **AC Loading**

Table 2-61 • **1.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	5

*Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-62 • **1.5 V LVCMOS Low Slew**
Military-Case Conditions: T_J = 125℃, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	9.53	0.05	2.19	3.06	0.52	9.69	7.88	3.38	2.67	11.90	10.09	ns
	–1	0.68	8.10	0.05	1.86	2.61	0.44	8.25	6.71	2.87	2.27	10.12	8.58	ns
4 mA	Std.	0.80	8.14	0.05	2.19	3.06	0.52	8.28	6.89	3.74	3.34	10.49	9.09	ns
	–1	0.68	6.93	0.05	1.85	2.61	0.44	7.05	5.86	3.18	2.84	8.92	7.74	ns
6 mA	Std.	0.80	7.64	0.05	2.19	3.06	0.52	7.78	6.70	3.82	3.52	9.98	8.91	ns
	–1	0.68	6.50	0.05	1.86	2.61	0.44	6.61	5.70	3.25	2.99	8.49	7.58	ns
8 mA	Std.	0.80	7.55	0.05	2.19	3.06	0.52	7.68	6.71	3.41	4.19	9.88	8.91	ns
	–1	0.68	6.42	0.05	1.86	2.61	0.44	6.53	5.71	2.90	3.56	8.41	7.58	ns
12 mA	Std.	0.80	7.55	0.05	2.19	3.06	0.52	7.68	6.71	3.41	4.19	9.89	8.91	ns
	–1	0.68	6.42	0.05	1.86	2.61	0.44	6.53	5.71	2.90	3.56	8.41	7.58	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-63 • **1.5 V LVCMOS High Slew**
Military-Case Conditions: T_J = 125℃, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	3.91	0.05	2.19	3.06	0.52	3.98	3.54	3.37	2.78	6.18	5.75	ns
	–1	0.68	3.33	0.05	1.86	2.61	0.44	3.38	3.01	2.86	2.36	5.26	4.89	ns
4 mA	Std.	0.80	3.34	0.05	2.19	3.06	0.52	3.39	2.90	3.73	3.45	5.60	5.11	ns
	–1	0.68	2.84	0.05	1.86	2.61	0.44	2.88	2.47	3.17	2.93	4.76	4.35	ns
6 mA	Std.	0.80	3.23	0.05	2.19	3.06	0.52	3.28	2.78	3.81	3.64	5.48	4.99	ns
	–1	0.68	2.74	0.05	1.86	2.61	0.44	2.79	2.37	3.24	3.09	4.66	4.24	ns
8 mA	Std.	0.80	3.19	0.05	2.19	3.06	0.52	3.24	2.63	3.93	4.33	5.45	4.84	ns
	–1	0.68	2.71	0.05	1.86	2.61	0.44	2.76	2.24	3.34	3.69	4.63	4.12	ns
12 mA	Std.	0.80	3.19	0.05	2.19	3.06	0.52	3.24	2.63	3.93	4.33	5.45	4.84	ns
	–1	0.68	2.71	0.05	1.86	2.61	0.44	2.76	2.24	3.34	3.69	4.63	4.12	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.5 V DC Core Voltage

Table 2-64 • **1.5 V LVCMOS Low Slew**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	9.39	0.04	1.88	2.77	0.40	9.54	7.77	3.22	2.47	11.00	9.24	ns
	–1	0.52	7.99	0.03	1.60	2.35	0.34	8.11	6.61	2.74	2.10	9.36	7.86	ns
4 mA	Std.	0.61	8.01	0.04	1.88	2.77	0.40	8.13	6.77	3.58	3.14	9.59	8.24	ns
	–1	0.52	6.81	0.03	1.60	2.35	0.34	6.91	5.76	3.05	2.67	8.16	7.01	ns
6 mA	Std.	0.61	7.51	0.04	1.88	2.77	0.40	7.62	6.59	3.66	3.32	9.09	8.05	ns
	–1	0.52	6.39	0.03	1.60	2.35	0.34	6.48	5.60	3.12	2.83	7.73	6.85	ns
8 mA	Std.	0.61	7.41	0.04	1.88	2.77	0.40	7.52	6.59	3.41	3.99	8.99	8.06	ns
	–1	0.52	6.30	0.03	1.60	2.35	0.34	6.40	5.61	2.90	3.40	7.64	6.85	ns
12 mA	Std.	0.61	7.41	0.04	1.88	2.77	0.40	7.52	6.59	3.41	3.99	8.99	8.06	ns
	–1	0.52	6.30	0.03	1.60	2.35	0.34	6.40	5.61	2.90	3.40	7.64	6.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-65 • **1.5 V LVCMOS High Slew**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.61	3.78	0.04	1.88	2.77	0.40	3.82	3.43	3.21	2.58	5.29	4.89	ns
	–1	0.52	3.21	0.03	1.60	2.35	0.34	3.25	2.92	2.73	2.20	4.50	4.16	ns
4 mA	Std.	0.61	3.20	0.04	1.88	2.77	0.40	3.23	2.79	3.57	3.25	4.70	4.25	ns
	–1	0.52	2.72	0.03	1.60	2.35	0.34	2.75	2.37	3.04	2.77	4.00	3.62	ns
6 mA	Std.	0.61	3.09	0.04	1.88	2.77	0.40	3.12	2.67	3.65	3.44	4.59	4.13	ns
	–1	0.52	2.63	0.04	1.60	2.35	0.34	2.65	2.27	3.11	2.93	3.90	3.52	ns
8 mA	Std.	0.61	3.05	0.04	1.88	2.77	0.40	3.09	2.52	3.77	4.14	4.55	3.98	ns
	–1	0.52	2.60	0.03	1.60	2.35	0.34	2.62	2.14	3.21	3.52	3.87	3.39	ns
12 mA	Std.	0.61	3.05	0.04	1.88	2.77	0.40	3.09	2.52	3.77	4.14	4.55	3.98	ns
	–1	0.52	2.60	0.03	1.60	2.35	0.34	2.62	2.14	3.21	3.52	3.87	3.39	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-66 • **Minimum and Maximum DC Output Levels**
1.2 V LVCMOS
Applicable to I/Os Operating at 1.2 V Core Voltage

Drive Strength	**VOL**	**VOH**	**IOL**	**IOH**	**IOSH**	**IOSL**
	Max. V	**Min. V**	**mA**	**mA**	**Max. mA**	**Max. mA**
	–55 ≤ T_J ≤ 125 (°C)		–55 ≤ T_J ≤ 125 (°C)		–55 ≤ T_J ≤ 100 (°C)	
2 mA	0.25 * VCCI	0.75 * VCCI	2	2	TBD	TBD

Note: Software default selection highlighted in gray.

Table 2-67 • **Minimum and Maximum DC Input and Output Levels**
1.2 V LVCMOS
Applicable to I/Os Operating at 1.2 V Core Voltage[1]

VIL		**VIH**		**IIL[2]**	**IIH[3]**
Min. V	**Max. V**	**Min. V**	**Max. V**	**µA**	**µA**
–55 ≤ T_J ≤ 125 (°C)		–55 ≤ T_J ≤ 125 (°C)		–55 ≤ T_J ≤ 125 (°C)	
–0.3	0.35 * VCCI	0.65 * VCCI	3.6	5	5

Notes:

1. Applicable to RT ProASIC3 devices operating at 1.2 V core voltage only.
1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).
2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.

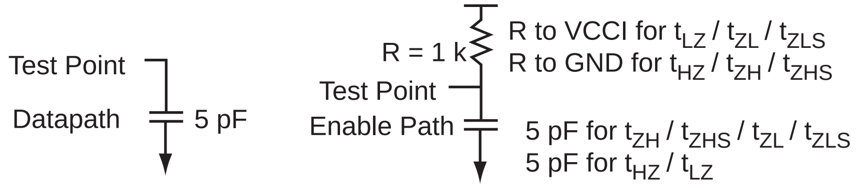


Figure 2-12 • **AC Loading**

Table 2-68 • **1.2 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**VREF (Typ) (V)**	**C_{LOAD} (pF)**
0	1.2	0.6	–	5

*Note: *Measuring point = $V_{trip.}$ See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-69 • **1.2 V LVCMOS Low Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	12.61	0.05	2.65	3.75	0.52	12.10	9.50	5.11	4.66	14.31	11.71	ns
	–1	0.68	10.72	0.05	2.25	3.19	0.44	10.30	8.08	4.35	3.97	12.17	9.96	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-70 • **1.2 V LVCMOS High Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	5.16	0.05	2.65	3.75	0.52	4.98	4.39	5.10	4.81	7.19	6.60	ns
	–1	0.68	4.39	0.05	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.2 V LVCMOS Wide Range

Table 2-71 • Minimum and Maximum DC Output Levels
1.2 V LVCMOS Wide Range
Applicable to I/Os Operating at 1.2 V Core Voltage

Drive Strength	Equiv. Software Default Drive Strength Option[1]	VOL	VOH	IOL	IOH	IOSH	IOSL
		Max. V	Min. V	µA	µA	Max. mA	Max. mA
		$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 100$ (°C)	
100 µA	2 mA	0.25 * VCCI	0.75 * VCCI	100	100	TBD	TBD

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Software default selection highlighted in gray.*

Table 2-72 • Minimum and Maximum DC Input Levels
1.2 V LVCMOS Wide Range
Applicable to I/Os Operating at 1.2 V Core Voltage[1]

VIL		VIH		IIL[2]	IIH[3]
Min. V	Max. V	Min. V	Max. V	µA	µA
$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)	
–0.3	0.3 * VCCI	0.7 * VCCI	3.6	5	5

Notes:

1. *Applicable to RT ProASIC3 devices operating at 1.2 V core voltage only.*
1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

Table 2-73 • 1.2 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	1.2	0.6	–	5

Note: *Measuring point = $V_{trip.}$ See Table 2-20 on page 2-22 for a complete table of trip points.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-74 • **1.2 V LVCMOS Wide Range Low Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	12.61	0.05	2.65	3.75	0.52	12.10	9.50	5.11	4.66	14.31	11.71	ns
	–1	0.68	10.72	0.05	2.25	3.19	0.44	10.30	8.08	4.35	3.97	12.17	9.96	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-75 • **1.2 V LVCMOS Wide Range High Slew**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	5.16	0.05	2.65	3.75	0.52	4.98	4.39	5.10	4.81	7.19	6.60	ns
	–1	0.68	4.39	0.05	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-76 • **Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**μA[4]**	**μA[4]**
Per PCI specification	Per PCI curves										5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.Currents are measured at 100°C junction temperature and maximum voltage.*
3. *Currents are measured at 125°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the database; Microsemi loadings for enable path characterization are described in Figure 2-13.

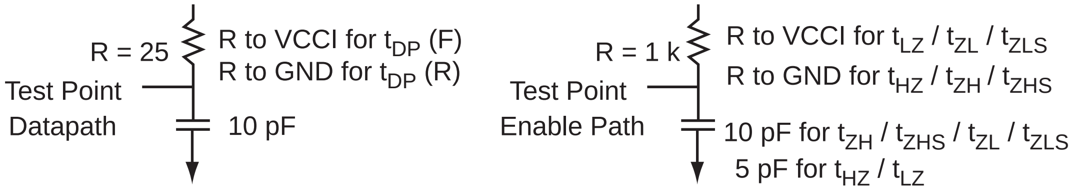


Figure 2-13 • **AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-77.

Table 2-77 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$	–	10

Note: *Measuring point =* $V_{trip.}$ *See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-78 • **3.3 V PCI/PCI-X**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.78	0.05	2.71	3.68	0.52	2.83	1.97	3.26	3.59	5.03	4.18	ns
–1	0.68	2.37	0.05	2.31	3.13	0.44	2.40	1.68	2.77	3.06	4.28	3.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

1.5 V DC Core Voltage

Table 2-79 • **3.3 V PCI/PCI-X**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.65	0.04	2.39	3.38	0.40	2.67	1.86	3.10	3.40	4.14	3.33	ns
–1	0.52	2.25	0.03	2.03	2.88	0.34	2.27	1.58	2.64	2.89	3.52	2.83	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 2-80 • **Minimum and Maximum DC Output Levels 3.3 V GTL**

Drive Strgth.	**VOL**		**VOH**		**IOL**	**IOH**	**IOSH**	**IOSL**
	Max. V		**Min. V**		**mA**	**mA**	**Max. mA**	**Max. mA**
	$-55 \le T_J \le 100$ (℃)	$100 < T_J \le 125$ (℃)	$-55 \le T_J \le 100$ (℃)	$100 < T_J \le 125$ (℃)	$-55 \le T_J \le 125$ (℃)		$-55 \le T_J \le 100$ (℃)	
20 mA*	0.4	0.5	–	–	20	20	268	181

Note: **Output drive strength is below JEDEC specification.*

Table 2-81 • **Minimum and Maximum DC Input Levels 3.3 V GTL**

VIL		**VIH**		**IIL**[1]	**IIH**[2]
Min. V	**Max. V**	**Min. V**	**Max. V**	**µA**[5]	**µA**[5]
$-55 \le T_J \le 125$ (℃)		$-55 \le T_J \le 125$ (℃)		$-55 \le T_J \le 125$ (℃)	
–0.3	VREF – 0.05	VREF + 0.05	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

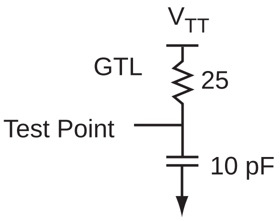


Figure 2-14 • **AC Loading**

Table 2-82 • **3.3 V GTL AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**VREF (typ.) (V)**	**V_{TT} (typ.) (V)**	**C_{LOAD} (pF)**
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: **Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

Table 2-83 • **3.3 V GTL**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V, VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.05	0.05	2.34	0.52	2.01	2.05			4.22	4.26	ns
–1	0.68	1.75	0.05	1.99	0.44	1.71	1.75			3.59	3.62	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-84 • **3.3 V GTL**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.97	0.04	2.11	0.40	1.86	1.97			3.32	3.43	ns
–1	0.52	1.68	0.03	1.79	0.34	1.58	1.68			2.83	2.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-85 • **Minimum and Maximum DC Output Levels**
2.5 V GTL

Drive Strgth.	**VOL**		**VOH**		**IOL**	**IOH**	**IOSH**	**IOSL**
	Max. V		**Min. V**		**mA**	**mA**	**Max. mA**	**Max. mA**
	$-55 \le T_J \le 100$ (℃)	$100 < T_J \le 125$ (℃)	$-55 \le T_J \le 100$ (℃)	$100 < T_J \le 125$ (℃)	$-55 \le T_J \le 125$ (℃)		$-55 \le T_J \le 100$ (℃)	
20 mA*	0.4	0.5	–	–	20	20	169	124

Note: **Output drive strength is below JEDEC specification.*

Table 2-86 • **Minimum and Maximum DC Input Levels**

VIL		**VIH**		**IIL**[1]	**IIH**[2]
Min. V	**Max. V**	**Min. V**	**Max. V**	**µA**	**µA**
$100 < T_J \le 125$ (ºC)		$100 < T_J \le 125$ (ºC)		$100 < T_J \le 125$ (ºC)	
–0.3	VREF – 0.05	VREF + 0.05	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.Output drive strength is below JEDEC specification.*

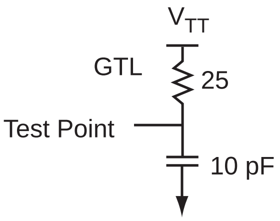


Figure 2-15 • **AC Loading**

Table 2-87 • **2.5 V GTL AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**VREF (typ.) (V)**	**V_{TT} (typ.) (V)**	**C_{LOAD} (pF)**
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: **Measuring point = Vtrip. See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

Table 2-88 • **2.5 V GTL**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V, VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.11	0.05	2.27	0.52	2.14	2.11			4.34	4.31	ns
–1	0.68	1.79	0.05	1.93	0.44	1.82	1.79			3.70	3.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-89 • **2.5 V GTL**
Military-Case Conditions: TJ = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.02	0.04	2.04	0.40	1.98	2.02			3.45	3.49	ns
–1	0.52	1.72	0.03	1.73	0.34	1.69	1.72			2.93	2.97	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-90 • **Minimum and Maximum DC Output Levels**
3.3 V GTL+

Drive Strgth.	VOL Max. V		VOH Min. V		IOL mA	I_{OH} mA	IOSH Max. mA	IOSL Max. mA
	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 100$ (ºC)	
35 mA	0.6	0.75	–	–	35	35	268	181

Table 2-91 • **Minimum and Maximum DC Input Levels**
3.3 V GTL+

VIL Min. V	VIL Max. V	VIH Min. V	VIH Max. V	IIL[1] µA	IIH[2] µA
$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)	
–0.3	VREF – 0.1	VREF + 0.1	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

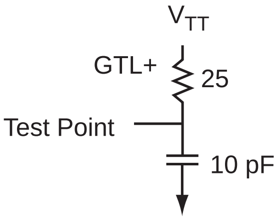


Figure 2-16 • **AC Loading**

Table 2-92 • **3.3 V GTL+ AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

Table 2-93 • **3.3 V GTL+**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.04	0.05	2.34	0.52	2.07	2.03			4.28	4.24	ns
–1	0.68	1.74	0.05	1.99	0.44	1.76	1.73			3.64	3.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-94 • **3.3 V GTL+**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.95	0.04	2.11	0.40	1.92	1.95			3.38	3.41	ns
–1	0.52	1.66	0.03	1.79	0.34	1.63	1.66			2.88	2.90	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-95 • **Minimum and Maximum DC Output Levels**
2.5 V GTL+

Drive Strgth.	VOL		VOH		IOL	IOH	IOSH	IOSL
	Max. V		Min. V		mA	mA	Max. mA	Max. mA
	–55 ≤ T_J ≤ 100 (ºC)	100 < T_J ≤ 125 (ºC)	–55 ≤ T_J ≤ 100 (ºC)	100 < T_J ≤ 125 (ºC)	–55 ≤ T_J ≤ 125 (ºC)		–55 ≤ T_J ≤ 100 (ºC)	
33 mA	0.6	0.75	–	–	33	33	169	124

Table 2-96 • **Minimum and Maximum DC Input Levels**
2.5 V GTL+

VIL		VIH		IIL[1]	IIH[2]
Min. V	Max. V	Min. V	Max. V	μA[5]	μA[5]
–55 ≤ T_J ≤ 125 (ºC)		–55 ≤ T_J ≤ 125 (ºC)		–55 ≤ T_J ≤ 125 (ºC)	
–0.3	VREF – 0.1	VREF + 0.1	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

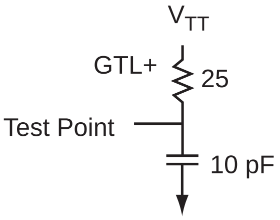


Figure 2-17 • **AC Loading**

Table 2-97 • **2.5 V GTL+ AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: _*Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points._

Timing Characteristics

Table 2-98 • 2.5 V GTL+
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.19	0.05	2.27	0.52	2.22	2.08			4.43	4.28	ns
–1	0.68	1.86	0.05	1.93	0.44	1.89	1.77			3.77	3.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-99 • 2.5 V GTL+
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.05	0.04	2.04	0.40	2.07	1.99			3.53	3.46	ns
–1	0.52	1.75	0.03	1.73	0.34	1.76	1.69			3.00	2.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). RT ProASIC3 devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-100* • Minimum and Maximum DC Input and Output Levels HSTL Class I**

Drive Strgth.	VOL Max. V		VOH Min. V		IOL mA	IOH mA	IOSH Max. mA	IOSL Max. mA
	$-55 \leq T_J \leq 100$ (ºC)	$100 < T_J \leq 125$ (ºC)	$-55 \leq T_J \leq 100$ (ºC)	$100 < T_J \leq 125$ (ºC)	$-55 \leq T_J \leq 125$ (ºC)		$-55 \leq T_J \leq 100$ (ºC)	
8 mA	0.4	0.4	VCCI – 0.4	VCCI – 0.4	8	8	32	39

***Table 2-101* • Minimum and Maximum DC Input and Output Levels**

VIL Min. V	VIL Max. V	VIH Min. V	VIH Max. V	IIL[1] µA[5]	I_{IH}[2] µA[5]
$-55 \leq T_J \leq 125$ (ºC)		$-55 \leq T_J \leq 125$ (ºC)		$-55 \leq T_J \leq 125$ (ºC)	
–0.3	VREF – 0.1	VREF + 0.1	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

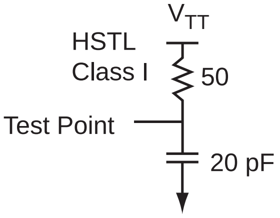


***Figure 2-18* • AC Loading**

***Table 2-102* • HSTL Class I AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.

Timing Characteristics

Table 2-103 • **HSTL Class I**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	3.15	0.05	2.76	0.52	3.20	3.11			5.41	5.32	ns
–1	0.68	2.68	0.05	2.34	0.44	2.73	2.65			4.60	4.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-104 • **HSTL Class I**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	3.02	0.04	2.52	0.40	3.05	3.00			4.51	4.46	ns
–1	0.52	2.57	0.03	2.14	0.34	2.59	2.55			3.84	3.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). RT ProASIC3 devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-105* • Minimum and Maximum DC Output Levels HSTL Class II**

Drive Strgth.	VOL		VOH		IOL	IOH	IOSH	IOSL
	Max. V		Min. V		mA	mA	Max. mA	Max. mA
	–55 ≤ T_J ≤ 100 (ºC)	100 < T_J ≤ 125 (ºC)	–55 ≤ T_J ≤ 100 (ºC)	100 < T_J ≤ 125 (ºC)	–55 ≤ T_J ≤ 125 (ºC)		–55 ≤ T_J ≤ 100 (ºC)	
15 mA*	0.4	0.5	VCCI – 0.4	VCCI – 0.5	15	15	66	55

Note: *Output drive strength is below JEDEC specification.

***Table 2-106* • Minimum and Maximum DC Input Levels HSTL Class II**

VIL		VIH		IIL[1]	IIH[2]
Min. V	Max. V	Min. V	Max. V	µA	µA
–55 ≤ T_J ≤ 125 (ºC)		–55 ≤ T_J ≤ 125 (ºC)		–55 ≤ T_J ≤ 125 (ºC)	
–0.3	VREF – 0.1	VREF + 0.1	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

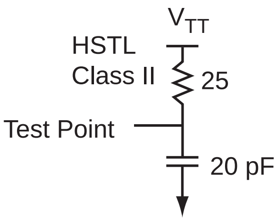


***Figure 2-19* • AC Loading**

***Table 2-107* • HSTL Class II AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.

Timing Characteristics

Table 2-108 • **HSTL Class II**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	3.00	0.05	2.76	0.52	3.05	2.69			5.25	4.89	ns
–1	0.68	2.55	0.05	2.34	0.44	2.59	2.28			4.47	4.16	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-109 • **HSTL Class II**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.86	0.04	2.52	0.40	2.89	2.57			4.36	4.04	ns
–1	0.52	2.44	0.03	2.14	0.34	2.46	2.19			3.71	3.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). RT ProASIC3 devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-110 **• Minimum and Maximum DC Output Levels SSTL 2 Class I**

Drive Strgth.	VOL		VOH		IOL	IOH	IOSH	IOSL
	Max. V		Min. V		mA	mA	Max. mA	Max. mA
	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 100$ (ºC)	
15 mA	0.54	0.54	VCCI – 0.62	VCCI – 0.62	15	15	83	87

Table 2-111 **• Minimum and Maximum DC Input Levels SSTL 2 Class I**

VIL		VIH		IIL[1]	IIH[2]
Min. V	Max. V	Min. V	Max. V	µA	µA
$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)	
–0.3	VREF – 0.2	VREF + 0.2	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

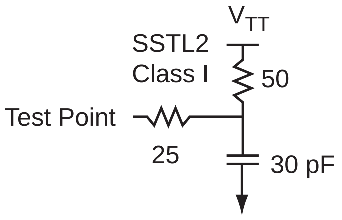


Figure 2-20 **• AC Loading**

Table 2-112 **• SSTL2 Class I AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.

Timing Characteristics

Table 2-113 • **SSTL2 Class I**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.11	0.05	2.09	0.52	2.14	1.83			2.14	1.83	ns
–1	0.68	1.80	0.05	1.78	0.44	1.82	1.55			1.82	1.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-114 • **SSTL2 Class I**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.98	0.04	1.85	0.40	1.99	1.71			1.99	1.71	ns
–1	0.52	1.68	0.03	1.58	0.34	1.69	1.46			1.69	1.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). RT ProASIC3 devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-115 • Minimum and Maximum DC Output Levels SSTL2 Class II

Drive Strgth.	VOL		VOH		IOL	IOH	IOSH	IOSL
	Max. V		Min. V		mA	mA	Max. mA	Max. mA
	–55 ≤ T_J ≤ 100 (ºC)	100 < T_J ≤ 125 (ºC)	–55 ≤ T_J ≤ 100 (ºC)	100 < T_J ≤ 125 (ºC)	–55 ≤ T_J ≤ 125 (ºC)		–55 ≤ T_J ≤ 100 (ºC)	
18 mA	0.35	0.44	VCCI – 0.43	VCCI – 0.43	18	18	169	124

Table 2-116 • Minimum and Maximum DC Input Levels SSTL2 Class II

VIL		VIH		IIL1	IIH[2]
Min. V	Max. V	Min. V	Max. V	µA	µA
–55 ≤ T_J ≤ 125 (ºC)		–55 ≤ T_J ≤ 125 (ºC)		–55 ≤ T_J ≤ 125 (ºC)	
–0.3	VREF – 0.2	VREF + 0.2	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

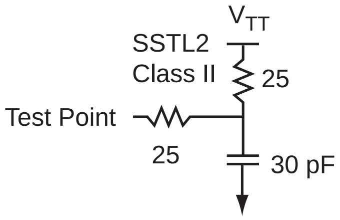


Figure 2-21 • AC Loading

Table 2-117 • SSTL2 Class II AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.

Timing Characteristics

Table 2-118 • **SSTL2 Class II
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V**

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.15	0.05	2.09	0.52	2.18	1.75			2.18	1.75	ns
–1	0.68	1.83	0.05	1.78	0.44	1.86	1.49			1.86	1.49	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-119 • **SSTL2 Class II
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V**

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.02	0.04	1.85	0.40	2.03	1.64			2.03	1.64	ns
–1	0.52	1.72	0.03	1.58	0.34	1.73	1.39			1.73	1.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). RT ProASIC3 devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-120 **• Minimum and Maximum DC Output Levels**
SSTL3 Class I

Drive Strgth.	VOL		VOH		IOL	IOH	IOSL	IOSH
	Max. V		Min. V		mA	mA	Max. mA	Max. mA
	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 100$ (ºC)	
14 mA	0.7	0.7	VCCI – 1.1	VCCI – 1.1	14	14	51	54

Table 2-121 **• Minimum and Maximum DC Input Levels**
SSTL3 Class I

VIL		VIH		IIL[1]	IIH2
Min. V	Max. V	Min. V	Max. V	µA	µA
$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)	
–0.3	VREF – 0.2	VREF + 0.2	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

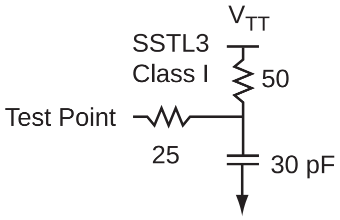


Figure 2-22 **• AC Loading**

Table 2-122 **• SSTL3 Class I AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

Table 2-123 • **SSTL3 Class I**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.29	0.05	2.00	0.52	2.32	1.82			2.32	1.82	ns
–1	0.68	1.95	0.05	1.71	0.44	1.98	1.55			1.98	1.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-124 • **SSTL3 Class I**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	2.15	0.04	1.77	0.40	2.17	1.70			2.17	1.70	ns
–1	0.52	1.83	0.03	1.51	0.34	1.84	1.45			1.84	1.45	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). RT ProASIC3 devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-125* • Minimum and Maximum DC Output Levels**
SSTL3 Class II

	VOL		VOH		IOL	IOH	IOSL	IOSH
Drive Strgth.	**Max. V**		**Min. V**		**mA**	**mA**	**Max. mA**	**Max. mA**
	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 100$ (ºC)	$100 < T_J \le 125$ (ºC)	$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 100$ (ºC)	
21 mA	0.5	0.625	VCCI – 0.9	VCCI – 0.9	21	21	103	109

***Table 2-126* • Minimum and Maximum DC Input Levels**
SSTL3 Class II

VIL		VIH		IIL[1]	IIH[2]
Min. V	**Max. V**	**Min. V**	**Max. V**	**µA[4]**	**µA[4]**
$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)		$-55 \le T_J \le 125$ (ºC)	
–0.3	VREF – 0.2	VREF + 0.2	3.6	5	5

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL (max.).*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH (min.) < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

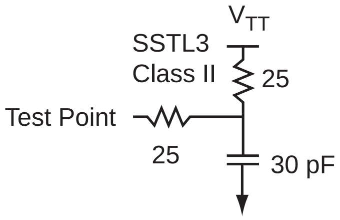


***Figure 2-23* • AC Loading**

***Table 2-127* • SSTL3 Class II AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.

Timing Characteristics

Table 2-128 • **SSTL3 Class II**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.80	2.05	0.05	2.00	0.52	2.08	1.65			2.08	1.65	ns
–1	0.68	1.75	0.05	1.71	0.44	1.77	1.41			1.77	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-129 • **SSTL3 Class II**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.61	1.91	0.04	1.77	0.40	1.92	1.54			1.92	1.54	ns
–1	0.52	1.63	0.03	1.51	0.34	1.64	1.31			1.64	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-24. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, military ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

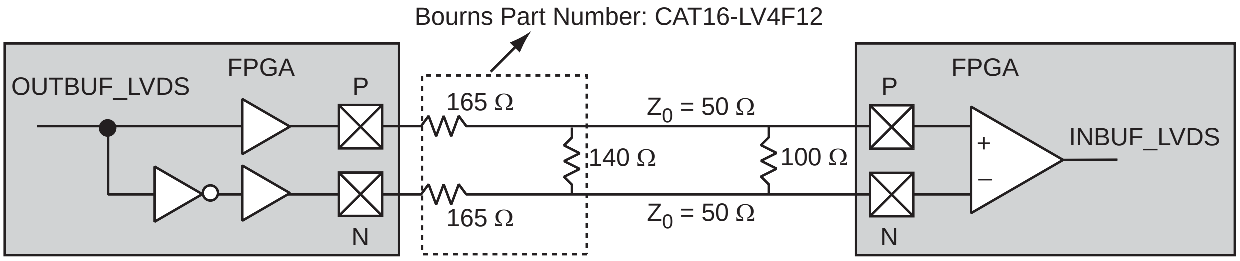


***Figure 2-24* •** **LVDS Circuit Diagram and Board-Level Implementation**

***Table 2-130* • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL [1]	Output Lower Current	0.65	0.91	1.16	mA
IOH [1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH [2]	Input High Leakage Current			5	µA
IIL [2]	Input Low Leakage Current			5	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

Notes:

1. *IOL/IOH is defined by VODIFF/(Resistor Network).*
2. *Currents are measured at 125°C junction temperature.*

***Table 2-131* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: *Measuring point = V_{trip}. See Table 2-20 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

***Table 2-132* • LVDS**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.80	1.87	0.05	2.48	ns
–1	0.68	1.59	0.05	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

1.5 V DC Core Voltage

***Table 2-133* • LVDS**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.61	1.75	0.04	2.18	ns
–1	0.52	1.48	0.03	1.86	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

*B-LVDS/M-LVDS***

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-25. The input and output buffer delays are available in the LVDS section in Table 2-130 on page 2-71.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

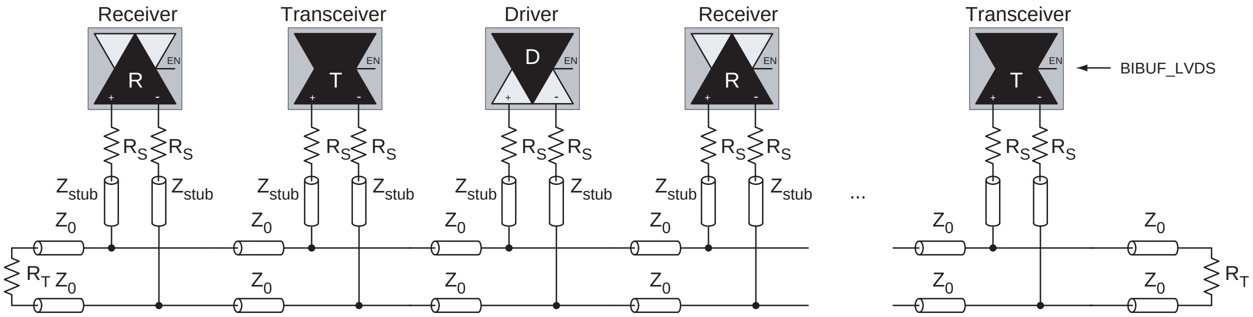


Figure 2-25 **• B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-26. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

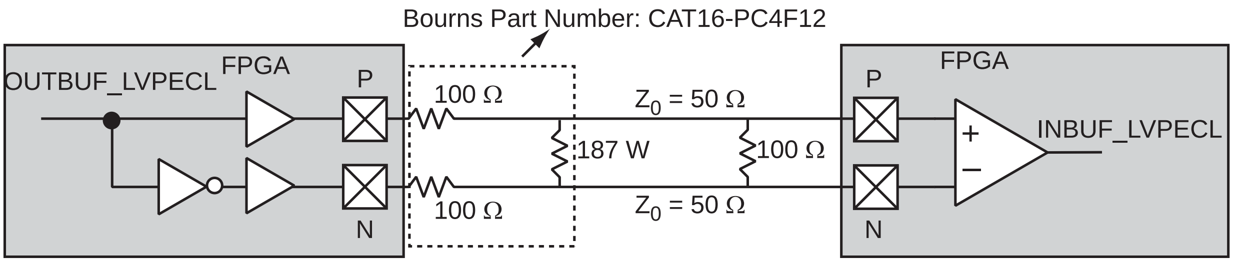


Figure 2-26 • LVPECL Circuit Diagram and Board-Level Implementation

Table 2-134 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-135 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: *Measuring point = Vtrip. See Table 2-20 on page 2-22 for a complete table of trip points.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-136 • **LVPECL**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.80	1.78	0.05	2.16	ns
–1	0.68	1.51	0.05	1.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

1.5 V DC Core Voltage

Table 2-137 • **LVPECL**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.61	1.65	0.04	1.89	ns
–1	0.52	1.40	0.03	1.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

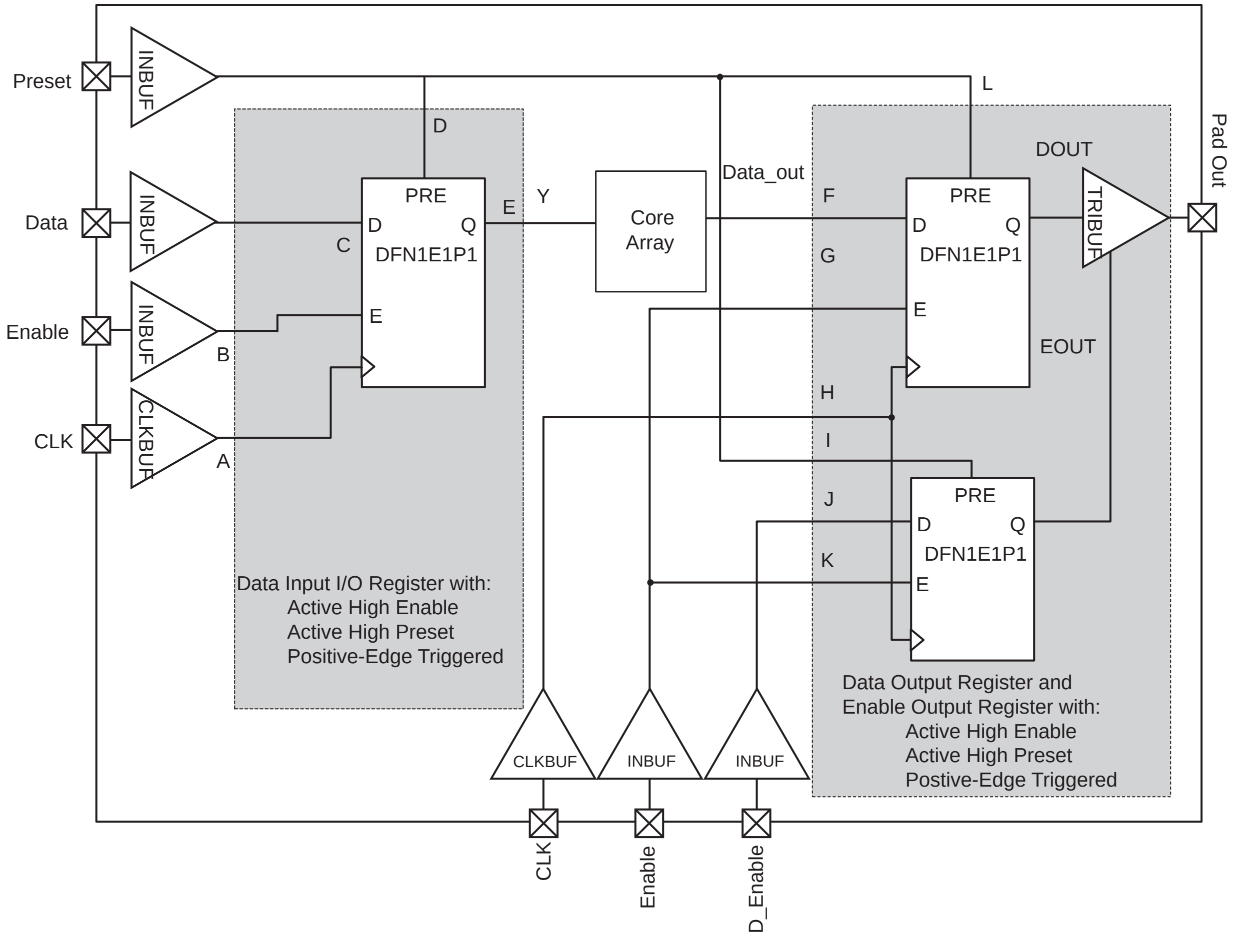


Figure 2-27 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 2-138 **• Parameter Definition and Measuring Nodes**

Parameter Name	**Parameter Definition**	**Measuring Nodes (from, to)***
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

** See Figure 2-27 on page 2-75 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

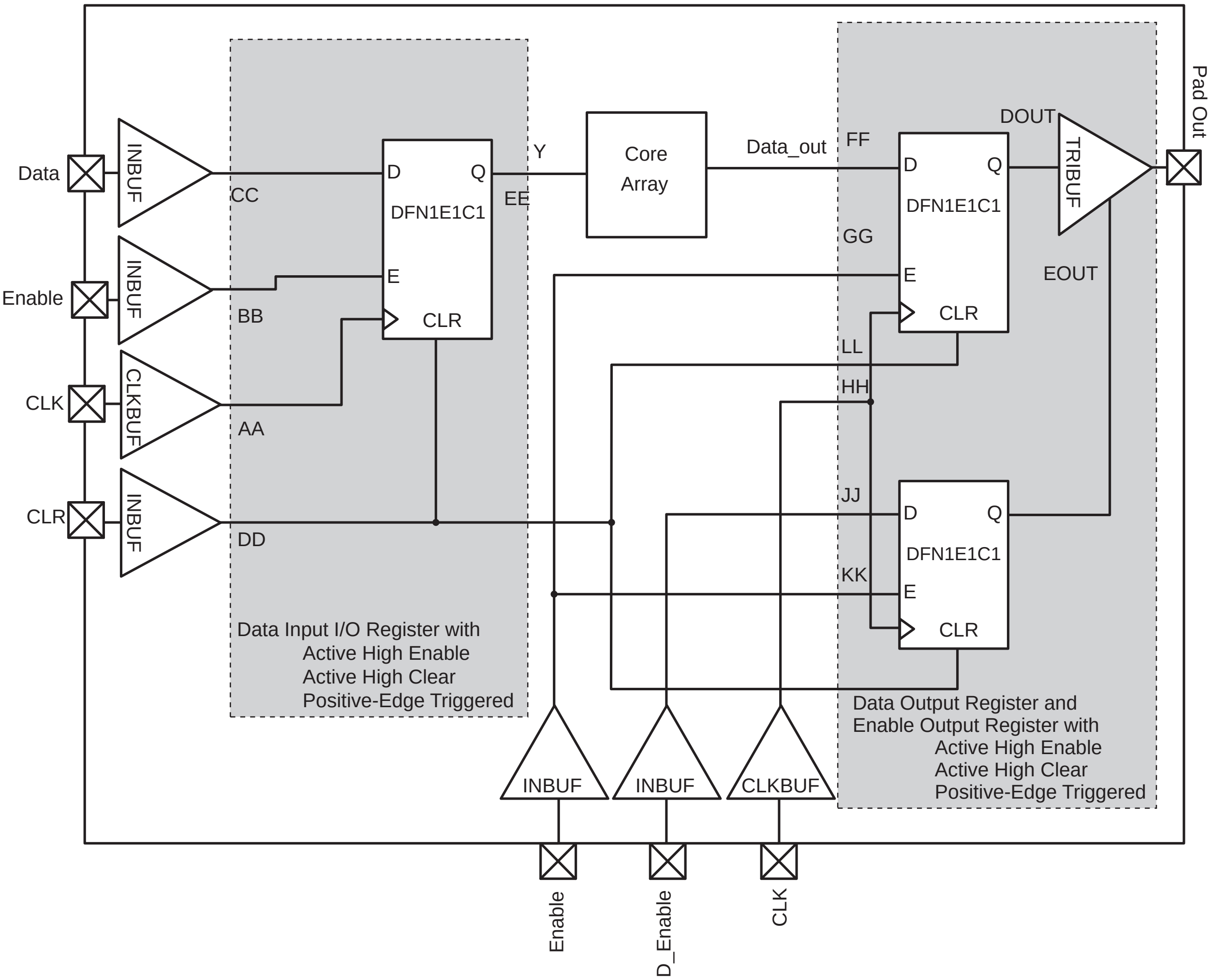


Figure 2-28 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-139 **• Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

*Note: *See Figure 2-28 on page 2-77 for more information.*

Input Register

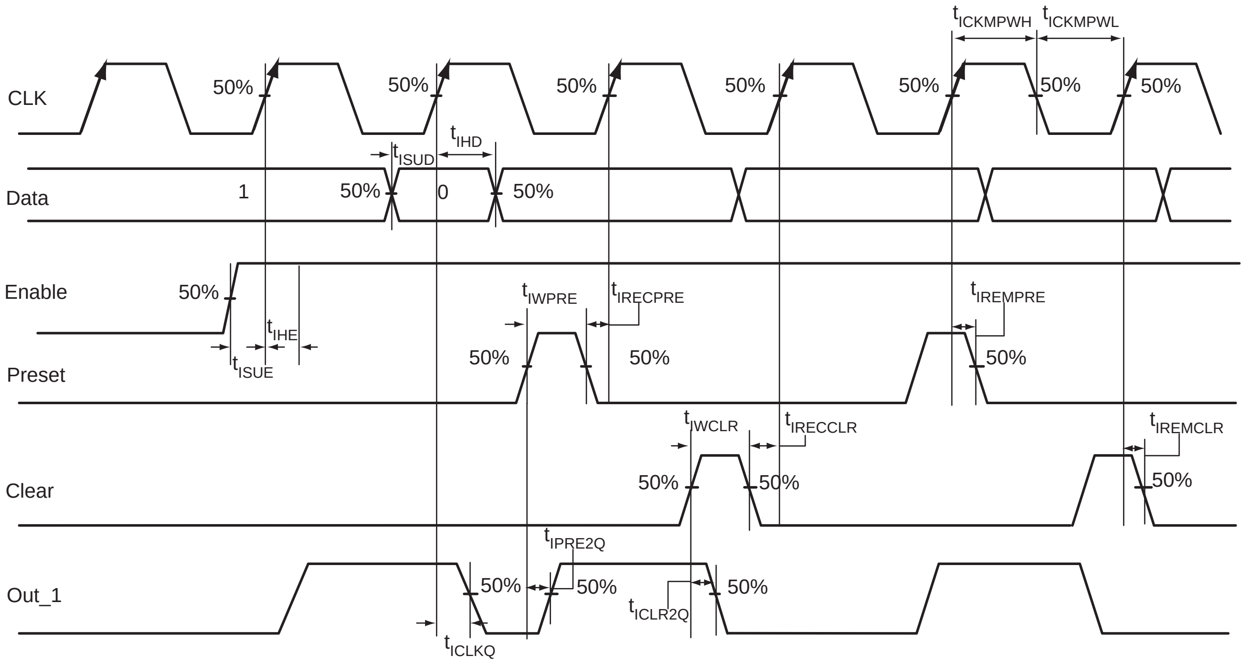


Figure 2-29 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-140 • **Input Data Register Propagation Delays**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.33	0.39	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.36	0.43	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.51	0.60	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.63	0.74	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.63	0.74	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.31	0.36	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.31	0.36	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-141 • **Input Data Register Propagation Delays**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.25	0.30	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.28	0.33	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.39	0.46	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.48	0.56	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.48	0.56	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	0.28	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	0.28	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Output Register

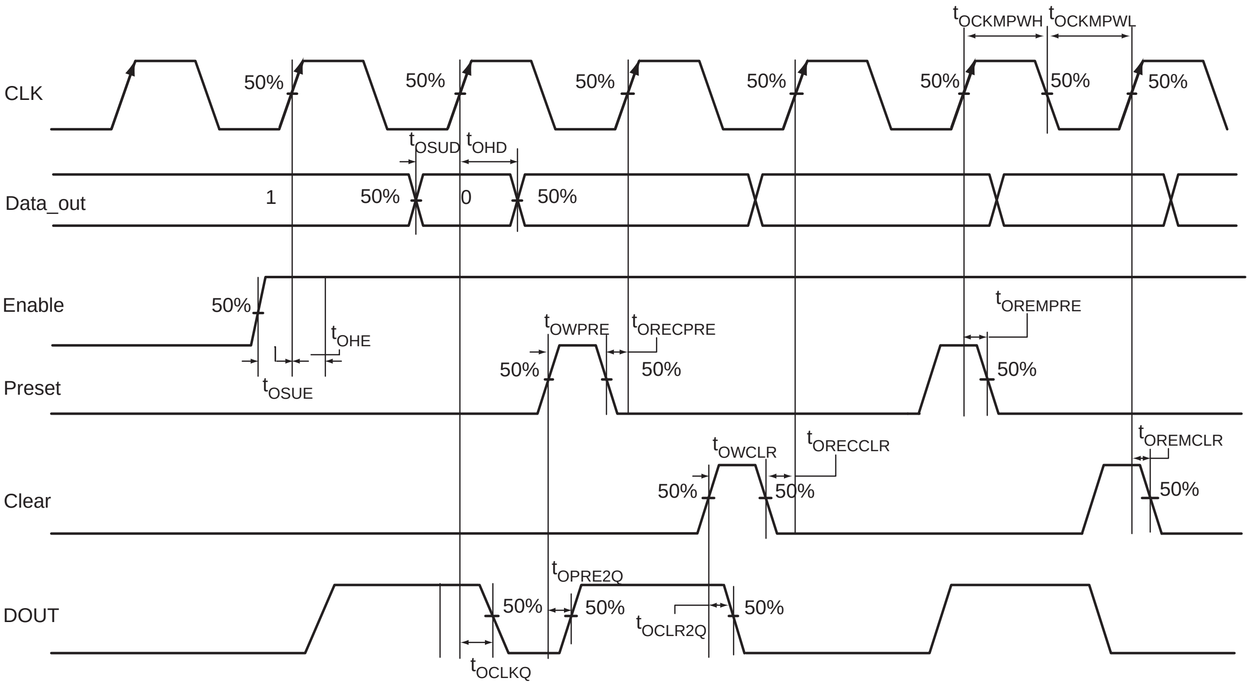


Figure 2-30 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-142 • **Output Data Register Propagation Delays**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.81	0.96	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.43	0.51	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.61	0.71	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.11	1.31	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.11	1.31	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.31	0.36	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.31	0.36	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-143 • **Output Data Register Propagation Delays**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.62	0.73	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	0.39	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.46	0.55	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.85	1.00	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.85	1.00	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	0.28	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	0.28	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Output Enable Register

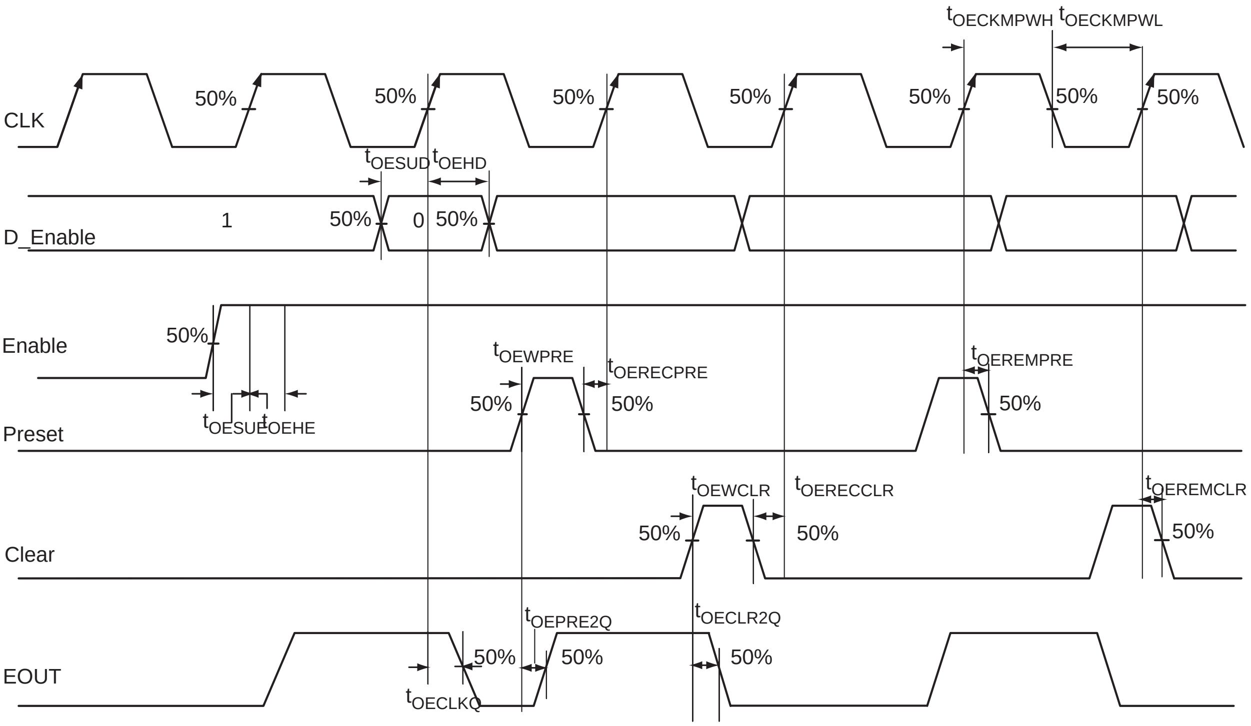


Figure 2-31 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-144 • **Output Enable Register Propagation Delays**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.62	0.72	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.43	0.51	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.60	0.71	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.92	1.08	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.92	1.08	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.31	0.36	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.31	0.36	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-145 • **Output Enable Register Propagation Delays**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.47	0.55	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.33	0.39	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.46	0.54	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.70	0.83	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.70	0.83	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	0.28	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	0.28	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

DDR Module Specifications

Input DDR Module

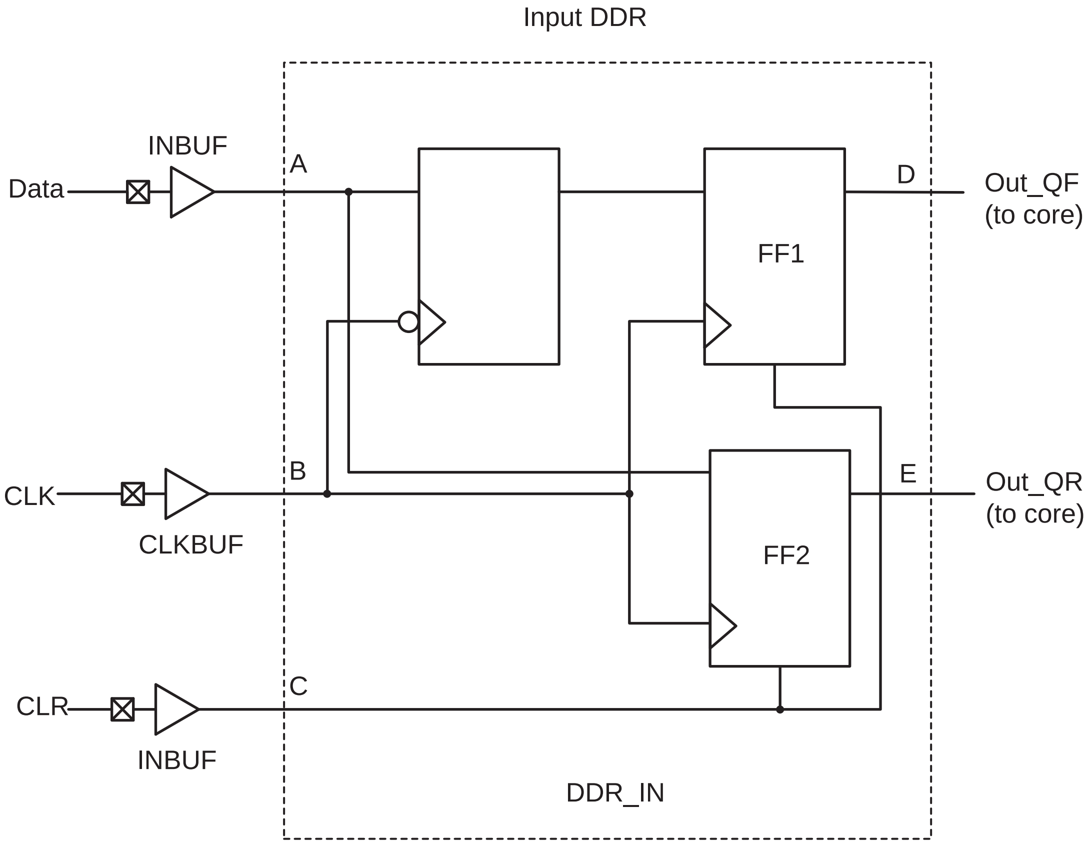


***Figure 2-32* • Input DDR Timing Model**

***Table 2-146* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

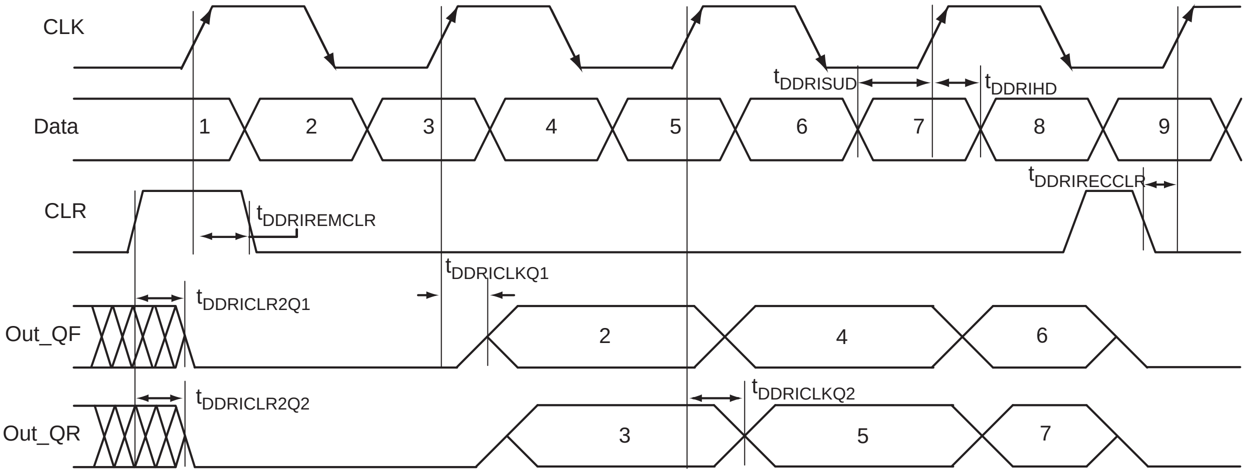


***Figure 2-33* • Input DDR Timing Diagram**

Timing Characteristics

***Table 2-147* • Input DDR Propagation Delays**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.38	0.45	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.54	0.63	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (fall)	0.39	0.46	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (rise)	0.34	0.40	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.64	0.75	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.79	0.93	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.31	0.36	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	0.22	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.31	0.36	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.28	0.32	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-148 • Input DDR Propagation Delays
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.29	0.34	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.41	0.48	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (fall)	0.30	0.35	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (rise)	0.26	0.31	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.49	0.58	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.60	0.71	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	0.28	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	0.22	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.31	0.36	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.28	0.32	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Output DDR Module

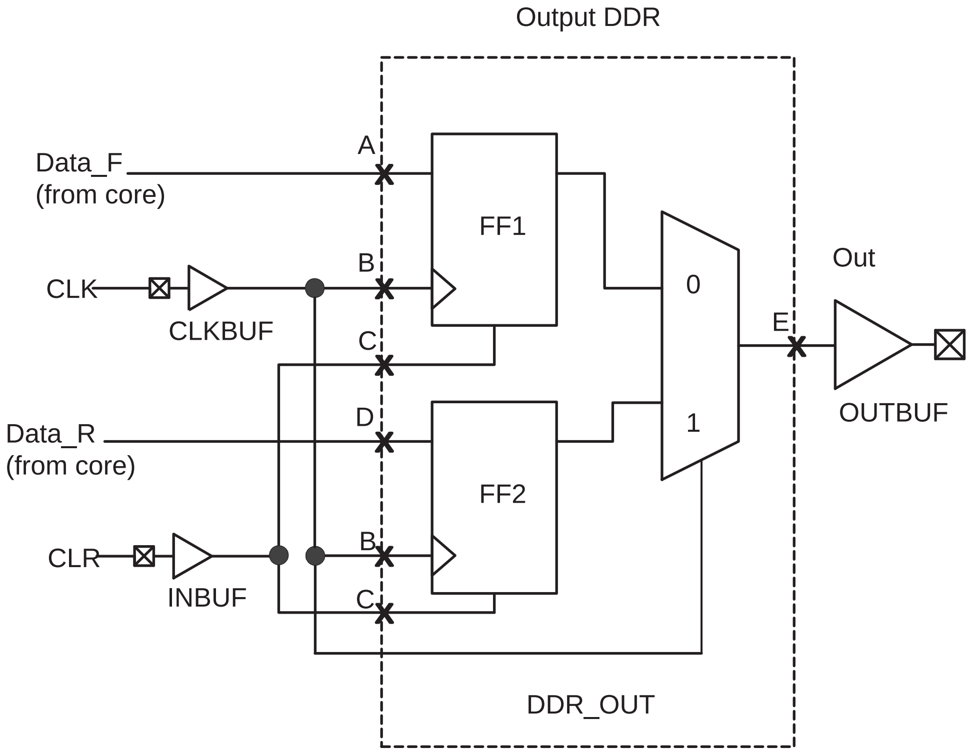


Figure 2-34 • **Output DDR Timing Model**

Table 2-149 • **Parameter Definitions**

Parameter Name	**Parameter Definition**	**Measuring Nodes (from, to)**
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

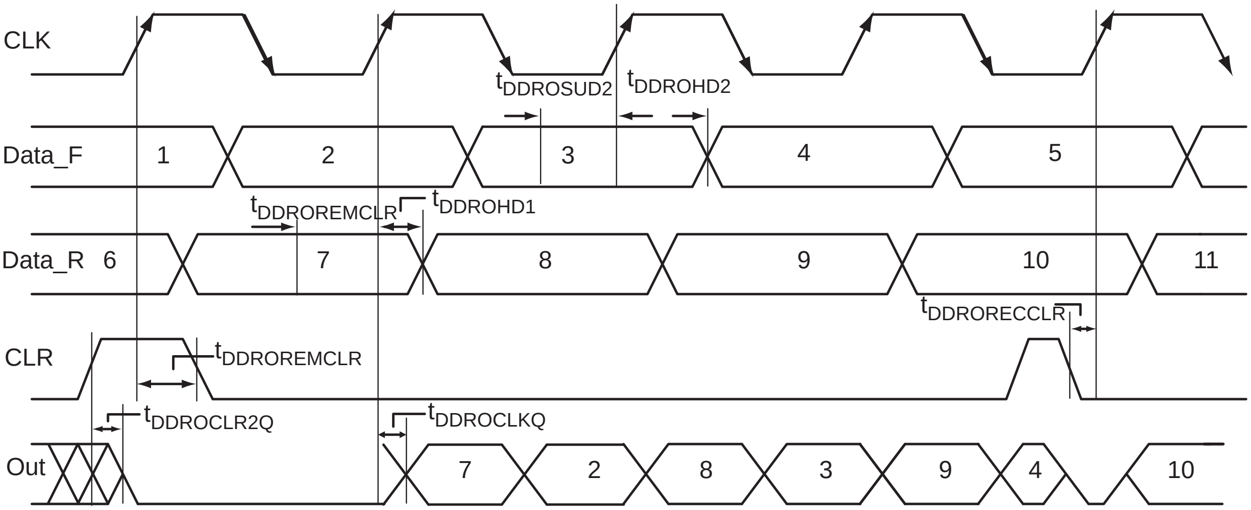


Figure 2-35 • **Output DDR Timing Diagram**

Timing Characteristics

Table 2-150 • **Output DDR Propagation Delays**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.97	1.14	ns
$t_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.52	0.62	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.52	0.62	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.11	1.30	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.31	0.36	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	0.22	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	0.36	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	0.32	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-151 **• Output DDR Propagation Delays**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.74	0.87	ns
$t_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.40	0.47	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.40	0.47	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.85	1.00	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	0.28	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	0.22	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	0.36	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	0.32	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The RT ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

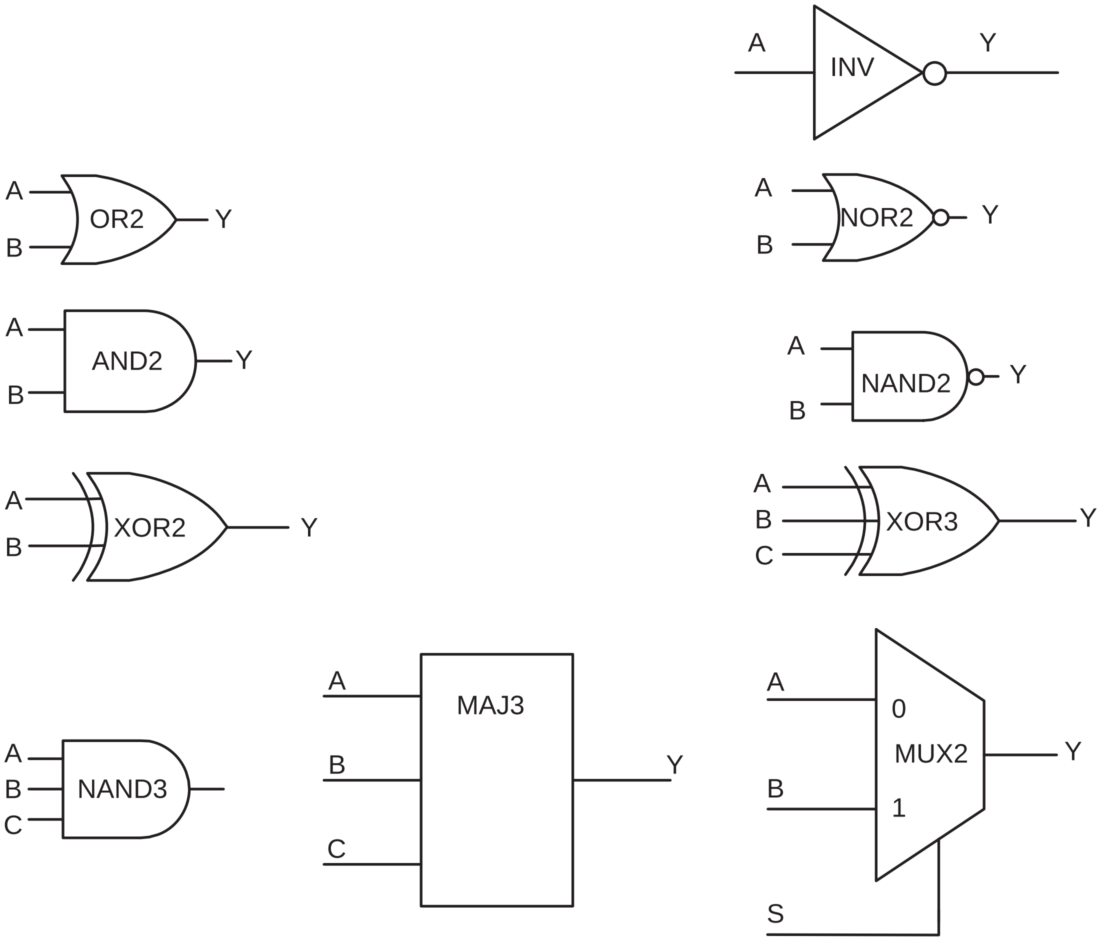


Figure 2-36 • **Sample of Combinatorial Cells**

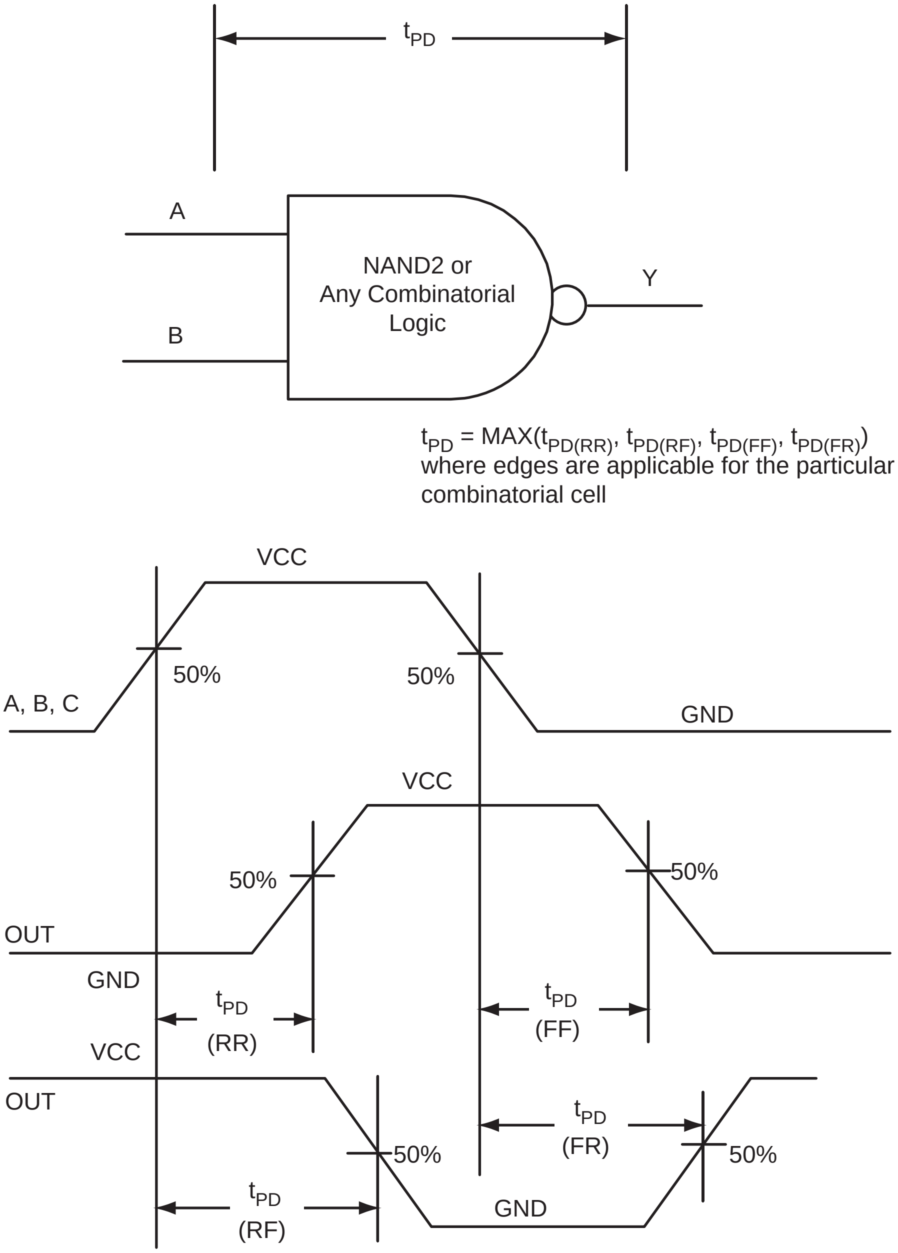


Figure 2-37 • **Timing Model and Waveforms**

Timing Characteristics

***Table 2-152* • Combinatorial Cell Propagation Delays**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	$Y = !A$	t_{PD}	0.56	0.65	ns
AND2	$Y = A \cdot B$	t_{PD}	0.65	0.77	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.65	0.77	ns
OR2	$Y = A + B$	t_{PD}	0.67	0.79	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.67	0.79	ns
XOR2	$Y = A \oplus B$	t_{PD}	1.02	1.20	ns
MAJ3	$Y = MAJ(A , B, C)$	t_{PD}	0.97	1.14	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.21	1.42	ns
MUX2	$Y = A\ !S + B\ S$	t_{PD}	0.70	0.82	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.78	0.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

***Table 2-153* • Combinatorial Cell Propagation Delays**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	$Y = !A$	t_{PD}	0.43	0.50	ns
AND2	$Y = A \cdot B$	t_{PD}	0.50	0.59	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.50	0.59	ns
OR2	$Y = A + B$	t_{PD}	0.51	0.61	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.51	0.61	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.78	0.92	ns
MAJ3	$Y = MAJ(A , B, C)$	t_{PD}	0.74	0.87	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.93	1.09	ns
MUX2	$Y = A\ !S + B\ S$	t_{PD}	0.54	0.63	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.59	0.70	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

VersaTile Specifications as a Sequential Module

The RT ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

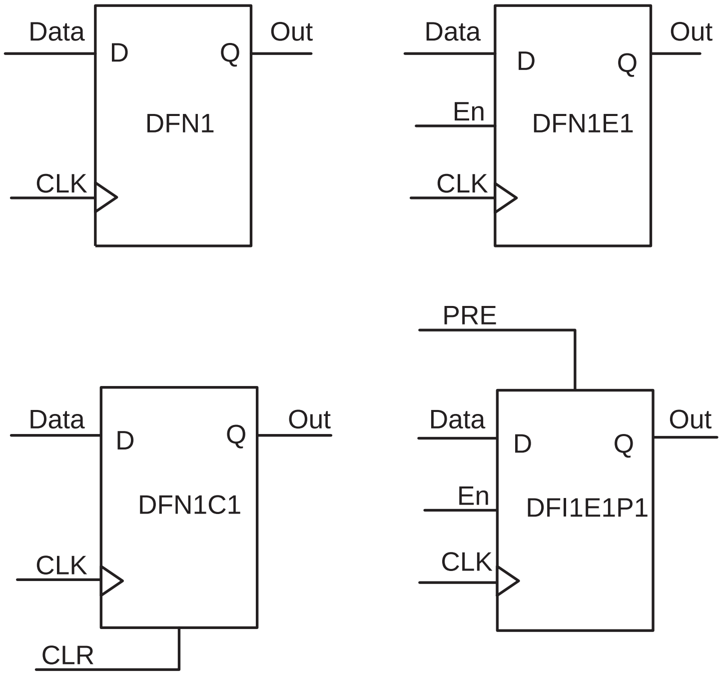


Figure 2-38 • **Sample of Sequential Cells**

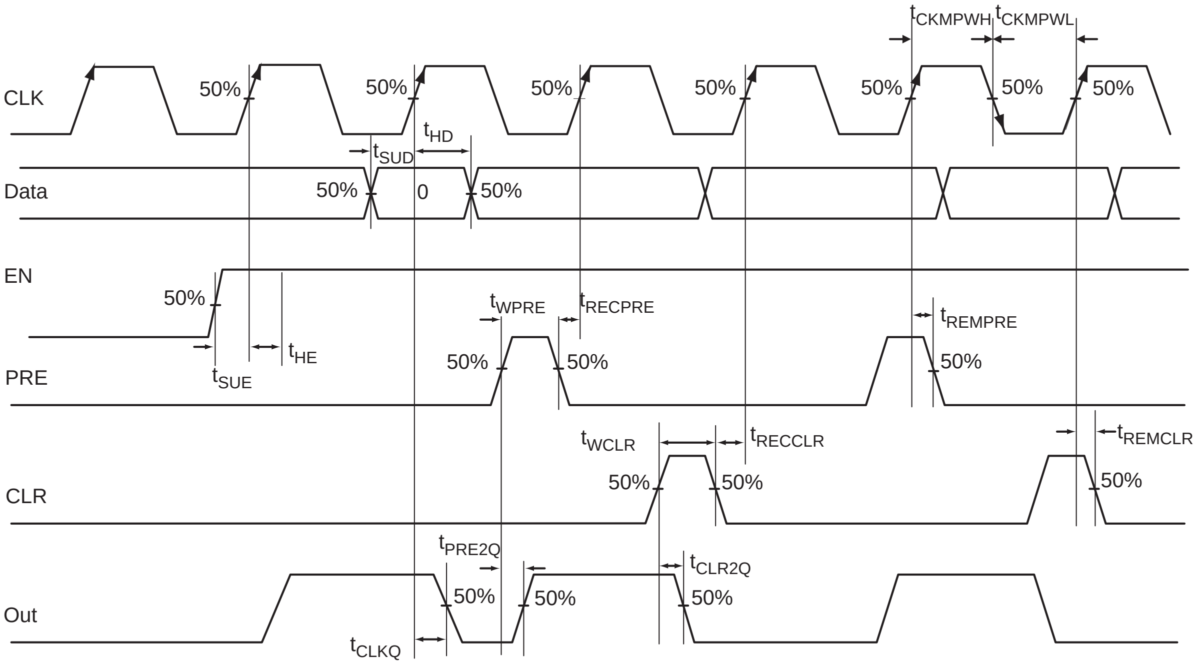


Figure 2-39 **• Timing Model and Waveforms**

Timing Characteristics

Table 2-154 • **Register Delays**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.76	0.90	ns
t_{SUD}	Data Setup Time for the Core Register	0.59	0.70	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.63	0.74	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.55	0.65	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.55	0.65	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.31	0.36	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.31	0.36	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	0.64	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-155 **• Register Delays**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.58	0.69	ns
t_{SUD}	Data Setup Time for the Core Register	0.45	0.53	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.48	0.57	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.42	0.50	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.42	0.50	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	0.28	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	0.28	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	0.64	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Global Resource Characteristics

RT3PE600L Clock Tree Topology

Clock delays are device-specific. Figure 2-40 is an example of a global tree used for clock routing. The global tree presented in Figure 2-40 is driven by a CCC located on the west side of the RT3PE600L device. It is used to drive all D-flip-flops in the device.

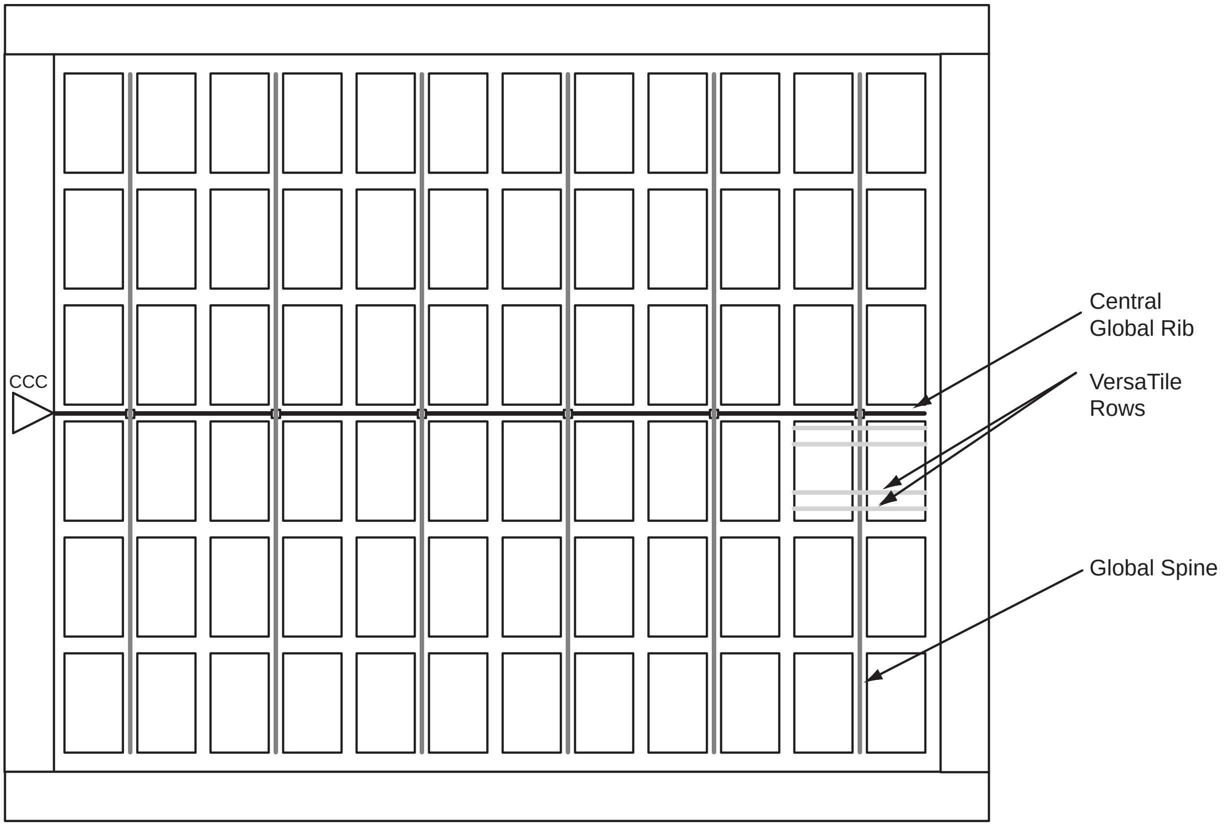


Figure 2-40 **• Example of Global Tree Use in an RT3PE600L Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-101. Table 2-156 to Table 2-159 on page 2-100 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-156 **• RT3PE600L Global Resource**
Military-Case Conditions: T_J = 125°C, VCC = 1.14 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.95	1.23	1.12	1.44	ns
t_{RCKH}	Input High Delay for Global Clock	0.94	1.26	1.10	1.48	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.15		1.35		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.33		1.56		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.32		0.38	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

Table 2-157 **• RT3PE3000L Global Resource**
Military-Case Conditions: T_J = 125°C, VCC = 1.14 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.81	2.09	2.13	2.45	ns
t_{RCKH}	Input High Delay for Global Clock	1.80	2.13	2.12	2.50	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.15		1.35		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.33		1.56		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.32		0.38	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

1.5 V DC Core Voltage

Table 2-158 • RT3PE600L Global Resource
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.82	1.07	0.97	1.26	ns
t_{RCKH}	Input High Delay for Global Clock	0.81	1.10	0.95	1.30	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.30		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

Table 2-159 • RT3PE3000L Global Resource
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.62	1.87	1.90	2.20	ns
t_{RCKH}	Input High Delay for Global Clock	1.61	1.90	1.89	2.24	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.30		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-160 • **RT ProASIC3 CCC/PLL Specification**
For Devices Operating at 1.2 V DC Core Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		360[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4]			100	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.2		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.5		ns
CCC Output Peak-to-Peak Period Jitter FCCC_OUT	Maximum peak-to-peak jitter data[6,7]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	0.60%	0.80%	1.60%
50 MHz to 160 MHz	2.50%	4.00%	6.00%	12.00%

Notes:

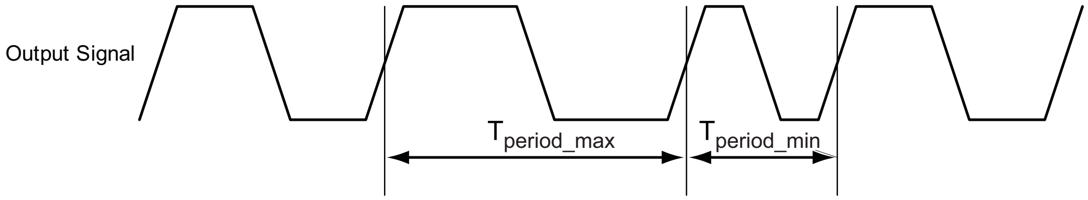
1. *This delay is a function of voltage and temperature. See Table 2-5 on page 2-7 for deratings.*
2. *T_J = 25°C, VCC = 1.2 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to SmartGen online help for more information.*
4. *Maximum value obtained for a –1 speed grade device in worst-case military conditions. For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*
6. *Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.14 V, VQ/PQ/TQ types of packages, 20 pF load.*
7. *Switching I/Os are placed outside of the PLL bank.*

Table 2-161 • RT ProASIC3 CCC/PLL Specification
For Devices Operating at 1.5 V DC Core Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		160[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4]			110	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			1.5	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		5.56	ns
Delay Range in Block: Fixed Delay [1, 2]		2.2		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum peak-to-peak period jitter data[6,7]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	0.50%	0.70%	1.00%
50 MHz to 200 MHz	1.00%	3.00%	5.00%	9.00%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-5 on page 2-7 for deratings.*
2. *T_J = 25°C, VCC = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to SmartGen online help for more information.*
4. *Maximum value obtained for a –1 speed grade device in worst-case military conditions. For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*
6. *Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.425 V, VQ/PQ/TQ types of packages, 20 pF load.*
7. *Switching I/Os are placed outside of the PLL bank.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-41 • Peak-to-Peak Jitter Definition

Embedded SRAM and FIFO Characteristics

SRAM

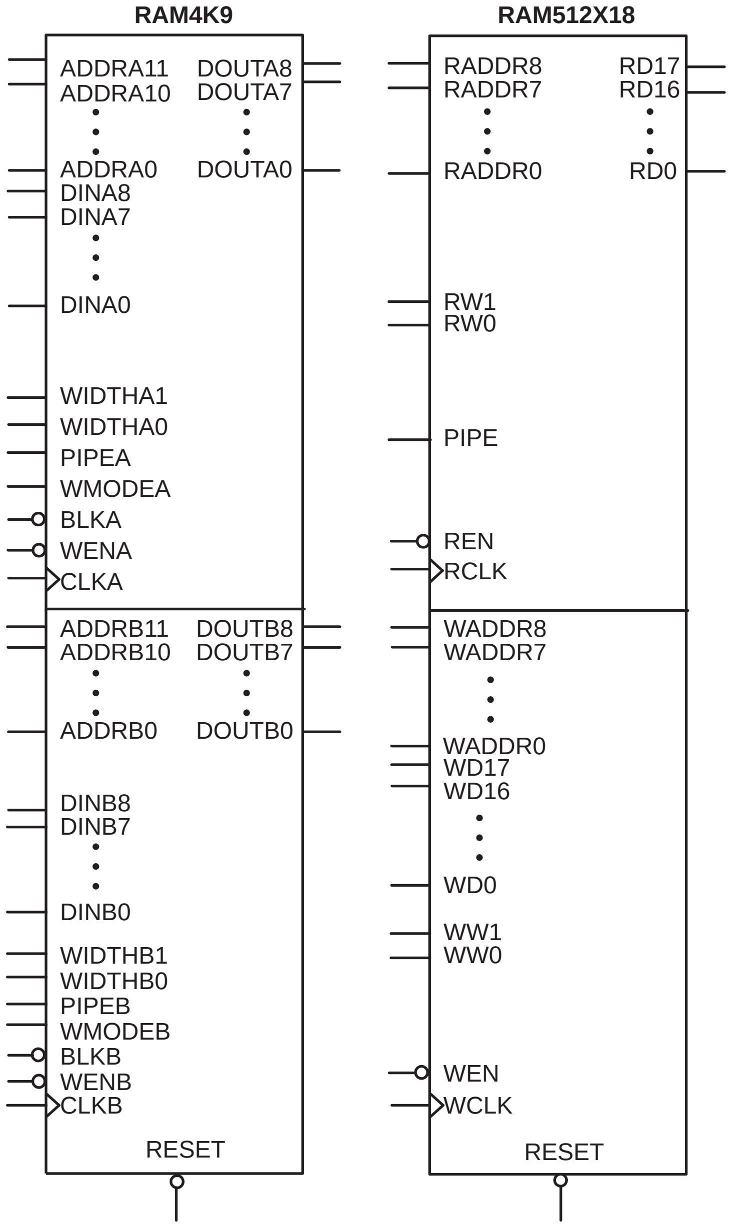


Figure 2-42 • **RAM Models**

Timing Waveforms

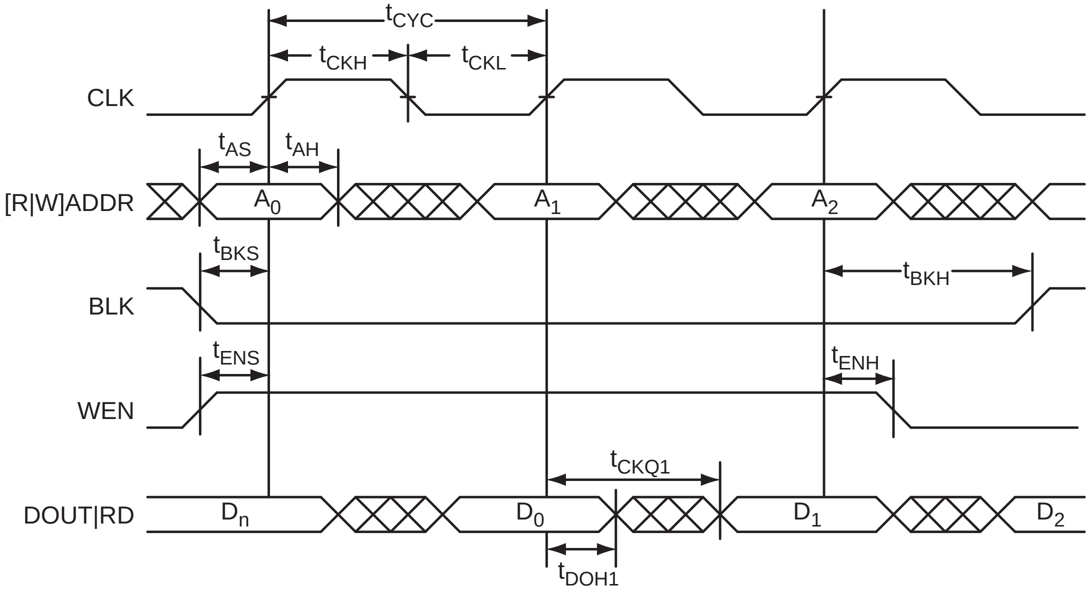


Figure 2-43 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512×18**

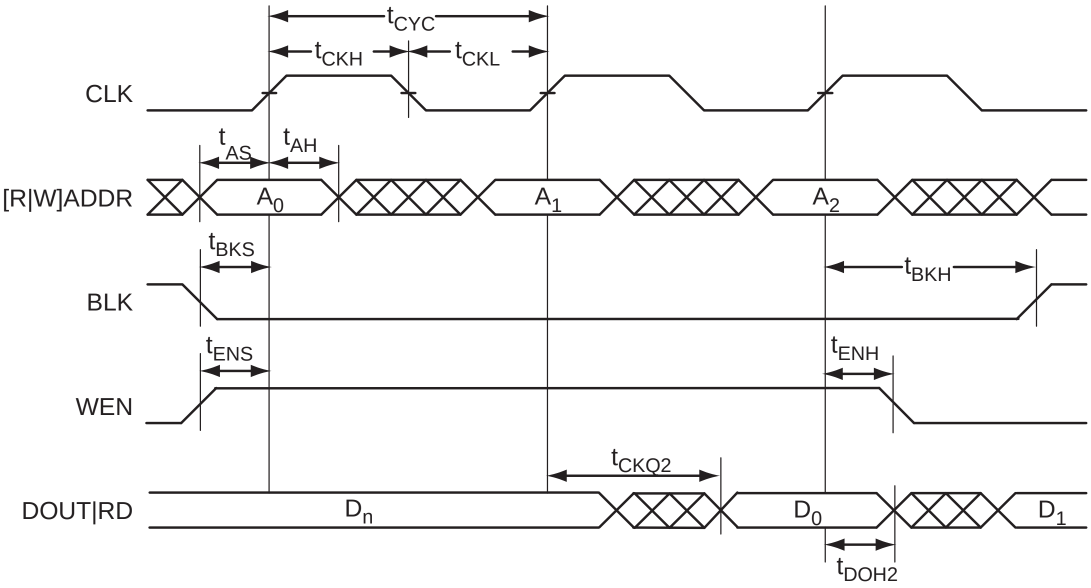


Figure 2-44 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512×18**

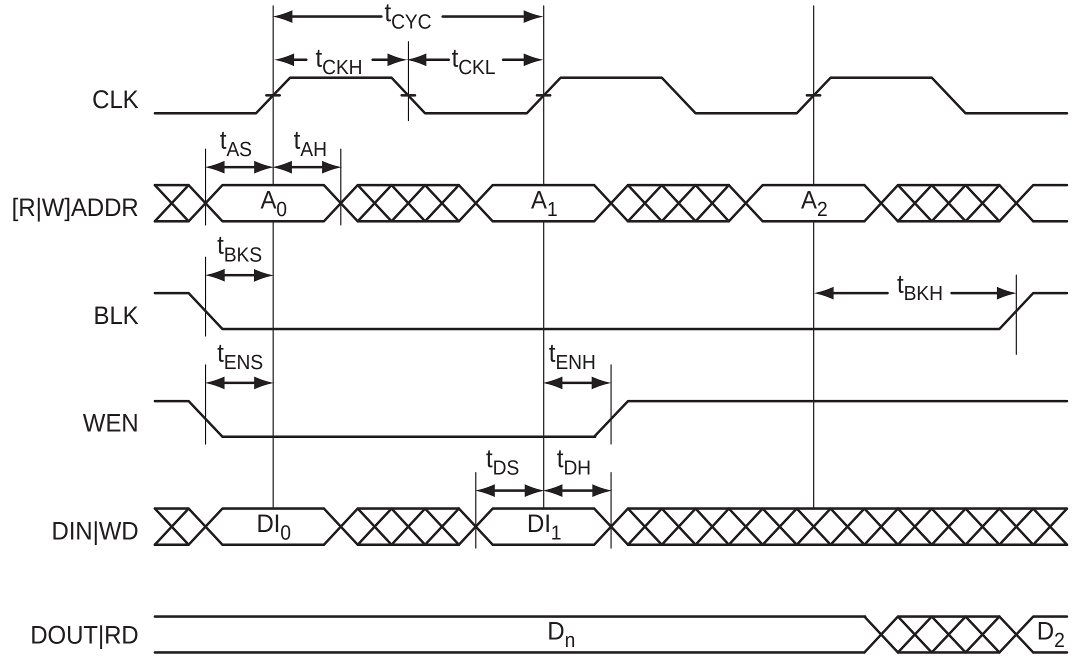


Figure 2-45 • **RAM Write, Output Retained Output. Applicable to Both RAM4K9 and RAM512×18**

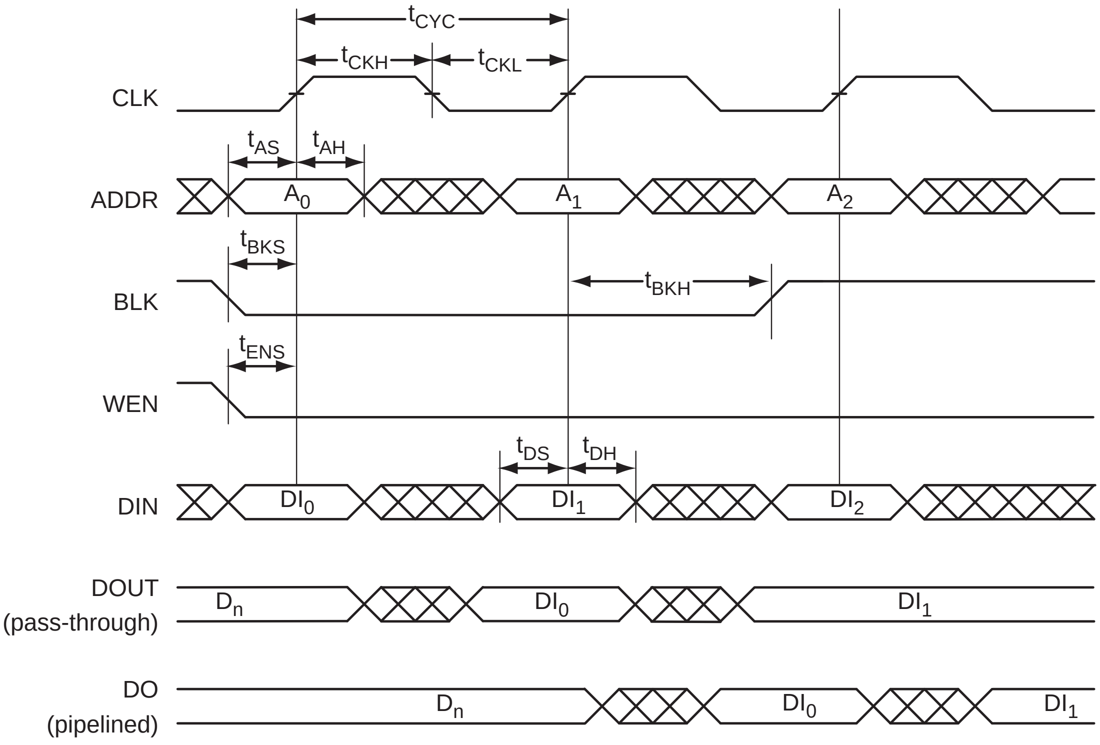


Figure 2-46 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

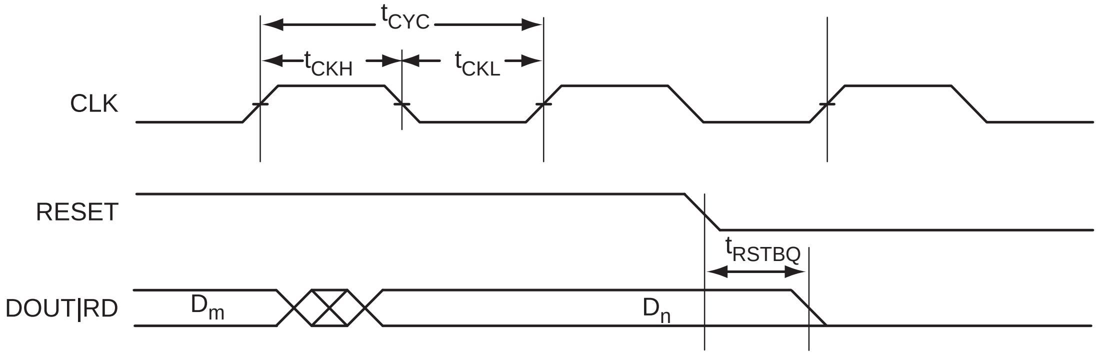


***Figure 2-47* • RAM Reset. Applicable to Both RAM4K9 and RAM512×18.**

Timing Characteristics

***Table 2-162* • RAM4K9**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.35	0.41	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.20	0.23	ns
t_{ENH}	REN, WEN hold time	0.13	0.16	ns
t_{BKS}	BLK setup time	0.32	0.38	ns
t_{BKH}	BLK hold time	0.03	0.03	ns
t_{DS}	Input data (DIN) setup time	0.25	0.30	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	3.26	3.84	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.47	2.91	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.24	1.46	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.25	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.27	0.32	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.37	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.28	1.50	ns
	RESET Low to data out Low on DOUT (pipelined)	1.28	1.50	ns
$t_{REMRSTB}$	RESET removal	0.40	0.47	ns
$t_{RECRSTB}$	RESET recovery	2.08	2.44	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.66	0.76	ns
t_{CYC}	Clock cycle time	6.08	6.99	ns
F_{MAX}	Maximum frequency	164	143	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

Table 2-163 **• RAM4K9**
Military-Case Conditions: T_J = 125℃, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.31	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.15	0.18	ns
t_{ENH}	REN, WEN hold time	0.10	0.12	ns
t_{BKS}	BLK setup time	0.25	0.29	ns
t_{BKH}	BLK hold time	0.02	0.02	ns
t_{DS}	Input data (DIN) setup time	0.19	0.23	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	2.50	2.93	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	1.89	2.22	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.95	1.11	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.24	0.29	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.20	0.24	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.25	0.30	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	0.98	1.15	ns
	RESET Low to data out Low on DOUT (pipelined)	0.98	1.15	ns
$t_{REMRSTB}$	RESET removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET recovery	1.59	1.87	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.59	0.67	ns
t_{CYC}	Clock cycle time	5.39	6.20	ns
F_{MAX}	Maximum frequency	185	161	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

***Table 2-164* • RAM512X18**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.35	0.41	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.13	0.15	ns
t_{ENH}	REN, WEN hold time	0.08	0.09	ns
t_{DS}	Input data (WD) setup time	0.25	0.30	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.99	3.52	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	1.24	1.46	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.25	0.29	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.31	0.36	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	1.28	1.50	ns
	RESET Low to data out Low on RD (pipelined)	1.28	1.50	ns
$t_{REMRSTB}$	RESET removal	0.40	0.47	ns
$t_{RECRSTB}$	RESET recovery	2.08	2.44	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.66	0.76	ns
t_{CYC}	Clock cycle time	6.08	6.99	ns
F_{MAX}	Maximum frequency	164	143	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

Table 2-165 **• RAM512X18**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.31	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.10	0.11	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.23	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.29	2.69	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.95	1.12	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.18	0.21	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.21	0.25	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	0.98	1.15	ns
	RESET Low to data out Low on RD (pipelined)	0.98	1.15	ns
$t_{REMRSTB}$	RESET removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET recovery	1.59	1.87	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.59	0.67	ns
t_{CYC}	Clock cycle time	5.39	6.20	ns
F_{MAX}	Maximum frequency	185	161	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.*

FIFO

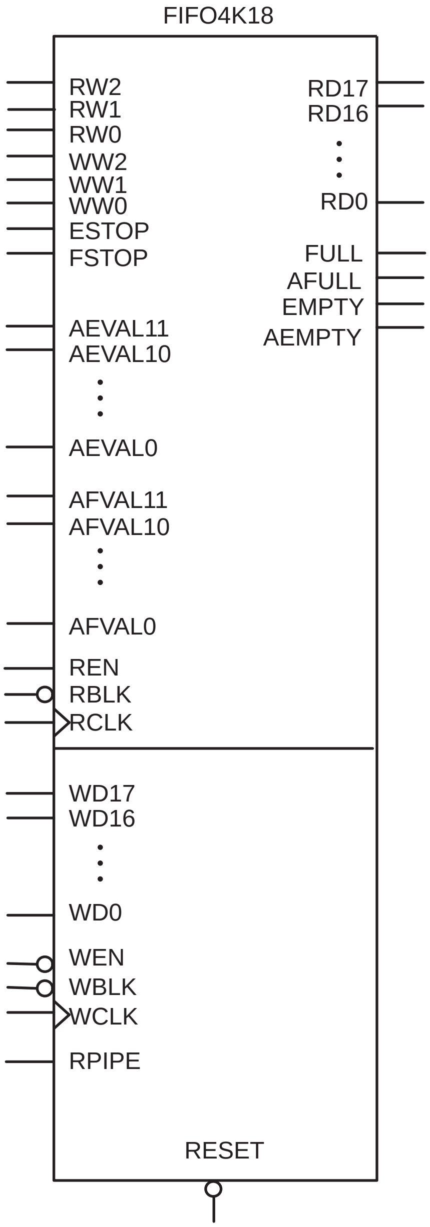


Figure 2-48 • **FIFO Model**

Timing Waveforms

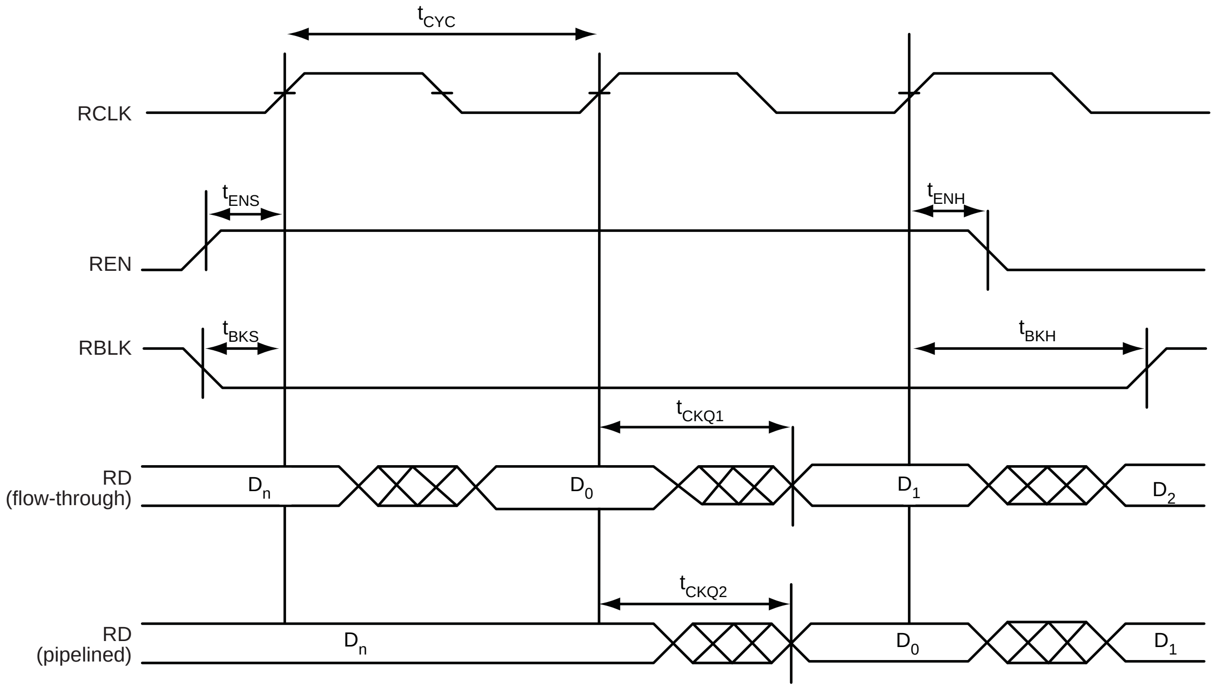


Figure 2-49 • **FIFO Read**

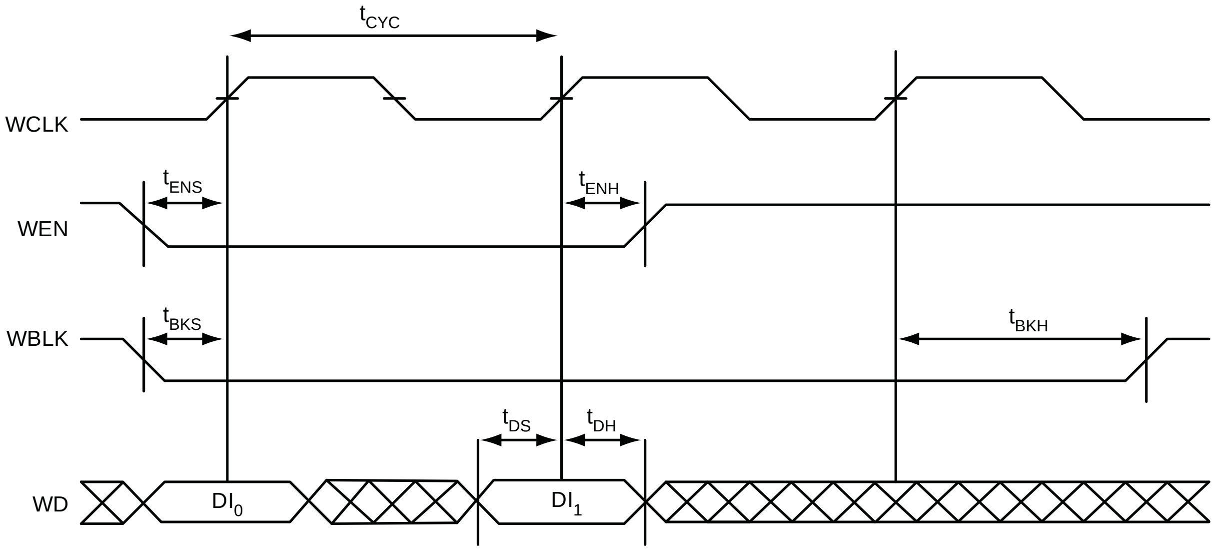


Figure 2-50 • **FIFO Write**

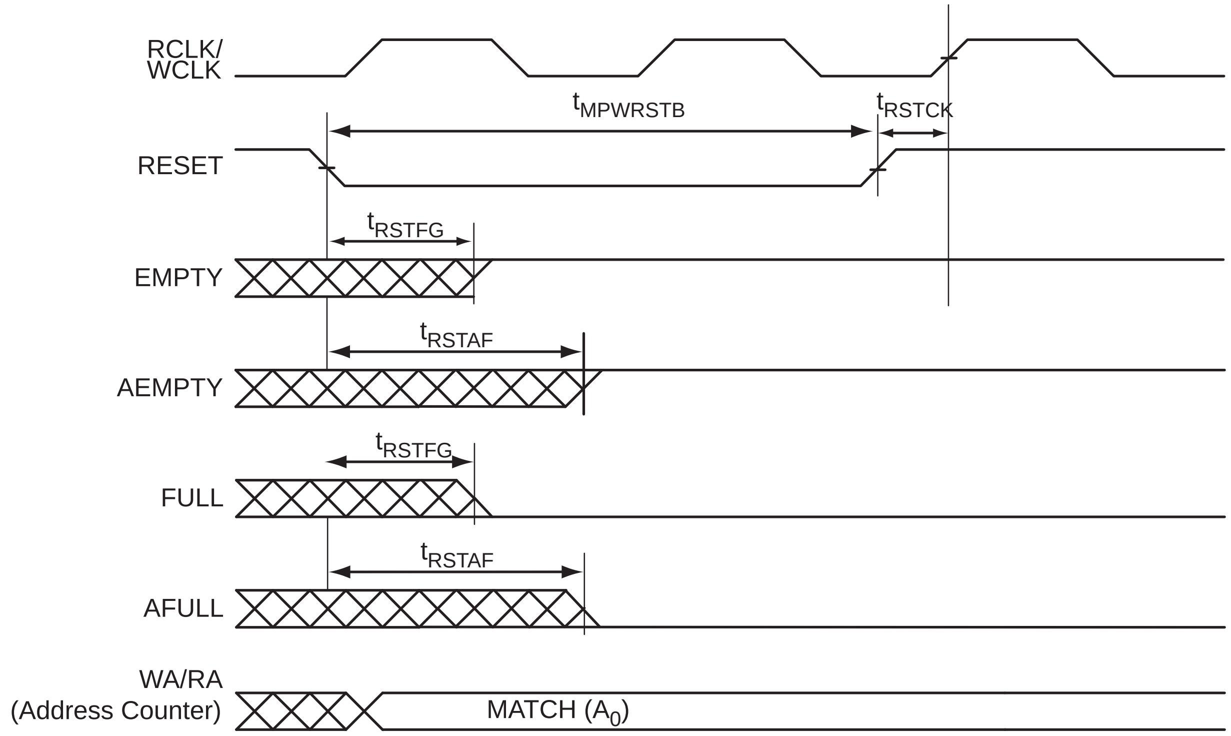


Figure 2-51 • **FIFO Reset**

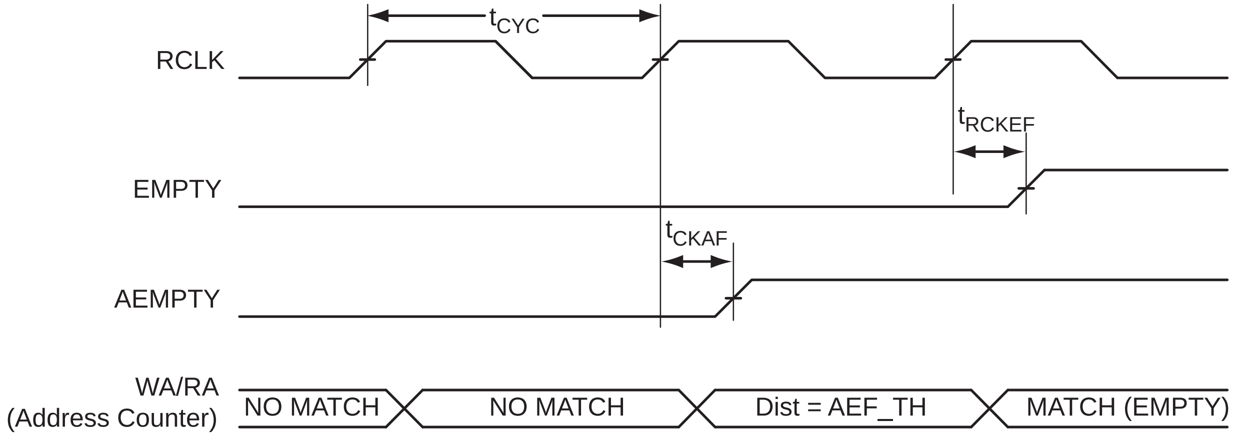


Figure 2-52 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

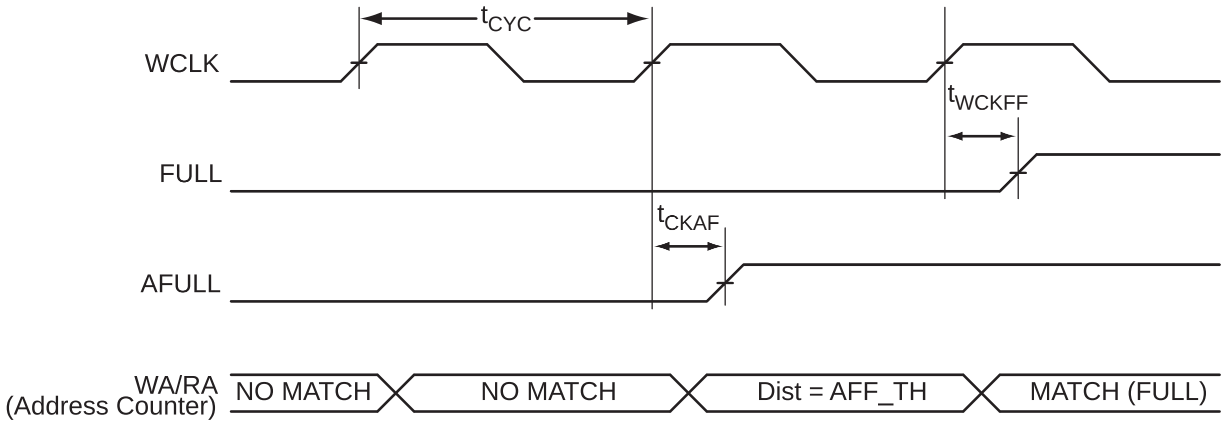


Figure 2-53 • **FIFO FULL Flag and AFULL Flag Assertion**

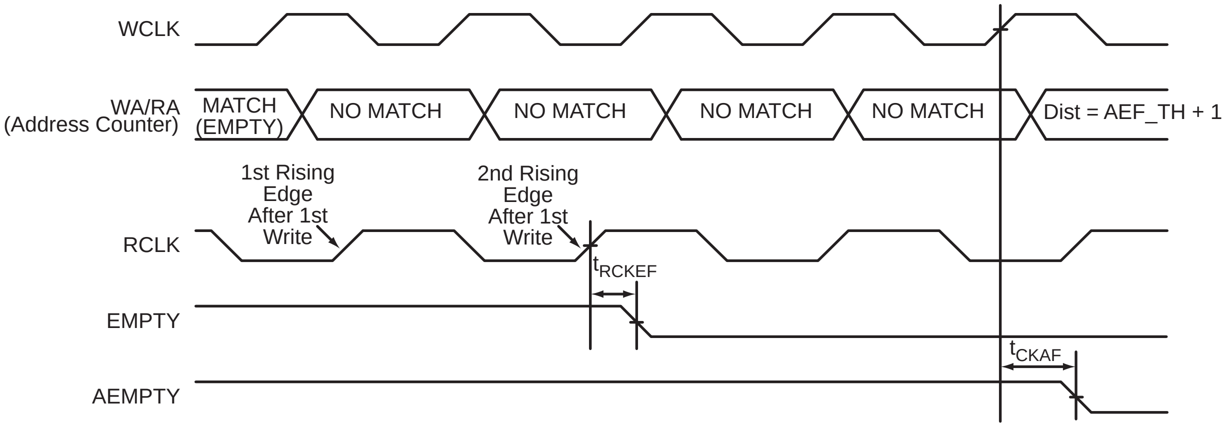


Figure 2-54 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

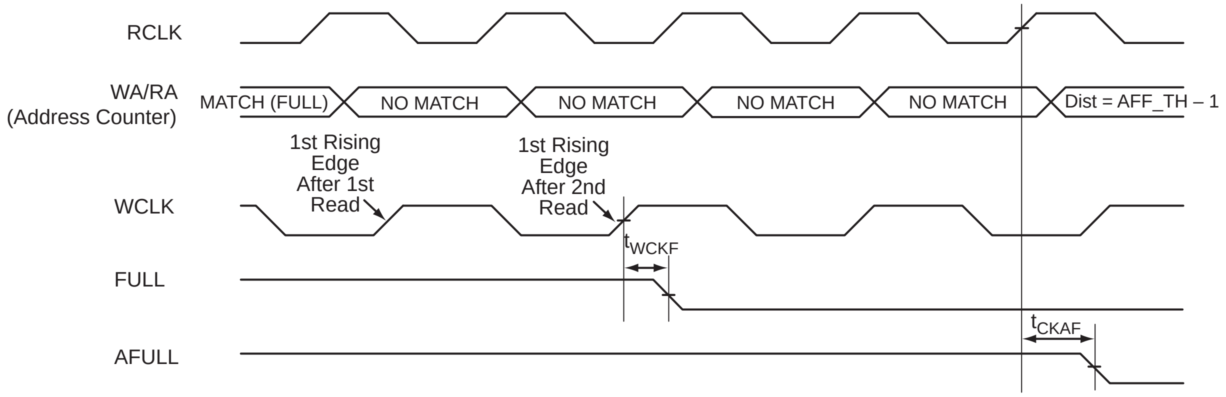


Figure 2-55 • **FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

***Table 2-166* • FIFO**
Worst Military-Case Conditions: T_J = 125°C, VCC = 1.14 V

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.91	2.24	ns
t_{ENH}	REN, WEN Hold Time	0.03	0.03	ns
t_{BKS}	BLK Setup Time	0.40	0.47	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.25	0.30	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	3.26	3.84	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.24	1.46	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.38	2.80	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.26	2.66	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	8.57	10.08	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.34	2.76	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	8.48	9.97	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.28	1.50	ns
	RESET Low to Data Out Low on RD (pipelined)	1.28	1.50	ns
$t_{REMRSTB}$	RESET Removal	0.40	0.47	ns
$t_{RECRSTB}$	RESET Recovery	2.08	2.44	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.66	0.76	ns
t_{CYC}	Clock Cycle Time	6.08	6.99	ns
F_{MAX}	Maximum Frequency for FIFO	164	143	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

***Table 2-167* • FIFO**
Worst Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.46	1.71	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.40	0.47	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.19	0.23	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.50	2.93	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.95	1.11	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.82	2.14	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.73	2.03	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.56	7.71	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.79	2.11	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.49	7.63	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.98	1.15	ns
	RESET Low to Data Out Low on RD (pipelined)	0.98	1.15	ns
$t_{REMRSTB}$	RESET Removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET Recovery	1.59	1.87	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.59	0.67	ns
t_{CYC}	Clock Cycle Time	5.39	6.20	ns
F_{MAX}	Maximum Frequency for FIFO	185	161	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Embedded FlashROM Characteristics

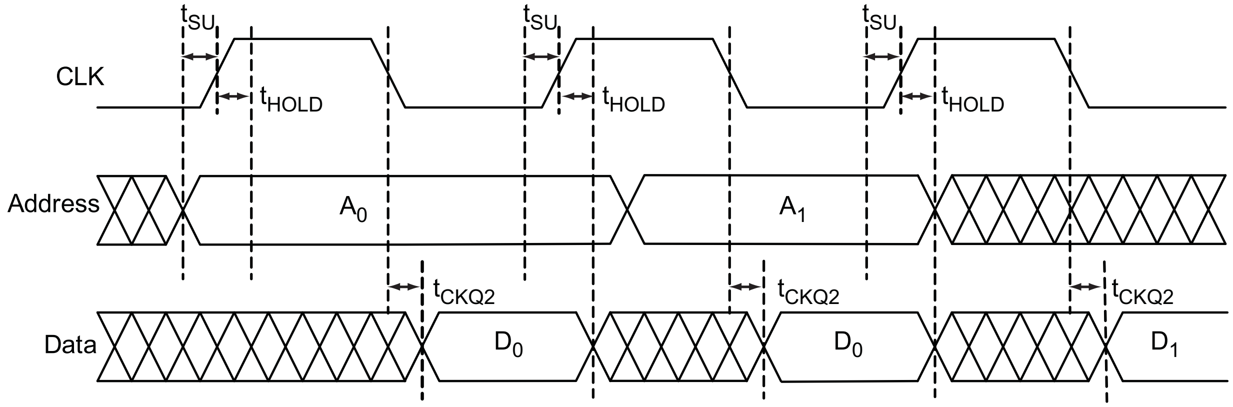


Figure 2-56 • **Timing Diagram**

Timing Characteristics

Table 2-168 • **Embedded FlashROM Access Time**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.74	0.87	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CK2Q}	Clock to Out	16.18	19.02	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

Table 2-169 • **Embedded FlashROM Access Time**
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.58	0.68	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CK2Q}	Clock to Out	12.77	15.01	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-16 for more details.

Timing Characteristics

***Table 2-170* • JTAG 1532**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.80	0.94	ns
t_{DIHD}	Test Data Input Hold Time	1.60	1.88	ns
t_{TMSSU}	Test Mode Select Setup Time	0.80	0.94	ns
t_{TMDHD}	Test Mode Select Hold Time	1.60	1.88	ns
t_{TCK2Q}	Clock to Q (data out)	6.39	7.52	ns
t_{RSTB2Q}	Reset to Q (data out)	26.63	31.33	ns
F_{TCKMAX}	TCK Maximum Frequency	18.70	15.90	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.48	0.56	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

***Table 2-171* • JTAG 1532**
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.60	0.71	ns
t_{DIHD}	Test Data Input Hold Time	1.21	1.42	ns
t_{TMSSU}	Test Mode Select Setup Time	0.60	0.71	ns
t_{TMDHD}	Test Mode Select Hold Time	1.21	1.42	ns
t_{TCK2Q}	Clock to Q (data out)	6.04	7.10	ns
t_{RSTB2Q}	Reset to Q (data out)	24.15	28.41	ns
F_{TCKMAX}	TCK Maximum Frequency	22.00	19.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.24	0.28	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-7 for derating values.

3 – Pin Descriptions

Supply Pins

GND	**Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ	**Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC	**Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V or 1.2 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx	**I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx	**I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F	**PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V.

When the PLLs are not used, the Microsemi Libero SoC place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *Radiation-Tolerant ProASIC3 Low Power Spaceflight FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on RT ProASIC3 devices.

VCOMPLA/B/C/D/E/F	**PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Microsemi Libero SoC place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on RT ProASIC3 devices.

VJTAG **JTAG Supply Voltage**

RT ProASIC3 devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP **Programming Supply Voltage**

During programming, VPUMP should be 3.3 V nominal. During operation, VPUMP should be tied to ground to optimize total ionizing dose performance in spaceflight applications.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User-Defined Supply Pins

VREF **I/O Voltage Reference**

Reference voltage for I/O minibanks in RT ProASIC3 devices. A minibank is the region of scope of a VREF pin. Refer to the "I/O Banks and I/O Standards Compatibility" section of the I/O Structures in IGLOOe and ProASIC3 Devices chapter of the *Radiation-Tolerant ProASIC Low Power Spaceflight FPGA Fabric User's Guide* for more information. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. 5 V input and output tolerance can be achieved with certain I/O standards and configuration; refer to the *Radiation-Tolerant ProASIC3 Low Power Spaceflight FPGA Fabric User's Guide* for more information.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *Radiation-Tolerant ProASIC3 Low Power*

Spaceflight FPGA Fabric User's Guide. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in IGLOOe and ProASIC3E Devices" section of the *Radiation-Tolerant ProASIC3 Low Power Spaceflight FPGA Fabric User's Guide* for an explanation of the naming of global pins.

FF Flash*Freeze Mode Activation Pin

Flash*Freeze mode is available on RT ProASIC3 devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O. The FF pin can be configured as a Schmitt trigger input.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for RT ProASIC3 devices. The Flash*Freeze pin location is independent of device, allowing migration to larger or smaller devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *Radiation-Tolerant ProASIC3 Low Power Spaceflight FPGA Fabric User's Guide* for more information on I/O states during Flash*Freeze mode.

Table 3-1 **• Flash*Freeze Pin Location in RT ProASIC3 Packages (device-independent)**

RT ProASIC3 Packages	Flash*Freeze Pin
CG/LG484	W6
CG/LG896	AH4

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

Table 3-2 gives JTAG pin recommendations for flight

***Table 3-2* • JTAG Pins – Recommendations for Flight**

JTAG Pins	Configurations
TCK	Tied off TCK to ground through a resistor placed close to the FPGA pins
TDO	Must be left unconnected
TDI	Can be left unconnected (equipped with internal weak pull-up resistor)
TMS	Can be left unconnected (equipped with internal weak pull-up resistor)
TRST	Tied off TRST to ground through a resistor placed close to the FPGA pin.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-3 for more information.

***Table 3-3* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-3 and must satisfy the parallel resistance value requirement. The values in Table 3-3 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Related Documents

User’s Guides

Radiation-Tolerant ProASIC3 Low Power Spaceflight FPGA Fabric User’s Guide

http://www.microsemi.com/soc/documents/RTPA3_UG.pdf

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

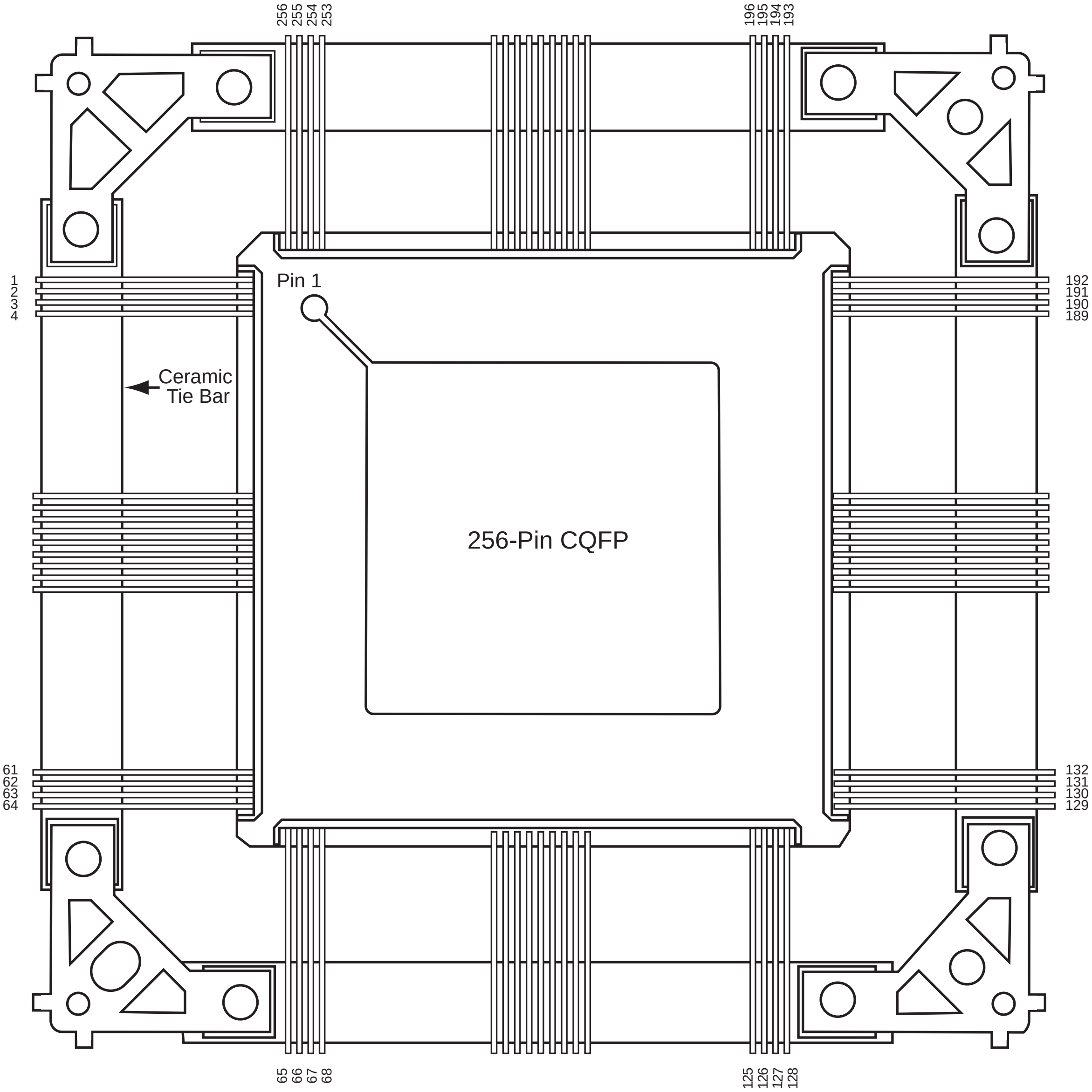
http://www.microsemi.com/soc/documents/PckgMechDrwngs.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are on the Microsemi SoC Products Group website at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

4 – Package Pin Assignments

CQ256



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CQ256	
Pin Number	RT3PE600L Function
1	VCCPLA
2	VCOMPLA
3	GNDQ
4	VCCIB7
5	GAC2/IO132PDB7V1
6	IO132NDB7V1
7	GAA2/IO134PDB7V1
8	IO134NDB7V1
9	VCC
10	GND
11	VCCIB7
12	IO128PDB7V1
13	IO128NDB7V1
14	IO130PDB7V1
15	IO130NDB7V1
16	IO124PDB7V0
17	IO124NDB7V0
18	IO126PDB7V0
19	IO126NDB7V0
20	VCC
21	GND
22	VCCIB7
23	IO123PDB7V0
24	IO123NDB7V0
25	IO122PDB7V0
26	IO122NDB7V0
27	GFC1/IO120PDB7V0
28	GFC0/IO120NDB7V0
29	GFB1/IO119PDB7V0
30	GFB0/IO119NDB7V0
31	GND
32	VCOMPLF
33	VCCPLF
34	GND
35	GFC2/IO115PDB6V1

CQ256	
Pin Number	RT3PE600L Function
36	IO115NDB6V1
37	GFA0/IO118NDB6V1
38	GFA1/IO118PDB6V1
39	IO112PDB6V1
40	IO112NDB6V1
41	IO114PDB6V1
42	IO114NDB6V1
43	VCC
44	GND
45	VCCIB6
46	IO109PDB6V0
47	IO109NDB6V0
48	IO110PDB6V0
49	IO110NDB6V0
50	IO108PDB6V0
51	IO108NDB6V0
52	IO106PDB6V0
53	IO106NDB6V0
54	VCC
55	GND
56	VCCIB6
57	GEC1/IO104PDB6V0
58	GEC0/IO104NDB6V0
59	GEA1/IO102PDB6V0
60	GEA0/IO102NDB6V0
61	VCCIB6
62	GNDQ
63	VCOMPLE
64	VCCPLE
65	GNDQ
66	IO101NDB5V2
67	GEA2/IO101PDB5V2
68	IO100NDB5V2
69	GEB2/IO100PDB5V2
70	VCC

CQ256	
Pin Number	RT3PE600L Function
71	GND
72	VCCIB5
73	IO98NDB5V2
74	IO98PDB5V2
75	IO94NDB5V1
76	IO94PDB5V1
77	IO96NDB5V2
78	IO96PDB5V2
79	IO92NDB5V1
80	IO92PDB5V1
81	GND
82	VCCIB5
83	IO90NDB5V1
84	IO90PDB5V1
85	IO93NDB5V1
86	IO93PDB5V1
87	IO88NDB5V0
88	IO88PDB5V0
89	VCC
90	GND
91	VCCIB5
92	IO86NDB5V0
93	IO86PDB5V0
94	IO87NDB5V0
95	IO87PDB5V0
96	IO80NDB4V1
97	IO80PDB4V1
98	IO79NDB4V1
99	IO79PDB4V1
100	VCC
101	GND
102	VCCIB4
103	IO78NDB4V1
104	IO78PDB4V1
105	IO76NDB4V1

CQ256	
Pin Number	**RT3PE600L Function**
106	IO76PDB4V1
107	IO77NDB4V1
108	IO77PDB4V1
109	GND
110	VCCIB4
111	IO74NDB4V1
112	IO74PDB4V1
113	IO71NDB4V0
114	IO71PDB4V0
115	IO72NDB4V0
116	IO72PDB4V0
117	IO70NDB4V0
118	GDC2/IO70PDB4V0
119	VCC
120	GND
121	VCCIB4
122	IO68NDB4V0
123	GDA2/IO68PDB4V0
124	GDB2/IO69PSB4V0
125	GNDQ
126	TCK
127	TDI
128	TMS
129	VCCPLD
130	VCOMPLD
131	VPUMP
132	GNDQ
133	TDO
134	TRST
135	VJTAG
136	GDB0/IO66NDB3V1
137	GDB1/IO66PDB3V1
138	IO64NDB3V1
139	IO64PDB3V1
140	VCCIB3

CQ256	
Pin Number	**RT3PE600L Function**
141	GND
142	VCC
143	IO62NDB3V1
144	IO62PDB3V1
145	IO60NDB3V1
146	IO60PDB3V1
147	IO61NDB3V1
148	IO61PDB3V1
149	VCCIB3
150	GND
151	VCC
152	IO58NDB3V0
153	IO58PDB3V0
154	IO56NDB3V0
155	IO56PDB3V0
156	IO55NDB3V0
157	GCC2/IO55PDB3V0
158	GCA1/IO52PDB3V0
159	GCA0/IO52NDB3V0
160	GND
161	VCCPLC
162	VCOMPLC
163	GND
164	IO49PSB2V1
165	GCC0/IO50NDB2V1
166	GCC1/IO50PDB2V1
167	IO48NDB2V1
168	IO48PDB2V1
169	IO47NDB2V1
170	IO47PDB2V1
171	IO46NDB2V1
172	IO46PDB2V1
173	VCCIB2
174	GND
175	VCC

CQ256	
Pin Number	**RT3PE600L Function**
176	IO44NDB2V1
177	IO44PDB2V1
178	IO42NDB2V0
179	IO42PDB2V0
180	IO40NDB2V0
181	IO40PDB2V0
182	VCCIB2
183	GND
184	VCC
185	IO38NDB2V0
186	GBC2/IO38PDB2V0
187	IO36NDB2V0
188	GBA2/IO36PDB2V0
189	VCCIB2
190	GNDQ
191	VCOMPLB
192	VCCPLB
193	GNDQ
194	GBA1/IO35PDB1V1
195	GBA0/IO35NDB1V1
196	GBB1/IO34PDB1V1
197	GBB0/IO34NDB1V1
198	VCCIB1
199	GND
200	VCC
201	GBC1/IO33PDB1V1
202	GBC0/IO33NDB1V1
203	IO29PDB1V1
204	IO29NDB1V1
205	IO30PDB1V1
206	IO30NDB1V1
207	VCCIB1
208	GND
209	IO31PDB1V1
210	IO31NDB1V1

CQ256	
Pin Number	RT3PE600L Function
211	IO25PDB1V0
212	IO25NDB1V0
213	IO27PDB1V0
214	IO27NDB1V0
215	IO24PDB1V0
216	IO24NDB1V0
217	VCCIB1
218	GND
219	VCC
220	IO23PDB1V0
221	IO23NDB1V0
222	IO22PDB1V0
223	IO22NDB1V0
224	IO19PDB0V2
225	IO19NDB0V2
226	IO15PDB0V2
227	IO15NDB0V2
228	VCCIB0
229	GND
230	VCC
231	IO13PDB0V2
232	IO13NDB0V2
233	IO11PDB0V1
234	IO11NDB0V1
235	IO14PDB0V2
236	IO14NDB0V2
237	IO09PDB0V1
238	IO09NDB0V1
239	VCCIB0
240	GND
241	IO05PDB0V0
242	IO05NDB0V0
243	IO08PDB0V1
244	IO08NDB0V1
245	IO07PDB0V1

CQ256	
Pin Number	RT3PE600L Function
246	IO07NDB0V1
247	IO03PDB0V0
248	IO03NDB0V0
249	VCCIB0
250	GND
251	VCC
252	GAB1/IO01PDB0V0
253	GAB0/IO01NDB0V0
254	GAA1/IO00PDB0V0
255	GAA0/IO00NDB0V0
256	GNDQ

CQ256	
Pin Number	**RT3PE3000L Function**
1	VCCPLA
2	VCOMPLA
3	GNDQ
4	VCCIB7
5	GAB2/IO308PDB7V4
6	IO308NDB7V4
7	GAA2/IO309PDB7V4
8	IO309NDB7V4
9	VCC
10	GND
11	VCCIB7
12	IO304PDB7V3
13	IO304NDB7V3
14	IO299PDB7V3
15	IO299NDB7V3
16	IO296PDB7V2
17	IO296NDB7V2
18	IO291PDB7V2
19	IO291NDB7V2
20	VCC
21	GND
22	VCCIB7
23	IO288PDB7V1
24	IO288NDB7V1
25	IO283PDB7V1
26	IO283NDB7V1
27	IO280PDB7V0
28	IO280NDB7V0
29	GFC1/IO275PDB7V0
30	GFC0/IO275NDB7V0
31	GND
32	VCOMPLF
33	VCCPLF
34	GND
35	IO267PDB6V4
36	IO267NDB6V4
37	GFA0/IO273NDB6V4
38	GFA1/IO273PDB6V4
39	IO259PDB6V3
40	IO259NDB6V3
41	IO264PDB6V3
42	IO264NDB6V3
43	VCC
44	GND
45	VCCIB6
46	IO251PDB6V2
47	IO251NDB6V2
48	IO256PDB6V2
49	IO256NDB6V2
50	IO243PDB6V1
51	IO243NDB6V1
52	IO248PDB6V1
53	IO248NDB6V1
54	VCC
55	GND
56	VCCIB6
57	GEB1/IO235PDB6V0
58	GEB0/IO235NDB6V0
59	IO240PDB6V0
60	IO240NDB6V0
61	VCCIB6
62	GNDQ
63	VCOMPLE
64	VCCPLE
65	GNDQ
66	IO233NDB5V4
67	GEA2/IO233PDB5V4
68	IO232NDB5V4
69	GEB2/IO232PDB5V4
70	VCC
71	GND
72	VCCIB5
73	IO223NDB5V3
74	IO223PDB5V3
75	IO226NDB5V4
76	IO226PDB5V4
77	IO215NDB5V2
78	IO215PDB5V2
79	IO218NDB5V3
80	IO218PDB5V3
81	GND
82	VCCIB5
83	IO207NDB5V1
84	IO207PDB5V1
85	IO210NDB5V2
86	IO210PDB5V2
87	IO199NDB5V0
88	IO199PDB5V0
89	VCC
90	GND
91	VCCIB5
92	IO202NDB5V1
93	IO202PDB5V1
94	IO194NDB5V0
95	IO194PDB5V0
96	IO192NDB4V4
97	IO192PDB4V4
98	IO186NDB4V4
99	IO186PDB4V4
100	VCC
101	GND
102	VCCIB4
103	IO183NDB4V3
104	IO183PDB4V3
105	IO178NDB4V3

CQ256	
Pin Number	**RT3PE3000L Function**
106	IO178PDB4V3
107	IO175NDB4V2
108	IO175PDB4V2
109	GND
110	VCCIB4
111	IO170NDB4V2
112	IO170PDB4V2
113	IO167NDB4V1
114	IO167PDB4V1
115	IO162NDB4V1
116	IO162PDB4V1
117	IO159NDB4V0
118	IO159PDB4V0
119	VCC
120	GND
121	VCCIB4
122	IO154NDB4V0
123	GDA2/IO154PDB4V0
124	GDB2/IO155PSB4V0
125	GNDQ
126	TCK
127	TDI
128	TMS
129	VCCPLD
130	VCOMPLD
131	VPUMP
132	GNDQ
133	TDO
134	TRST
135	VJTAG
136	GDB0/IO152NDB3V4
137	GDB1/IO152PDB3V4
138	IO139NDB3V3
139	IO139PDB3V3
140	VCCIB3

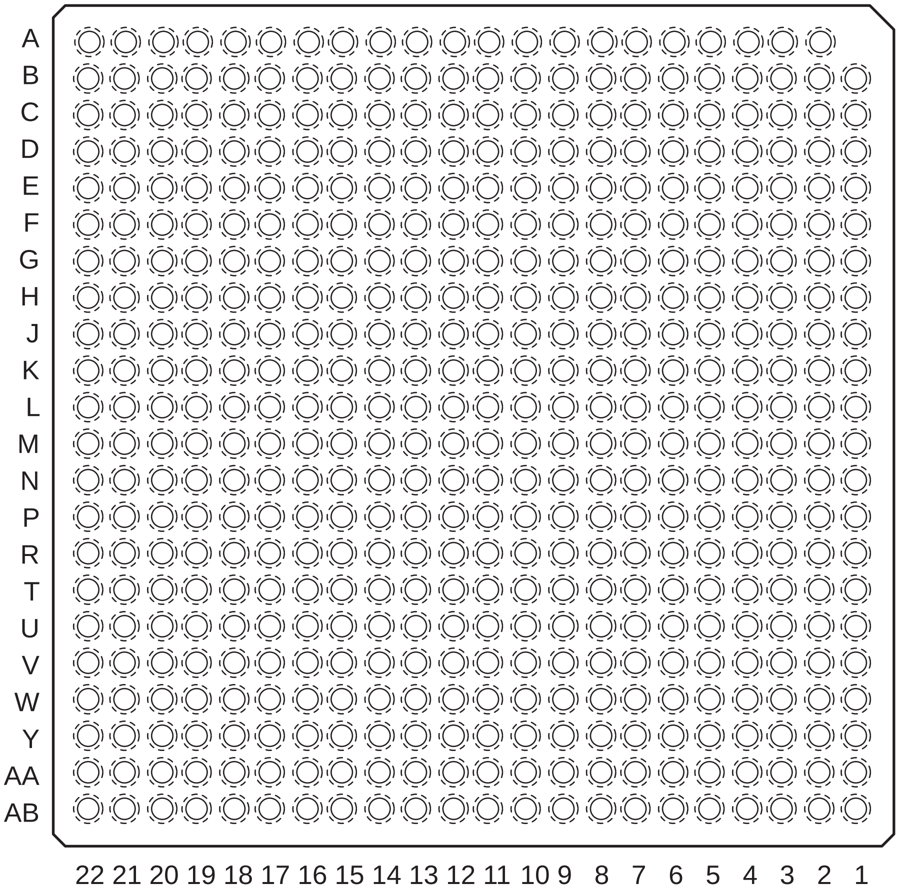
CQ256	
Pin Number	**RT3PE3000L Function**
141	GND
142	VCC
143	IO144NDB3V3
144	IO144PDB3V3
145	IO131NDB3V2
146	IO131PDB3V2
147	IO136NDB3V2
148	IO136PDB3V2
149	VCCIB3
150	GND
151	VCC
152	IO128NDB3V1
153	IO128PDB3V1
154	IO123NDB3V1
155	IO123PDB3V1
156	IO120NDB3V0
157	IO120PDB3V0
158	GCA1/IO114PDB3V0
159	GCA0/IO114NDB3V0
160	GND
161	VCCPLC
162	VCOMPLC
163	GND
164	GCB1/IO113PSB2V3
165	GCC0/IO112NDB2V3
166	GCC1/IO112PDB2V3
167	IO107NDB2V3
168	IO107PDB2V3
169	IO104NDB2V2
170	IO104PDB2V2
171	IO99NDB2V2
172	IO99PDB2V2
173	VCCIB2
174	GND
175	VCC

CQ256	
Pin Number	**RT3PE3000L Function**
176	IO96NDB2V1
177	IO96PDB2V1
178	IO91NDB2V1
179	IO91PDB2V1
180	IO88NDB2V0
181	IO88PDB2V0
182	VCCIB2
183	GND
184	VCC
185	IO83NDB2V0
186	GBB2/IO83PDB2V0
187	IO82NDB2V0
188	GBA2/IO82PDB2V0
189	VCCIB2
190	GNDQ
191	VCOMPLB
192	VCCPLB
193	GNDQ
194	GBA1/IO81PDB1V4
195	GBA0/IO81NDB1V4
196	GBB1/IO80PDB1V4
197	GBB0/IO80NDB1V4
198	VCCIB1
199	GND
200	VCC
201	IO75PDB1V4
202	IO75NDB1V4
203	IO72PDB1V3
204	IO72NDB1V3
205	IO67PDB1V3
206	IO67NDB1V3
207	VCCIB1
208	GND
209	IO64PDB1V2
210	IO64NDB1V2

CQ256	
Pin Number	**RT3PE3000L Function**
211	IO59PDB1V2
212	IO59NDB1V2
213	IO56PDB1V1
214	IO56NDB1V1
215	IO51PDB1V1
216	IO51NDB1V1
217	VCCIB1
218	GND
219	VCC
220	IO48PDB1V0
221	IO48NDB1V0
222	IO42PDB1V0
223	IO42NDB1V0
224	IO40PDB0V4
225	IO40NDB0V4
226	IO32PDB0V3
227	IO32NDB0V3
228	VCCIB0
229	GND
230	VCC
231	IO35PDB0V4
232	IO35NDB0V4
233	IO24PDB0V2
234	IO24NDB0V2
235	IO27PDB0V3
236	IO27NDB0V3
237	IO16PDB0V1
238	IO16NDB0V1
239	VCCIB0
240	GND
241	IO19PDB0V2
242	IO19NDB0V2
243	IO08PDB0V0
244	IO08NDB0V0
245	IO11PDB0V1

CQ256	
Pin Number	**RT3PE3000L Function**
246	IO11NDB0V1
247	GAC1/IO02PDB0V0
248	GAC0/IO02NDB0V0
249	VCCIB0
250	GND
251	VCC
252	GAB1/IO01PDB0V0
253	GAB0/IO01NDB0V0
254	GAA1/IO00PDB0V0
255	GAA0/IO00NDB0V0
256	GNDQ

CG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CG484	
Pin Number	**RT3PE600L**
A2	GND
A3	VCCIB0
A4	IO06NDB0V1
A5	IO06PDB0V1
A6	IO08NDB0V1
A7	IO08PDB0V1
A8	IO11PDB0V1
A9	IO17PDB0V2
A10	IO18NDB0V2
A11	IO18PDB0V2
A12	IO22PDB1V0
A13	IO26PDB1V0
A14	IO29NDB1V1
A15	IO29PDB1V1
A16	IO31NDB1V1
A17	IO31PDB1V1
A18	IO32NDB1V1
A19	NC
A20	VCCIB1
A21	GND
A22	GND
AA1	GND
AA2	VCCIB6
AA3	NC
AA4	IO98PDB5V2
AA5	IO96NDB5V2
AA6	IO96PDB5V2
AA7	IO86NDB5V0
AA8	IO86PDB5V0
AA9	IO85PDB5V0
AA10	IO85NDB5V0
AA11	IO78PPB4V1
AA12	IO79NDB4V1
AA13	IO79PDB4V1
AA14	NC
AA15	NC
AA16	IO71NDB4V0
AA17	IO71PDB4V0
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO97NDB5V2
AB5	IO97PDB5V2
AB6	IO93NDB5V1
AB7	IO93PDB5V1
AB8	IO87NDB5V0
AB9	IO87PDB5V0
AB10	NC
AB11	NC
AB12	IO75NDB4V1
AB13	IO75PDB4V1
AB14	IO72NDB4V0
AB15	IO72PDB4V0
AB16	IO73NDB4V0
AB17	IO73PDB4V0
AB18	NC
AB19	NC
AB20	VCCIB4
AB21	GND
AB22	GND
B1	GND
B2	VCCIB7
B3	NC
B4	IO03NDB0V0
B5	IO03PDB0V0
B6	IO07NDB0V1
B7	IO07PDB0V1
B8	IO11NDB0V1
B9	IO17NDB0V2
B10	IO14PDB0V2
B11	IO19PDB0V2
B12	IO22NDB1V0
B13	IO26NDB1V0
B14	NC
B15	NC
B16	IO30NDB1V1
B17	IO30PDB1V1
B18	IO32PDB1V1
B19	NC
B20	NC
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO04NDB0V0
C7	IO04PDB0V0
C8	VCC
C9	VCC
C10	IO14NDB0V2
C11	IO19NDB0V2
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC

CG484	
Pin Number	**RT3PE600L**
C22	VCCIB2
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO05PDB0V0
D9	IO10PDB0V1
D10	IO12PDB0V2
D11	IO16NDB0V2
D12	IO23NDB1V0
D13	IO23PDB1V0
D14	IO28NDB1V1
D15	IO28PDB1V1
D16	GBB1/IO34PDB1V1
D17	GBA0/IO35NDB1V1
D18	GBA1/IO35PDB1V1
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO133PDB7V1
E5	GAA2/IO134PDB7V1
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO05NDB0V0
E9	IO10NDB0V1
E10	IO12NDB0V2
E11	IO16PDB0V2
E12	IO20NDB1V0
E13	IO24NDB1V0
E14	IO24PDB1V0
E15	GBC1/IO33PDB1V1
E16	GBB0/IO34NDB1V1
E17	GNDQ
E18	GBA2/IO36PDB2V0
E19	IO42NDB2V0
E20	GND
E21	NC
E22	NC
F1	NC
F2	IO131NDB7V1
F3	IO131PDB7V1
F4	IO133NDB7V1
F5	IO134NDB7V1
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO15NDB0V2
F11	IO15PDB0V2
F12	IO20PDB1V0
F13	IO25NDB1V0
F14	IO27PDB1V0
F15	GBC0/IO33NDB1V1
F16	VCCPLB
F17	VMV2
F18	IO36NDB2V0
F19	IO42PDB2V0
F20	NC
F21	NC
F22	NC
G1	IO127NDB7V1
G2	IO127PDB7V1
G3	NC
G4	IO128PDB7V1
G5	IO129PDB7V1
G6	GAC2/IO132PDB7V1
G7	VCOMPLA
G8	GNDQ
G9	IO09NDB0V1
G10	IO09PDB0V1
G11	IO13PDB0V2
G12	IO21PDB1V0
G13	IO25PDB1V0
G14	IO27NDB1V0
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO37PDB2V0
G18	IO39PDB2V0
G19	IO39NDB2V0
G20	IO43PDB2V0
G21	IO43NDB2V0
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO128NDB7V1
H5	IO129NDB7V1
H6	IO132NDB7V1
H7	IO130PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO13NDB0V2
H12	IO21NDB1V0
H13	VCCIB1
H14	VCCIB1
H15	VMV1
H16	GBC2/IO38PDB2V0
H17	IO37NDB2V0
H18	IO41NDB2V0
H19	IO41PDB2V0

CG484	
Pin Number	**RT3PE600L**
H20	VCC
H21	NC
H22	NC
J1	IO123NDB7V0
J2	IO123PDB7V0
J3	NC
J4	IO124PDB7V0
J5	IO125PDB7V0
J6	IO126PDB7V0
J7	IO130NDB7V1
J8	VCCIB7
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB2
J16	IO38NDB2V0
J17	IO40NDB2V0
J18	IO40PDB2V0
J19	IO45PPB2V1
J20	NC
J21	IO48PDB2V1
J22	IO46PDB2V1
K1	IO121NDB7V0
K2	IO121PDB7V0
K3	NC
K4	IO124NDB7V0
K5	IO125NDB7V0
K6	IO126NDB7V0
K7	GFC1/IO120PPB7V0
K8	VCCIB7
K9	VCC
K10	GND
K11	GND

CG484	
Pin Number	**RT3PE600L**
K12	GND
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO50PPB2V1
K17	IO44NDB2V1
K18	IO44PDB2V1
K19	IO49NPB2V1
K20	IO45NPB2V1
K21	IO48NDB2V1
K22	IO46NDB2V1
L1	NC
L2	IO122PDB7V0
L3	IO122NDB7V0
L4	GFB0/IO119NPB7V0
L5	GFA0/IO118NDB6V1
L6	GFB1/IO119PPB7V0
L7	VCOMPLF
L8	GFC0/IO120NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO50NPB2V1
L16	GCB1/IO51PPB2V1
L17	GCA0/IO52NPB3V0
L18	VCOMPLC
L19	GCB0/IO51NPB2V1
L20	IO49PPB2V1
L21	IO47NDB2V1
L22	IO47PDB2V1
M1	NC
M2	IO114NPB6V1
M3	IO117NDB6V1

CG484	
Pin Number	**RT3PE600L**
M4	GFA2/IO117PDB6V1
M5	GFA1/IO118PDB6V1
M6	VCCPLF
M7	IO116NDB6V1
M8	GFB2/IO116PDB6V1
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO54PPB3V0
M16	GCA1/IO52PPB3V0
M17	GCC2/IO55PPB3V0
M18	VCCPLC
M19	GCA2/IO53PDB3V0
M20	IO53NDB3V0
M21	IO56PDB3V0
M22	NC
N1	IO114PPB6V1
N2	IO111NDB6V1
N3	NC
N4	GFC2/IO115PPB6V1
N5	IO113PPB6V1
N6	IO112PDB6V1
N7	IO112NDB6V1
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO54NPB3V0
N17	IO57NPB3V0

CG484	
Pin Number	**RT3PE600L**
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	VCC
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1
V15	IO69NDB4V0

CG484	
Pin Number	**RT3PE600L**
V16	GDB2/IO69PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO63NDB3V1
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO100NDB5V2
W6	FF/GEB2/IO100PDB5V2
W7	IO99NDB5V2
W8	IO88NDB5V0
W9	IO88PDB5V0
W10	IO89NDB5V0
W11	IO80NDB4V1
W12	IO81NDB4V1
W13	IO81PDB4V1
W14	IO70NDB4V0
W15	GDC2/IO70PDB4V0
W16	IO68NDB4V0
W17	GDA2/IO68PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB6
Y2	NC
Y3	NC
Y4	IO98NDB5V2
Y5	GND
Y6	IO94NDB5V1

CG484	
Pin Number	**RT3PE600L**
Y7	IO94PDB5V1
Y8	VCC
Y9	VCC
Y10	IO89PDB5V0
Y11	IO80PDB4V1
Y12	IO78NPB4V1
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB3

CG484	
Pin Number	**RT3PE3000L Function**
A2	GND
A3	VCCIB0
A4	IO10NDB0V1
A5	IO10PDB0V1
A6	IO16NDB0V1
A7	IO16PDB0V1
A8	IO18PDB0V2
A9	IO24PDB0V2
A10	IO28NDB0V3
A11	IO28PDB0V3
A12	IO46PDB1V0
A13	IO54PDB1V1
A14	IO56NDB1V1
A15	IO56PDB1V1
A16	IO64NDB1V2
A17	IO64PDB1V2
A18	IO72NDB1V3
A19	IO74NDB1V4
A20	VCCIB1
A21	GND
A22	GND
AA1	GND
AA2	VCCIB6
AA3	IO228PDB5V4
AA4	IO224PDB5V3
AA5	IO218NDB5V3
AA6	IO218PDB5V3
AA7	IO212NDB5V2
AA8	IO212PDB5V2
AA9	IO198PDB5V0
AA10	IO198NDB5V0
AA11	IO188PPB4V4
AA12	IO180NDB4V3
AA13	IO180PDB4V3
AA14	IO170NDB4V2
AA15	IO170PDB4V2
AA16	IO166NDB4V1
AA17	IO166PDB4V1
AA18	IO160NDB4V0
AA19	IO160PDB4V0
AA20	IO158NPB4V0
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO216NDB5V2
AB5	IO216PDB5V2
AB6	IO210NDB5V2
AB7	IO210PDB5V2
AB8	IO208NDB5V1
AB9	IO208PDB5V1
AB10	IO197NDB5V0
AB11	IO197PDB5V0
AB12	IO174NDB4V2
AB13	IO174PDB4V2
AB14	IO172NDB4V2
AB15	IO172PDB4V2
AB16	IO168NDB4V1
AB17	IO168PDB4V1
AB18	IO162NDB4V1
AB19	IO162PDB4V1
AB20	VCCIB4
AB21	GND
AB22	GND
B1	GND
B2	VCCIB7
B3	IO06PPB0V0
B4	IO08NDB0V0
B5	IO08PDB0V0
B6	IO14NDB0V1
B7	IO14PDB0V1
B8	IO18NDB0V2
B9	IO24NDB0V2
B10	IO34PDB0V4
B11	IO40PDB0V4
B12	IO46NDB1V0
B13	IO54NDB1V1
B14	IO62NDB1V2
B15	IO62PDB1V2
B16	IO68NDB1V3
B17	IO68PDB1V3
B18	IO72PDB1V3
B19	IO74PDB1V4
B20	IO76NPB1V4
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	IO303PDB7V3
C3	IO305PDB7V3
C4	IO06NPB0V0
C5	GND
C6	IO12NDB0V1
C7	IO12PDB0V1
C8	VCC
C9	VCC
C10	IO34NDB0V4
C11	IO40NDB0V4
C12	IO48NDB1V0
C13	IO48PDB1V0
C14	VCC
C15	VCC
C16	IO70NDB1V3
C17	IO70PDB1V3
C18	GND

CG484	
Pin Number	**RT3PE3000L Function**
C19	IO76PPB1V4
C20	IO88NDB2V0
C21	IO94PPB2V1
C22	VCCIB2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	VCCPLB
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	VCOMPLA
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	VCC
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO36NDB0V4
H12	IO42NDB1V0
H13	VCCIB1

CG484	
Pin Number	**RT3PE3000L Function**
H14	VCCIB1
H15	VMV1
H16	GBC2/IO84PDB2V0
H17	IO83NDB2V0
H18	IO100NDB2V2
H19	IO100PDB2V2
H20	VCC
H21	VMV2
H22	IO105PDB2V2
J1	IO285NDB7V1
J2	IO285PDB7V1
J3	VMV7
J4	IO279PDB7V0
J5	IO283PDB7V1
J6	IO281PDB7V0
J7	IO287NDB7V1
J8	VCCIB7
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB2
J16	IO84NDB2V0
J17	IO104NDB2V2
J18	IO104PDB2V2
J19	IO106PPB2V3
J20	GNDQ
J21	IO109PDB2V3
J22	IO107PDB2V3
K1	IO277NDB7V0
K2	IO277PDB7V0
K3	GNDQ
K4	IO279NDB7V0
K5	IO283NDB7V1
K6	IO281NDB7V0
K7	GFC1/IO275PPB7V0
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO112PPB2V3
K17	IO108NDB2V3
K18	IO108PDB2V3
K19	IO110NPB2V3
K20	IO106NPB2V3
K21	IO109NDB2V3
K22	IO107NDB2V3
L1	IO257PSB6V2
L2	IO276PDB7V0
L3	IO276NDB7V0
L4	GFB0/IO274NPB7V0
L5	GFA0/IO273NDB6V4
L6	GFB1/IO274PPB7V0
L7	VCOMPLF
L8	GFC0/IO275NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO112NPB2V3
L16	GCB1/IO113PPB2V3
L17	GCA0/IO114NPB3V0
L18	VCOMPLC
L19	GCB0/IO113NPB2V3
L20	IO110PPB2V3
L21	IO111NDB2V3
L22	IO111PDB2V3
M1	GNDQ
M2	IO255NPB6V2
M3	IO272NDB6V4
M4	GFA2/IO272PDB6V4
M5	GFA1/IO273PDB6V4
M6	VCCPLF
M7	IO271NDB6V4
M8	GFB2/IO271PDB6V4
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO116PPB3V0
M16	GCA1/IO114PPB3V0
M17	GCC2/IO117PPB3V0
M18	VCCPLC
M19	GCA2/IO115PDB3V0
M20	IO115NDB3V0
M21	IO126PDB3V1
M22	IO124PSB3V1
N1	IO255PPB6V2
N2	IO253NDB6V2
N3	VMV6
N4	GFC2/IO270PPB6V4
N5	IO261PPB6V3
N6	IO263PDB6V3
N7	IO263NDB6V3
N8	VCCIB6

CG484	
Pin Number	**RT3PE3000L Function**
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO116NPB3V0
N17	IO132NPB3V2
N18	IO117NPB3V0
N19	IO132PPB3V2
N20	GNDQ
N21	IO126NDB3V1
N22	IO128PDB3V1
P1	IO247PDB6V1
P2	IO253PDB6V2
P3	IO270NPB6V4
P4	IO261NPB6V3
P5	IO249PPB6V1
P6	IO259PDB6V3
P7	IO259NDB6V3
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO152NPB3V4
P17	IO136NDB3V2
P18	IO136PDB3V2
P19	IO138PDB3V3
P20	VMV3
P21	IO130PDB3V2

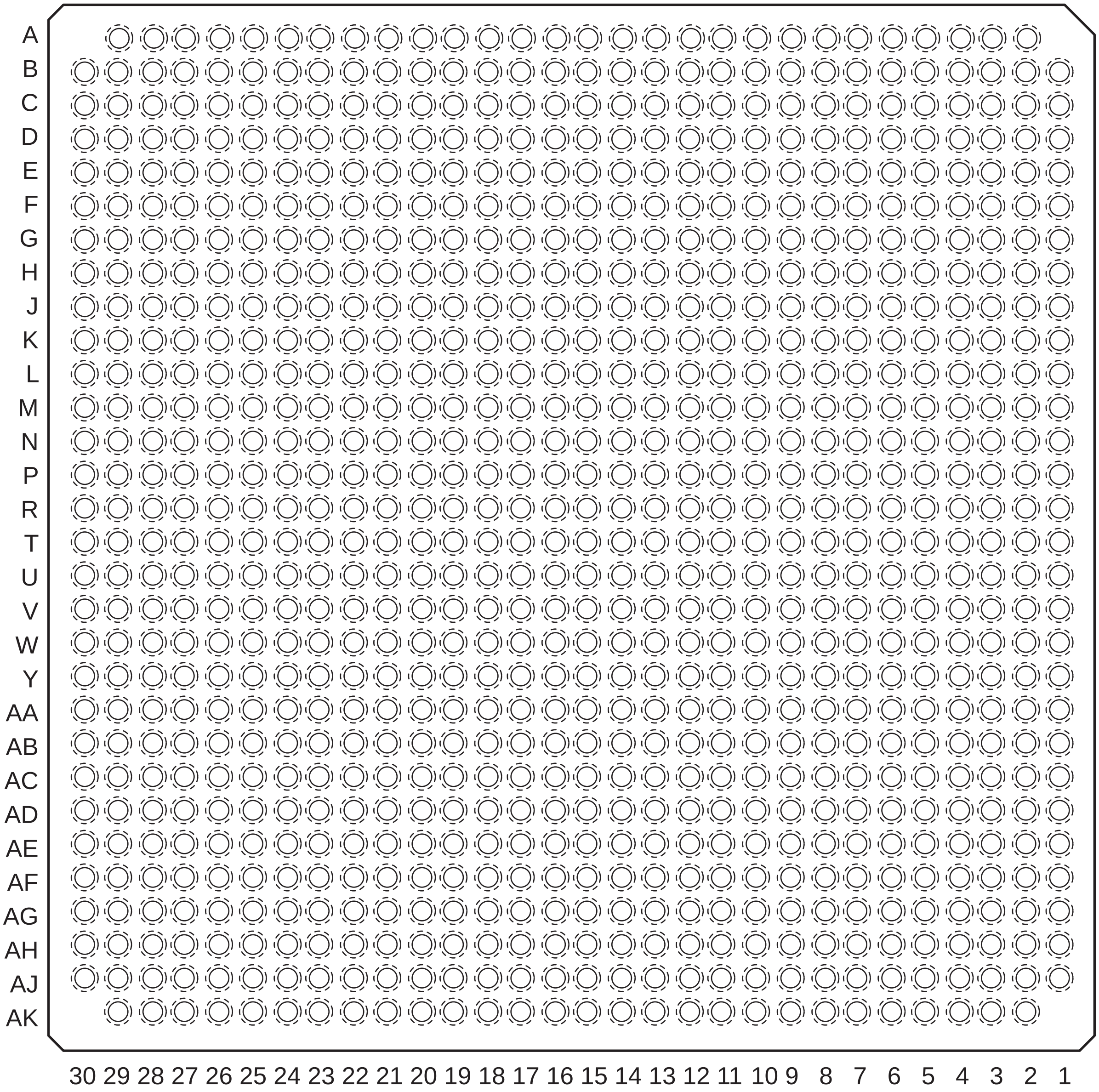
CG484	
Pin Number	**RT3PE3000L Function**
P22	IO128NDB3V1
R1	IO247NDB6V1
R2	IO245PDB6V1
R3	VCC
R4	IO249NPB6V1
R5	IO251NDB6V2
R6	IO251PDB6V2
R7	GEC0/IO236NPB6V0
R8	VMV5
R9	VCCIB5
R10	VCCIB5
R11	IO196NDB5V0
R12	IO196PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO152PPB3V4
R18	GDC1/IO151PDB3V4
R19	IO138NDB3V3
R20	VCC
R21	IO130NDB3V2
R22	IO134PDB3V2
T1	IO243PPB6V1
T2	IO245NDB6V1
T3	IO243NPB6V1
T4	IO241PDB6V0
T5	IO241NDB6V0
T6	GEC1/IO236PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO233PPB5V4
T10	IO206NDB5V1
T11	IO202NDB5V1
T12	IO194NDB5V0

CG484	
Pin Number	**RT3PE3000L Function**
T13	IO186NDB4V4
T14	IO186PDB4V4
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO151NDB3V4
T19	GDA1/IO153PDB3V4
T20	IO144PDB3V3
T21	IO140PDB3V3
T22	IO134NDB3V2
U1	IO240PPB6V0
U2	IO238PDB6V0
U3	IO238NDB6V0
U4	GEB1/IO235PDB6V0
U5	GEB0/IO235NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO233NPB5V4
U9	IO222PPB5V3
U10	IO206PDB5V1
U11	IO202PDB5V1
U12	IO194PDB5V0
U13	IO176NDB4V2
U14	IO176PDB4V2
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO153NDB3V4
U20	IO144NDB3V3
U21	IO140NDB3V3
U22	IO142PDB3V3
V1	IO239PDB6V0
V2	IO240NPB6V0
V3	GND

CG484	
Pin Number	**RT3PE3000L Function**
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0
V13	IO178NDB4V3
V14	IO178PDB4V3
V15	IO155NDB4V0
V16	GDB2/IO155PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	IO146PDB3V4
V22	IO142NDB3V3
W1	IO239NDB6V0
W2	IO237PDB6V0
W3	IO230PSB5V4
W4	GND
W5	IO232NDB5V4
W6	FF/GEB2/IO232PDB5V4
W7	IO231NDB5V4
W8	IO214NDB5V2
W9	IO214PDB5V2
W10	IO200NDB5V0
W11	IO192NDB4V4
W12	IO184NDB4V3
W13	IO184PDB4V3
W14	IO156NDB4V0
W15	GDC2/IO156PDB4V0

CG484	
Pin Number	**RT3PE3000L Function**
W16	IO154NDB4V0
W17	GDA2/IO154PDB4V0
W18	TMS
W19	GND
W20	IO150NDB3V4
W21	IO146NDB3V4
W22	IO148PPB3V4
Y1	VCCIB6
Y2	IO237NDB6V0
Y3	IO228NDB5V4
Y4	IO224NDB5V3
Y5	GND
Y6	IO220NDB5V3
Y7	IO220PDB5V3
Y8	VCC
Y9	VCC
Y10	IO200PDB5V0
Y11	IO192PDB4V4
Y12	IO188NPB4V4
Y13	IO187PSB4V4
Y14	VCC
Y15	VCC
Y16	IO164NDB4V1
Y17	IO164PDB4V1
Y18	GND
Y19	IO158PPB4V0
Y20	IO150PDB3V4
Y21	IO148NPB3V4
Y22	VCCIB3

CG896



Note: This is the bottom view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CG896	
Pin Number	**RT3PE3000L Function**
A2	GND
A3	GND
A4	IO14NPB0V1
A5	GND
A6	IO07NPB0V0
A7	GND
A8	IO09NDB0V1
A9	IO17NDB0V2
A10	IO17PDB0V2
A11	IO21NDB0V2
A12	IO21PDB0V2
A13	IO33NDB0V4
A14	IO33PDB0V4
A15	IO35NDB0V4
A16	IO35PDB0V4
A17	IO41NDB1V0
A18	IO43NDB1V0
A19	IO43PDB1V0
A20	IO45NDB1V0
A21	IO45PDB1V0
A22	IO57NDB1V2
A23	IO57PDB1V2
A24	GND
A25	IO69PPB1V3
A26	GND
A27	GBC1/IO79PPB1V4
A28	GND
A29	GND
AA1	IO256PDB6V2
AA2	IO248PDB6V1
AA3	IO248NDB6V1
AA4	IO246NDB6V1
AA5	GEA1/IO234PDB6V0
AA6	GEA0/IO234NDB6V0
AA7	IO243PPB6V1

CG896	
Pin Number	**RT3PE3000L Function**
AA8	IO245NDB6V1
AA9	GEB1/IO235PPB6V0
AA10	VCC
AA11	IO226PPB5V4
AA12	VCCIB5
AA13	VCCIB5
AA14	VCCIB5
AA15	VCCIB5
AA16	VCCIB4
AA17	VCCIB4
AA18	VCCIB4
AA19	VCCIB4
AA20	IO174PDB4V2
AA21	VCC
AA22	IO142NPB3V3
AA23	IO144NDB3V3
AA24	IO144PDB3V3
AA25	IO146NDB3V4
AA26	IO146PDB3V4
AA27	IO147PDB3V4
AA28	IO139NDB3V3
AA29	IO139PDB3V3
AA30	IO133NDB3V2
AB1	IO256NDB6V2
AB2	IO244PDB6V1
AB3	IO244NDB6V1
AB4	IO241PDB6V0
AB5	IO241NDB6V0
AB6	IO243NPB6V1
AB7	VCCIB6
AB8	VCCPLE
AB9	VCC
AB10	IO222PDB5V3
AB11	IO218PPB5V3
AB12	IO206NDB5V1

CG896	
Pin Number	**RT3PE3000L Function**
AB13	IO206PDB5V1
AB14	IO198NDB5V0
AB15	IO198PDB5V0
AB16	IO192NDB4V4
AB17	IO192PDB4V4
AB18	IO178NDB4V3
AB19	IO178PDB4V3
AB20	IO174NDB4V2
AB21	IO162NPB4V1
AB22	VCC
AB23	VCCPLD
AB24	VCCIB3
AB25	IO150PDB3V4
AB26	IO148PDB3V4
AB27	IO147NDB3V4
AB28	IO145PDB3V3
AB29	IO143PDB3V3
AB30	IO137PDB3V2
AC1	IO254PDB6V2
AC2	IO254NDB6V2
AC3	IO240PDB6V0
AC4	GEC1/IO236PDB6V0
AC5	IO237PDB6V0
AC6	IO237NDB6V0
AC7	VCOMPLE
AC8	GND
AC9	IO226NPB5V4
AC10	IO222NDB5V3
AC11	IO216NPB5V2
AC12	IO210NPB5V2
AC13	IO204NDB5V1
AC14	IO204PDB5V1
AC15	IO194NDB5V0
AC16	IO188NDB4V4
AC17	IO188PDB4V4

CG896	
Pin Number	**RT3PE3000L Function**
AC18	IO182PPB4V3
AC19	IO170NPB4V2
AC20	IO164NDB4V1
AC21	IO164PDB4V1
AC22	IO162PPB4V1
AC23	GND
AC24	VCOMPLD
AC25	IO150NDB3V4
AC26	IO148NDB3V4
AC27	GDA1/IO153PDB3V4
AC28	IO145NDB3V3
AC29	IO143NDB3V3
AC30	IO137NDB3V2
AD1	GND
AD2	IO242NPB6V1
AD3	IO240NDB6V0
AD4	GEC0/IO236NDB6V0
AD5	VCCIB6
AD6	GNDQ
AD7	VCC
AD8	VMV5
AD9	VCCIB5
AD10	IO224PPB5V3
AD11	IO218NPB5V3
AD12	IO216PPB5V2
AD13	IO210PPB5V2
AD14	IO202PPB5V1
AD15	IO194PDB5V0
AD16	IO190PDB4V4
AD17	IO182NPB4V3
AD18	IO176NDB4V2
AD19	IO176PDB4V2
AD20	IO170PPB4V2
AD21	IO166PDB4V1
AD22	VCCIB4

CG896	
Pin Number	**RT3PE3000L Function**
AD23	TCK
AD24	VCC
AD25	TRST
AD26	VCCIB3
AD27	GDA0/IO153NDB3V4
AD28	GDC0/IO151NDB3V4
AD29	GDC1/IO151PDB3V4
AD30	GND
AE1	IO242PPB6V1
AE2	VCC
AE3	IO239PDB6V0
AE4	IO239NDB6V0
AE5	VMV6
AE6	GND
AE7	GNDQ
AE8	IO230NDB5V4
AE9	IO224NPB5V3
AE10	IO214NPB5V2
AE11	IO212NDB5V2
AE12	IO212PDB5V2
AE13	IO202NPB5V1
AE14	IO200NDB5V0
AE15	IO196PDB5V0
AE16	IO190NDB4V4
AE17	IO184PDB4V3
AE18	IO184NDB4V3
AE19	IO172PDB4V2
AE20	IO172NDB4V2
AE21	IO166NDB4V1
AE22	IO160PDB4V0
AE23	GNDQ
AE24	VMV4
AE25	GND
AE26	GDB0/IO152NDB3V4
AE27	GDB1/IO152PDB3V4

CG896	
Pin Number	**RT3PE3000L Function**
AE28	VMV3
AE29	VCC
AE30	IO149PDB3V4
AF1	GND
AF2	IO238PPB6V0
AF3	VCCIB6
AF4	IO220NPB5V3
AF5	VCC
AF6	IO228NDB5V4
AF7	VCCIB5
AF8	IO230PDB5V4
AF9	IO229NDB5V4
AF10	IO229PDB5V4
AF11	IO214PPB5V2
AF12	IO208NDB5V1
AF13	IO208PDB5V1
AF14	IO200PDB5V0
AF15	IO196NDB5V0
AF16	IO186NDB4V4
AF17	IO186PDB4V4
AF18	IO180NDB4V3
AF19	IO180PDB4V3
AF20	IO168NDB4V1
AF21	IO168PDB4V1
AF22	IO160NDB4V0
AF23	IO158NPB4V0
AF24	VCCIB4
AF25	IO154NPB4V0
AF26	VCC
AF27	TDO
AF28	VCCIB3
AF29	GNDQ
AF30	GND
AG1	IO238NPB6V0
AG2	VCC

CG896	
Pin Number	**RT3PE3000L Function**
AG3	IO232NPB5V4
AG4	GND
AG5	IO220PPB5V3
AG6	IO228PDB5V4
AG7	IO231NDB5V4
AG8	GEC2/IO231PDB5V4
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	VJTAG
AG29	VCC
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	VCC
AH4	FF/GEB2/IO232PPB5V4
AH5	VCCIB5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	VCCIB4
AH27	TDI
AH28	VCC
AH29	VPUMP
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	VCC
AJ5	IO217NPB5V2
AJ6	VCC
AJ7	IO215NPB5V2
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	VCC
AJ26	IO156NPB4V0
AJ27	VCC
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4

CG896	
Pin Number	**RT3PE3000L Function**
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1
AK23	IO169PDB4V1
AK24	GND
AK25	IO167PPB4V1
AK26	GND
AK27	GDC2/IO156PPB4V0
AK28	GND
AK29	GND
B1	GND
B2	GND
B3	GAA2/IO309PPB7V4
B4	VCC
B5	IO14PPB0V1
B6	VCC
B7	IO07PPB0V0
B8	IO09PDB0V1
B9	IO15PPB0V1
B10	IO19NDB0V2
B11	IO19PDB0V2
B12	IO29NDB0V3
B13	IO29PDB0V3
B14	IO31PPB0V3
B15	IO37NDB0V4
B16	IO37PDB0V4
B17	IO41PDB1V0
B18	IO51NDB1V1
B19	IO59PDB1V2
B20	IO53PDB1V1
B21	IO53NDB1V1
B22	IO61NDB1V2
B23	IO61PDB1V2

CG896	
Pin Number	**RT3PE3000L Function**
B24	IO69NPB1V3
B25	VCC
B26	GBC0/IO79NPB1V4
B27	VCC
B28	IO64NPB1V2
B29	GND
B30	GND
C1	GND
C2	IO309NPB7V4
C3	VCC
C4	GAA0/IO00NPB0V0
C5	VCCIB0
C6	IO03PDB0V0
C7	IO03NDB0V0
C8	GAB1/IO01PDB0V0
C9	IO05PDB0V0
C10	IO15NPB0V1
C11	IO25NDB0V3
C12	IO25PDB0V3
C13	IO31NPB0V3
C14	IO27NDB0V3
C15	IO39NDB0V4
C16	IO39PDB0V4
C17	IO55PPB1V1
C18	IO51PDB1V1
C19	IO59NDB1V2
C20	IO63NDB1V2
C21	IO63PDB1V2
C22	IO67NDB1V3
C23	IO67PDB1V3
C24	IO75NDB1V4
C25	IO75PDB1V4
C26	VCCIB1
C27	IO64PPB1V2
C28	VCC

CG896	
Pin Number	**RT3PE3000L Function**
C29	GBA1/IO81PPB1V4
C30	GND
D1	IO303PPB7V3
D2	VCC
D3	IO305NPB7V3
D4	GND
D5	GAA1/IO00PPB0V0
D6	GAC1/IO02PDB0V0
D7	IO06NPB0V0
D8	GAB0/IO01NDB0V0
D9	IO05NDB0V0
D10	IO11NDB0V1
D11	IO11PDB0V1
D12	IO23NDB0V2
D13	IO23PDB0V2
D14	IO27PDB0V3
D15	IO40PDB0V4
D16	IO47NDB1V0
D17	IO47PDB1V0
D18	IO55NPB1V1
D19	IO65NDB1V3
D20	IO65PDB1V3
D21	IO71NDB1V3
D22	IO71PDB1V3
D23	IO73NDB1V4
D24	IO73PDB1V4
D25	IO74NDB1V4
D26	GBB0/IO80NPB1V4
D27	GND
D28	GBA0/IO81NPB1V4
D29	VCC
D30	GBA2/IO82PPB2V0
E1	GND
E2	IO303NPB7V3
E3	VCCIB7

CG896	
Pin Number	**RT3PE3000L Function**
E4	IO305PPB7V3
E5	VCC
E6	GAC0/IO02NDB0V0
E7	VCCIB0
E8	IO06PPB0V0
E9	IO24NDB0V2
E10	IO24PDB0V2
E11	IO13NDB0V1
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1

CG896	
Pin Number	RT3PE3000L Function
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0
H26	IO84NDB2V0
H27	IO96PDB2V1
H28	IO96NDB2V1
H29	IO89PDB2V0
H30	IO89NDB2V0
J1	IO290NDB7V2
J2	IO290PDB7V2
J3	IO302NDB7V3
J4	IO302PDB7V3
J5	IO295NDB7V2
J6	IO299NDB7V3
J7	VCCIB7
J8	VCCPLA
J9	VCC
J10	IO04NPB0V0
J11	IO18NDB0V2
J12	IO20NDB0V2
J13	IO20PDB0V2
J14	IO32NDB0V3
J15	IO32PDB0V3
J16	IO42PDB1V0
J17	IO44NDB1V0
J18	IO44PDB1V0
J19	IO54NDB1V1
J20	IO54PDB1V1
J21	IO76NPB1V4
J22	VCC
J23	VCCPLB

CG896	
Pin Number	RT3PE3000L Function
J24	VCCIB2
J25	IO90PDB2V1
J26	IO90NDB2V1
J27	GBB2/IO83PDB2V0
J28	IO83NDB2V0
J29	IO91PDB2V1
J30	IO91NDB2V1
K1	IO288NDB7V1
K2	IO288PDB7V1
K3	IO304NDB7V3
K4	IO304PDB7V3
K5	GAB2/IO308PDB7V4
K6	IO308NDB7V4
K7	IO301PDB7V3
K8	IO301NDB7V3
K9	GAC2/IO307PPB7V4
K10	VCC
K11	IO04PPB0V0
K12	VCCIB0
K13	VCCIB0
K14	VCCIB0
K15	VCCIB0
K16	VCCIB1
K17	VCCIB1
K18	VCCIB1
K19	VCCIB1
K20	IO76PPB1V4
K21	VCC
K22	IO78PPB1V4
K23	IO88NDB2V0
K24	IO88PDB2V0
K25	IO94PDB2V1
K26	IO94NDB2V1
K27	IO85PDB2V0
K28	IO85NDB2V0

CG896	
Pin Number	RT3PE3000L Function
K29	IO93PDB2V1
K30	IO93NDB2V1
L1	IO286NDB7V1
L2	IO286PDB7V1
L3	IO298NDB7V3
L4	IO298PDB7V3
L5	IO283PDB7V1
L6	IO291NDB7V2
L7	IO291PDB7V2
L8	IO293PDB7V2
L9	IO293NDB7V2
L10	IO307NPB7V4
L11	VCC
L12	VCC
L13	VCC
L14	VCC
L15	VCC
L16	VCC
L17	VCC
L18	VCC
L19	VCC
L20	VCC
L21	IO78NPB1V4
L22	IO104NPB2V2
L23	IO98NDB2V2
L24	IO98PDB2V2
L25	IO87PDB2V0
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2

CG896	
Pin Number	**RT3PE3000L Function**
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	VCCIB7
M11	VCC
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M18	GND
M19	GND
M20	VCC
M21	VCCIB2
M22	NC
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0

CG896	
Pin Number	**RT3PE3000L Function**
N9	IO281PDB7V0
N10	VCCIB7
N11	VCC
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND
N20	VCC
N21	VCCIB2
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	VCCIB7
P11	VCC
P12	GND
P13	GND

CG896	
Pin Number	**RT3PE3000L Function**
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	VCC
P21	VCCIB2
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	VCOMPLF
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	VCCIB7
R11	VCC
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND

CG896	
Pin Number	**RT3PE3000L Function**
R19	GND
R20	VCC
R21	VCCIB2
R22	GCC0/IO112NDB2V3
R23	GCB2/IO116PDB3V0
R24	IO118PDB3V0
R25	IO111PPB2V3
R26	IO122PPB3V1
R27	GCA0/IO114NPB3V0
R28	VCOMPLC
R29	GCB1/IO113PPB2V3
R30	IO115NPB3V0
T1	IO270NDB6V4
T2	VCCPLF
T3	GFA2/IO272PPB6V4
T4	GFA1/IO273PDB6V4
T5	IO272NPB6V4
T6	IO267NDB6V4
T7	IO267PDB6V4
T8	IO265PDB6V3
T9	IO263PDB6V3
T10	VCCIB6
T11	VCC
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	GND
T19	GND
T20	VCC
T21	VCCIB3
T22	IO109NPB2V3
T23	IO116NDB3V0
T24	IO118NDB3V0
T25	IO122NPB3V1
T26	GCA1/IO114PPB3V0
T27	GCB0/IO113NPB2V3
T28	GCA2/IO115PPB3V0
T29	VCCPLC
T30	IO121PDB3V0
U1	IO268PDB6V4
U2	IO264NDB6V3
U3	IO264PDB6V3
U4	IO258PDB6V3
U5	IO258NDB6V3
U6	IO257PPB6V2
U7	IO261PPB6V3
U8	IO265NDB6V3
U9	IO263NDB6V3
U10	VCCIB6
U11	VCC
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	VCC
U21	VCCIB3
U22	IO120PDB3V0
U23	IO128PDB3V1
U24	IO124PDB3V1
U25	IO124NDB3V1
U26	IO126PDB3V1
U27	IO129PDB3V1
U28	IO127PDB3V1
U29	IO125PDB3V1
U30	IO121NDB3V0
V1	IO268NDB6V4
V2	IO262PDB6V3
V3	IO260PDB6V3
V4	IO252PDB6V2
V5	IO257NPB6V2
V6	IO261NPB6V3
V7	IO255PDB6V2
V8	IO259PDB6V3
V9	IO259NDB6V3
V10	VCCIB6
V11	VCC
V12	GND
V13	GND
V14	GND
V15	GND
V16	GND
V17	GND
V18	GND
V19	GND
V20	VCC
V21	VCCIB3
V22	IO120NDB3V0
V23	IO128NDB3V1
V24	IO132PDB3V2
V25	IO130PPB3V2
V26	IO126NDB3V1
V27	IO129NDB3V1
V28	IO127NDB3V1
V29	IO125NDB3V1
V30	IO123PDB3V1
W1	IO266NDB6V4
W2	IO262NDB6V3
W3	IO260NDB6V3

CG896	
Pin Number	**RT3PE3000L Function**
W4	IO252NDB6V2
W5	IO251NDB6V2
W6	IO251PDB6V2
W7	IO255NDB6V2
W8	IO249PPB6V1
W9	IO253PDB6V2
W10	VCCIB6
W11	VCC
W12	GND
W13	GND
W14	GND
W15	GND
W16	GND
W17	GND
W18	GND
W19	GND
W20	VCC
W21	VCCIB3
W22	IO134PDB3V2
W23	IO138PDB3V3
W24	IO132NDB3V2
W25	IO136NPB3V2
W26	IO130NPB3V2
W27	IO141PDB3V3
W28	IO135PDB3V2
W29	IO131PDB3V2
W30	IO123NDB3V1
Y1	IO266PDB6V4
Y2	IO250PDB6V2
Y3	IO250NDB6V2
Y4	IO246PDB6V1
Y5	IO247NDB6V1
Y6	IO247PDB6V1
Y7	IO249NPB6V1
Y8	IO245PDB6V1

CG896	
Pin Number	**RT3PE3000L Function**
Y9	IO253NDB6V2
Y10	GEB0/IO235NPB6V0
Y11	VCC
Y12	VCC
Y13	VCC
Y14	VCC
Y15	VCC
Y16	VCC
Y17	VCC
Y18	VCC
Y19	VCC
Y20	VCC
Y21	IO142PPB3V3
Y22	IO134NDB3V2
Y23	IO138NDB3V3
Y24	IO140NDB3V3
Y25	IO140PDB3V3
Y26	IO136PPB3V2
Y27	IO141NDB3V3
Y28	IO135NDB3V2
Y29	IO131NDB3V2
Y30	IO133PDB3V2

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the RT ProASIC3 datasheet.

Revision	Changes	Page
Revision 5 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2
Revision 4 (August 2012)	"LVCMOS 2.5 V / 5.0 V Input" was removed from the "Advanced and Pro (Professional) I/Os" section. The following sentence was removed from the "2.5 V LVCMOS" section: "It uses a 5 V–tolerant input buffer and push-pull output buffer." The following sentence was added to the "I/O User Input/Output" pin description: "5 V input and output tolerance can be achieved with certain I/O standards and configuration; refer to the *Radiation-Tolerant ProASIC3 Low Power Spaceflight FPGA Fabric User's Guide* for more information" (SAR 36961).	I, 2-35, 3-2
	"RT ProASIC3 Ordering Information" was revised to add Extended Flow and PROTO. The Temperature Grade Offerings table was retitled "Screening Levels". Extended Flow and PROTO information was added to "Screening Levels" and the "Speed Grade Offerings" (SAR 39780).	III
	The "Extended Flow (E Flow)" section was added (SAR 38635).	V
	t_{DOUT} was corrected to t_{DIN} in Figure 2-5 • Input Buffer Timing Model and Delays (example) (SAR 37113).	2-17
	In Table 2-20 • Summary ofAC Measuring Points*, the Input/Output Supply Voltage column of values was corrected. Most of the values had been incorrect due to the column being offset by one row (SAR 36646).	2-22
	IIH and IIL were changed from 10 µA or 15 µA to 5 µA in the following tables to align with actual testing values used (SAR 39976). Minimum and Maximum DC Input Levels: Table 2-32, Table 2-39, Table 2-46, Table 2-53, Table 2-60, Table 2-67, Table 2-72, Table 2-76, Table 2-81, Table 2-86, Table 2-91, Table 2-96, Table 2-101, Table 2-106, Table 2-111, Table 2-116, Table 2-121, Table 2-126, Table 2-130.	2-29 through 2-71
	The values for maximum VIH and VIL for LVPECL in Table 2-134 • Minimum and Maximum DC Input and Output Levels was corrected to 3.6 V across all supply voltages (SAR 37694).	2-73
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from Table 2-156 • RT3PE600L Global Resourcethrough Table 2-159 • RT3PE3000L Global Resourcebecause a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 28993).	2-99 through 2-100
	Figure 2-49 • FIFO Readand Figure 2-50 • FIFO Writeare new (SAR 34850).	2-112
	The units were corrected from W to Ω in the last paragraph of the "TRST Boundary Scan Reset Pin" description (SAR 36562).	3-4

Revision	Changes	Page
Revision 4 (continued)	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain." The replacement text is "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38325). The "VMVx I/O Supply Voltage (quiet)" section states that "VMV pins must be connected to the corresponding VCCI pins," which is for an ESD enhancement.	3-1
	Table 3-2 • JTAG Pins – Recommendations for Flightis new (SAR 36563).	3-4
Revision 3 (October 2011)	Values for the CQ256 package were added to the "I/Os Per Package 1" table (SAR 33799).	II
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *RT ProASIC3 FPGA Fabric User's Guide* (SAR 34168).	2-14
	The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-22, 2-32, 2-46
	The formula for $R_{\text{(WEAK PULL-DOWN-MAX)}}$, given in a note for Table 2-26 • I/O Weak Pull-Up/Pull-Down Resistances, was corrected to the following (SAR 32470): $R_{\text{(WEAK PULL-DOWN-MAX)}} = VOL_{\text{spec}} / I_{\text{(WEAK PULL-DOWN-MIN)}}$	2-26
	The following notes were removed from Table 2-130 • Minimum and Maximum DC Input and Output Levels (SAR 29428): ±5% Differential input voltage = ±350 mV	2-71
	Table 2-160 • RT ProASIC3 CCC/PLL Specificationand Table 2-161 • RT ProASIC3 CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 25705).	2-101, 2-102
	A table note was added to tables in the SRAM "Timing Characteristics" section to reference an application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers simultaneous read/write cases in detail (SAR 21770).	2-107
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	4-1
	The "CQ256" section and pin tables for RT3PE600L and RT3PE3000L are new (SAR 33771).	4-1
Revision 2 (July 2011)	The "Low Power" section was revised, deleting text regarding Flash*Freeze mode, single-voltage operation, and low-impedance switches. The "Radiation Tolerant" section was renamed to "Radiation Performance" and the performance information was updated (SAR 30167).	I
	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865).	I, 2

Revision	Changes	Page
Revision 2 (continued)	The "RT ProASIC3 Device Status" table was revised to change the status for RT3PE600L and RT3PE3000L from advance to production (SARs 32097, 32395).	II
	The Y security option and Licensed DPA Logo were added to the "RT ProASIC3 Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 32151).	
	Table 2 • MIL-STD-883 Class B Product Flow for RT ProASIC3 Devices*is new (SAR 27924).	IV
	Reference to flash programming and retention maximum limits in a note for Table 2-1 • Absolute Maximum Ratingswas removed. This information will be added in a future revision of the datasheet (SAR 31645).	2-1
	Table 2-2 • Recommended Operating Conditions1,2 was updated for wide range (SARs 29700, 30472). VPUMP during operating was changed from "0 to 3.6" to 0. The table note stating VPUMP can be left floating during normal operation was revised to state, "VPUMP should be tied to 0 V to optimize total ionizing dose performance during operation in spaceflight applications" (SAR 32490).	2-2
	Table 2-4 • Package Thermal Resistivities was updated with information for the CG896 package (SARs 31947, 28960).	2-7
	Table 2-5 • Temperature and Voltage Derating Factors for Timing Delays was updated to reflect the latest changes in the software (SAR 32395).	2-7
	Table 2-6 • Power Supply State per Modeis new (SARs 24112, 32181, 32490).	2-8
	New information was added to the following tables in the "Quiescent Supply Current " section (SAR 30619, SAR 30397): Table 2-7 • Quiescent Supply Current (IDD) Characteristics, Flash*Freeze Mode* Table 2-9 • Quiescent Supply Current (IDD) Characteristics Shutdown Mode Table 2-10 • Quiescent Supply Current (IDD), Static Mode and Active Mode1 (the name of this table changed from "Quiescent Supply Current IDD, RT ProASIC Flash*Freeze Mode" per SAR 32181)	2-8
	Tables in the "Power per I/O Pin" section were updated and 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added (SAR 29700).	2-10
	More information was added to the note explaining PDC6 in the following tables (SAR 32181): Table 2-11 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1	2-10, 2-11
	Global parameters were updated in the dynamic power consumption tables in the "Power Consumption of Various Internal Resources" section (SAR 32451).	2-12
	Table 2-15 • Different Components Contributing to the Static Power Consumption in RT ProASIC3 Devices and "Total Static Power Consumption—PSTAT" were updated to add PDC0 (SARs 32451, 32181).	2-13
	The "Timing Model" was updated to reflect changes made in the I/O timing tables (SARs 29793, 32097, 32395).	2-16
	The title of Table 2-20 • Summary of AC Measuring Points* was revised. It was formerly "Summary of AC Memory Points" (SAR 32446).	2-22

Revision	Changes	Page
Revision 2 (continued)	Table 2-18 • Summary of Maximum and Minimum DC Output Levels and related tables for each I/O standard were updated to note differences in VOL and VOH for the following ranges: –55ºC ≤ T_J ≤ 100ºC 100 ºC < T_J ≤ 125ºC The T_J range for each parameter is specified in the tables (SAR 29793).	2-20
	The drive strength for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SARs 31995, 27973). Table 2-18 • Summary of Maximum and Minimum DC Output Levels Table 2-22 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-23 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-25 • I/O Output Buffer Maximum Resistances1 Table 2-27 • I/O Short Currents IOSH/IOSL (SAR 31718)	2-20 through 2-27
	The following tables were updated in accordance with SmartTime and SmartPower software (SARs 32097, 32457, 32395): Table 2-23 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-43 • 3.3 V LVCMOS Wide Range Low Slew Table 2-44 • 3.3 V LVCMOS Wide Range High Slew Timing characteristics tables for 1.5 V in the "Voltage-Referenced I/O Characteristics" section Table 2-133 • LVDS and Table 2-137 • LVPECL	 2-24 2-34 2-34 2-50 2-71
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 32448).	2-29
	Table 2-26 • I/O Weak Pull-Up/Pull-Down Resistances was updated (SAR 29793).	2-26
	3.3 V LVCMOS and 1.2 V LVCMOS wide range were added (SARs 29700, 31926).	2-20 to 2-68
	Values were revised in the "Global Tree Timing Characteristics" section tables (SAR 30698).	2-99
	Table 2-160 • RT ProASIC3 CCC/PLL Specification and Table 2-161 • RT ProASIC3 CCC/PLL Specification were updated (SAR 79388). Specification of jitter in the presence of SSO was added (SAR 32526).	2-101, 2-102
	The following figures were deleted (SAR 29991). Future application notes will cover these timing issues in detail (SAR 21770). Figure 2-47 • Write Access after Write onto Same Address Figure 2-48 • Read Access after Write onto Same Address Figure 2-49 • Write Access after Read onto Same Address The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-51 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 29991).	N/A 2-104, 2-107
	The values for t_{CKQ1} in Table 2-162 • RAM4K9 and Table 2-163 • RAM4K9 were reversed with respect to WMODE and have been corrected (SAR 32344).	2-107, 2-108
	The timing tables in the "SRAM" section were updated, including changes in the names and definitions of address collision parameters (SAR 21770).	2-107 to 2-110
	Table 2-169 • Embedded FlashROM Access Time was updated (SAR 32393).	2-117

Revision	Changes	Page
Revision 2 (continued)	The "Pin Descriptions" chapter was added (SAR 21642).	3-1
	Pin A1 was removed from the package diagram for the "CG484" package and the corresponding pin tables (SAR 30549).	4-8
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Screening Levels" table on page III indicates the status for each device in the device family.	N/A
Revision 1 (November 2009)	The CQFP package was added. The tables in this chapter and the "RT ProASIC3 Ordering Information" section were revised to reflect this.	I-I to I-III

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "RT ProASIC3 Device Status" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

International Traffic in Arms Regulations (ITAR)

The product described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR). They require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed Microsemi's qualification process. Microsemi may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all Microsemi SoC products is available on the SoC Products Group website at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.