SmartFusion2 Pin Descriptions

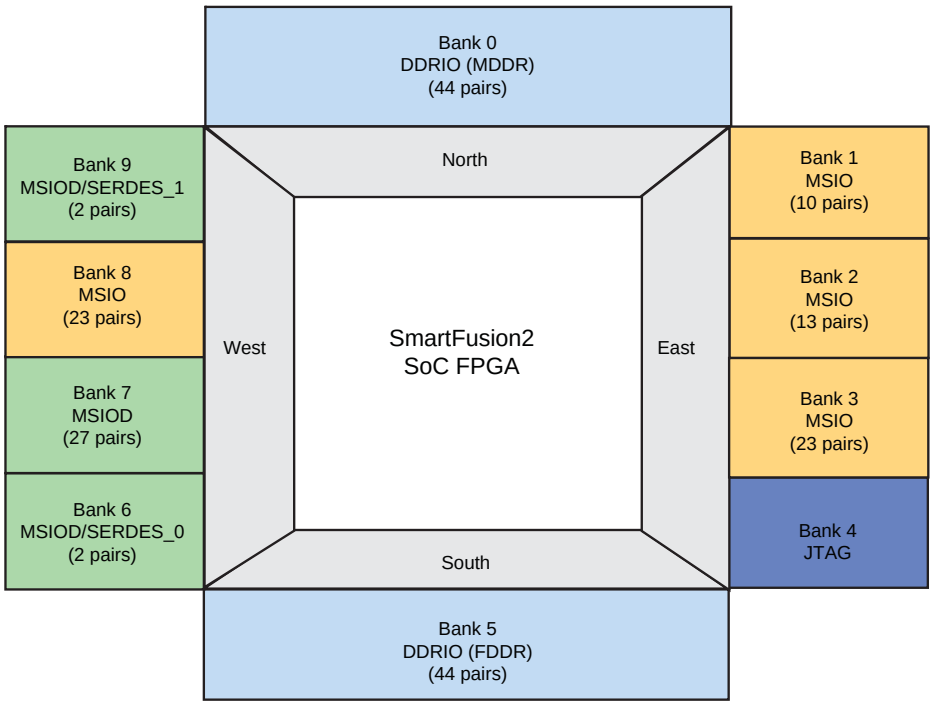
User I/Os

SmartFusion2 devices feature a flexible I/O structure that supports a range of mixed voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The MSIO, MSIOD, and DDRIO can be configured as differential I/Os or two single-ended I/Os. These I/Os use one I/O slot to implement single-ended standards and two I/O slots for differential standards. The DDRIO is shared between fabric logic and MDDR/FDDR whereas MSIO/MSIOD is shared between MSS peripherals and fabric logic. When an MDDR/FDDR controller or MSS peripheral is not used, the respective I/Os are available to fabric logic. For functional block diagrams of MSIO, MSIOD, and DDRIO, refer to the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

For supported I/O standards, refer to the "Supported Voltage Standards" table in the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

Bank Location Diagrams

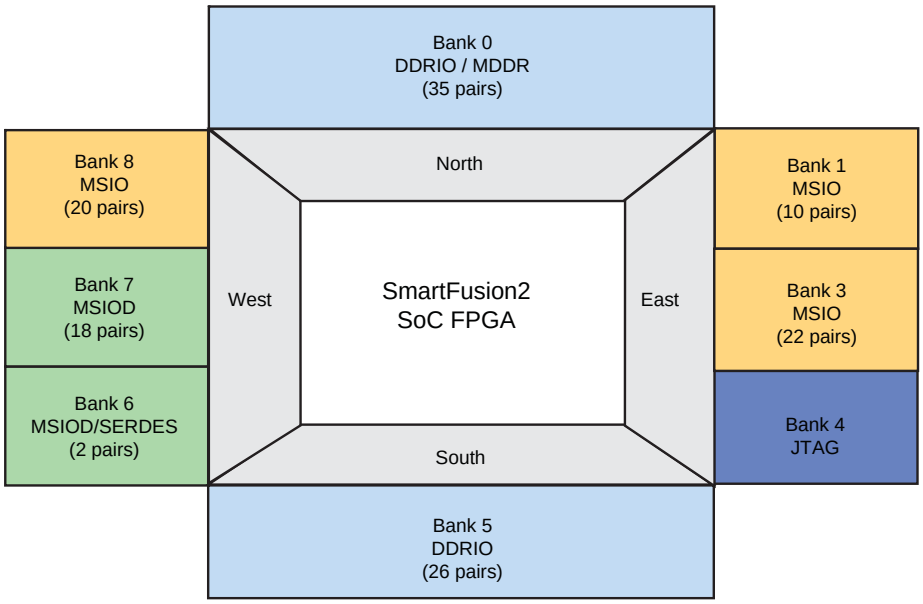
I/Os are grouped on the basis of I/O voltage standard. The grouped I/Os of each voltage standard form an I/O bank. Each I/O bank has dedicated I/O supply and ground voltages. Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank.



Notes:

1. *In bank 1 there are 21 single-ended user I/Os. Pin H27, MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.*
2. *For the M2S050S-FG896 and M2S050-FG896 devices, SERDES blocks are not available in bank 6 and bank 9.*

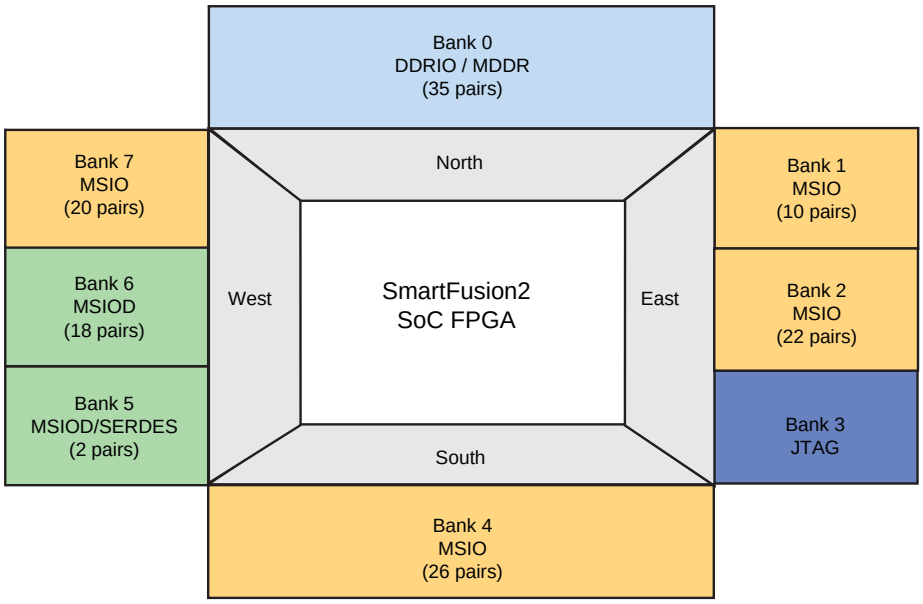
***Figure 1* • SmartFusion2 M2S050TS/M2S050T-FG896 I/O Bank Locations**



Notes:

1. *In bank 1 there are 21 single-ended user I/Os.*
   Pin D21, MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.
2. *For the M2S050S-FG484 and M2S050-FG484 devices, SERDES blocks are not available in bank 6.*

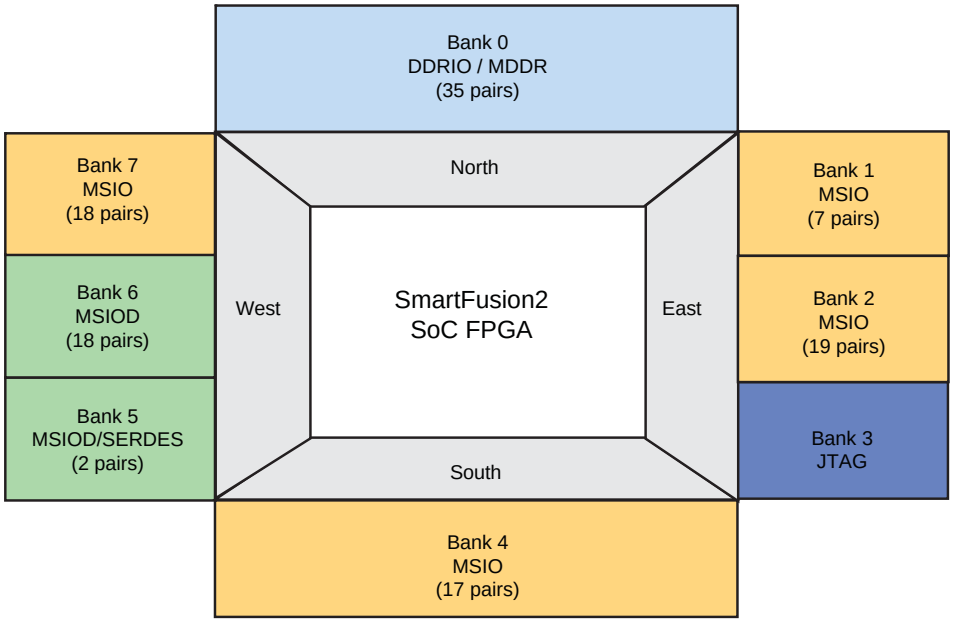
***Figure 2* • SmartFusion2 M2S050TS/M2S050T-FG484 I/O Bank Locations**



Notes:

1. *In bank 1 there are 21 single-ended user I/Os.*
   Pin D21, MSI32NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.
2. *For the M2S025S-FG484 and M2S025-FG484 devices, SERDES blocks are not available in bank 5.*

***Figure 3* • SmartFusion2 M2S025TS/M2S025T-FG484 I/O Bank Locations**



Notes:

1. *In bank 1 there are 15 single-ended user I/Os.*
   Pin D21, MSI26NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.
2. *For the M2S010S-FG484 and M2S010-FG484 devices, SERDES blocks are not available in bank 5.*

Figure 4 • **SmartFusion2 M2S010TS/M2S010T-FG484 I/O Bank Locations**

Table 1 • **The Organization of I/O Banks in SmartFusion2 Devices**

	FG896	FG484		
Bank No.	**M2S050T**	**M2S050T**	**M2S025T**	**M2S010T**
Bank 0	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric
Bank 1	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 2	MSIO: MSS or fabric		MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 3	MSIO: MSS or fabric	MSIO: MSS or fabric	JTAG/SWD	JTAG/SWD
Bank 4	JTAG/SWD	JTAG/SWD	MSIO: fabric	MSIO: fabric
Bank 5	DDRIO: FDDR or fabric	DDRIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric
Bank 6	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIOD: fabric
Bank 7	MSIOD: fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric
Bank 8	MSIO: fabric	MSIO: fabric		
Bank 9	MSIOD: SERDES 1 or fabric			

Table 2 • **Multi-Standard I/O Types**

Name	Type	Description
MSIOxyBz	In/out	MSIOs provide programmable drive strength, weak pull-up, and weak-pull-down. In single-ended mode, the I/O pair operates as two separate I/Os named P and N. Some of these pins are also multiplexed with integrated peripherals in the MSS (I2C, USB, SPI, UART, CAN, and fabric I/Os).This allows MSIO pins to be multiplexed as I/Os for the FPGA fabric, the ARM Cortex-M3 processor, or for given integrated MSS peripherals. MSIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. SmartFusion2 I/O ports also support ESD protection.
MSIODxyBz	In/out	MSIOD is very similar to MSIO, but drops 3.3 V and hot-plug support and adds pre-emphasis, in order to achieve higher speeds. MSIODs provide programmable drive strength, weak pull-up, and weak pull-down. MSIOD I/O cells operate at up to 2.5 V and are capable of high-speed LVDS operation. Some of these pins are also multiplexed with the SERDES interface. SmartFusion2 I/O ports support ESD protection.
DDRIOxyBz	In/out	The double data input output (DDRIO) is a multi-standard I/O optimized for LPDDR/DDR2/DDR3 performance. In SmartFusion2 devices there are two DDR subsystems: the fabric DDR and MSS DDR controllers. All DDRIOs can be configured as differential I/Os or two single-ended I/Os. If you select MDDR/FDDR, Libero SoC automatically connects MDDR/FDDR signals to the DDRIOs. DDRIOs can be connected to the respective DDR subsystem PHYs or can be used as user I/Os. Depending on the memory configuration, only the required DDRIOs are used by Libero SoC. The unused DDRIOs are available to connect to the fabric.

Naming Conventions

User I/O Naming Conventions

The naming convention used for each FPGA user I/O is **IOxyBz**, where:

IO is the type of I/O—MSIO, MSIOD, or DDRIO.

x refers the I/O pair number in bank z.

y is P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/Os named P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.

B is bank.

z refers to bank number (0–9 for M2S050-FG896).

Differential standards are implemented as true differential outputs and complementary single-ended outputs for SSTL/HSTL. In the single-ended mode, the I/O pair operates as two separate I/Os named P and N. All the configuration and data inputs/outputs are then separate and use names ending in P and N to differentiate between the two I/Os.

For more information, refer to the "I/Os" chapter of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

Dedicated Global I/O Naming Conventions

Dedicated global I/Os are dual-use I/Os which can drive the global blocks either directly or through clock conditioning circuits (CCC) or virtual clock conditioning circuits (VCCC). They can also be used as regular user I/Os. These global I/Os are the primary source for bringing in the external clock inputs into the SmartFusion2 device.

In the M2S050T-FG896 device, there are 16 global blocks located in the center of the fabric and 32 global I/Os located 8 each on the north, east, south, and west sides of the fabric. There are 6 CCC blocks, located 2 each on northwest, northeast, and southwest side of the fabric and 2 VCCC blocks on the southeast side of the fabric.

Dedicated global I/Os that drive the global blocks (GB) directly are named as **GBn,** where

n is 0 to 15.

Dedicated global I/Os that drive GBs through CCCs are named as **CCC_xyz_CLKlw**, where:

xy is the location—NE, SW, or NW.

z is 0 or 1.

l represents input clock

w refers to one of the four possible output clocks of the associated CCC_xyz—GL0, GL1, GL2, or GL3.

Dedicated global I/Os that drive GBs through VCCCs are named as **VCCC_SEz**, where:

SE is southeast.

z is 0 or 1.

Unused global pins are configured as inputs with pull-up resistors by Libero software.

For further details, refer to the "Fabric Global Routing Resources" chapter of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

Multi-Function I/Os

Certain I/Os can have more than one function. Users select the functionality through Libero configuration tools.

The name of a pin shows the functionalities for which that pin can be configured and used.

Example pin name: **MSIO48NB1/I2C_0_SCL/GPIO_31_B/USB_DATA1_C**

This I/O port is multi-purpose and can be configured as MSIO, I2C0 clock, fabric I/O, or USB_DATA1_C.

Impedance Calibration

The DDRIO can use fixed impedance calibration for different drive strengths, and these values can be programmed using Libero SoC for the selected I/O standard. These values are fed to the pull-up/pull-down reference network to match the impedance with an external resistor.

For the different drive modes, refer to the *SmartFusion2 FPGA Fabric Architecture User's Guide* for reference resistor values.

Table 3 • **Reference Resistors**

Pin Name	Type	Reference Resistor (Ohm)
FDDR_IMP_CALIB	Reference	Pulled down with resistor depending on voltage/standard: DDR2 – 150 Ohms DDR3 1.5 V – 240 Ohms DDR3 1.8 V – 150 Ohms LPDDR – 150 Ohms
MDDR_IMP_CALIB	Reference	Pulled down with resistor depending on voltage/standard: DDR2 – 150 Ohms DDR3 1.5 V – 240 Ohms DDR3 1.8 V – 150 Ohms LPDDR – 150 Ohms

Note: If impedance calibration is not required, the pin can be left open or connect to ground, or be grounded through the corresponding resistor.

Supply Pins

SmartFusion2 devices support multi-standard I/Os (MSIOs), MSIODs, double data rate I/Os (DDRIOs), microcontroller serial interfaces, high speed serial interfaces, and a debugging JTAG interface. SmartFusion2 devices require the power supplies listed in Table 4.

Table 4 • **Supply Pins**

Name	Type	Description
VDD	Supply	DC core supply voltage. Must always power this pin.
VPP	Supply	Power supply for charge pumps (for normal operation and programming). Must always power this pin.
VPPNVM	Supply	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.

Notes:

1. *If unused, all bank supplies can be left floating in order to reduce leakage, except the JTAG I/O bank supply. The JTAG bank should always be powered with the appropriate VDDI bank supply. An MSIO bank supports 1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V voltages and an MSIOD/DDRIO bank supports 1.2 V / 1.5 V / 1.8 V / 2.5 V voltages. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the SmartFusion2 SoC FPGAs Fabric Architecture User's Guide.*
2. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry.*
3. *If used, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding PLL return path on-board. Unused PLLs can be left floating, using the software configuration to assert the power-down signal of the PLL to reduce the static power.*
4. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding return path on-board. In an **unused** condition, the entire group of pins must be connected to VSS (ground). Among quadrant-related pins, a different configuration for a subset of them is not allowed.*
5. *If used, **DO NOT** short to ground directly on the package or PCB. In an **unused** condition, the pins can be left floating, since they are connected on-die to VSS.*

Table 4 • **Supply Pins**

Name	Type	Description
VDDI0	Bank power supplies[1]	VDDI port 0, bank 0 power
VDDI1		VDDI port 1, bank 1 power
VDDI2		VDDI port 2, bank 2 power
VDDI3		VDDI port 3, bank 3 power
VDDI4		VDDI port 4, bank 4 power
VDDI5		VDDI port 5, bank 5 power
VDDI6		VDDI port 6, bank 6 power
VDDI7		VDDI port 7, bank 7 power
VDDI8		VDDI port 8, bank 8 power
VDDI9		VDDI port 9, bank 9 power
VREF0	Supply[2]	Reference voltage for MDDR signals which are located in bank 0. In an **unused** condition, it can be left floating if VDDI0 is floating.
VREF5		Reference voltage for FDDR signals, which are located in bank 5. In an unused condition, it can be left floating if VDDI5 is floating.
CCC_NE0_PLL_VDDA	PLL power supplies[3]	Analog power pad for PLL0
CCC_NE1_PLL_VDDA		Analog power pad for PLL1
CCC_NW0_PLL_VDDA		Analog power pad for PLL2
CCC_NW1_PLL_VDDA		Analog power pad for PLL3
CCC_SW0_PLL_VDDA		Analog power pad for PLL4
CCC_SW1_PLL_VDDA		Analog power pad for PLL5
MDDR_PLL_VDDA		Analog power pad for PLL of MDDR
FDDR_PLL_VDDA		Analog power pad for PLL of FDDR

Notes:

1. *If unused, all bank supplies can be left floating in order to reduce leakage, except the JTAG I/O bank supply. The JTAG bank should always be powered with the appropriate VDDI bank supply. An MSIO bank supports 1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V voltages and an MSIOD/DDRIO bank supports 1.2 V / 1.5 V / 1.8 V / 2.5 V voltages. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the SmartFusion2 SoC FPGAs Fabric Architecture User's Guide.*
2. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry.*
3. *If used, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding PLL return path on-board. Unused PLLs can be left floating, using the software configuration to assert the power-down signal of the PLL to reduce the static power.*
4. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding return path on-board. In an **unused** condition, the entire group of pins must be connected to VSS (ground). Among quadrant-related pins, a different configuration for a subset of them is not allowed.*
5. *If used, **DO NOT** short to ground directly on the package or PCB. In an **unused** condition, the pins can be left floating, since they are connected on-die to VSS.*

Table 4 • **Supply Pins**

Name	Type	Description
SERDES_0_VDD	SERDES0 power supplies[4]	PCIe/PCS supply. It is a +1.2 V supply
SERDES_0_L01_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for lane0 and lane1 of SERDESIF0, located on the left side. It is a +1.2 V SERDES PMA supply.
SERDES_0_L23_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for lane2 and lane3 of SERDESIF0, located on the right side. It is a +1.2 V SERDES PMA supply.
SERDES_0_L01_VDDAPLL		Analog power for SERDES0 PLL of lane0 and lane1. It is a +2.5 V SERDES internal PLL supply.
SERDES_0_L23_VDDAPLL		Analog power for SERDES0 PLL of lane2 and lane3. It is a +2.5 V SERDES internal PLL supply.
SERDES_0_L01_REFRET		Local on-chip ground return path for SERDES_0_L01_VDDAPLL for lane0 and lane1 of SERDESIF0, located on the left side.
SERDES_0_L23_REFRET		Local on-chip ground return path for SERDES_0_L23_VDDAPLL for lane2 and lane3 of SERDESIF0, located on the right side
SERDES_0_PLL_VDDA		High supply voltage for PLL SERDES0. It can be +2.5 V or +3.3 V.
SERDES_0_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL SERDES0
SERDES_1_VDD	SERDES1 power supplies[4]	PCIe/PCS supply. It is a +1.2 V supply.
SERDES_1_L01_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for lane0 and lane1 of SERDESIF1, located on the left side. It is a +1.2 V SERDES PMA supply.
SERDES_1_L23_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for lane2 and lane3 of SERDESIF1, located on the right side. It is a +1.2 V SERDES PMA supply.
SERDES_1_L01_VDDAPLL		Analog power for SERDES1 PLL of lane0 and lane1. It is a +2.5 V SERDES internal PLL supply.
SERDES_1_L23_VDDAPLL		Analog power for SERDES1 PLL of lane2 and lane3. It is a +2.5 V SERDES internal PLL supply.
SERDES_1_L01_REFRET		Local on-chip ground return path for SERDES_1_L01_VDDAPLL for lane0 and lane1 of SERDESIF1, located on the left side. In a used condition, do not short to ground directly.
SERDES_1_L23_REFRET		Local on-chip ground return path for SERDES_1_L23_VDDAPLL for lane2 and lane3 of SERDESIF1, located on the right side.
SERDES_1_PLL_VDDA		High supply voltage for PLL SERDES1. It can be +2.5 V or +3.3 V.
SERDES_1_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL SERDES1

Notes:

1. *If unused, all bank supplies can be left floating in order to reduce leakage, except the JTAG I/O bank supply. The JTAG bank should always be powered with the appropriate VDDI bank supply. An MSIO bank supports 1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V voltages and an MSIOD/DDRIO bank supports 1.2 V / 1.5 V / 1.8 V / 2.5 V voltages. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the SmartFusion2 SoC FPGAs Fabric Architecture User's Guide.*
2. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry.*
3. *If used, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding PLL return path on-board. Unused PLLs can be left floating, using the software configuration to assert the power-down signal of the PLL to reduce the static power.*
4. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding return path on-board. In an **unused** condition, the entire group of pins must be connected to VSS (ground). Among quadrant-related pins, a different configuration for a subset of them is not allowed.*
5. *If used, **DO NOT** short to ground directly on the package or PCB. In an **unused** condition, the pins can be left floating, since they are connected on-die to VSS.*

Table 4 • **Supply Pins**

Name	Type	Description
CCC_NE0_PLL_VSSA	PLL return paths[5]	VDDA to on-die VSSA high pass filter connection for PLL0
CCC_NE_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL1
CCC_NW0_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL2
CCC_NW1_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL3
CCC_SW0_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL4
CCC_SW1_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL5
MDDR_PLL_VSSA		Analog ground pad for PLL of MDDR
FDDR_PLL_VSSA		Analog ground pad for PLL of FDDR
VSS	Ground	Ground pad for core and I/Os. Must always connect to ground.
VSSNVM		Analog sense circuit ground of eNVM. Must always connect to ground.

Notes:

1. *If unused, all bank supplies can be left floating in order to reduce leakage, except the JTAG I/O bank supply. The JTAG bank should always be powered with the appropriate VDDI bank supply. An MSIO bank supports 1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V voltages and an MSIOD/DDRIO bank supports 1.2 V / 1.5 V / 1.8 V / 2.5 V voltages. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the SmartFusion2 SoC FPGAs Fabric Architecture User's Guide.*
2. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry.*
3. *If used, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding PLL return path on-board. Unused PLLs can be left floating, using the software configuration to assert the power-down signal of the PLL to reduce the static power.*
4. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding return path on-board. In an **unused** condition, the entire group of pins must be connected to VSS (ground). Among quadrant-related pins, a different configuration for a subset of them is not allowed.*
5. *If used, **DO NOT** short to ground directly on the package or PCB. In an **unused** condition, the pins can be left floating, since they are connected on-die to VSS.*

Additional Notes on Supply Pins

1. As an alternative to leaving unused positive and ground level supplies floating (not connected, open), they can be shorted to VSS on-board. This could be considered a better practice in avionics, so that floating supplies do not pick up charge from radiation.
2. For on-board connectivity solutions, refer to the *SmartFusion2 Board Design Guidelines* application note (to be released).

JTAG Pins

JTAG pins can operate at any voltage—1.2 V / 1.5 V / 1.8 V /2.5 V / 3.3 V (nominal).

The debug port is implemented using a serial wire JTAG debug port (SWJ-DP) rather than a serial wire debug port (SW-DP). This enables either the M3 JTAG or the SW protocol to be used for debugging.

Table 5 • **JTAG Pin Names and Descriptions**

Name	Type	Bus Size	Description
JTAGSEL	In	1	JTAG controller selection. If JTAGSEL is pulled High, an external TAP controller connects to the JTAG interface—system controller TAP. If JTAGSEL is pulled Low, an external TAP controller connects to either the Cortex-M3 JTAG TAP (if debug is enabled) or an auxiliary TAP (if debug is disabled).
JTAG_TCK/ M3_TCK	In	1	Test clock. Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/pull-down resistor. If JTAG is not used, Microsemi recommends tying it off. Connect TCK to GND or +3.3 V through a resistor placed close to the FPGA pin. This prevents totem-pole current on the input buffer and operation in case TMS enters an undesired state. Note that to operate at all +3.3 V voltages, 500 Ohms to 1 KOhm will satisfy the requirements.
JTAG_TDI/ M3_TDI	In	1	Test data. Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
JTAG_TDO/ M3_TDO/ M3_SWO	Out	1	Test data. Serial output for JTAG boundary scan, ISP, and UJTAG usage. The TDO pin does not have an internal pull-up/-down resistor. M3_SWO: Serial Wire Viewer output
JTAG_TMS/ M3_TMS/ M3_SWDIO		1	Test mode select. The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, and TRST). There is an internal weak pull-up resistor on the TMS pin. M3_SWDIO: Serial Wire Debug data input/output
JTAG_TRSTB/ M3_TRSTB		1	Boundary scan reset pin. The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor (1K) could be included to ensure the TAP is held in Reset mode. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends that you tie off TRST to GND through a resistor (1K) placed close to the FPGA pin. The TRSTB pin also resets the serial wire JTAG debug port (SWJ-DP) circuitry within the Cortex-M3 processor.

Programming SPI

The system controller contains a dedicated SPI block for programming. The SPI is operated in either Master or Slave mode. In Master mode, the SmartFusion2 device is interfaced with an external SPI flash device and the programming data is downloaded from it to the FPGA. In Slave mode, it is communicated with a remote device that initiates download of the programming data to the FPGA..

Table 6 • **Programming SPI Interface**

Name	Type	Description
SC_SPI_SS	Out	SPI slave select
SC_SPI_SDO	Out	SPI data output
SC_SPI_SDI	In	SPI data input
SC_SPI_CLK	Out	SPI clock
FLASH_GOLDEN_N	In	If pulled Low, this indicates that the device is to be re-programmed from an image in the external SPI flash attached to the SPI interface. If pulled High, the SPI is put into slave mode. Add an external pull-up resistor value of 10 KOhms to +3.3 V.

Notes:

1. *If unused, SPI programming pins can be left floating.*
2. *For more details related to reset, clock, and programming, refer to the* SmartFusion2 Board Design Guidelines *application note (to be released).*

Dedicated I/Os

Dedicated I/Os (Table 7 and Table 8 on page 12) can be used for a single purpose such as SERDES, device reset, or clock functions. SmartFusion2 dedicated I/Os:

- Device reset pins
- Crystal oscillator pins
- SERDES I/Os
- Programming SPI pins

Table 7 • **Device Reset and Crystal Oscillator Pin Types and Descriptions**

Pin	Type	Description
Device Reset I/Os		
DEVRST_N	Input	Device reset; asserted Low and powered by VPP
Crystal Oscillator I/Os[1,2]		
EXTLOSC_x	Input	Crystal connection or external RC network.
XTLOSC_x	Input	Input clock from the main crystal oscillator

Notes:

1. *The M2S050 device has only a main crystal oscillator.*
2. *If unused, crystal oscillator pins should be grounded.*

SERDES I/Os

The SERDES I/Os available in SmartFusion2 devices are dedicated for high speed serial communication protocols. The SERDES I/Os support protocols such as PCI Express 2.0, XAUI, serial gigabit media independent interface (SGMII), serial rapid IO (SRIO), and any user-defined high speed serial protocol implementation in fabric. Refer to the *SmartFusion2 Board Design Guidelines* application note (to be released) for further information.

Table 8 • **SERDES I/O Port Names and Descriptions**

Port Name	Type	Description
Data / Reference Pads		
SERDES_x_RXD0_P	Input[1]	Receive data. SERDES differential positive input for each lane. Each SERDESIF consists of 4 RX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_RXD1_P		
SERDES_x_RXD2_P		
SERDES_x_RXD3_P		
SERDES_x_RXD0_N	Input[1]	Receive data. SERDES differential negative input for each lane. Each SERDESIF consists of 4 RX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1. I
SERDES_x_RXD1_N		
SERDES_x_RXD2_N		
SERDES_x_RXD3_N		
SERDES_x_TXD0_P	Output[2]	Transmit data. SERDES differential positive output for each lane. Each SERDESIF consists of 4 TX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_TXD1_P		
SERDES_x_TXD2_P		
SERDES_x_TXD3_P		
SERDES_x_TXD0_N	Output[2]	Transmit data. SERDES differential negative output for each lane. Each SERDESIF consists of 4 TX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_TXD1_N		
SERDES_x_TXD2_N		
SERDES_x_TXD3_N		
Common I/O Pads per SERDES Interface		
SERDES_x_L01_REXT	Reference[2]	External reference resistor connection to calibrate TX/RX termination value. Each SERDESIF consists of 2 REXT signals—one for lane0 and lane1, and another for lane2 and lane3. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_L23_REXT		
SERDES_x_REFCLK0_P	Clock[3]	Reference clock differential positive. Each SERDESIF consists of two signals (REFCLK0_P, REFCLK1_P). Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_REFCLK1_P		
SERDES_x_REFCLK0_N	Clock[3]	Reference clock differential negative. Each SERDESIF consists of two signals (REFCLK0_P, REFCLK1_P). Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_REFCLK1_N		

Notes:

1. *If unused, must always connect to VSS (ground).*
2. *If the SERDES unit is not being used, these pins must remain floating.*
3. *These pins are MUXed with MSIOD functionality. If SERDES functionality and MSIOD functionality are not used, the pins can be left floating. Libero SoC will disable unused I/Os and weakly pull them up.*

Special Pins

The two live probe I/O cells are dual-purpose. If live probe functionality will never be used on these I/Os, the user can configure the I/O as an input, output, or bidirectional. However, if the intent is to perform live switching between the user I/O and probe functionality, then use the I/O only as an output. If it were configured as an input during general use, then as soon as it is switched over to live probe operation, the probe circuitry would drive out onto this IO, potentially causing device damage.

Table 9 • **Special Pins**

Pin Name	Type	Description
PROBE_A	In/out	The two live probe IO cells are dual-purpose. 1. Live probe functionality 2. User I/O
PROBE_B		

Microcontroller Subsystem (MSS)

***Table 10* • MSS Pin Names and Descriptions**

Name	Type	Description
Inter-Integrated Circuit (I2C) Peripherals		
I2C_0_SCL	In/out	I2C bus serial clock output. Can also be used as an MSS GPIO or USB_DATA1_C or fabric I/O.
I2C_0_SDA	In/out	I2C bus serial data input/output. Can also be used as an MSS GPIO or USB_DATA0_C or fabric I/O.
I2C_1_SCL	in/out	I2C bus serial clock output. Can also be used as an MSS GPIO or USB_DATA4_A.
I2C_1_SDA	in/out	I2C bus serial data input/output. Can also be used as an MSS GPIO or USB_DATA3_A.
Universal Asynchronous Receiver/Transmitter (UART) Peripherals		
MMUART_0_CLK	Out	UART clock. Can also be used as an MSS GPIO or USB_NXT_C or fabric I/O.
MMUART_0_TXD	Out	UART transmit data. Can also be used as an MSS GPIO or USB_DIR_C or fabric I/O.
MMUART_0_RXD	In	UART receive data. Can also be used as an MSS GPIO or USB_STP_C or fabric I/O.
MMUART_0_CTS	In	UART clear to send. Can also be used as an MSS GPIO or USB_DATA7_C or fabric I/O.
MMUART_0_RTS	Out	UART request to send. Can also be used as an MSS GPIO or USB_DATA5_C or fabric I/O.
MMUART_0_DTR	Out	Modem data terminal ready. Can also be used as an MSS GPIO or USB_DATA6_C or fabric I/O.
MMUART_0_DCD	In	Modem data carrier detects. Can also be used as an MSS GPIO or fabric I/O.
MMUART_0_DSR	In	Modem data set ready. Can also be used as an MSS GPIO or fabric I/O.
MMUART_0_RI	In	Modem ring indicator. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_CLK	Out	UART Clock. Can also be used as an MSS GPIO or USB_DATA4_C.
MMUART_1_TXD	Out	UART transmit data. Can also be used as an MSS GPIO or USB_DATA2_C or fabric I/O.
MMUART_1_RXD	In	UART receive data. Can also be used as an MSS GPIO or USB_DATA3_C or fabric I/O.
MMUART_1_CTS	In	UART clear to send. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_RTS	Out	UART request to send. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_DTR	Out	Modem data terminal ready. Can also be used as an MSS GPIO or fabric I/O.

***Table 10* • MSS Pin Names and Descriptions (continued)**

Name	Type	Description
MMUART_1_DCD	In	Modem data carrier detects. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_DSR	In	Modem data set ready. Can also be used as an MSS GPIO or fabric I/O.
MMUART_1_RI	In	Modem ring indicator. Can also be used as an MSS GPIO or fabric I/O.
Serial Peripheral Interface (SPI) Controllers		
SPI_0_SS0	Out	SPI slave select0. Can also be used as an MSS GPIO or USB_NXT_A or fabric I/O.
SPI_0_SS1	Out	SPI slave select1. Can also be used as an MSS GPIO or USB_DATA5_A or fabric I/O.
SPI_0_SS2	Out	SPI slave select2. Can also be used as an MSS GPIO or USB_DATA6_A or fabric I/O.
SPI_0_SS3	Out	SPI slave select3. Can also be used as an MSS GPIO or USB_DATA7_A or fabric I/O.
SPI_0_SS4	Out	SPI slave select4. Can also be used as an MSS GPIO or fabric I/O.
SPI_0_SS5	Out	SPI slave select5. Can also be used as an MSS GPIO or fabric I/O.
SPI_0_SS6	Out	SPI slave select6. Can also be used as an MSS GPIO or fabric I/O.
SPI_0_SS7	Out	SPI slave select7. Can also be used as an MSS GPIO or fabric I/O.
SPI_0_CLK	Out	SPI clock. Can also be used as an MSS GPIO or USB_XCLK_A.
SPI_0_SDO	Out	SPI data output. Can also be used as an MSS GPIO or USB_STP_A or fabric I/O.
SPI_0_SDI	In	SPI data input. Can also be used as an MSS GPIO or USB_DIR_A or fabric I/O.
SPI_1_SS0	Out	SPI slave select0. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS1	Out	SPI slave select1. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS2	Out	SPI slave select2. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS3	Out	SPI slave select3. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS4	Out	SPI slave select4. Can also be used as an MSS GPIO or fabric I/O.

***Table 10* • MSS Pin Names and Descriptions (continued)**

Name	Type	Description
SPI_1_SS5	Out	SPI slave select5. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS6	Out	SPI slave select6. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SS7	Out	SPI slave select7. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_CLK	Out	SPI clock. Can also be used as an MSS GPIO.
SPI_1_SDO	Out	SPI data output. Can also be used as an MSS GPIO or fabric I/O.
SPI_1_SDI	In	SPI data input. Can also be used as an MSS GPIO or fabric I/O.

I/O Programmable Features

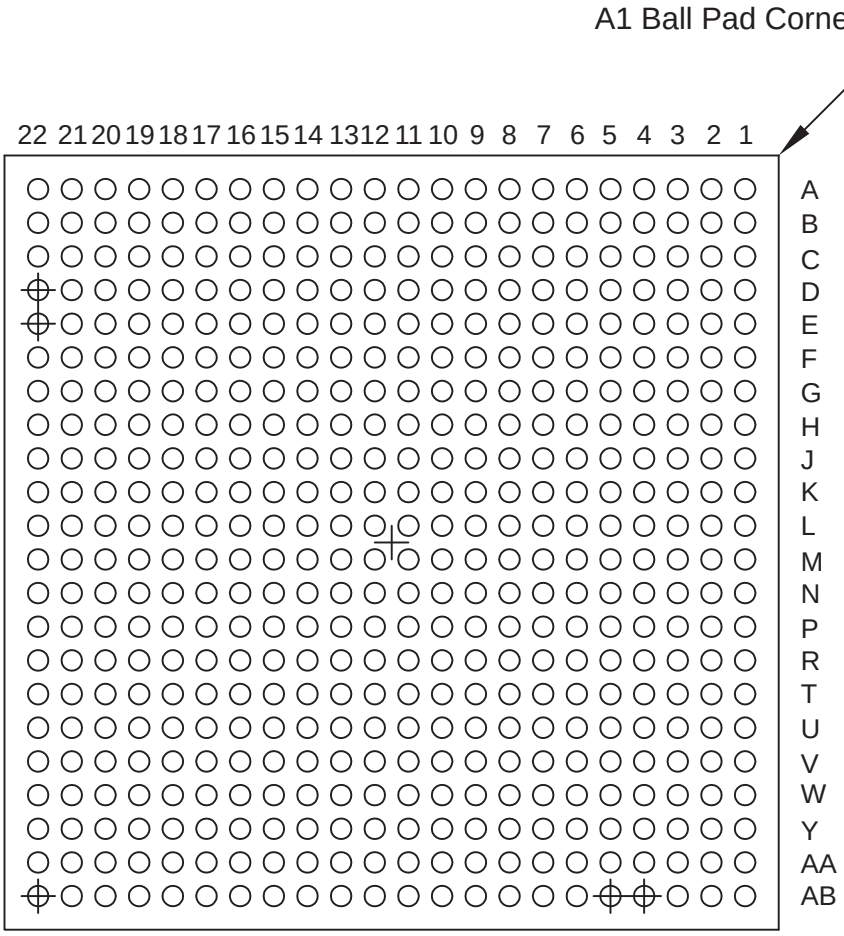
SmartFusion2 devices support different I/O programmable features for MSIO, MSIOD, and DDRIO. Each I/O pair (P, N) supports the following programmable features:

- Programmable drive strength
- Programmable weak pull-up and pull-down
- Configurable ODT and driver impedance
- Programmable input delay
- Programmable Schmitt input and receiver

For more information on SmartFusion2 I/O programmable features, refer to the "SmartFusion2 I/O Features" table of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

Packaging Information

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Pin Tables

Pin tables in Excel® format are located here:

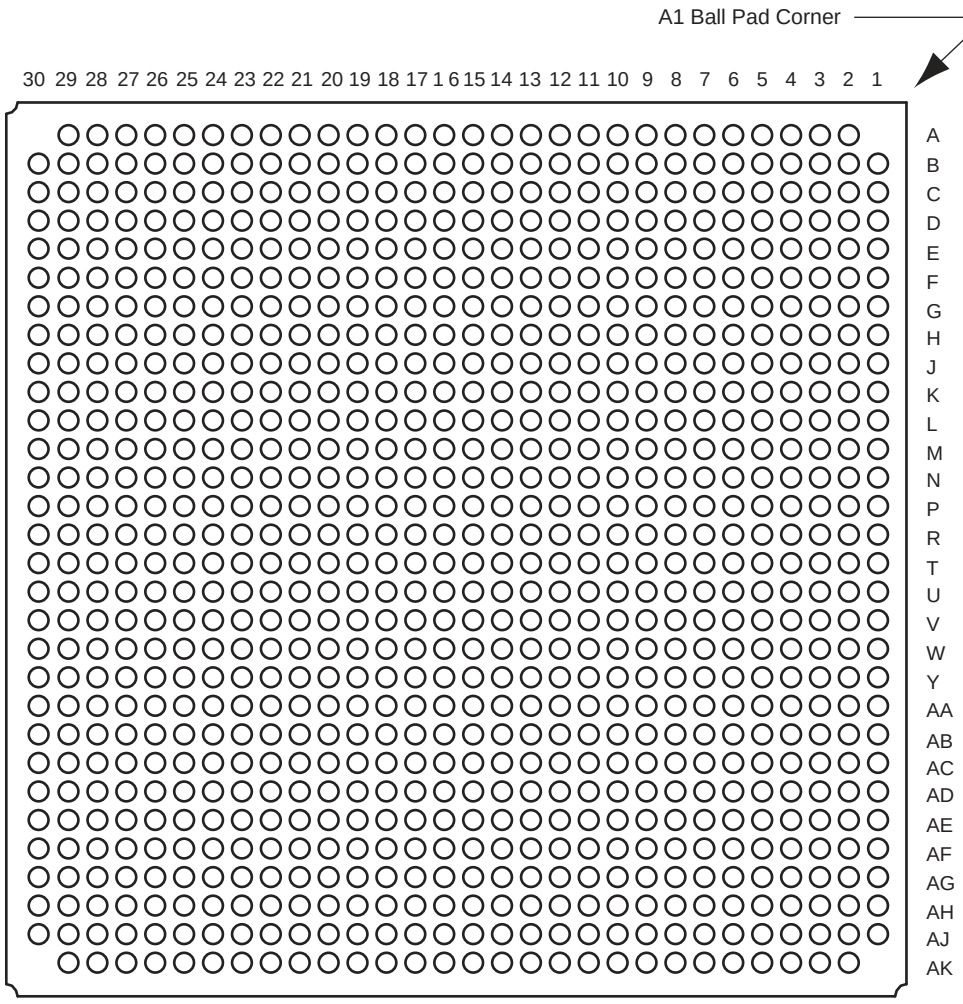
www.microsemi.com/soc/documents/SmartFusion2_FG484_pinouts.zip.

M2S010T

M2S025T

M2S050T

FG896



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Pin Tables

Pin tables in Excel format are located here:

www.microsemi.com/soc/documents/SmartFusion2_FG896_pinouts.zip.

M2S050T

List of Changes

The following table lists critical changes that were made in each revision of the SmartFusion2 Pin Descriptions.

Revision	Changes	Page
Revision 3 (February 2013)	The "SmartFusion2 Pin Descriptions" section has been separated from the rest of the SmartFusion2 datasheet and is now published separately. Pin tables have been removed from the document and replaced by links to sortable pin tables in an Excel spreadsheet. Pin tables for non-T devices are being reworked and will be included in a future release of the document (SAR 45184). The contents of the document have been reorganized (SAR 45275).	N/A
	Table 1 • The Organization of I/OBanks in SmartFusion2 Devices was corrected to change MSIOD to MSIO for bank 4 and bank 7, M2S010T and M2S025T devices on the FG484 package (SAR 45188).	3
	Notes were added to several tables giving instructions on how to handle pins if unused (SAR 45172): Table 3 • Reference Resistors Table 6 • Programming SPI Interface Table 7 • Device Reset and Crystal Oscillator Pin Types and Descriptions	 6 11 11
	The "Special Pins" section is new (SAR 44597).	13
	Connection information for some of the SERDES pins was clarified in the notes to Table 8 • SERDES I/O Port Names and Descriptions(SAR 45172).	12
Revision 2 (February 2013)	The document was revised extensively, including major changes to Table 4 • Supply Pins, new bank location diagrams, renaming of many pins and new pin tables for FG484 and FG896 (SARs 42905, 42497, 43861, 45081).	6
Revision 1 (January 2013)	Table 4 • Supply Pinswas revised to clarify instructions for unused pins (SAR 42435).	6
	Figure 1 • SmartFusion2 (M2S050T) I/O Bank Location and Namingwas revised. The number of pairs in bank 1 was corrected to 10 (was 11) and the number of pairs in bank 3 was corrected to 23 (was 25). Table 2 • SmartFusion2 (M2S050T) I/O Bank Resource Usage is new (SAR 42412).	5
	Table 3 • Reference Resistorsis new (SAR 42835).	6
	The description for the FLASH_GOLDEN pin in Table 6 • Programming SPI Interface was corrected to reverse the conditions for High and Low (SAR 42484).	11
	Table 8 • SERDES I/O Port Names and Descriptionswas revised to clarify handling of pins with and without transceiver (SAR 42494).	12
	The "FG484" section is new, including pin tables for M2S010T, M2S025T, and M2S050T (SAR 42480).	17

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