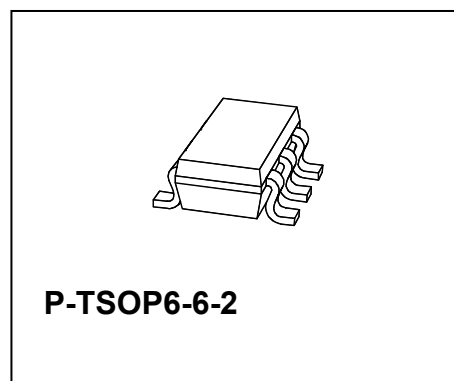


## Low Power Hall Switch

**TLE 4917**

### Features

- Micro power design
- 2.4 V to 5.5 V battery operation
- High sensitivity and high stability of the magnetic switching points
- High resistance to mechanical stress
- Digital output signal
- Switching for both poles of a magnet (omnipolar)
- Programming pin for the switching direction of the output
- Not suitable for automotive application



### Functional Description

The TLE 4917 is an Integrated Hall-Effect Sensor designed specifically to meet the requirements of low-power devices. e.g. as an On/Off switch in Cellular Flip-Phones, with battery operating voltages of 2.4V – 5.5V.

Precise magnetic switching points and high temperature stability are achieved through the unique design of the internal circuit.

An onboard clock scheme is used to reduce the average operating current of the IC.

During the operate phase the IC compares the actual magnetic field detected with the internally compensated switching points. The output Q is switched at the end of each operating phase.

During the Stand-by phase the output stage is latched and the current consumption of the device reduced to some  $\mu\text{A}$ .

The IC switching behaviour is omnipolar, i.e. it can be switched on with either the North or South pole of a magnet.

The PRG pin can be connected to  $V_S$  which holds the output  $V_Q$  at a High level for  $B=0\text{mT}$ ; conversely the output  $V_Q$  can be inverted by connecting the PRG pin to GND, which will hold the output  $V_Q$  at a Low level for  $B=0\text{mT}$ . In this later case the presence of an adequate magnetic field will cause the output  $V_Q$  to switch to a High level ( i.e. off state ).

Type	Marking	Ordering Code	Package
TLE 4917	17s	Q62705K 605	P-TSOP6-6-2

## Pin Configuration (top view)

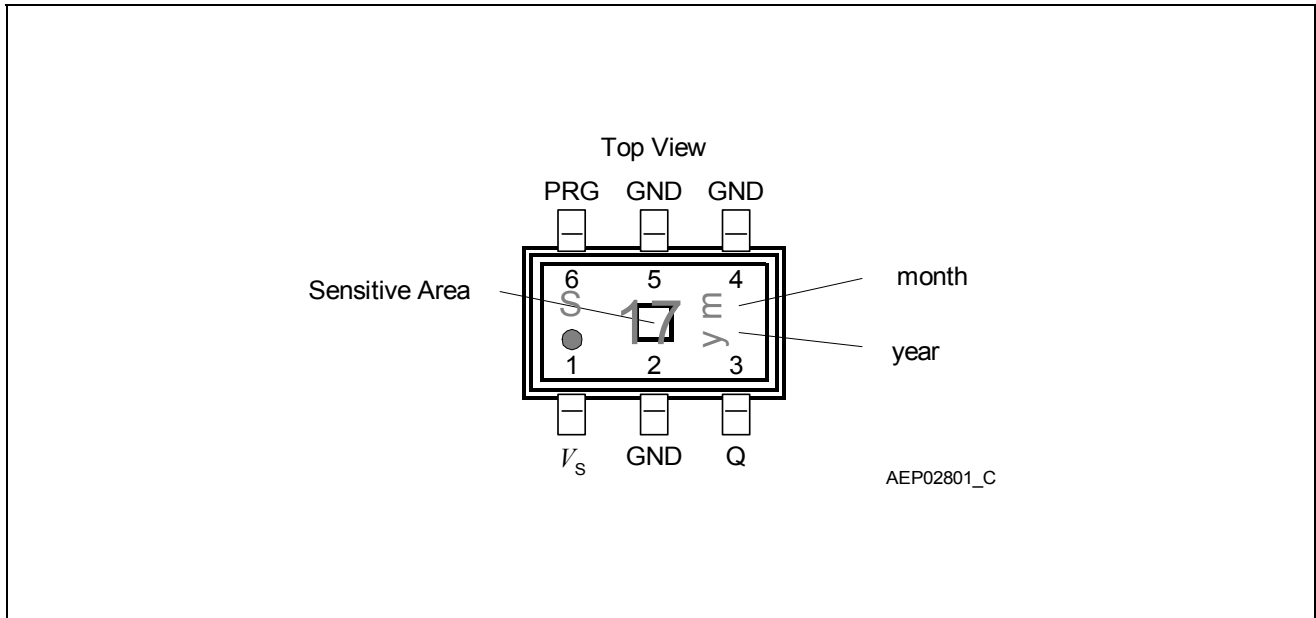
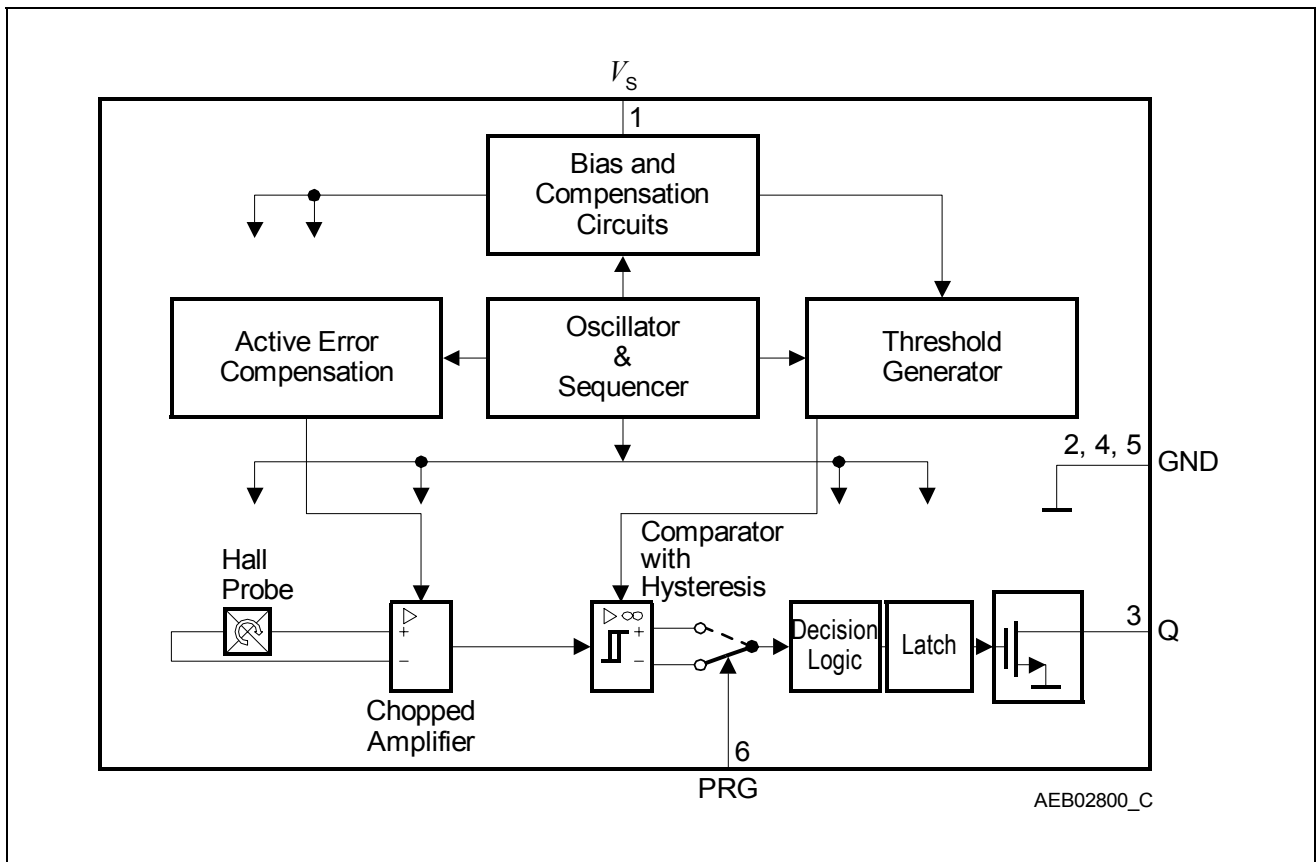


Figure 1

## Pin Definitions and Functions

Pin	Symbol	Function
1	$V_S$	Supply Voltage
2	$GND$	Ground
3	$Q$	Open Drain Input
4	$GND$	Ground
5	$GND$	Ground
6	$PRG$	Programming Input



**Figure 2 Block Diagram**

## Circuit Description

The Low Power Hall IC Switch comprises a Hall probe, bias generator, compensation circuits, oscillator, output latch and an n-channel open drain output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce technology variations.

The Active Error Compensation rejects offsets in signal stages and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stresses in the package. This chopper technique together with the threshold generator and the comparator ensures high accurate magnetic switching points.

Very low power consumption is achieved with a timing scheme controlled by an oscillator and a sequencer. This circuitry activates the sensor for 50  $\mu\text{s}$  (typical operating time) sets the output state after sequential questioning of the switch points and latches it with the beginning of the following standby phase (typ. 130 ms). In the standby phase the average current is reduced to typical 3.5  $\mu\text{A}$ . Because of the long standby time compared to the operating time the overall averaged current is only slightly higher than the standby current.

By connecting the programming pin to GND (normal to  $V_S$ ) the Output State can be inverted to further reduce the current consumption in applications where a high magnetic field is the

normal state. In that case the output Q is off at high magnetic fields and no current is flowing in the open drain transistor.

The output transistor can sink up to 1 mA with a maximal saturation voltage  $V_{QSAT}$ .

### Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply Voltage	$V_S$	- 0.3	5.5	V	
Supply Current	$I_S$	- 1	2.5	mA	
Output Voltage	$V_Q$	- 0.3	5.5	V	
Output Current	$I_Q$	- 1	2	mA	
Programming Pin Voltage	$V_{PRG}$	- 0.3	5.5 <sup>1)</sup>	V	
Junction temperature	$T_j$	- 40	150	°C	
Storage temperature	$T_S$	- 40	150	°C	
Magnetic Flux Density	$B$	-	unlimited	mT	
Thermal Resistance P-TSOP6-6-2	$R_{th JA}$	-	35	K/W	

<sup>1)</sup>  $V_{PRG}$  must not exceed  $V_S$  by more than 0.3V

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### ESD Protection

Human Body Model (HBM) tests according to:  
EOS/ESD Association Standard S5.1-1993 and Mil. Std. 883D method 3015.7

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	max.		
ESD Voltage	$V_{ESD}$	± 2		kV	$R = 1.5 \text{ k}\Omega$ , $C = 100 \text{ pF}$ ; $T = 25 \text{ }^\circ\text{C}$

## Operating Range

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	typ.	max.		
Supply voltage	$V_S$	2.4	2.7	5.5	V	<sup>1)</sup>
Output voltage	$V_Q$	- 0.3	2.7	5.5	V	
Programming Pin Voltage	$V_{PRG}$	- 0.3	0	0.3	V	Inverted output state
		$V_S - 0.3$	$V_S$	$V_S + 0.3$		Standard output state
Ambient Temperature	$T_A$	- 40	25	85	°C	

<sup>1)</sup> A Ceramic Bypass Capacitor of 10 nF at  $V_S$  to GND is highly recommended.

## AC/DC Characteristics

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	typ.	Max.		
Averaged Supply Current	$I_{SAVG}$	1	4	20	μA	
Averaged Supply Current during Operating Time	$I_{SOPAVG}$	0.5	1.1	2.5	mA	
Transient Peak Supply Current during Operating Time	$I_{SOPT}$	–	–	2.5	mA	$t < 100$ ns
Supply Current during Standby Time	$I_{SSTB}$	1	3.5	20	μA	
Output Saturation Voltage	$V_{QSAT}$	–	0.13	0.4	V	$I_Q = 1$ mA
Output Leakage Current	$I_{QLEAK}$	–	0.01	1	μA	
Output Rise Time	$t_r$	–	0.3	1	μs	$R_L = 2.7$ kΩ; $C_L = 10$ pF
Output Fall Time	$t_f$	–	0.1	1	μs	$R_L = 2.7$ kΩ; $C_L = 10$ pF
Operating Time	$t_{op}$	15	50	93 <sup>1) 2)</sup>	μs	
Standby Time	$t_{stb}$	–	130	240 <sup>3)</sup>	ms	
Duty Cycle	$t_{op} / t_{stb}$	–	0.039	–	%	
Start-up Time of IC	$t_{stu}$	–	6	12	μs	<sup>4)</sup>

<sup>1)</sup> for  $V_S=3.5$ V the max. Operating Time  $t_{op \max} = 85$ μs

<sup>2)</sup> includes the Start-up Time  $t_{stu}$

<sup>3)</sup> for  $V_S=3.5$ V the max. Standby Time  $t_{stb \max} = 220$ ms

<sup>4)</sup> initial power on time.  $V_S$  must be applied in this time ( typ. 6μs to max. 12μs ) to get already a valid output state after the first operating phase (typ. 56μs). For rise times of  $V_S > 12$ μs, the output state is valid after the second operating phase (includes one standby phase), e.g. happens only when the battery in flip phones is changed.

## Magnetic Characteristics

### PRG Pin Connected to $V_S$

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	typ.	max.		
Operate Points	B <sub>OPS</sub>	3.5	5	7	mT	1)
	B <sub>OPN</sub>	-7	-5	-3.5	mT	
Release Points	B <sub>RPS</sub>	2.2	4	6	mT	1)
	B <sub>RPN</sub>	-6	-4	-2.2	mT	
Hysteresis	B <sub>HYS</sub>	0.2	1	2	mT	

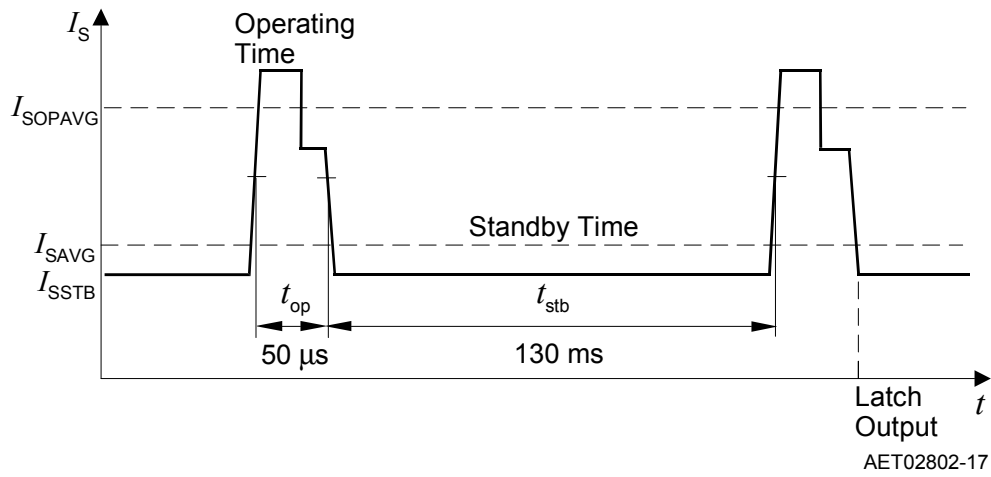
<sup>1)</sup> Positive magnetic fields are related to the approach of a magnetic south pole to the branded side of package

### PRG Pin Connected to GND

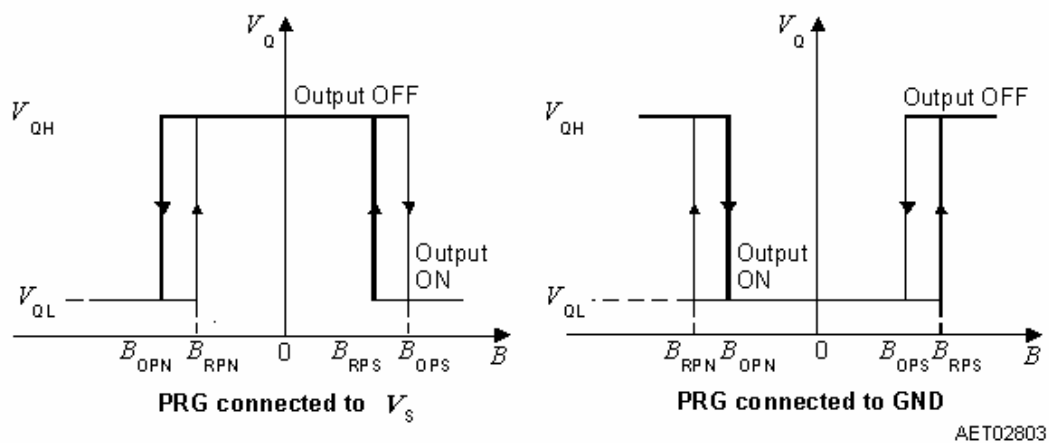
Parameter	Symbol	Limit Values			Unit	Notes
		Min.	typ.	max.		
Operate Points	B <sub>OPS</sub>	2.2	4	6	mT	1)
	B <sub>OPN</sub>	-6	-4	-2.2	mT	
Release Points	B <sub>RPS</sub>	3.5	5	7	mT	1)
	B <sub>RPN</sub>	-7	-5	-3.5	mT	
Hysteresis	B <sub>HY</sub>	0.2	1	2	mT	

<sup>1)</sup> Positive magnetic fields are related to the approach of a magnetic south pole to the branded side of package

*Note: The listed AC/DC and magnetic characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not other specified, typical characteristics apply at  $T_j = 25\text{ °C}$  and  $V_S = 2.7\text{ V}$ .*



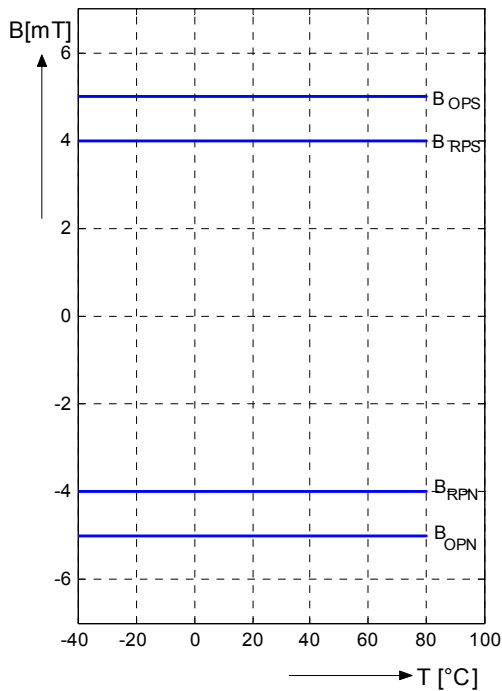
**Figure 3 Timing Diagram**



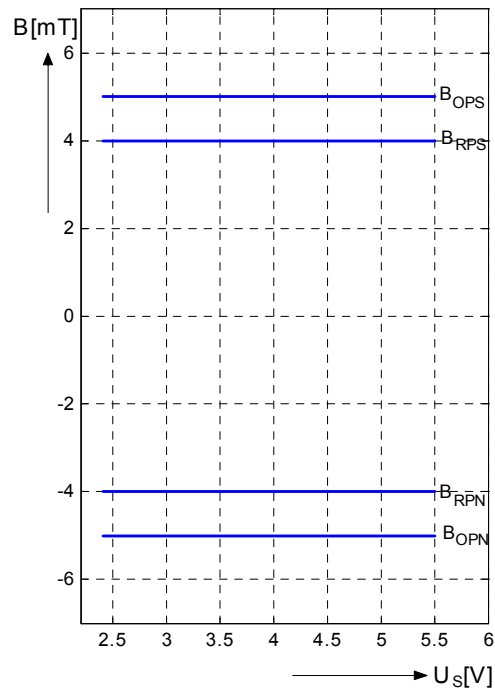
**Figure 4 Programming of Output with the PRG Pin**

All curves reflect typical values at the given parameters for  $T_A$  in  $^{\circ}\text{C}$  and  $V_S$  in V.

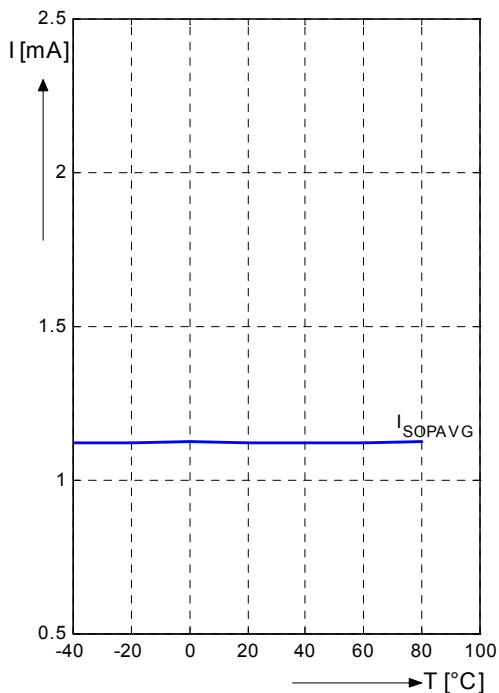
**Magnetic Switching Points versus Temperature ( $V_S=2.7\text{V}$ )**  
(PRG Pin Connected to  $V_S$ )



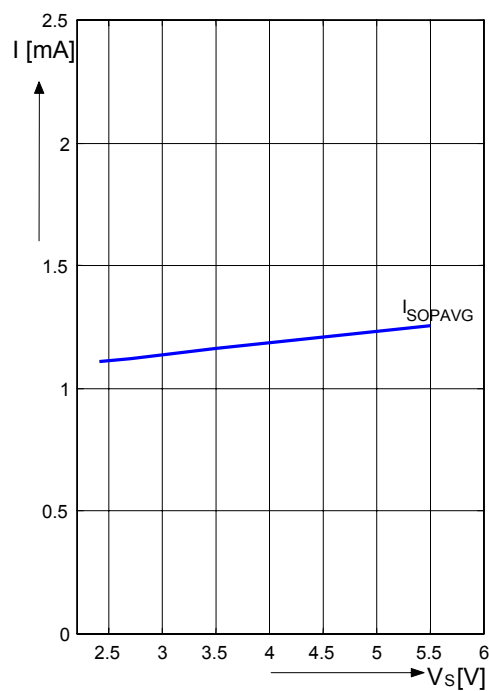
**Magnetic Switching Points versus Supply Voltage  $V_S$  ( $T_A=20^{\circ}\text{C}$ )**  
(PRG Pin Connected to  $V_S$ )



**Supply current  $I_{SOPAVG}$  during Operating Time versus Temperature ( $V_S=2.7\text{V}$ )**

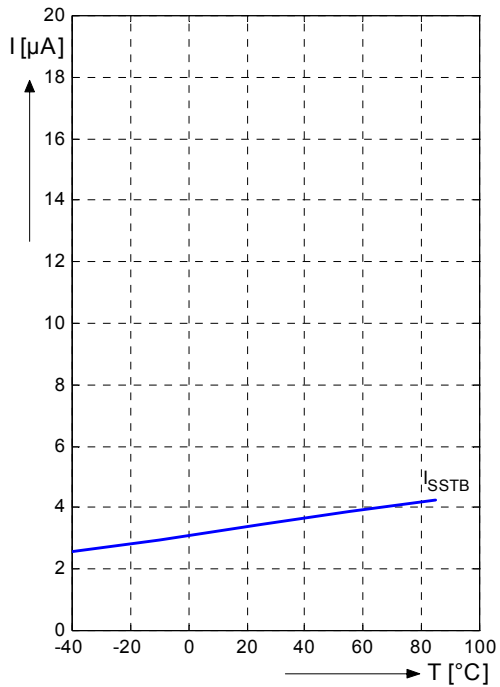


**Supply current  $I_{SOPAVG}$  during Operating Time versus Supply Voltage  $V_S$  ( $T_A=20^{\circ}\text{C}$ )**

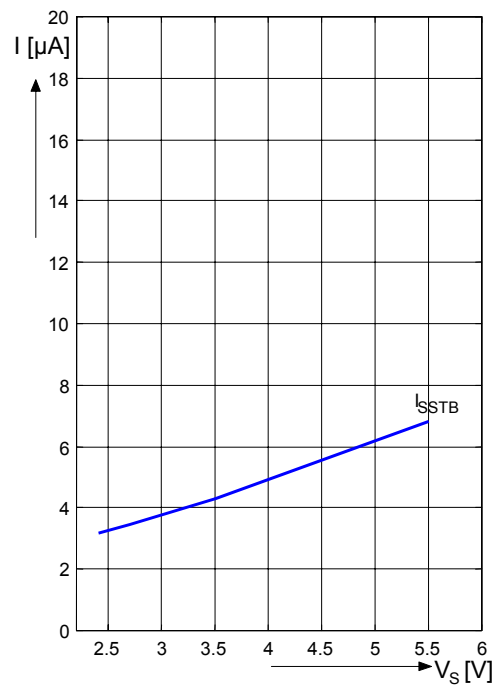




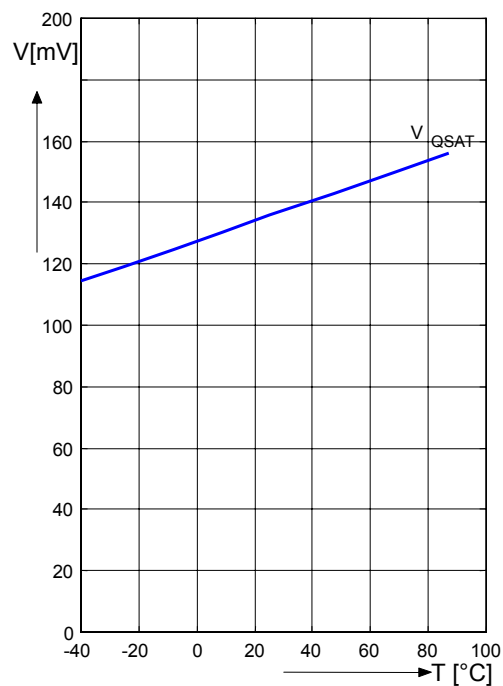
**Supply current  $I_{SSTB}$  during Standby  
Time versus Temperature ( $V_S=2.7V$ )**



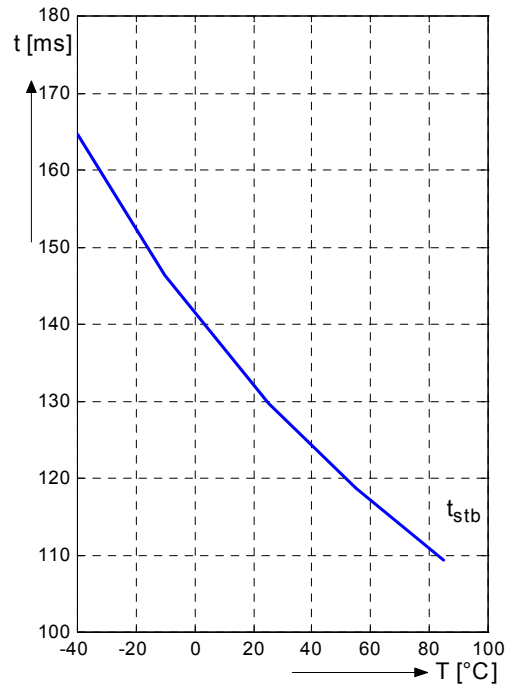
**Supply current  $I_{SSTB}$  during Standby  
Time versus Supply Voltage  $V_S$  ( $T_A=20^{\circ}C$ )**

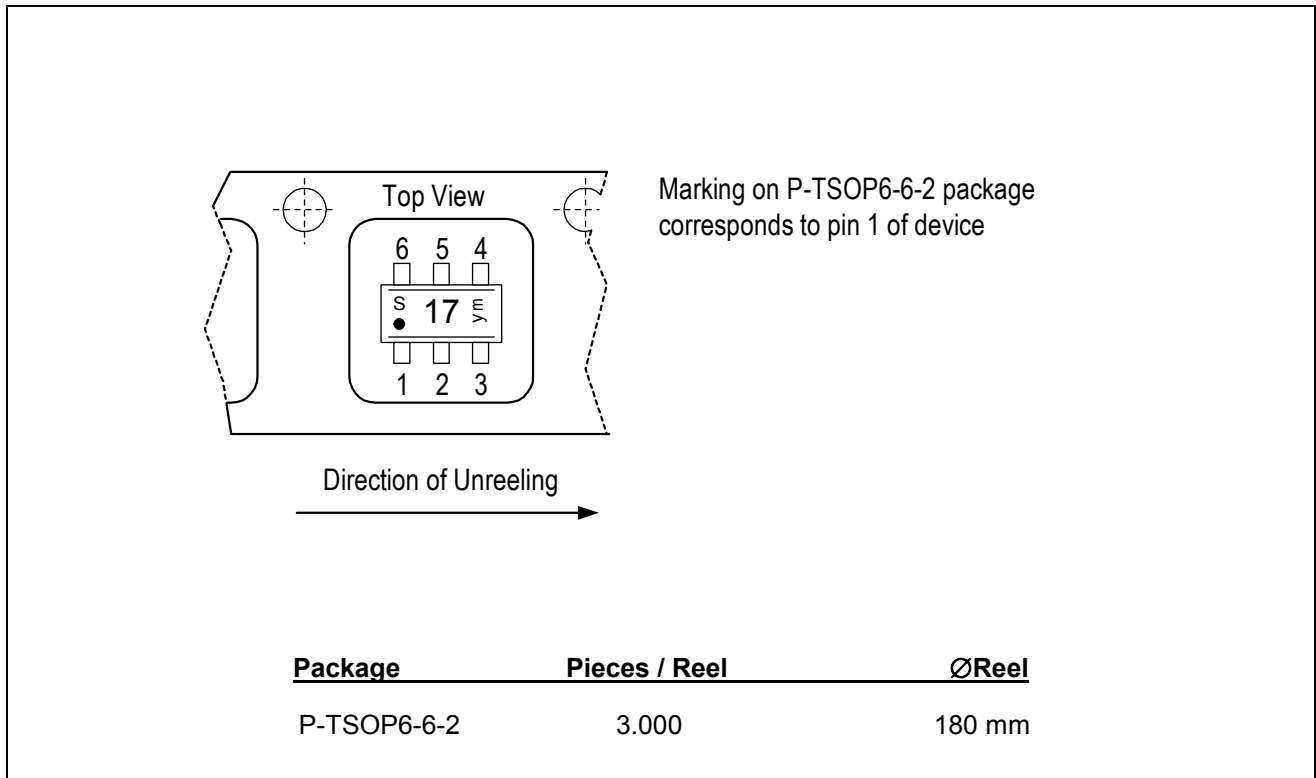


**Output Saturation voltage  $V_{QSAT}$   
versus Temperature ( $I_Q=1mA$ )**

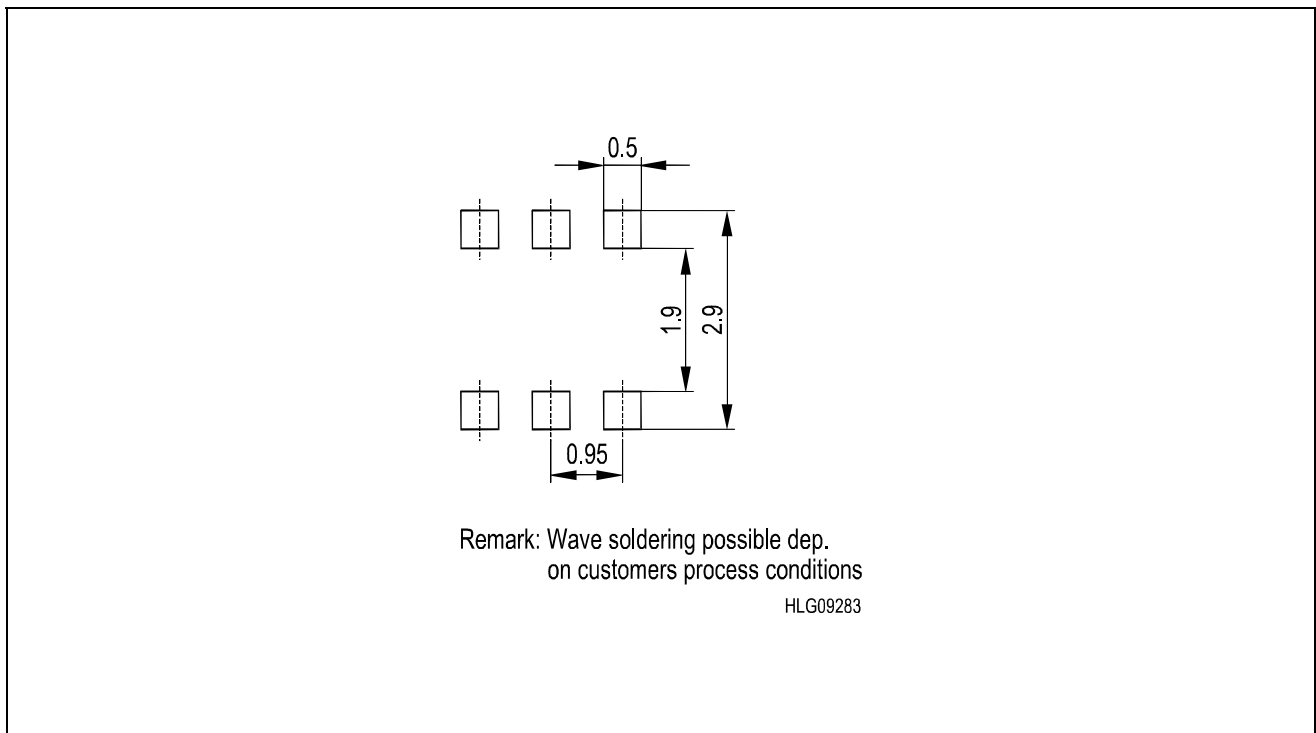


**Standby Time  $t_{stb}$  versus Temperature  
( $V_S = 2.7V$ )**





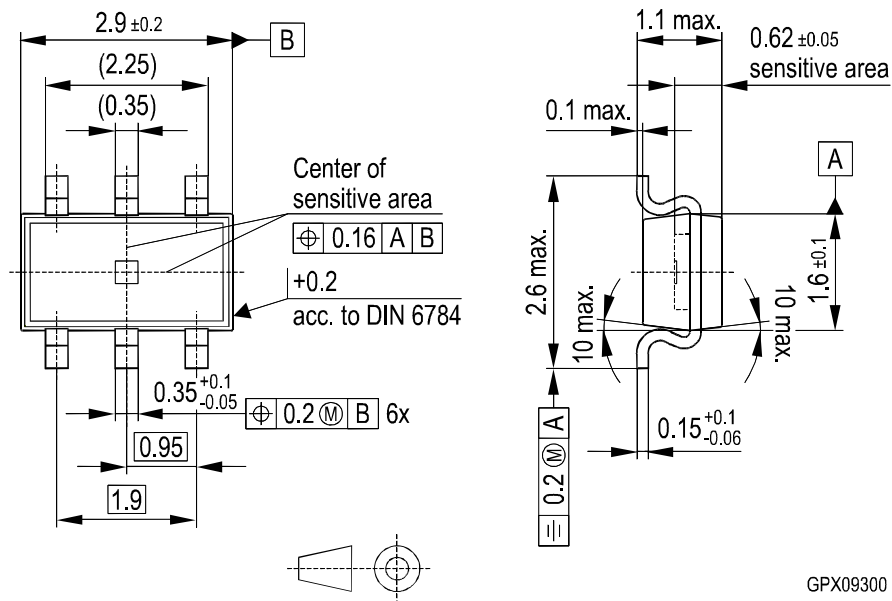
**Figure 5 Marking and Tape Loading Orientation**



**Figure 6 Foot Print Reflow Soldering**

## Package Dimensions

### P-TSOP6-6-2 (Plastic Thin Small Outline-Package)



weight : 0.015g  
coplanary : 0.1mm

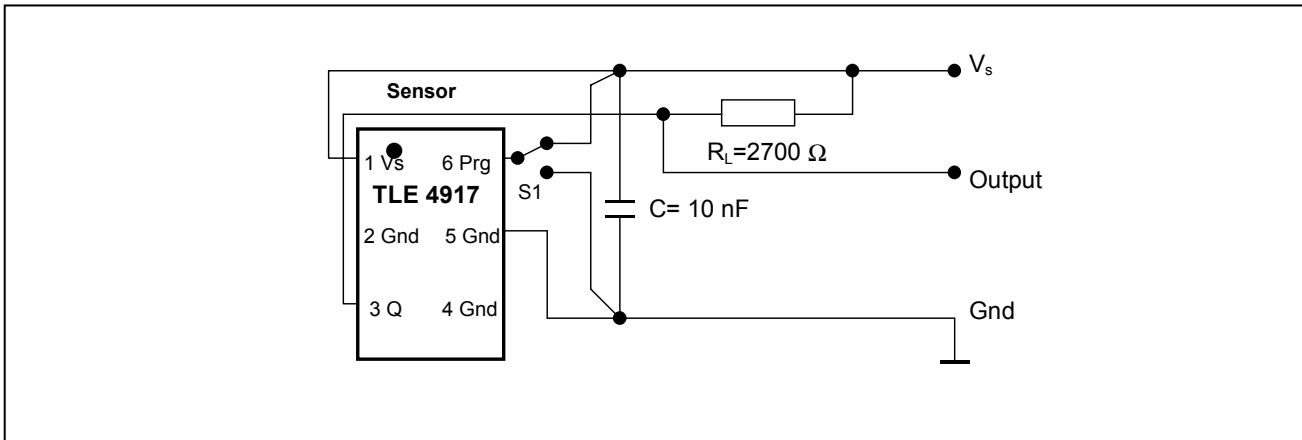
## Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

## Information about the application circuit of the TLE 4917



### Application circuit TLE 4917

The minimum value for the pull up resistor can be calculated with the power supply voltage  $V_s$ , the maximum current  $I_{Qmax}$  and the minimum output saturation voltage  $V_{QSAT}$ .

Example:

for  $V_s = 3\text{ V}$ :  $R_{Lmin} = (V_s - V_{QSATmin})/I_{Qmax} = (3\text{ V} - 0,1\text{ V})/0,002\text{ A} = 1435\ \Omega$

Larger values for  $R_L$  will reduce the current  $I_Q$  and therefore the power consumption. If the resistor  $R_L$  is very large ( $>100\text{ k}\Omega$ ) a capacitor (app. 10pF) between Output and GND pin could be useful if capacitive coupled noise occurs.

The load at the output Q should have a large input resistance to reduce the current through  $R_L$  and the power consumption.

The TLE 4917 has 3 ground pins. From a mechanical point of view all ground pins should be connected to ground. Shortest wires should be used to avoid ground loops.

If there is a need to reduce the number of used ground-pins any ground-pin combination may be used. Furthermore it is possible using only one ground-pin at the application, all pins are equivalent.

The capacitor C is highly recommended to reduce noise on the power supply voltage and it will improve the EMI/EMC performance.

Furthermore it decreases the transient peak supply current during operation time. The IC toggles between low and high current consumption. This behaviour might produce additional noise at the power supply. The capacitor will reduce this noise.

Furthermore this capacitor is used to supply the sensor if microbreaks (short loss of supply voltage) occur.

Shortest connection wires between IC and capacitor should be used to avoid noise.

The switch S1 shows the programming feature of the output.

Example:

If the PRG-pin is connected to  $V_s$  the IC will hold the output Q at a high voltage level for  $B = 0\text{ mT}$  in this circuit. A magnetic field larger than the operating point will switch the output to low level. In typical applications the PRG-pin is connected directly to  $V_s$  or to GND depending on the technical needs. Avoid using a floating PRG-pin.

<b>TLE 4917</b>	
<b>Revision History: 2002-08-22</b>	
Previous Version:	
Page	Subjects (major changes since last revision)

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