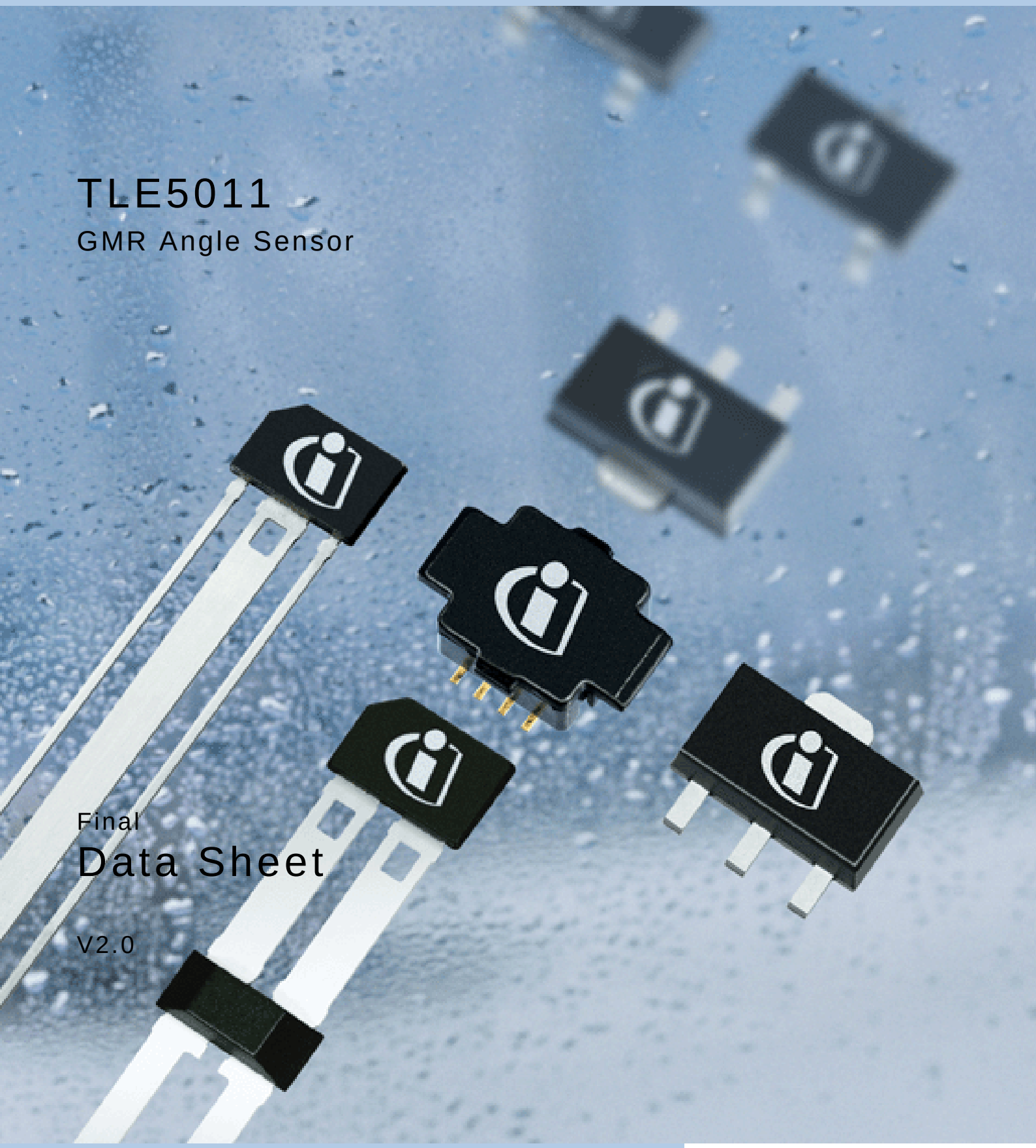
March 2011

TLE5011

GMR Angle Sensor



Final

Data Sheet

V2.0

Sensors

Never stop thinking

Edition 2011-03

Published by
Infineon Technologies AG
81726 Munich, Germany

© 2011 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History: 2011-03, V2.0

Previous Revision: V1.0

Page	Subjects (major changes since last revision)
6	Ordering code updated
7	Section 1.2 updated
14	Table 3, supply voltage and magnetic induction expanded; figure 7 added
15	Table 4; notes of supply current expanded
16	Table 5; table 6 added
17	Table 7, ESD expanded
21	Table 10, Notes updated
27	Table 14, register 0x0D updated
42	Package outline in figure 23 modified
43	Figure 24 added
general	Spelling and typing errors

We Listen to Your Comments

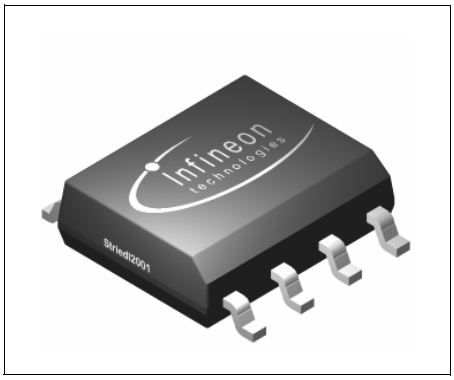
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continously improve the quality of this document.

Please send your proposal (including a reference to this document) to:

sensors@infineon.com

Table of Contents

1 Product Description



1.1 Overview

The TLE5011 is a 360° angle sensor that detects the orientation of a magnetic field by measuring sine and cosine angle components with monolithic **i**ntegrated **G**iant **M**agneto **R**esistance (**iGMR**) elements.

Data communications are accomplished with a bi-directional **S**ynchronous **S**erial **C**ommunication (**SSC**) interface that is SPI compatible.

The sine and cosine values can be read out digitally. These signals can be digitally processed to calculate the angle orientation of the magnetic field (magnet). This calculation can be done by using a **CO**ordinate **R**otation **DI**gital **C**omputer (**CORDIC**) algorithm.

It is possible to connect more than one TLE5011 to one SSC interface of a microcontroller for redundancy or any other reason. If multiple TLE5011 devices are used, the synchronization of the connected TLE5011 is performed by a broadcast command.

Each connected TLE5011 can be addressed by a dedicated Chip Select $\overline{CS}$ pin.

Type	Marking	Ordering Code	Package
TLE5011	5011	SP000857850	PG-DSO-8

1.2 Features

- **G**iant **M**agneto **R**esistance (GMR)-based principle
- Integrated magnetic field sensing for angle measurement
- Designed for 3.3 V and 5 V systems
- Full 0 - 360° angle measurement
- Highly accurate single-bit SD-ADC
- 16-bit representation of sine / cosine values on the interface
- Wide magnetic operating range: 30mT to 50mT
- Bi-directional SSC interface up to 2 Mbit/s
- 3-pin SSC interface, SPI compatible with open drain
- ADCs and filters synchronized with external commands via SSC
- Test resistors for simulating angle values
- Core supply voltage 2.5 V
- 0.25-µm CMOS technology
- Automotive qualified: -40°C to +150°C (junction temperature)
- Latch-up immunity according JEDEC standard
- ESD > 4 kV (HBM)
- Green package with lead-free (Pb-free) plating

1.3 Application Example

The TLE5011 GMR angle sensor is designed for angular position sensing in automotive applications, such as:

- Steering angle
- Brushless DC motor commutation (e.g. **E**lectric **P**ower **S**teering (**EPS**))
- Rotary switch
- General angular sensing

2 Functional Description

2.1 General

The GMR angle sensor is implemented in vertical integration. This means that the GMR active areas are integrated above the logic portion of the TLE5011 device. GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone sensor bridge. These GMR elements sense either of two components of the applied magnetic field:

- X component, V_X (cosine)
- Y component, V_Y (sine)

The advantage of a full-bridge structure is that the amplitude of the GMR signal is doubled.

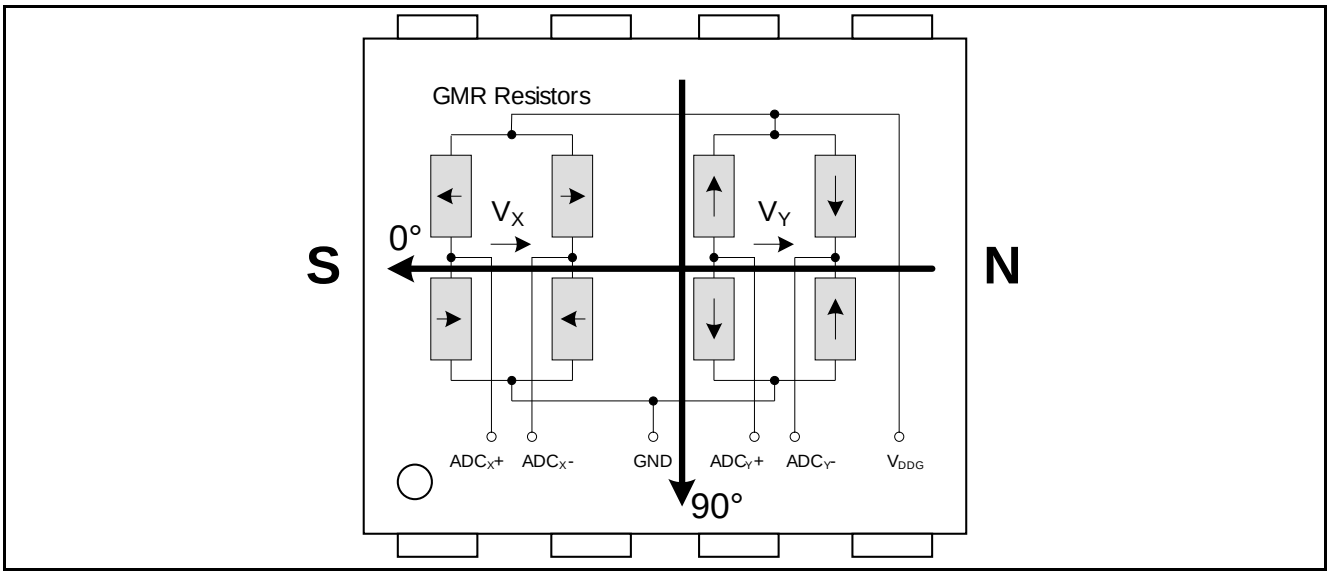


Figure 1 Sensitive Bridges of the GMR Angle Sensor

*Note: In **Figure 1**, the arrows in the resistor symbols denote the direction of the reference layer, which is used for the further explanation (**Figure 2**).*

The output signal of each bridge is only unambiguous over 180°between two maxima. Therefore two bridges are orientated orthogonally to each other to measure the 360°angle range.

Using the ARCTAN function, the true 360°angle value can be calculated that is represented by the relation of the cosine (here X) and sine (here Y) signals.

Because only the relative values influence the result, the absolute size of the two signals is of minor importance. Therefore, most influences on the amplitudes are compensated.

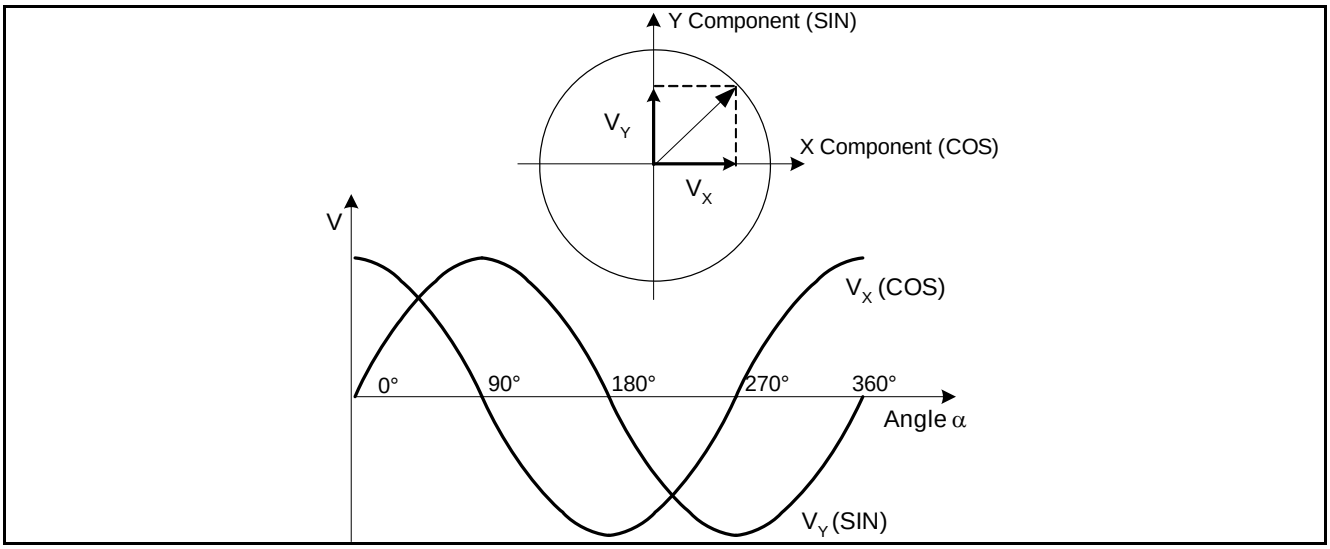


Figure 2 Ideal Output of the GMR Angle Sensor

2.2 Pin Configuration

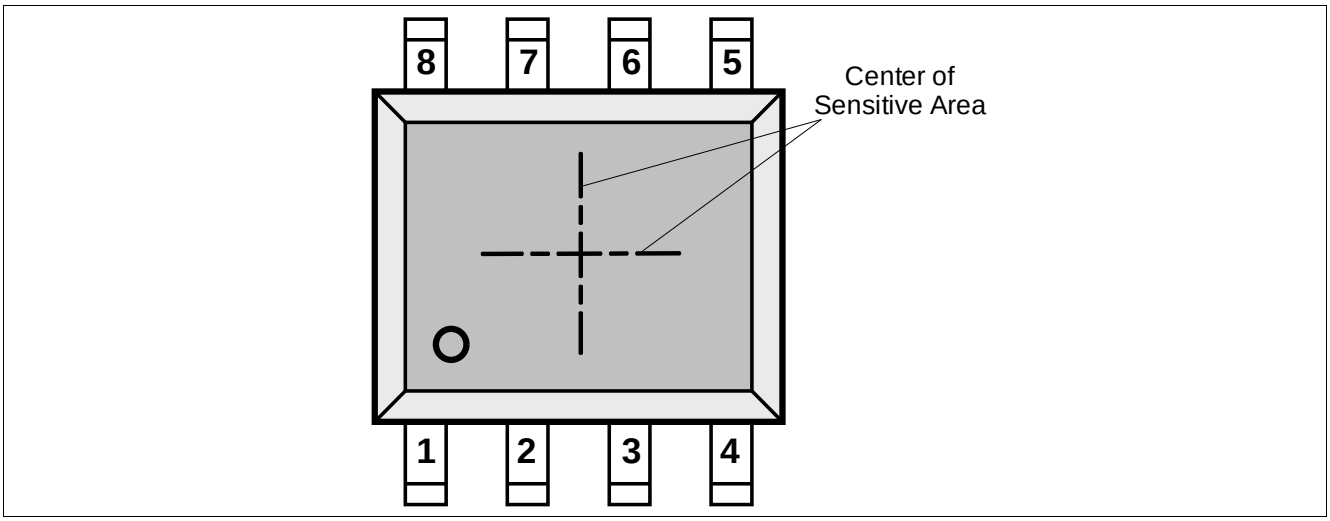


Figure 3 Pin Configuration (Top View)

2.3 Pin Description

Table 1 Pin Describtion

Pin No.	Symbol	In/Out	Function
1	*CLK*	*I*	Chip Clock
2	*SCK*	*I*	SSC Clock
3	$\overline{CS}$	*I*	SSC Chip Select
4	*DATA*	*I/O*	SSC Data, open drain
5	*TST1*	*I/O*	Test Pin 1, must be connected to GND
6	V_{DD}	-	Supply Voltage
7	*GND*	-	Ground
8	*TST2*	*I/O*	Test Pin 2, must be connected to GND

2.4 Block Diagram

The block diagram shows all switches in the reset position.

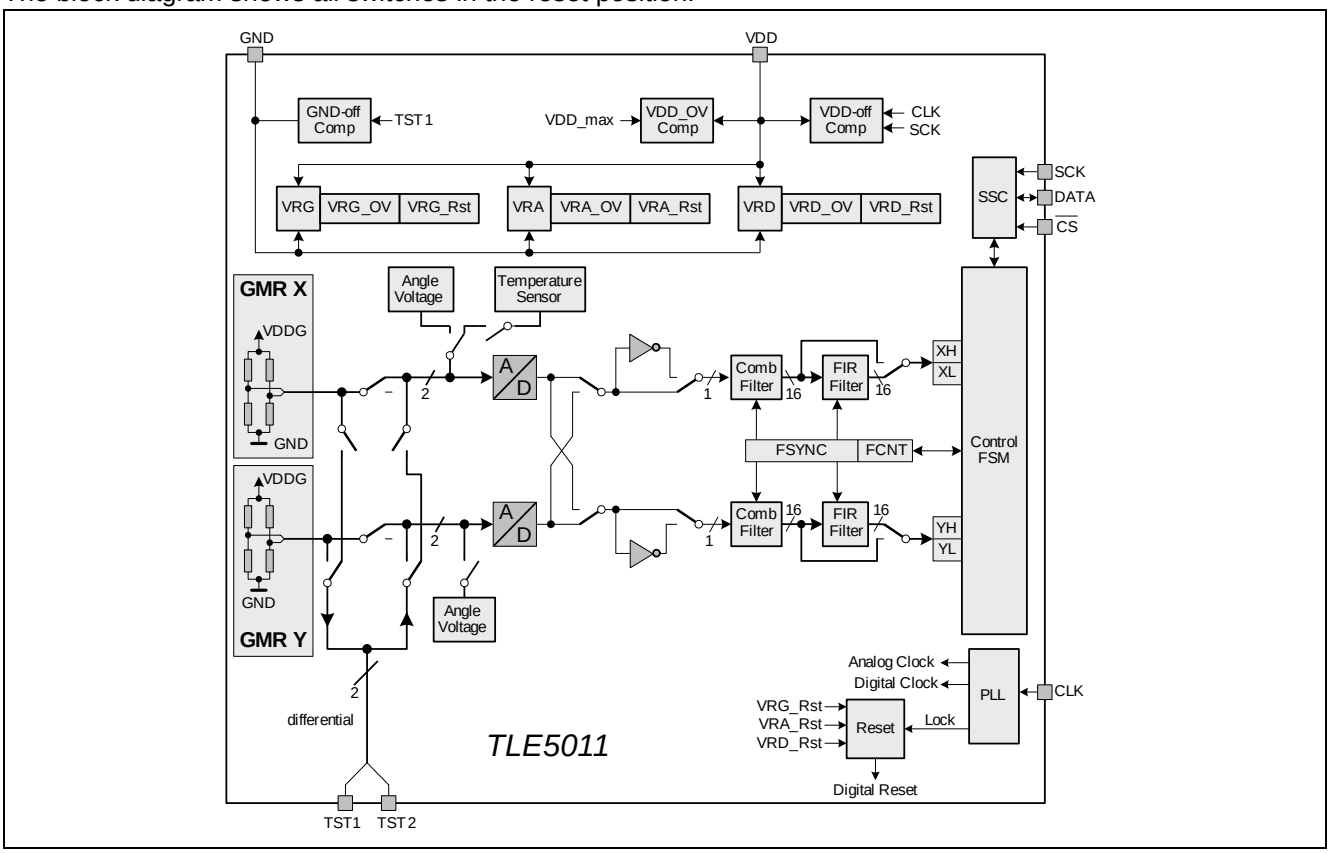


Figure 4 Block Diagram

2.5 Functional Block Description

2.5.1 Internal Power Supply

The internal stages of the TLE5011 are supplied with different voltage regulators:

- GMR Voltage Regulator VRG
- Analog Voltage Regulator VRA
- Digital Voltage Regulator VRD

Each voltage regulator has its own overvoltage and undervoltage detection circuits.

2.5.2 GMR Voltage Regulator VRG (VDDG-Voltage)

The GMR voltage regulator supplies all GMR parts:

- GMR bridges
- Test voltages for angle test
- ADC reference voltage

The voltages are monitored in the VRG overvoltage and undervoltage detectors.

2.5.3 Analog Voltage Regulator VRA (VDDA-Voltage)

The analog voltage regulator supplies the analog parts:

- ADCs
- PLL (analog)
- VDD-off comparator
- GND-off comparator
- V_{DD} Overvoltage detection

The voltages are monitored in the VRA overvoltage and undervoltage detectors.

2.5.4 Digital Voltage Regulator VRD (VDDD-Voltage)

The digital voltage regulator supplies all digital parts:

- Comb filters, FIR filters
- PLL (digital)
- Control FSM with bitmap
- SSC interface
- Counters (Reset, FSYNC, FCNT)

The voltages are monitored in the VRD overvoltage and undervoltage detectors.

2.5.5 Phase-Locked Loop (PLL)

The clock for the sensors is provided externally. This ensures synchronous operation in case of multiple system participants.

The sensor has its own PLL to generate the necessary clock frequency for the chip operation.

2.5.6 Safety Features

The TLE5011 has a multiplicity on safety features to support Safety Integrity Level (SIL). Sensors meeting this performance standard are identified by Infineon with the following logo:

Figure 5 PRO SIL Logo

Safety features are:

- Angle test (generated via test voltages feeding the ADC).
- Crossed signal paths (switchable for comparison)
- Invertable ADC bitstreams
- Overvoltage and undervoltage detection of internal and external voltages
- V_{DD}-off and GND-off to detect supply malfunctions
- Frame counter and synchronisation counter
- Separate bandgap-reference voltages for regulators and comparators
- CRC-protected SSC protocol
- Locked configuration registers

Disclaimer

PRO-SIL™ is a Registered Trademark of Infineon Technologies AG
The PRO-SIL™ Trademark designates Infineon products which contain SIL Supporting Features.
SIL Supporting Features are intended to support the overall System Design to reach the desired SIL (according to IEC61508) or A-SIL (according to ISO26262) level for the Safety System with high efficiency.
SIL respectively A-SIL certification for such a System has to be reached on system level by the System Responsible at an accredited Certification Authority.
SIL stands for Safety Integrity Level (according to IEC 61508)
A-SIL stands for Automotive-Safety Integrity Level (according to ISO 26262)

3 Specification

3.1 Application Circuit

The application circuit shows the microcontroller version with open-drain capabilities.

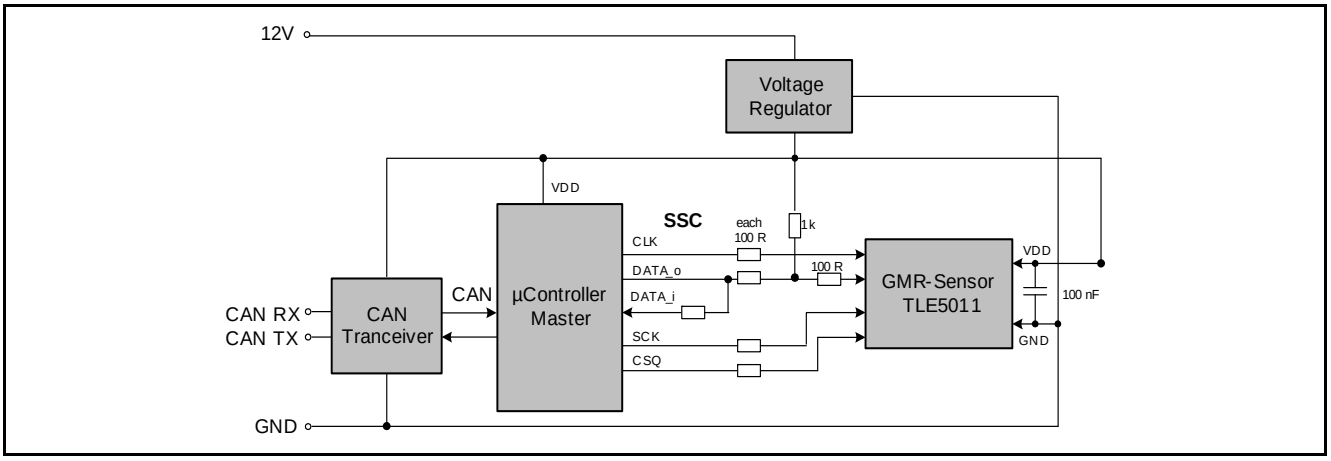


Figure 6 Application Circuit

A complete system may consist of one TLE5011 and a microcontroller. The second TLE5011 may be used for redundancy to increase system reliability. The microcontroller should contain a CORDIC coprocessor for fast angle calculations, and flash memory for the calibration data storage.

3.2 Absolute Maximum Ratings

Table 2 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Voltage on V_{DD} pin with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	max 40 h / lifetime
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	6.5	V	V_{DD} + 0.5 V may not be exceeded
Junction temperature	T_J	-40	150	℃	
			150	℃	for 1000 h not additive
Magnetic field induction	B	-	|125|	mT	max 5 min. @ T_A = 25℃
		-	|100|		max 5 h @ T_A = 25℃
		-	|70|		max 1000 h @ T_A = 85℃ not additive
		-	|60|		max 1000 h @ T_A = 100℃ not additive
Storage temperature	T_{ST}	-40	150	℃	without magnetic field

Note: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.3 Operating Range

To ensure correct operation of the TLE5011, the operating conditions identified in **Table 3** must not be exceeded. All parameters specified in the following sections refer to these operating conditions, unless otherwise indicated. **Table 3** is valid for -40℃ < T_J < 150℃

Table 3 Operating Range

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply Voltage	V_{DD}	3.0	-	5.5	V	For 3.3 & 5.0V systems[1)]
Output Current	I_Q	-	-5	-10	mA	2) 3)
Input Voltage	V_{IN}	-0.3	-	5.5	V	V_{DD} + 0.35 V may not be exceeded
Magnetic Induction at T_A= 25℃ 4) 5)	B_{XY}	30	-	50	mT	-40℃ < T_J<150℃
	B_{XY}	30	-	60	mT	-40℃ < T_J<100℃
	B_{XY}	30	-	70	mT	-40℃ < T_J<85℃
Expanded Magnetic Induction at T_A = 25℃ 4) 5)	B_{XY}	25	-	30	mT	Additional angle error of 0.1° 6)
Angle Range	*Ang*	0	-	360	°	Sine / cosine

1) Directly blocked with 100-nF ceramic capacitor
2) Maximum current to GND over Open Drain Output
3) The corresponding voltage levels are listed in **Table 5** and **Table 6**
4) Values refer to an homogenous magnetic field (B_{XY}) without vertical magnetic induction (B_Z = 0mT)
5) See **Figure 7**
6) 0h

The field strength of a magnet can be selected within the colored area in **Figure 7**. By limitation of the junction temperature, a higher magnetic field can be applied. In case of a maximum temperature T_J = 100℃ a magnet with up to 60mT at T_A = 25℃ is allowed.

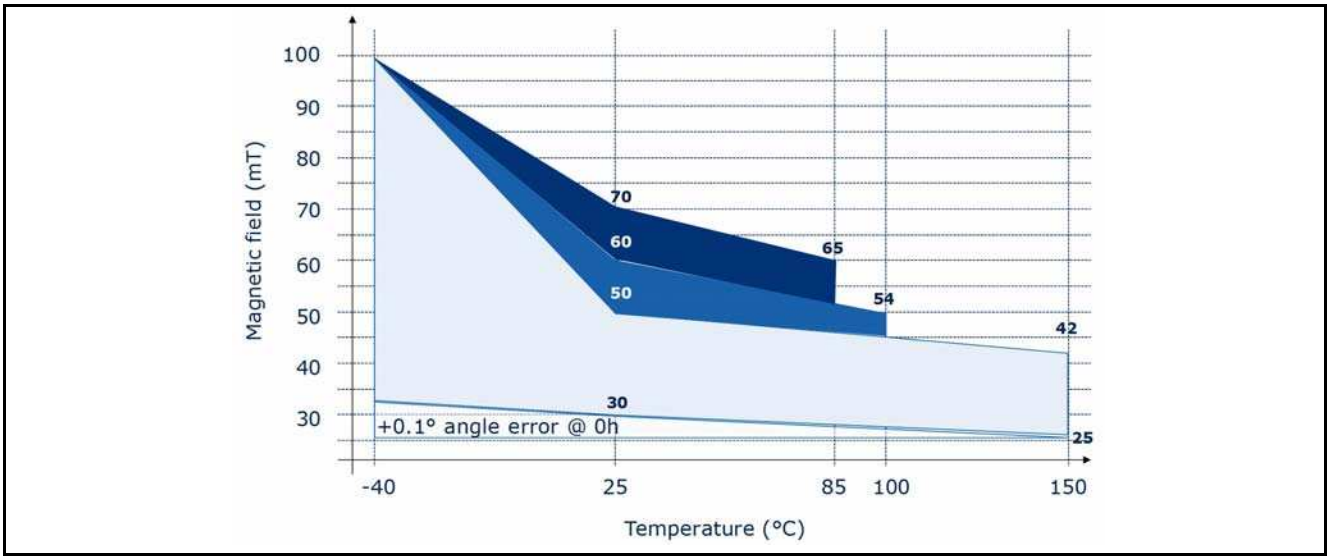


Figure 7 Magnet performance (ambient temperature)

Note: The thermal resistances listed in ***Table 21 "Package Parameters" on Page 42*** *must be used to calculate the corresponding ambient temperature.*

Calculation of the Junction Temperature

The total power dissipation P_{TOT} of the chip increases its temperature above the ambient temperature.

The power multiplied by the total thermal resistance R_{thJA} (Junction to Ambient) leads to the final junction temperature. R_{thJA} is the sum of the addition of the values of the two components *Junction to Case* and *Case to Ambient*.

$R_{thJA} = R_{thJC} + R_{thCA}$

$T_J = T_A + \Delta T$

$\Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + V_{OUT} \times I_{OUT})$ I_{DD} , $I_{OUT} > 0$, *if direction is into IC*

Example (assuming no load on Vout):

– V_{DD} = 5 V
– I_{DD} = 15 mA
– $\Delta T = 150$ [K/W] x (5 [V] x 0.015 [A] + 0 [VA]) =11.25 K

For moulded sensors, the calculation with R_{thJC} is more adequate.

3.4 Characteristics

3.4.1 Electrical Parameters

The indicated electrical parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage V_{DD} = 5.0 V and 25℃, unless individually specified. All other values correspond to - 40℃ < T_J < 150℃.

Table 4 Electrical Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply Current [1]	I_{DD}	-	15	20	mA	V_{DD} = 3.0 to 5.5V
		-	-	21		V_{DD} = 6.5 V
POR Level	V_{POR}	2.0	2.3	2.9	V	Power-On Reset
POR Hysteresis	V_{PORhy}	-	30	-	mV	
Power-On Time	t_{Pon}	50	100	200	µs	$V_{DD} > V_{DDmin}$ & after first edge on f_{CLK}
PLL Jitter	t_{PLLjit_S}	-	1.3	2.0 [2]	ns	short term [3]
	t_{PLLjit_L}		3.0	3.9		long term [4]
ADC Noise [5]	N_{ADC}	-	1	2.2	digits	1 σ @ FIR_BYP = 0
		-	2	4.4[2]		1 σ @ FIR_BYP = 1

Table 4 Electrical Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Signal Low Level	V_L	-0.35	-	0.3 V_{DD}	V	Tested only at DATA pin as structures of all pins are identical
Input Signal High Level	V_H	0.7 V_{DD}	-	V_{DD} +0.35	V	
Capacitance of SSC Data Pin	C_{LDATA}	-	4	6 [2]	pF	Internal

1) Without external pull-up resistor for SSC interface
2) Not subject to production test - verified by design/characterization
3) From pulse to pulse
4) Accumulated over 1 ms
5) ADC noise with respect to the peak ADC value specified in **"Signal Processing" on Page 21**.
Noise tested using 1 σ of 100 sample values from Angle Test "000"

Table 5 Electrical Parameters for 3.0V < V_{DD} < 3.6V

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Hysteresis	V_{HY3}	0.02 V_{DD}	-	-	V	
Pull-Up Current	I_{PU3}	-5	-	-50	µA	$\overline{CS}$, DATA
Pull-Down Current	I_{PD3}	10	-	150	µA	SCK, CLK
		8	-	100		TST1
		5	-	50		TST2
Output Signal Low Level	V_{OL3}	- - -	- - -	1.3 0.9 0.4	V	I_Q = - 10 mA I_Q = - 7 mA[1] I_Q = - 2.5 mA [1]

1) Not subject to production test - verified by design/characterization

Table 6 Electrical Parameters for 4.5V < V_{DD} < 5.5V

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Hysteresis	V_{HY5}	0.07 V_{DD}	-	-	V	
Pull-Up Current	I_{PU5}	-10	-	-150	µA	$\overline{CS}$, DATA
Pull-Down Current	I_{PD5}	15	-	225	µA	SCK, CLK
		15	-	225		TST1
		10	-	150		TST2
Output Signal Low Level	V_{OL5}	- -	- -	0.7 0.4	V	I_Q = - 10 mA I_Q = - 5 mA [1]

1) Not subject to production test - verified by design/characterization

3.4.2 ESD Protection

Table 7 ESD Protection

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
ESD Voltage	V_{HBM}	-	± 4	kV	HBM [1]
	V_{SDM}	-	± 500	V	SDM [2]

1) Human Body Model (HBM) according to: AEC-Q100-002

2) Socketed Device Model (SDM) according to: ESDA/ANSI/ESD SP5.3.2-2008

3.4.3 GMR Parameters

All parameters apply over the full operating range, unless otherwise specified.

Table 8 Basic GMR Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
X, Y Output range	RG_{ADC}	-	-	±23230	digits	
X, Y Amplitude [1]	A_X, A_Y	6000	9500	15781	digits	at calibration conditions
		3922	-	20620		Operating Range
X, Y Synchronism [2]	k	80	100	120	%	at calibration conditions
X, Y Offset [3]	O_X, O_Y	-3000	0	3000	digits	at calibration conditions
X, Y Orthogonality Error	φ	-10.0	0	10.0	°	at calibration conditions
X, Y without field	X_0, Y_0	-5000	-	5000	digits	without magnet[4]

1) See **Figure 2**

2) k = 100 x (A_X / A_Y).

3) O_{SIN} = (Y_{MAX} + Y_{MIN}) / 2 ; O_{COS} = (X_{MAX} + X_{MIN}) / 2

4) Not subject to production test - verified by design/characterization

Offset and Amplitude

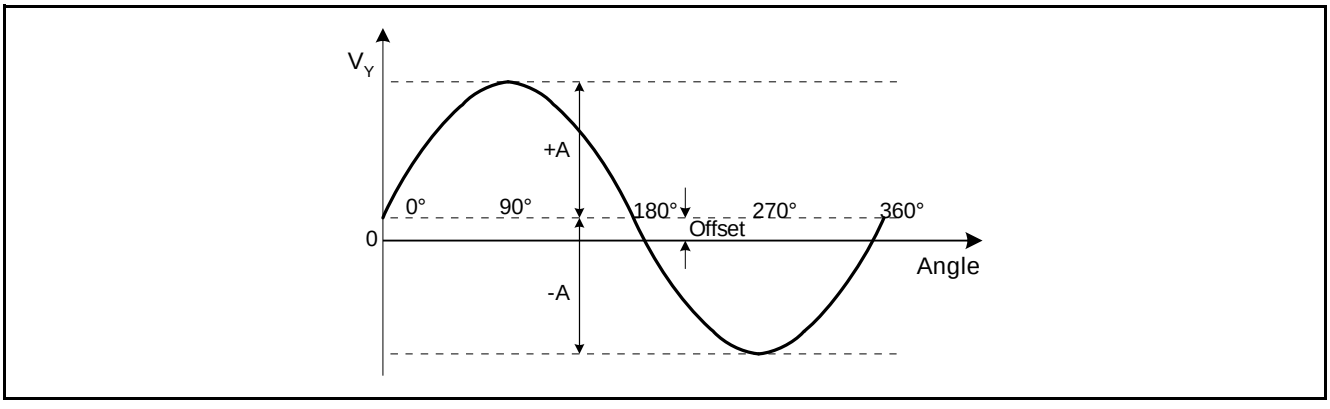


Figure 8 Offset and Amplitude Definition

Offset Definition

The offset of the X and Y signals is defined as the mean value between the signed maximum and minimum values of the idealized sine or cosine wave.

$$O_X = \frac{X_{MAX} + X_{MIN}}{2}$$

$$O_Y = \frac{Y_{MAX} + Y_{MIN}}{2}$$

Amplitude Definition

The amplitude is defined as half the difference between the signed maximum and minimum values of the idealized sine or cosine wave.

$$A_X = \frac{X_{MAX} - X_{MIN}}{2}$$

$$A_Y = \frac{Y_{MAX} - Y_{MIN}}{2}$$

Temperature-dependent behavior

The temperature offset gradients for both channels depend on the value at 25°C. The gradients can be calculated using the following linear equations:

$$KT_{OX} = tco\_d\_x + (tco\_k\_x \times O_{X25})$$
$$KT_{OY} = tco\_d\_y + (tco\_k\_y \times O_{Y25})$$

O_{X25}, O_{Y25}: Offset values at 25°C in digits.

The application note “TLE5011 Calibration” describes in chapter 2.3, how to determine the coefficients (KT_{OX}, KT_{OY}).

Orthogonality Definition

The corresponding maximum and zero-crossing points of the SIN and COS signals do not occur at the precise distance of 90°. The difference between X and Y phase is called the **orthogonality error**.

$$\varphi = \varphi_X - \varphi_Y$$

φ_{ideal} = 0°

φ_X: Phase error of X (= cos) signal

φ_Y: Phase error of Y (= sin) signal

3.5 Calibration

GMR Values

The end-of-line calibration can be accomplished using following sequence:

1. Turn magnetic field 360° **left** and measure X and Y values
2. Calculate amplitude, offset, phase correction values of left turn
3. Turn further 90° left and 90° back right without measurement
4. Turn magnetic field 360° **right** and measure X and Y values
5. Calculate amplitude, offset, phase correction values of right turn
6. Calculate **mean** values of amplitude, offset, phase correction values

The conditions are specified in **Table 9**.

The values obtained from this sequence must be stored in a non-volatile memory. They are used for the correction of the read-out X and Y values before the angular calculation.

The resulting angular deviation is calculated using the parameters determined above.

Temperature Measurement

The signal amplitude T_{25} of the temperature measurement path at the calibration conditions must be measured and stored.

Calibration Conditions

All errors are related to calibration performed by Infineon under the following conditions:

Table 9 GMR test calibration conditions at IFX

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Flux density	B_{CAL}	-	30	-	mT	B_Z = 0 mT
Temperature	T_{CAL}	-	25	-	°C	

3.6 Angle Calculation

3.6.1 Components of the Output Signals

The X and Y signals at the output can be described by the following equations:

$$X = A_X \times \cos(\alpha + \varphi_X) + O_X$$

$$Y = A_Y \times \sin(\alpha + \varphi_Y) + O_Y$$

A_X : Amplitude of X (= cos) signal — A_Y : Amplitude of Y (= sin) signal

O_X : Offset of X (= cos) signal — O_Y : Offset of Y (= sin) signal

φ_X : Phase error of X (= cos) signal — φ_Y : Phase error of Y (= sin) signal

3.6.2 GMR Error Compensation

Temperature-dependent Offset Value

To increase the accuracy, the temperature-dependent offset drift can be compensated. The temperature of the chip must be read out. The offset values O_X and O_Y can be described by the following equations.

$$O_X = O_{X25} + \frac{KT_{OX}}{S_T} \times (T - T_{25})$$

$$O_Y = O_{Y25} + \frac{KT_{OY}}{S_T} \times (T - T_{25})$$

O_{X25} , O_{Y25} : Offset value at 25℃ in digits

T_{25} : Temperature value at 25℃ in digits

T : Temperature value in digits

S_T : Sensitivity of the temperature measurement path, (see **“Temperature Measurement” on Page 38**).

Offset Correction

After the X and Y values are read out, the temperature-corrected offset value must be subtracted.

$$X_1 = X - O_X$$

$$Y_1 = Y - O_Y$$

Amplitude Normalization

Next, the X and Y values are normalized using the peak values determined in the calibration.

$$X_2 = \frac{X_1}{A_X}$$

$$Y_2 = \frac{Y_1}{A_Y}$$

Non-Orthogonality Correction

The influence of the non-orthogonality can be compensated using thefollowing equation, in which only the Y channel must be corrected.

$$Y_3 = \frac{Y_2 - X_2 \times \sin(-\varphi)}{\cos(-\varphi)}$$

Resulting Angle

After correction of all errors, the resulting angle can be calculated using the arctan function[1)].

$$\alpha = \arctan\left(\frac{Y_3}{X_2}\right) - \varphi_X$$

1) Microcontroller function “arctan2(Y_3,X_2)” to resolve 360°

3.6.3 GMR Parameters after Calibration

After calibration under the conditions specified in **Table 9 “GMR test calibration conditions at IFX” on Page 19**, the sensor has a remaining error as shown in **Table 10**.

The error value refers to B_Z = 0 mT and operating conditions given in **Table 3 “Operating Range” on Page 14**.

Table 10 GMR Parameter with Temperature-Dependent Offset Compensation

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.[1]	max.		
Overall Angle Error	α_{err}	-	0.7	1.6	°	Including temperature drift [2] [3]
		-	-	2.2	°	Including lifetime and temperature drift [2] [4]

1) At 25℃, B=30mT
2) Including hysteresis error
3) At 0h
4) Not subject to production test - verified by design/characterization

3.7 Signal Processing

Table 11 Signal Processing

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.[1]	max.		
Internal Cutoff Frequency (-3dB) of sin or cos Value	$f_{Cut\text{-}Off}$	-	4.9	-	kHz	FIR_BYP=0
			19.6			FIR_BYP=1
Update Time of sin or cos Value[2]	t_{upd}	-	81.9	-	µs	FIR_BYP=0
		-	20.5	-		FIR_BYP=1
Settle Time [3]	t_{settle}	-	163.8	-		FIR_BYP=0
		-	41.0	-		FIR_BYP=1
Peak ADC Output value	ADC_{Pk}	-	-	23230	digits	Signed 16-bit integer (2s complement) [4] [5] [6]

1) For 4-MhHz input frequency
2) t_{upd} = 8192 / (25 x f_{CLK}) for FIR_BYP = 0
   t_{upd} = 8192 / (100 x f_{CLK}) for FIR_BYP = 1
3) t_{settle} = 2 x t_{upd} , after change of ADC input source
4) Output values are valid up to this limit. Above it, corrupted results may occur due to non-linearity of the ADC.
5) One digit typically represents 5.166 µV
6) Corresponds to max. GMR output value

3.8 Clock Supply (CLK Timing Definition)

The clock signal input “CLK” must fulfill certain requirements described in this section:

- The high or low pulse width must not exceed the specified values, because the PLL needs a minimum pulse width and must be spike filtered.
- The duty-cycle factor should be 0.5 but can deviate from the values limited by $t_{CLKh(f\_min)}$ and $t_{CLKl(f\_min)}$.
- The PLL is triggered at the positive edge of the clock. If more than 2 edges are missing, a chip reset is generated automatically.

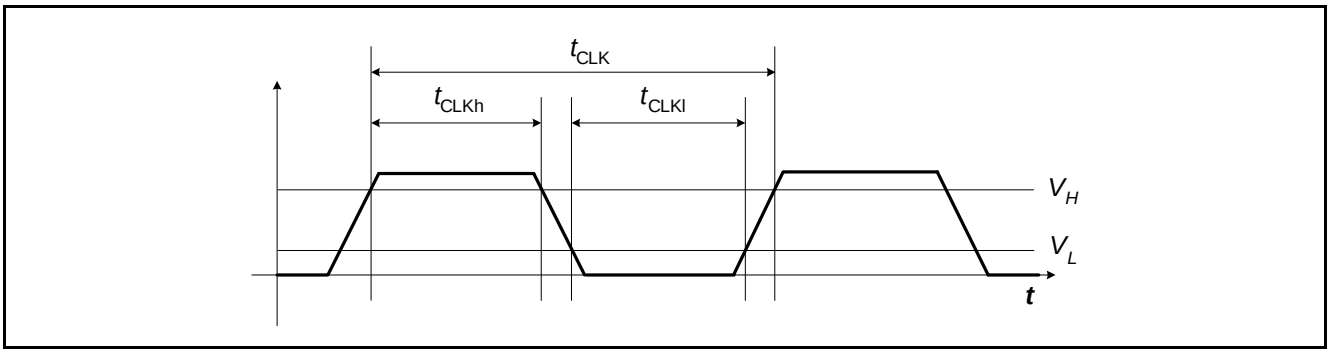


Figure 9 CLK Timing Definition

Table 12 CLK Timing Specification

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Frequency	f_{CLK}	3.8	4.00	4.2	MHz	
CLK Duty Cycle [1)]	CLK_{DUTY}	30	50	70	%	
CLK rise time	t_{CLKr}	-	-	20	ns	from V_L to V_H
CLK fall time	t_{CLKf}	-	-	20	ns	from V_H to V_L
PLL Frequency	f_{PLL}	-	100	-	MHz	f_{CLK} * 25
Digital Clock	f_{DIG}	-	25	-	MHz	(25 / 4) * f_{CLK}
Digital Clock Periode	t_{DIG}	-	40	-	ns	4 / (25 * f_{CLK})

1) Minimum duty-cycle factor: $t_{CLKh(f\_min)}$ / $t_{CLK(f\_min)}$ with $t_{CLK(f\_min)}$ = 1 / $f_{CLK(f\_min)}$
Maximum duty-cycle factor: $t_{CLKh(f\_max)}$ / $t_{CLK(f\_min)}$ with $t_{CLKh(f\_max)}$ = $t_{CLK(f\_min)}$ - $t_{CLKl(min)}$

3.9 Synchronous Serial Communication Interface (SSC)

The 3-pin SSC interface has a bidirectional data line (open drain), a serial clock signal, and Chip Select.

The SSC interface is designed to communicate with a microcontroller with bi-directional SSC interface supporting open drain. Other microcontrollers may require an external NPN transistor.

This allows communication with SPI-compatible devices.

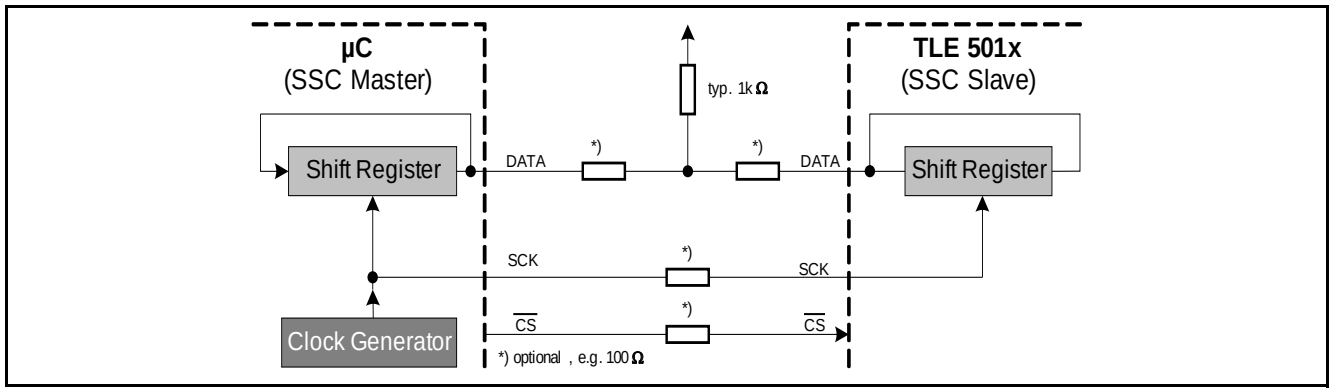


Figure 10 SSC Half-Duplex Configuration - Microcontroller with Open Drain

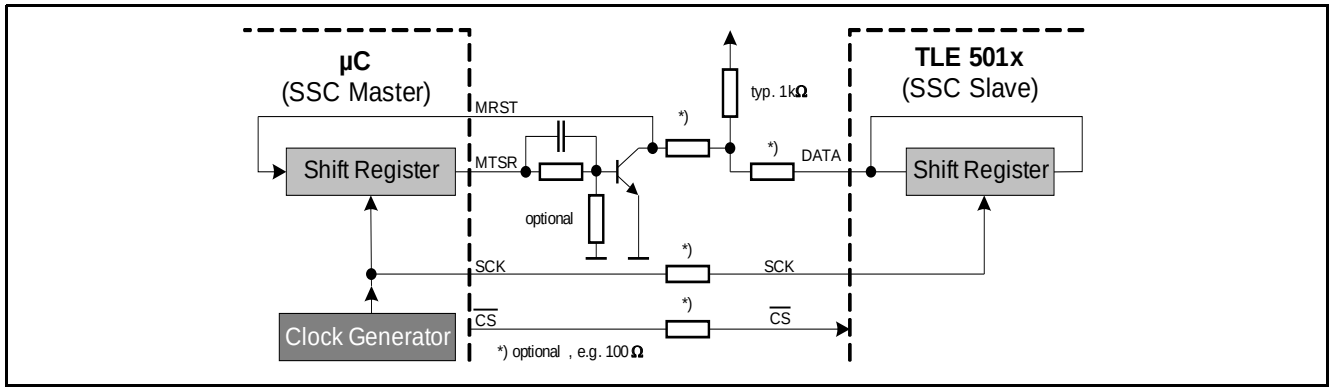


Figure 11 SSC Half-Duplex Configuration - Microcontroller without Open Drain

3.9.1 SSC Timing Definition

SSC Timing Diagram

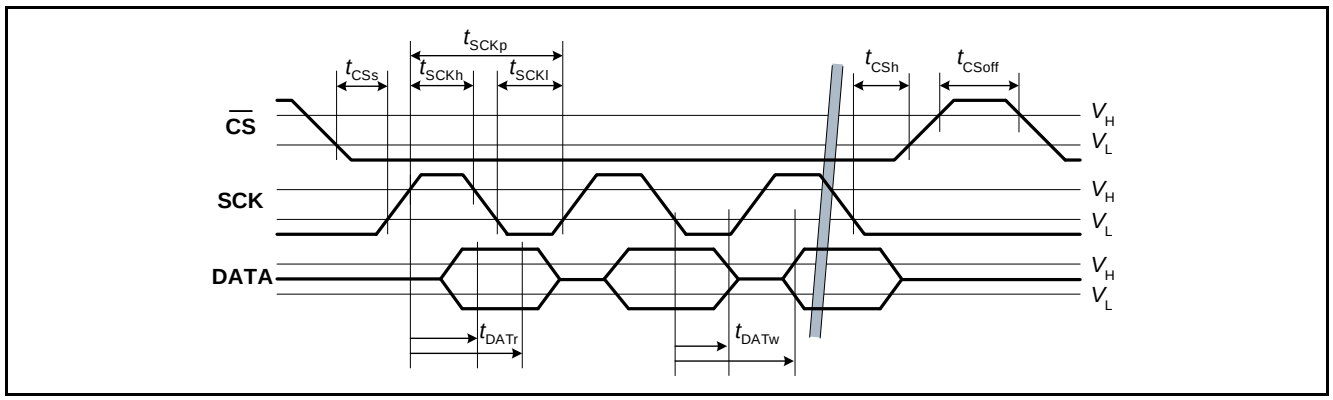


Figure 12 SSC Timing Definition

SSC Inactive Time ($\overline{CS}_{off}$)

The SSC Inactive Time defines the delay before the TLE5011 can be selected again after a transfer. The TLE5011 reacts only to one command after an SSC Inactive Time. Then the SSC interface of the TLE5011 is disabled until the next SSC Inactive Time occurs.

DATA Write Time (t_{DATW})

During this time, the TLE5011 changes the data line, so the data are invalid. The DATA Write Time values are defined without a pull-up resistor.

Pull-up Time Value (t_{PU})

The value in **Table 13 "SSC Timing Specification" on Page 24** is estimated at 60 ns.

Table 13 SSC Timing Specification

Note: Timing must be calculated according to ***Table 12 "CLK Timing Specification" on Page 22***

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
SSC Baud Rate	f_{SSC}	-	2.0	2.1 [1]	Mbit / s	
$\overline{CS}$ Setup Time	t_{CSs}	$3*t_{DIG}+10$	-	-	ns	
$\overline{CS}$ Hold Time	t_{CSh}	$5*t_{DIG}+10$	-	-	ns	
$\overline{CS}_{off}$	t_{CSoff}	$10*t_{DIG}$	-	-	ns	SSC inactive time
SCK High	t_{SCKh}	$5*t_{DIG}$	-	-	ns	
SCK Low	t_{SCKl}	$5*t_{DIG}$	-	-	ns	
DATA Read Time (Data Valid Time)	t_{DATr}	$6*t_{DIG}-10$	-	$7*t_{DIG}+10$	ns	SSC_FILT = 0
		$5*t_{DIG}-10$	-	$7*t_{DIG}+10$		SSC_FILT = 1
DATA Write Time (Data Valid Time) [2]	t_{DATw}	$6*t_{DIG}+25$	-	$7*t_{DIG}+50 + t_{PU}$	ns	
DATA slope	t_{DATs}	-	20	30 [3]	ns	Falling edge [4]

1) $f_{CLK}/2$, synchronized to f_{CLK} if fCLK = f_{CLK}(max)
2) t_{PU} is the time generated by the pull-up resistor
3) Not subject to production test - verified by design/characterization
4) Internal slope control of falling edge for data bit transition from V_H to V_L.

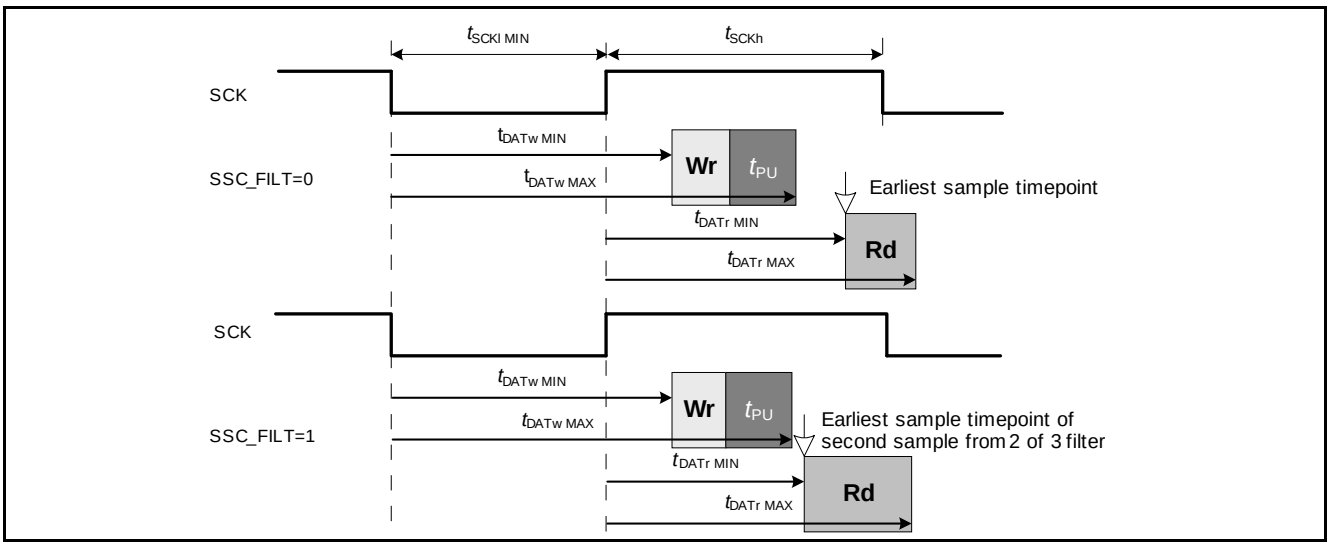


Figure 13 SSC Interface Timing Details - Worst-Case Specified Timing

Note: The read window includes the sampling of the data bit. For SSC_FILT = 1, the 2-of-3 selection is already considered. Only the two last data values need to be equal. For SSC_FILT = 0, only one sample point is selected.

The margin time shown in **Table 14** is the time between write access to the SSC data line and the earliest possible sample read of the TLE5011 itself for read-back.

It is useful to have a maximum distance between the WRITE and subsequent READ. This ensures a reliable read-back of the written data for the Slave-Active Byte generation.

Table 14 Maximum Pull-up Time Margin with Worst-Case Specified Timing

SSC_FILT	SSC_TIMING	Min. t_{PU} Margin [1)]	Unit	Comment
0	don't care	90	ns	
1		50		

1) Calculation: Margin=$t_{SCKl(min)}$+$t_{DATwMAX}$-(t_{PU})-$t_{DATrMIN}$.For Margin<50 ns no problems can occur.

3.9.2 SSC Baud rate

The SSC baud rate depends on the internal clock frequency.

Twelve internal digital clock cycles are necessary to ensure reliable operation. Therefore, the maximum SSC baud rate depends on the external CLK.

$$f_{SSC} = \frac{f_{CLK}}{2}$$

3.9.3 SSC Spike Filter

A spike filter for all SSC lines can be selected via the **SSC_FILT** bit.

SSC Spike Filter Off

When the spike filter is disabled, each slope with rising voltage is used to define a bit. This is independent of the length of the sampled pulse. For example, a positive spike generates a rising and a falling edge.

SSC Spike Filter On

A sliding window with four consecutive sample bits is analyzed.

The sample frequency is:

$$f_S = \frac{1}{f_{DIGIT}}$$

Rising Edge Detect for SCK

- After a rising edge (LH combination), at least one of the two following samples must be high.*Valid bit combinations: 01**11** , 01**10** , 01**01**.*
- A falling condition must be detected previously.

Falling Edge Detect for SCK

- After a falling edge (HL combination), at least one of the two following samples must be low. *Valid bit combinations: 10**00** , 10**01** , 10**10**.*
- A rising condition must be detected previously.

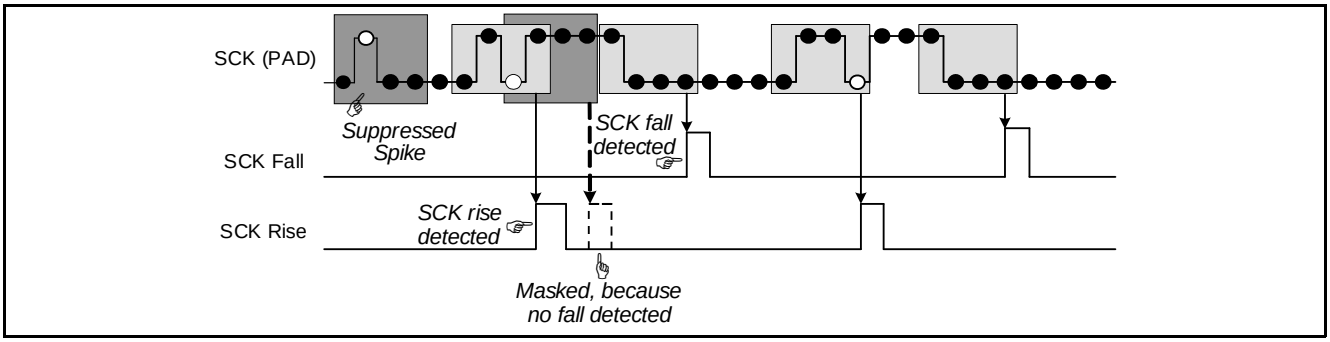


Figure 14 SSC Spike Filter

Filter for DATA and $\overline{CS}$

The following conditions apply:

- The DATA pin has a '2-of-3' filter
- The $\overline{CS}$ input has a '2-of-3' filter that suppresses only positive spikes

3.9.4 SSC Data Transfer

The following transfer Byte are possible:

- Command Byte (to access and change operating modes of the TLE5011)
- Data Bytes (any data transferred in any direction)
- CRC Byte (cyclic redundancy check)
- Slave-active Byte (response of all selected slaves)

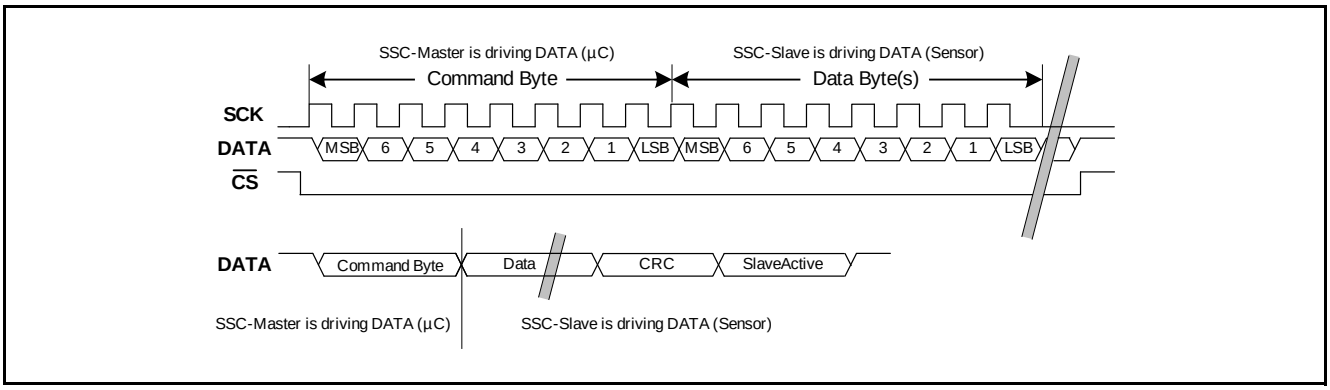


Figure 15 SSC Data Transfer (Data Read Example)

3.9.5 SSC Command Byte

The TLE5011 is controlled by a command Byte. It is sent first at every data transmission.

Table 15 Structure of the Command Byte

Name	Bits	Description
RW	[7]	Read - Write 0 = write, 1 = read
ADDR	[6..3]	Address to be read / written 0..15 - register start address (address auto increment)
ND	[2..0]	Number of data Bytes 0..7 - number of data Bytes to be transferred

Register Table

This section describes the complete address range as well as all registers of the TLE5011. It also defines the read/write access rights of the specific registers. **Table 16** identifies the values with symbols. Access to the registers is accomplished via the SSC interface.

Table 16 Address Map

Addr.	Name	Bits							
		7	6	5	4	3	2	1	0
00_H	CTRL1	-	-	-	-	SSC_ FILT	-	AUTO	UR
01_H	XL	X_{Low}							
02_H	XH	X_{High}							
03_H	YL	Y_{Low}							
04_H	YH	Y_{High}							
05_H	FCNT_ STAT	-	STAT_ VR	GMR_ OFF	UPDATE	FCNT			
06_H	FSYNC_IN V	FILT_ INV	FSYNC						
07_H	ANGT	-	ANGT_E N	ANGT_Y		ANGT_X			
08_H	-	reserved							
09_H	-	reserved							
$0A_H$	-	reserved							
$0B_H$	-	reserved							
$0C_H$	TST	TEMP_E N	ADCPY	FILT_ PAR	FILT_ CRS	FILT_ BYP	TST_ ADC	TST_ GMR	TST_ CHAN
$0D_H$	ID	DEV_ID				reserved			
$0E_H$	LOCK	LOCK							
$0F_H$	CRTL2	VDD_OV	VDD_ OFF	GND_OF F	VRG_ OV	VRA_ OV	VRD_ OV	S_NO	

Bit Types

The types of bits used in the registers are listed here:

Abbreviation	Function	Description
L	Locked	Locked register. Locked registers can be written only when the unlock-value is written in the lock register (**$0E_H$**). This ensures that these bits cannot be modified unintentionally during normal operation.
U	Update	Update buffer for this bit is present. If an Update Command is issued and the Update-Mode bit (UR in CTRL1) is set, the immediate values are stored in this Update Buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time.

Abbreviation	Function	Description
S	Status	Reset only after readout
R	Read	Read-only registers
W	Write	Read and write registers

CTRL1

Addr: 00_H **Reset Value: 01_H**

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**reserved**	**SSC_FILT**	**reserved**	**AUTO**	**UR**
-	-	-	W L	W L	-	W L	W L

Field	Bits	Type	Description
reserved	7	-	Reserved, must be set to 0
reserved	6	-	Reserved, must be set to 0
reserved	5	-	Reserved, must be set to 0
reserved	4	-	Reserved, must be set to 0
SSC_FILT	3	W L	SSC Digital Spike Filter enable for all SSC lines ($\overline{CS}$, CLK and DATA) 0: Digital SSC Spike filters off 1: Digital SSC Spike filters on (modified timing)
reserved	2	-	Reserved, must be set to 0
AUTO	1	W L	Automatic update at angle tests 0: no automatic update in Angle Test Mode 1: automatic update-command after t_{settle}, counters FSYNC and FCNT are reset to 0. Then the Angle-Test (ANGT_EN) is automatically disabled and switches back to normal operation. Also, the UPDATE bit is toggled
UR	0	W L	Update / Run Mode 0: Run Mode (Buffer1 values are immediate values) 1: Update Mode (Buffer2 values are stored values)

The values in Register 01H to 04H represent one Byte of two's complement signed 16 bit integer values.

X_L

Addr: 01_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
X Low Byte							
R U							

X_H

Addr: 02_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
X High Byte							
R U							

Y_L

Addr: 03_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
Y Low Byte							
R U							

Y_H

Addr: 04_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
Y High Byte							
R U							

FCNT_STAT

Addr: 05_H **Reset Value: 80_H**

7	6	5	4	3	2	1	0
reserved	STAT_VR	GMR_OFF	UPDATE	FCNT			
-	R S	R U	R S	R U			

Field	Bits	Type	Description
reserved	7	-	
STAT_VR	6	RS	Voltage Regulator Status This bit is a logical OR combination of Digital, Analog, GMR and VDD_OV Comparator and GND_OFF, and VDD_OFF Comparator outputs. 0: Voltage Supply OK 1: Voltage Supply is not OK
GMR_OFF	5	RU	ADC Values are no GMR values (e.g.: Temperature measurement is active) This bit indicates whether or not GMR values or any other values are connected to the ADCs. This value is read back from the multiplexer control signals. 0: X,Y Values are GMR values 1: X,Y Values normally represent temperature measurement or angle test values. In the case of non-functional MUX, this bit is set to 1
UPDATE	4	RU	Update Toggle bit. This bit toggles after every update (update command or automatic update at angle test) The bit is independent of UR bit in CTRL1
FCNT	3-0	RU	Frame Counter (4-bit unsigned integer value) This counter counts every new X,Y value pair coming out of the data path. (approx. 80µs) This counter is reset to 0_H after any write to FSYNC and after every change of the ANGT_EN bit. As t_{settle} time has to elapse for valid X,Y data, this counter must be $\geq 2_H$ to indicate valid X,Y values. If it overflows, it resets to 3_H to show that values are still valid. *Note: If FIR_BYP is activated, this counter counts four times faster!*

FSYNC_INV

Addr: 06_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
FILT_INV	**FSYNC**						
WU	WU						

Field	Bits	Type	Description
FILT_INV	7	WU	Filter Input Inversion (to check the digital data path during operation) 0: Filter Inputs are not inverted 1: Filter Inputs are inverted
FSYNC	6-0	WU	Frame Synchronization (7-bit unsigned integer value) The Filter Update time of approx. 80 µs results from the filter decimation. The phase of this decimation can be set and checked by this counter. If FIR_BYP is activated, this counter overflows at the value 31_D.

ANGT

Addr: 07_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
reserved	**ANGT_EN**	**ANGT_Y**			**ANGT_X**		
-	W	W			W		

Field	Bits	Type	Description
reserved	7	-	Reserved, must be set to 0
ANGT_EN	6	W	Angle Test Enable 0: Angle Test disable command 1: Angle Test enable command in this case X and Y values represent resistive test values that can be used to simulate angle values
ANGT_Y	5-3	W	Angle Test X and Y value See : **Table 18 “Functional Angle Test” on Page 37**
ANGT_X	2-0	W	

Reserved Registers (08_H to $0B_H$)

The values in these registers are 8-bit unsigned integer values.

The values in addr.8 and addr.9 have to be in reset status.

Reserved

Addr: 08_H **Reset Value: FF_H**

7	6	5	4	3	2	1	0
Reserved							

Reserved

Addr: 09_H - $0B_H$ **Reset Value: 00_H**

7	6	5	4	3	2	1	0
Reserved							

TST

Addr: $0C_H$ **Reset Value: 00_H**

7	6	5	4	3	2	1	0
TEMP_EN	**ADCPY**	**FILT_PAR**	**FILT_CRS**	**FIR_BYP**	**TST_ADC**	**TST_GMR**	**TST_ CHAN**
W L	W L	W L	W L	W L	W L	W L	W L

Field	Bits	Type	Description
TEMP_EN	7	W L	Temperature Device Enable 0: Temperature Measurement disabled 1: Temperature Measurement enabled The X value represents the temperature. Automatic update mode enabled, if AUTO=1
ADCPY	6	W L	Y Polarity 0: No inversion of Y bitstream 1: Inversion of Y bitstream (rotating direct. changed)
FILT_PAR	5	W L	Filter switched parallel 0: Filters in normal mode 1: Filters parallel, input selected by TST_CHAN
FILT_CRS	4	W L	Filter switched across 0: Filters in normal mode 1: Filters crossed, X and Y outputs are exchanged
FIR_BYP	3	W L	FIR Filter Bypass 0: No FIR Bypass 1: FIR Bypass
TST_ADC [1)]	2	W L	ADC input switch to TST1and TST2 0: No ADC input switch, normal operation 1: ADC input switched to TST1,2, ADC selected by TST_CHAN [2)]
TST_GMR [1)]	1	W L	GMR switch to TST1and TST2 0: No GMR switch, normal operation 1: GMR switched to TST1,2 selected by TST_CHAN [2)]
TST_CHAN	0	W L	Test Channel select 0: X channel linked to TST1and TST2 1: Y channel linked to TST1and TST2

1) Only for test purposes

2) if TST_ADC and TST_GMR are set to 1 at the same time, TST_GMR is forced to 0. TST_ADC has the higher priority.

ID

Addr: $0D_H$ **Reset Value: 12_H**

7	6	5	4	3	2	1	0
DEV_ID				Reserved			
R				R			

Field	Bits	Type	Description
DEV_ID	7-4	R	Device Identifier 001_H: TLE5011 production chip
reserved	3-0	-	

LOCK

Addr: $0E_H$ **Reset Value: 00_H**

7	6	5	4	3	2	1	0
LOCK							
W							

Field	Bits	Type	Description
LOCK	7-0	W	Lock Byte $\neq 5A_H$: Lock registers locked $= 5A_H$: Lock registers unlocked

CTRL2

Addr: $0F_H$ **Reset Value: 00_H**

7	6	5	4	3	2	1	0
VDD_OV	VDD_OFF	GND_OFF	VRG_OV	VRA_OV	VRD_OV	S_NO	
R S	R S	R S	R S	R S	R S	W L	

Field	Bits	Type	Description
VDD_OV	7	R S	V_{DD} Overvoltage Comparator 0: No V_{DD} Overvoltage occurred 1: V_{DD} Overvoltage occurred
VDD_OFF	6	R S	V_{DD} - off Comparator 0: No V_{DD} - off occurred 1: V_{DD} - off occurred
GND_OFF	5	R S	GND - off Comparator 0: No GND - off occurred 1: GND - off occurred
VRG_OV	4	R S	GMR Voltage Regulator Overvoltage Comparator 0: Voltage ok 1: VRG Overvoltage occurred

Field	Bits	Type	Description
VRA_OV	3	R S	Analog Voltage Regulator Overvoltage Comparator 0: Voltage ok 1: VRA Overvoltage occurred
VRD_OV	2	R S	Digital Voltage Regulator Overvoltage Comparator 0: Voltage ok 1: VRD Overvoltage occurred
S_NO	1-0	W L	Slave Number Used in the SSC protocol

3.9.6 Data Communication via SSC

Data communication via the SSC interface has the following characteristics:

- The data transmission order is "Most Significant Bit (MSB) first".
- Data is put on the data line with the rising edge on SCK and read with the falling edge on SCK.
- The SSC interface is Byte-aligned. All functions are activated after each transmitted Byte.
- A "high" condition on the negated Chip Select pin ($\overline{CS}$) of the selected TLE5011 interrupts the transfer immediately. The CRC calculator is automatically reset.
- Every access to the TLE5011 with the number of data (ND) ≥ 1 is performed with address auto-increment.
- After an auto-increment overflow, the addresses begin from 00_H.
- For every data transfer with ND ≥ 1, an 8-bit CRC Byte will be appended by the selected TLE5011. No CRC Byte is sent in a data transfer with ND = 0 (e.g. Update Command).
- After the CRC Byte is sent, the bit represented by S_NO is pulled low by the selected slave in the Slave-Active-Byte (bits [3..0], low nibble). In this way, broadcast messages also produce individual feedback of every selected slave. This is necessary to differentiate among the individual TLE5011 slave responses, because the CRC Byte is written by both TLE5011 units in parallel.
- If the CRC Byte on the bus is the same as the internally generated CRC of each TLE5011, each slave pulls the dedicated bit in the Slave-Active Byte (bits [7..4], high nibble) low. If not, the bit in the high nibble remains 1.
- A write command to address 00_H with ND = 0 will update all values inside the TLE5011, and only in this case can the transfer proceed. Furthermore, this command is added to the CRC calculation of the following SSC transfer.
- A command of 0000_0000 is called **Update Command**.
  This command transfers the present immediate values of each register to the update register. After an Update Command, the $\overline{CS}$ line does not need to be set and reset again.
- The transfer ends after the CRC and Slave-active Byte have been sent.
  The TLE5011 always sends logical 1 and all following sent bits from the SSC Master are ignored (TLE5011 is in Idle mode). To enable data transfers again, the Chip Select pin ($\overline{CS}$) of the TLE5011 must be deselected for $\overline{CS}_{off}$ (see **Table 13**) once.
- If the Update Mode is selected (CTRL register, UR = 1), all accesses are performed to update registers where update registers are present. Other registers are accessed directly.

3.9.7 CRC Generation

These are the requirements for CRC generation:

- This CRC is defined according to the *J1850* Bus-Specification of 15.Feb.1994 for Class B Data Communication.
- Every new transfer resets the CRC generation.
- Every Byte of a transfer will be taken into account to generate the CRC [also the sent command(s)].
- Generator Polynomial: X8+X4+X3+X2+1, the fast CRC generation circuit, is used for CRC generation. (See **Figure 16**)
- The remainder of the fast CRC circuit is initially set to 11111111_B.
- The remainder is bit-inverted before transmission.

Figure 16 shows the fast CRC Polynomial.

The zero extension for initial CRC calculation is included!

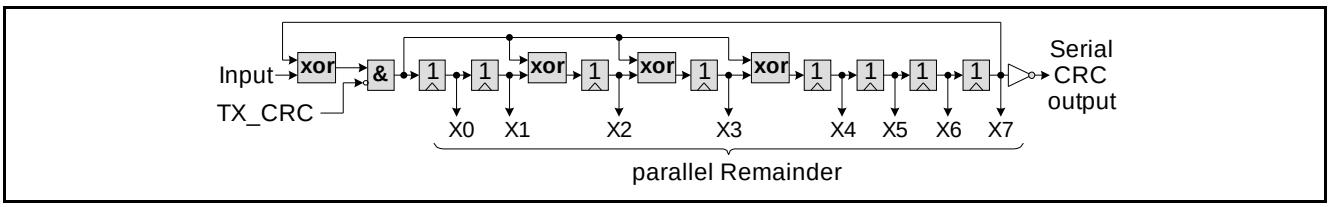


Figure 16 Fast CRC Polynomial Division Circuit

3.9.8 Slave-active Byte Generation

The position of the 0 in a nibble corresponds to the given slave number.

The slave-active Byte (cccc_nnnn) consists of:

- **low nibble** (nnnn). One 0 is generated always according to the slave number.
- **high nibble** (cccc). The 0 is only generated, if the readback CRC is correct.

Slave1: S_NO = 0 ⇨ bit 0 is pulled low Slave-active Byte: 1110_1110

Slave2: S_NO = 1 ⇨ bit 1 is pulled low Slave-active Byte: 1101_1101

Slave3: S_NO = 2 ⇨ bit 2 is pulled low Slave-active Byte: 1011_1011

Slace4: S_NO = 3 ⇨ bit 3 is pulled low Slave-active Byte: 0111_0111

Example of a communication disturbed by other bus participants:

Slave1: S_NO = 0 ⇨ bit 0 is pulled low, but the high nibble remains as ’1111’.
> Slave-active Byte: 111**1**_1110

Example1: CRC calculation (Update X and Y and set ADC-Test Mode)

```
    Command   Data     CRC (init all '0')
    00000001  00000101 00000000
    -----------------------------------
xor 11111111
    --------
   =11111110.0       .        .A
xor 10001110.1       .        .
    --------.-       .        .
  = 01110000.10      .        .B
 xor 1000111.01      .        .
     -------.--      .        .
   = 0110111.110     .        .C
  xor 100011.101     .        .
      ------.---     .        .
     = 10100.0110    .        .D
   xor 10001.1101    .        .
       -----.----    .        .
     = 00101.101101  .        .E
     xor 100.011101  .        .
         ---.------  .        .
       = 001.11000001.        .F
       xor 1.00011101.        .
         ---.------  .        .
           =.11011100.0       .G
         xor.10001110.1       .
            .--------.-       .
           = 1010010.10       .H
          xor 1000111.01      .
              -------.-       .
            = 10101.1100      .I
          xor 10001.1101      .
               ----.-----     .
             = 100.000100     .J
           xor 100.011101     .
               ---.------     .
                  =01100100. Remainder
                   10011011  inverted Remainder
Transmitted Sequence:
Command  Data     CRC
00000001 00000101 10011011
```

Example2: Use of two TLE5011 units in a bus mode.

Table 17 Update X,Y of two TLE5011 units, and read first TLE5011

SSC Byte no.	Description	Master transmitting	TLE5011 transmitting
1	Command[1)]	0_0000_000 (update all TLE5011)	-
2	Command[2)]	1_0001_110 (read first TLE5011)	-
3	Data Byte 1 to 01_H	-	XL
4	Data Byte 2 to 02_H	-	XH
5	Data Byte 3 to 03_H	-	YL
6	Data Byte 4 to 04_H	-	YH
7	Data Byte 5 to 05_H	-	FCNT_STAT
8	Data Byte 6 to 06_H	-	FSYNC_INV
9	CRC	-	calc. CRC value
10	Slave-active	-	cccc_nnnn
11	Command[3)]	1_0001_110 (read second TLE5011)	-
12	Data Byte 1 to 01_H	-	XL
13	Data Byte 2 to 02_H	-	XH
14	Data Byte 3 to 03_H	-	YL
15	Data Byte 4 to 04_H	-	YH
16	Data Byte 5 to 05_H	-	FCNT_STAT
17	Data Byte 6 to 06_H	-	FSYNC_INV
18	CRC	-	calc. CRC value
19	Slave-active	-	cccc_nnnn

1) Both TLE5011 are selected ($\overline{CS}_1$=$\overline{CS}_2$=active) during this command Byte.
2) $\overline{CS}_2$ of the second TLE5011 slave is deactivated after the second command Byte.
3) $\overline{CS}_1$ of the first TLE5011 slave is deactivated after the third command Byte.

3.10 Test Structures

Two different test signal structures are implemented in the TLE5011:

- Functional Angle Test. In this case, well-known signals feed the ADCs.
- Temperature Measurement. This is useful to readout the chip temperature for compensation purposes.

3.10.1 Functional Angle Tests

It is possible to feed the ADCs with appropriate values to simulate a certain magnet position and other GMR effects.

The values are generated with resistors on the chip.

The following X / Y ADC values can be programmed:

- 4 points, circle amplitude = 70.7%
  (0°, 90°, 180°, 270°)
- 8 points, circle amplitude = 100.0%
  (0°, 45°, 90°, 135°,180°, 225°, 270°, 315°)
- 8 points, circle amplitude = 122.1%
  (35.3°, 54.7°, 125.3°, 144.7°, 215.3°, 234.7°, 305.3°, 324.7°)
- 4 points, circle amplitude = 141.4%
  (45°, 135°, 225°, 315°)

Note: The 100% values typically correspond to 21700 digits and a voltage of ~ 110 mV.

Table 18 Functional Angle Test

Register bits	X / Y Values (decimal)		
	min.	**typ.**	**max.**
000	-400	0	400
001	14800	15500	16200
010	20700	21700	22700
011	32767		
100 [1)]	-400	0	400
101	-16200	-15500	-14800
110	-22700	-21700	-20700
111	-32768		

1) Not allowed to use.

ADC Test Vectors

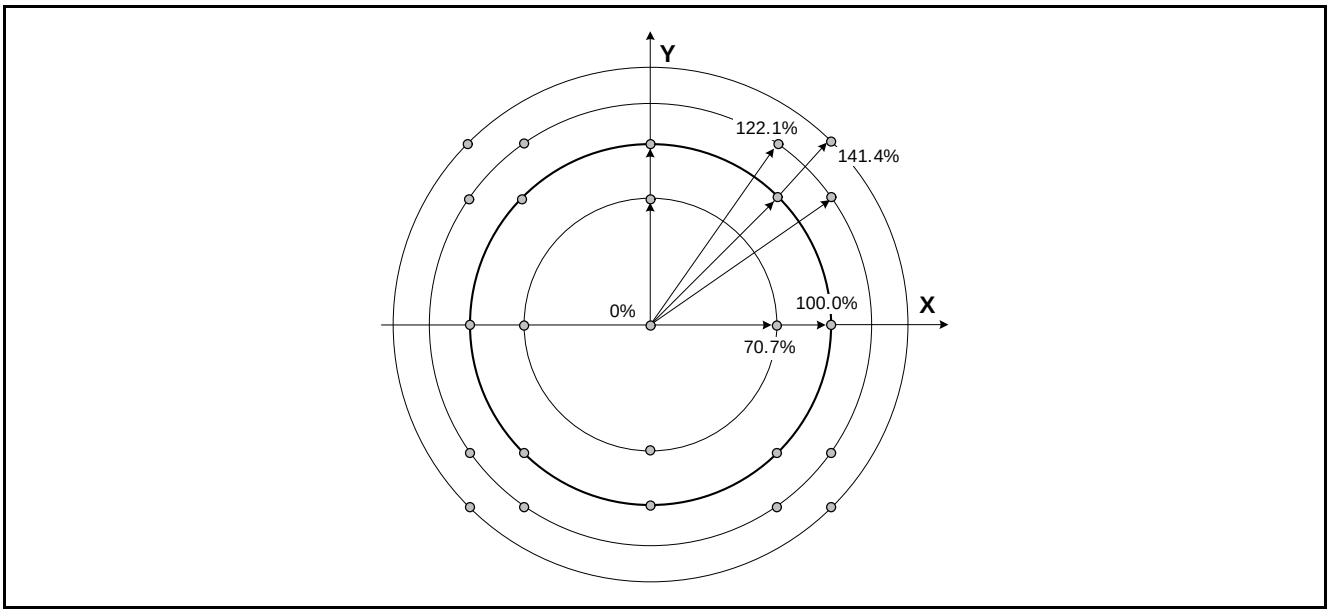


Figure 17 ADC Test Vectors

3.10.2 Temperature Measurement

An internal bandgap voltage can be used to measure the temperature on the chip.
This may be used to compensate for temperature-dependent errors.

The temperature values is sent out instead of the X value.

Table 19 Temperature Measurement

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Value at -40℃	T_{-40}	-	-	+22000	digits	
Value at 25℃	T_{25}	+2550	+5775	+9000	digits	
Value at 150℃	T_{150}	-22000	-	-	digits	
Temperature Sensitivity	S_T	-	-188.75	-	dig / K	1)

1) Should be used for temperature compensation of offset errors

3.10.3 Functional Angle Test and Temperature Measurement Timing

The functional angle test and the temperature readout are based on the same mechanism.

In the Normal Mode, the output path is linked to the functional angle test or to the temperature measurement unit until the mode is terminated.

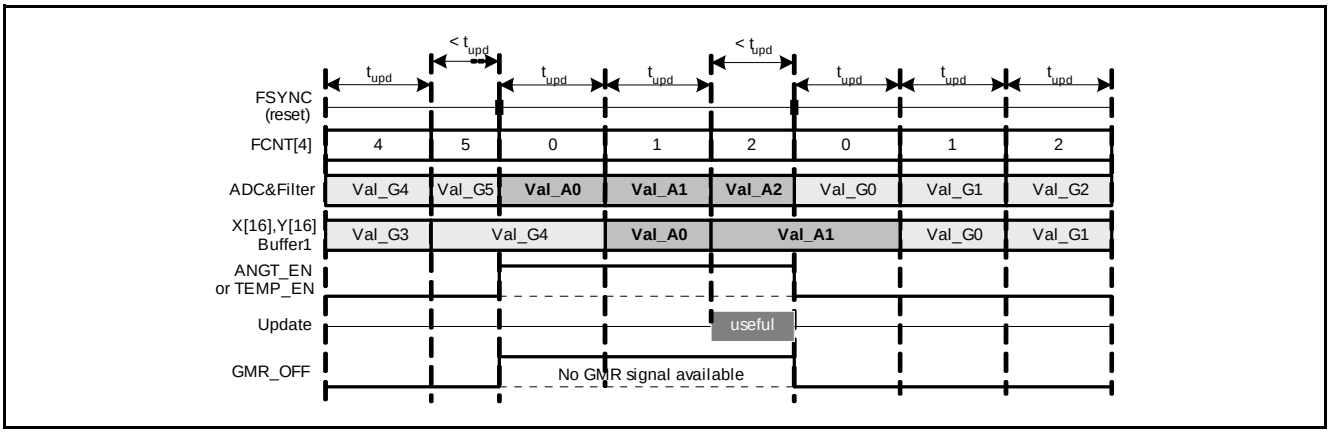


Figure 18 Measurement in Normal Mode

In Automatic Mode, the signal is automatically switched back to GMR measurement after the read-out of one value.

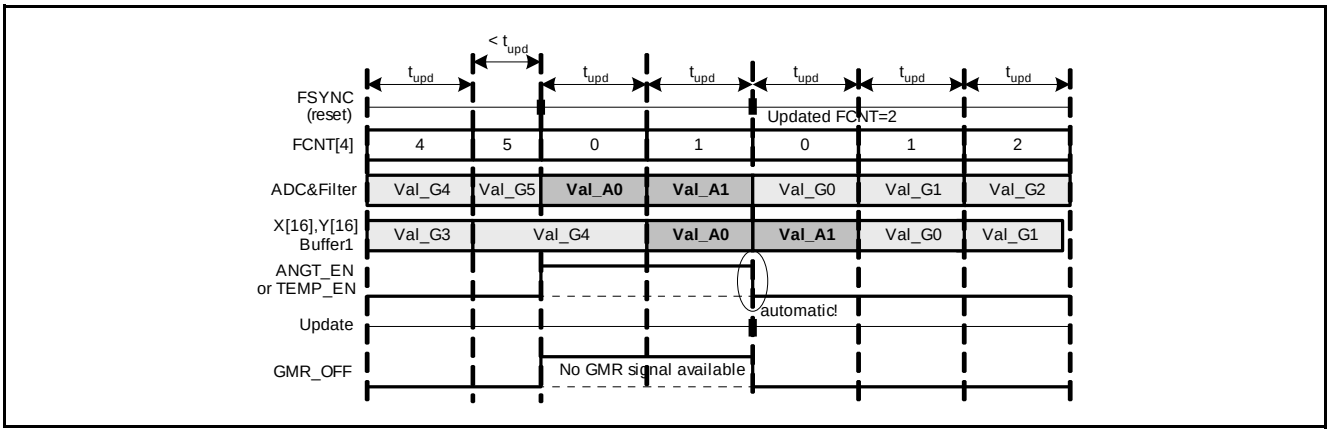


Figure 19 Measurement in Automatic Mode

3.11 Overvoltage Comparators

Various comparators monitor the voltage in order to ensure error-free operation.
The overvoltages must be active for at least t_{DEL} to set the test comparator bits in the SSC interface registers. This works as digital spike suppression.

Table 20 Test Comparators

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Overvoltage Detection	V_{OVG}	-	2.80	-	V	
	V_{OVA}	-	2.80	-	V	
	V_{OVD}	-	2.80	-	V	
V_{DD} Overvoltage	V_{DDOV}	-	6.5	-	V	
GND - off Voltage	V_{GNDoff}	-	0.54	-	V	$V_{GNDoff} = V_{GND} - V_{TST1}$
V_{DD} - off Voltage	V_{VDDoff}	-	0.48	-	V	$V_{VDDoff} = V_{CLK} - V_{DD}$ or $V_{SCK} - V_{DD}$
Spike filter Delay	t_{DEL}	-	10	-	µs	The error condition has to last longer than this value (min. 256 clocks of f_{DIG})

3.11.1 Internal Supply Voltage Comparators

Every voltage regulator has an overvoltage comparator to detect a malfunction.
If the nominal output voltage of 2.5 V is larger than V_{OVG}, V_{OVA} and V_{OVD}, then this overvoltage comparator is activated. It sets the *VRx_OV* bit.

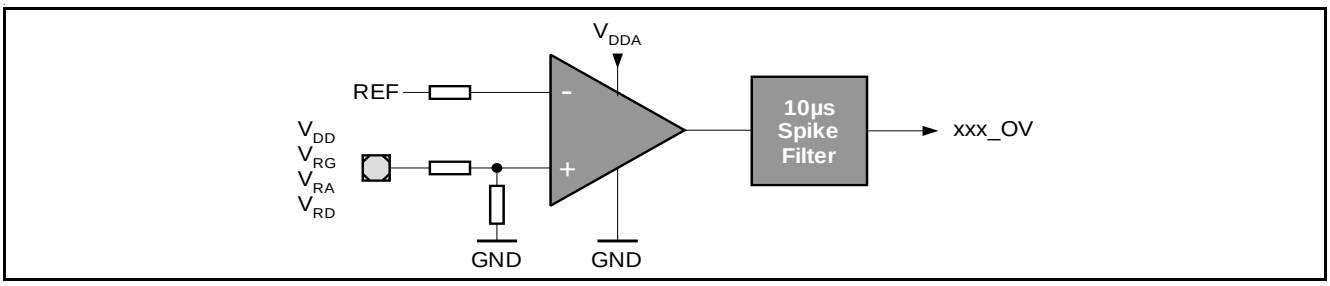


Figure 20 OV Comparator

3.11.2 V_{DD} Overvoltage Detection

The Overvoltage Detection Comparator monitors the external supply voltage at the V_{DD} pin. It activates the *STAT_VR* (see **Figure 20**).

3.11.3 GND-off Comparator

The GND-off Comparator is used to detect a voltage difference between the GND pin and TST1 (which must be soldered to GND in the application). It activates the *STAT_VR* bit. This circuit can detect a disconnection of the Supply GND Pin.

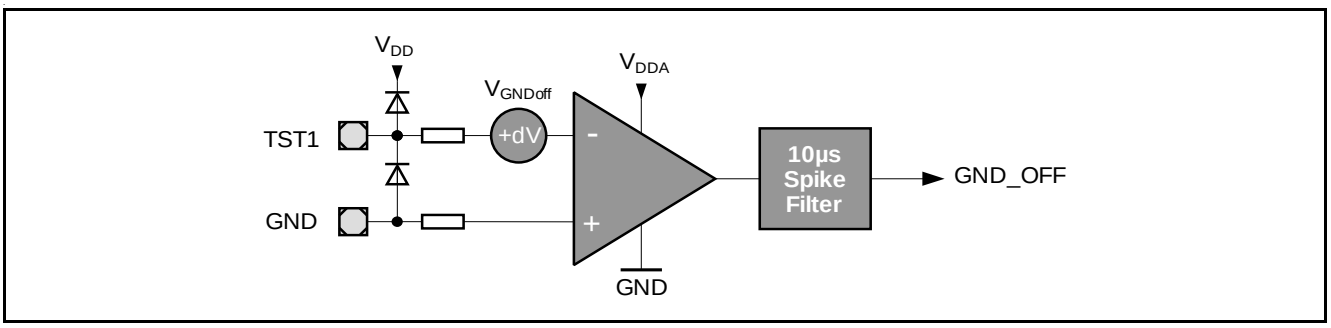


Figure 21 GND-off Comparator

3.11.4 V_{DD} - off Comparator

The V_{DD}-off Comparator detects a disconnection of the V_{DD} pin supply voltage. In this case, the TLE5011 is supplied by the SCK, CLK and $\overline{CS}$ input pins via the ESD structures. It activates the *STAT_VR* bit.

The retriggerable analog monoflop is necessary because of the non-static signal of the CLK and SCK signals.

This comparator is also activated if spikes on CLK or SCK achieve the condition:

$(V_{CLK} - V_{DD}) > V_{VDDoff}$ or $(V_{SCK} - V_{DD}) > V_{VDDoff}$

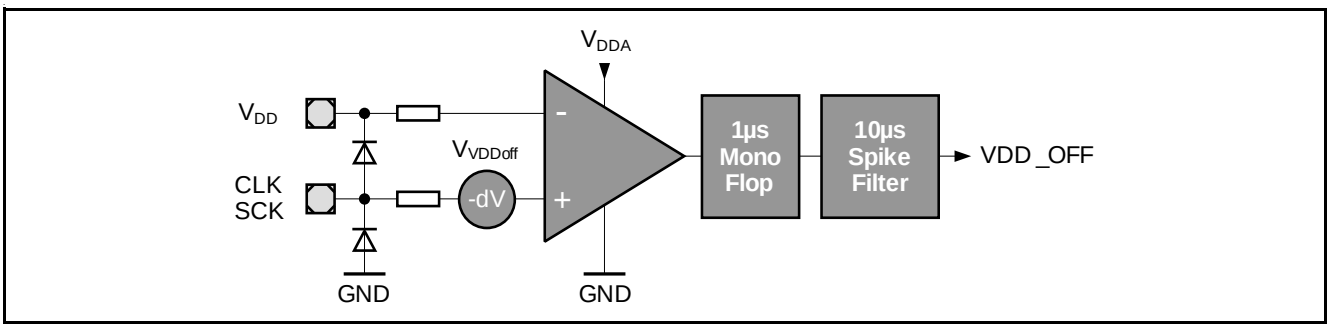


Figure 22 V_{DD} - off Comparator

4 Package Information

4.1 Package Parameters

Table 21 Package Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal Resistance	R_{thJA}	-	150	200	K/W	Junction to air 1)
	R_{thJC}	-	-	75	K/W	Junction to case
	R_{thJL}	-	-	85	K/W	Junction to lead
Soldering Moisture Level	MSL 3					260℃
Lead frame	Cu					
Plating	Sn 100%					> 7 µm

1) According to Jedec JESD51-7

Package Outline PG-DSO-8

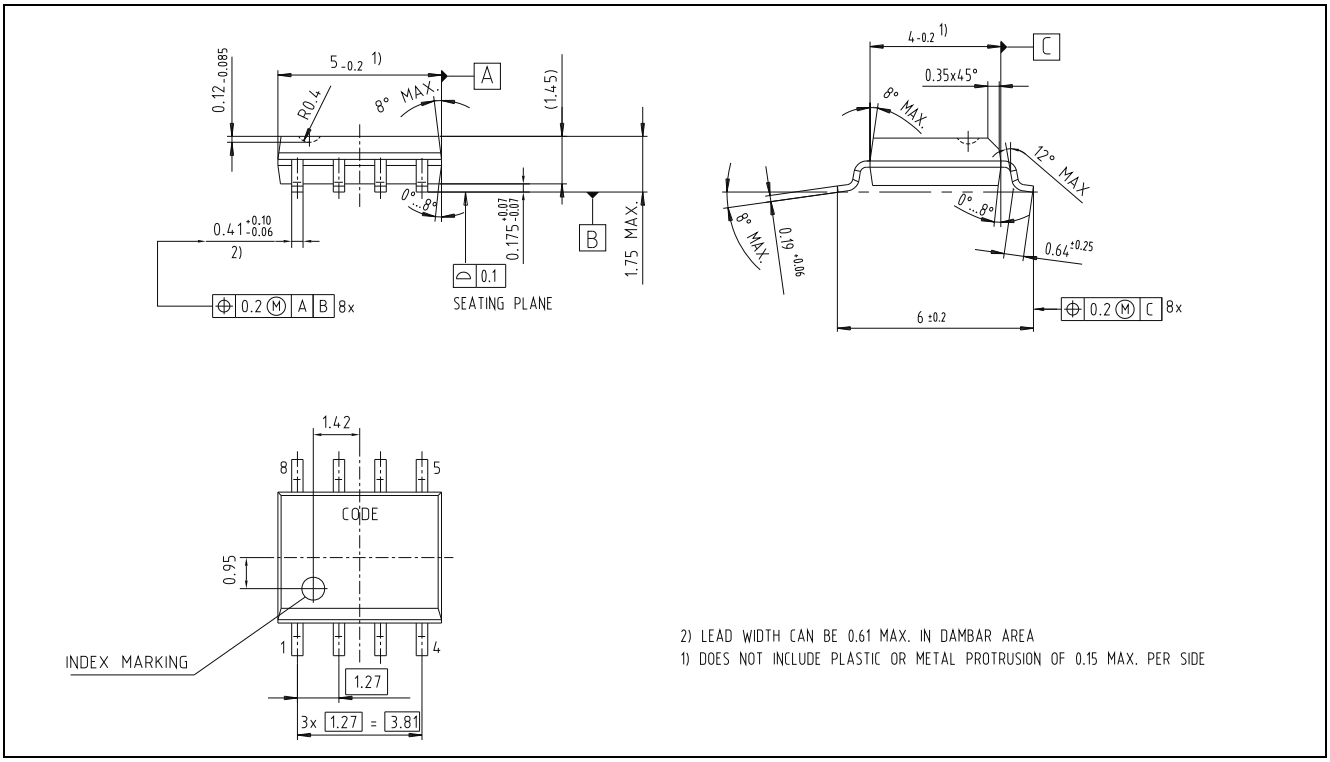


Figure 23 PG-DSO-8 Package Dimension

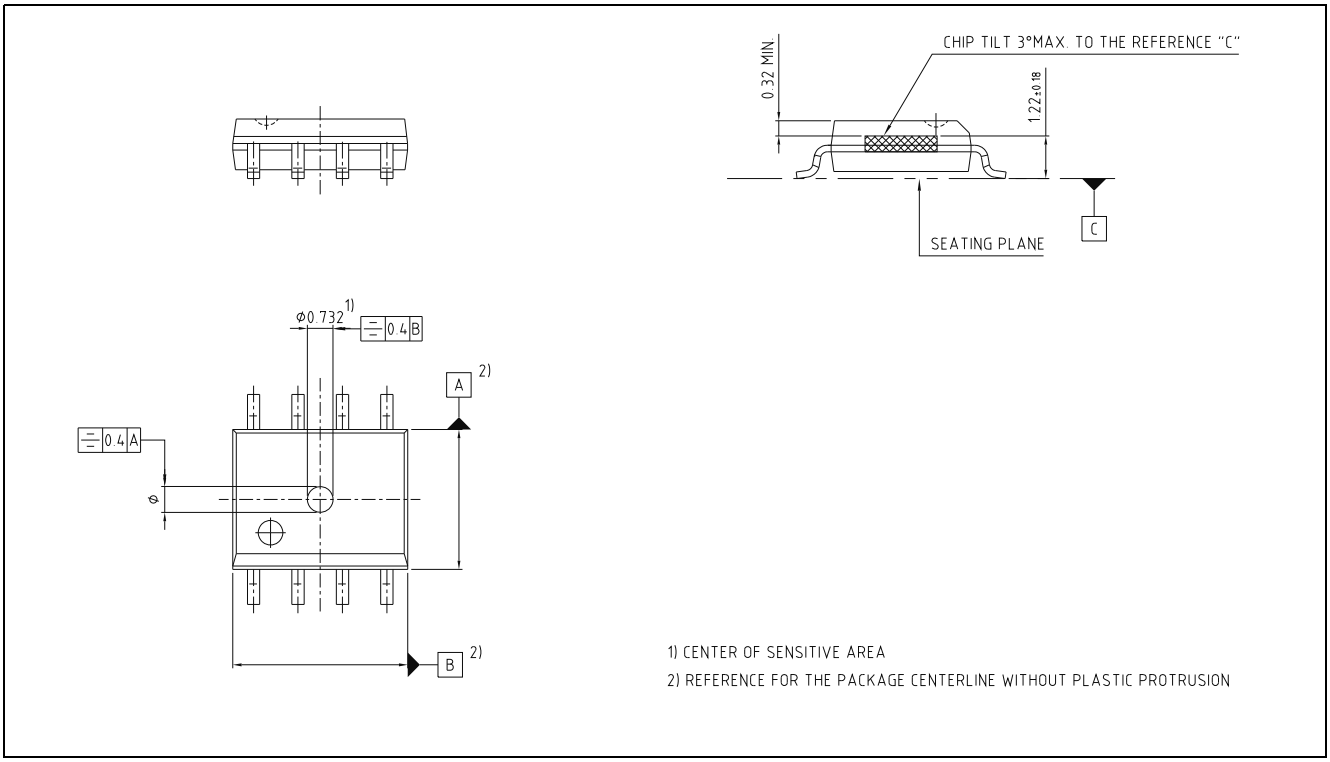


Figure 24 Position of Sensing Element

Footprint PG-DSO-8

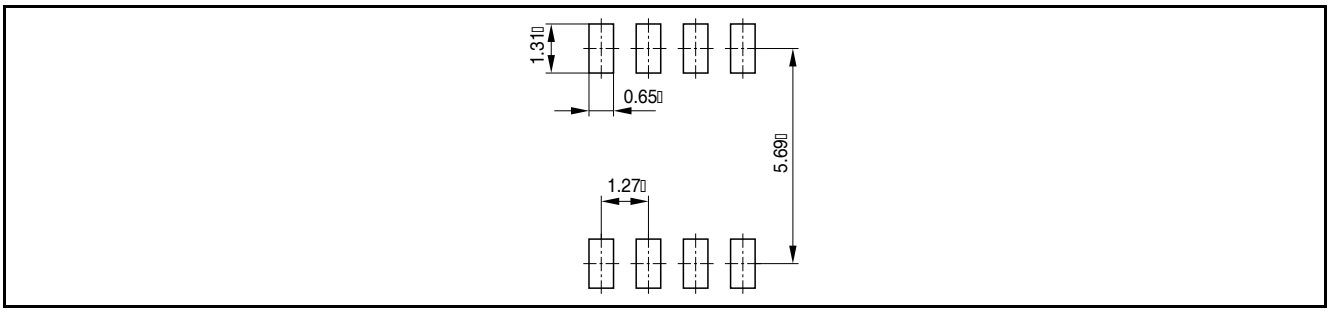


Figure 25 Footprint PG-DSO-8

Packing

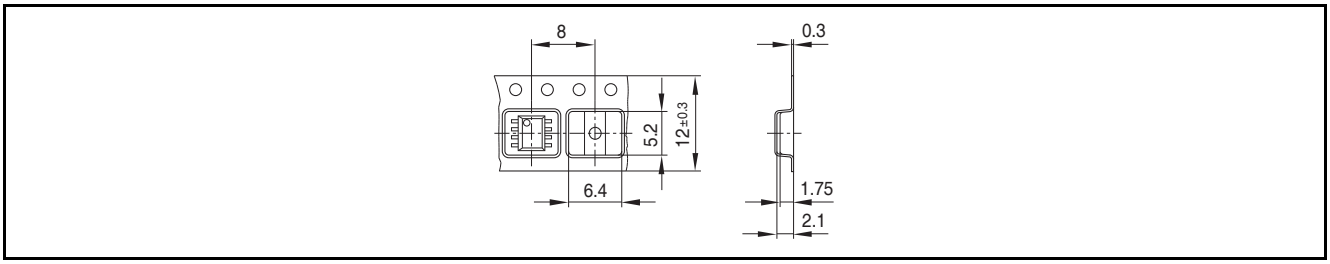


Figure 26 Tape and Reel

Marking

Position	Marking	Description
1st Line	*5011xx*	See ordering table on page 6
2nd Line	*xxx*	Lot code
3rd Line	*Gxxxx*	G .. green, 4-digit .. date code

Processing

Note: For processing recommendations, please refer to Infineon's Notes on Processing

www.infineon.com

Published by Infineon Technologies AG