

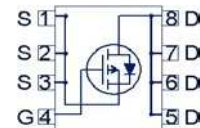
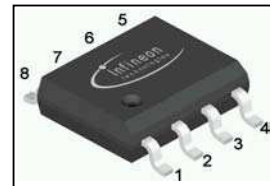
OptiMOS® -P Power-Transistor
Features

- P-Channel
- Enhancement mode
- Logic level
- 150°C operating temperature
- Avalanche rated
- Qualified according JEDEC for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21


Product Summary

V_{DS}		-30	V
$R_{DS(on),max}$	$V_{GS}= 10\text{ V}$	8.0	m Ω
	$V_{GS}= 4.5\text{ V}$	12.0	A
I_D		-14.9	A

PG-DSO-8



Type	Package	Marking	Leadfree	Halogen free	packing
BSO301SP H	PG-DSO-8	301SP	Yes	Yes	dry

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			≤10 secs	steady state	
Continuous drain current	I_D	$T_A=25\text{ °C}^{1)}$	-14.9	-12.6	A
		$T_A=70\text{ °C}^{1)}$	-11.9	-10	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}^{2)}$	-60		
Avalanche energy, single pulse	E_{AS}	$I_D=-14.9\text{ A}, R_{GS}=25\ \Omega$	248		mJ
Gate source voltage	V_{GS}		±20		V
Power dissipation	P_{tot}	$T_A=25\text{ °C}^{1)}$	2.5	1.79	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
ESD class		JESD22-A114 HBM	1C (1kV - 2kV)		
Soldering temperature			260		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - soldering point	R_{thJS}		-	-	35	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, $t_p \leq 10$ s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm ² cooling area ¹⁾ , $t_p \leq 10$ s	-	-	50	
		6 cm ² cooling area ¹⁾ , steady state	-	-	80	

Electrical characteristics, at $T_j=25$ °C, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0$ V, $I_D=-250$ μ A	-30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-250$ μ A	-1	-1.5	-2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-30$ V, $V_{GS}=0$ V, $T_j=25$ °C	-	-0.1	-1	μ A
		$V_{DS}=-30$ V, $V_{GS}=0$ V, $T_j=125$ °C	-	-10	-100	
Gate-source leakage current	I_{GSS}	$V_{GS}=-20$ V, $V_{DS}=0$ V	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5$ V, $I_D=-12$ A	-	8.8	12	m Ω
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-10$ V, $I_D=-14.9$ A	-	6.3	8.0	
Transconductance	g_{fs}	$ V_{DS} > 2 I_D R_{DS(on)max}$, $I_D=-14.9$ A	22	44	-	S

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μ m thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V},$ $V_{DS}=-25\text{ V}, f=1\text{ MHz}$	-	4430	5890	pF
Output capacitance	C_{oss}		-	1180	1570	
Reverse transfer capacitance	C_{rss}		-	970	1500	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-15\text{ V},$ $V_{GS}=-10\text{ V},$ $I_D=-1\text{ A}, R_G=6\ \Omega$	-	15	23	ns
Rise time	t_r		-	22	33	
Turn-off delay time	$t_{d(off)}$		-	130	195	
Fall time	t_f		-	110	165	

Gate Charge Characteristics³⁾

Gate to source charge	Q_{gs}	$V_{DD}=-24\text{ V},$ $I_D=-14.9\text{ A},$ $V_{GS}=0\text{ to }-10\text{ V}$	-	-11	-15	nC
Gate charge at threshold	$Q_{g(th)}$		-	-7.1	-9.5	
Gate to drain charge	Q_{gd}		-	-35		
Switching charge	Q_{sw}		-	-40	-59	
Gate charge total	Q_g		-	-102	-136	
Gate plateau voltage	$V_{plateau}$		-	-2.5	-	V
Output charge	Q_{oss}	$V_{DD}=-15\text{ V}, V_{GS}=0\text{ V}$	-	-36	-48	

Reverse Diode

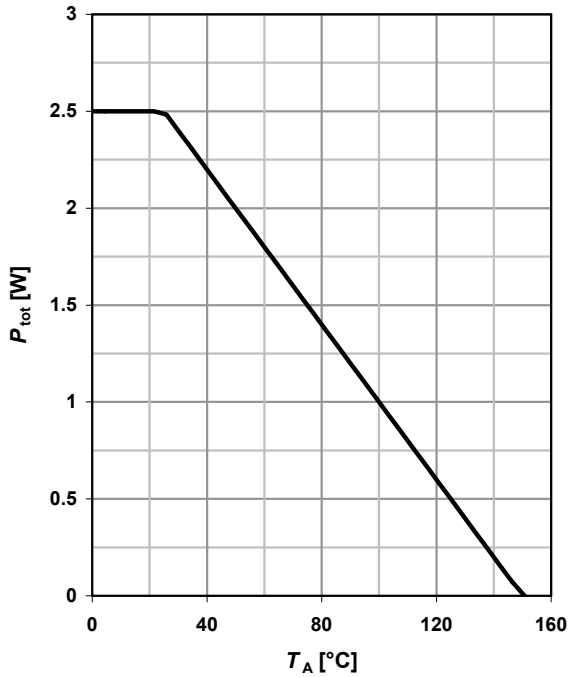
Diode continuous forward current	I_S	$T_A=25\text{ }^\circ\text{C}$	-	-	-2.1	A
Diode pulse current	$I_{S,pulse}$		-	-	-60	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=-14.9\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	-0.82	-1.2	V
Reverse recovery time	t_{rr}	$V_R=15\text{ V}, I_F=-14.9\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	32	40	ns
Reverse recovery charge	Q_{rr}		-	-20	-25	nC

²⁾ See figure 3

³⁾ See figure 16 for gate charge parameter definition

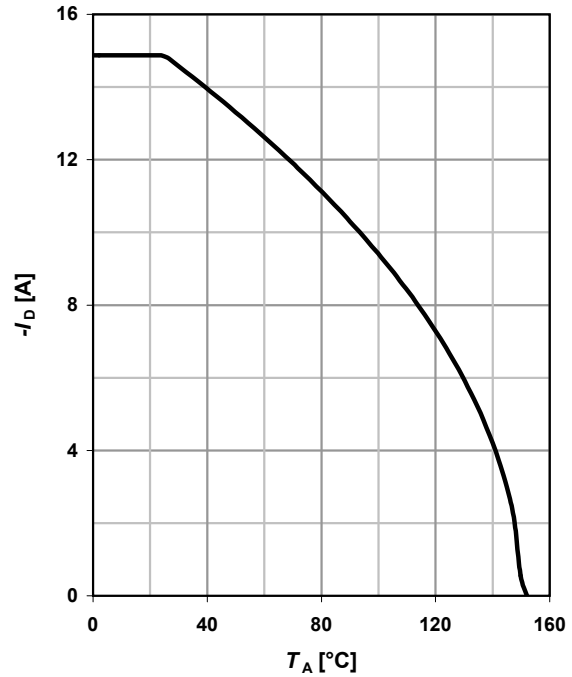
1 Power dissipation

$P_{tot}=f(T_A); t_p \leq 10 \text{ s}$



2 Drain current

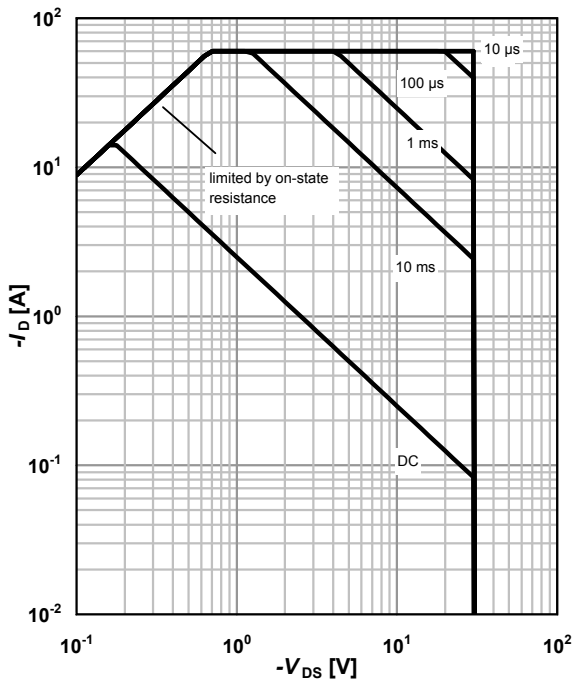
$I_D=f(T_A); |V_{GS}| \geq 10 \text{ V}; t_p \leq 10 \text{ s}$



3 Safe operating area

$I_D=f(V_{DS}); T_A=25 \text{ }^\circ\text{C}^1; D=0$

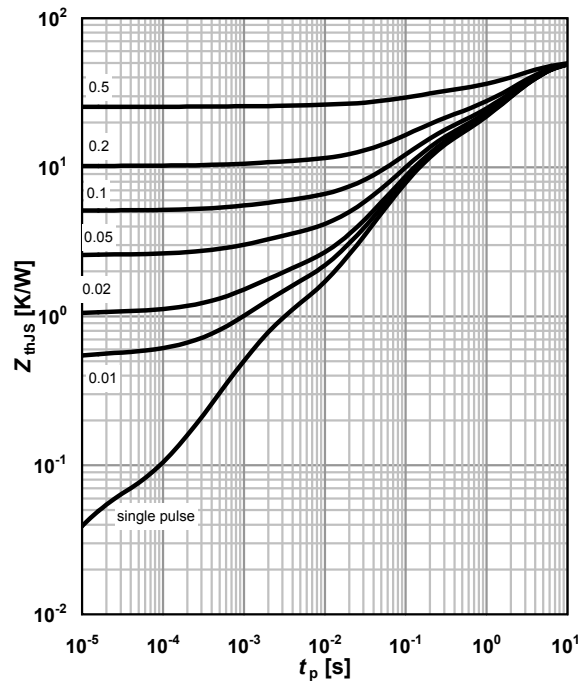
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJS}=f(t_p)$

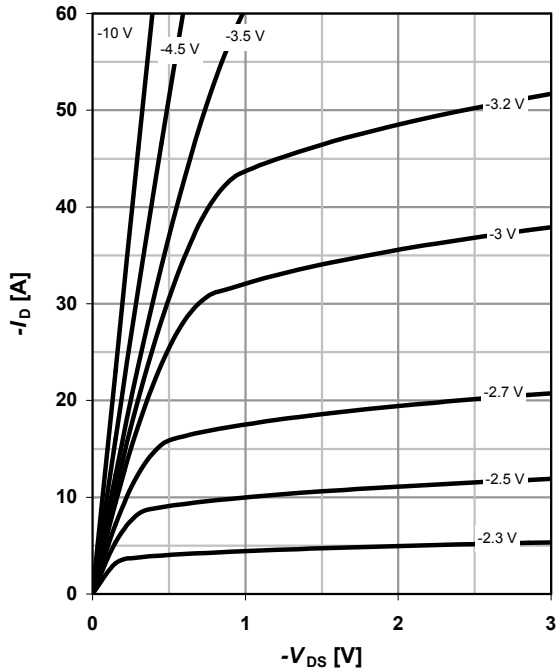
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

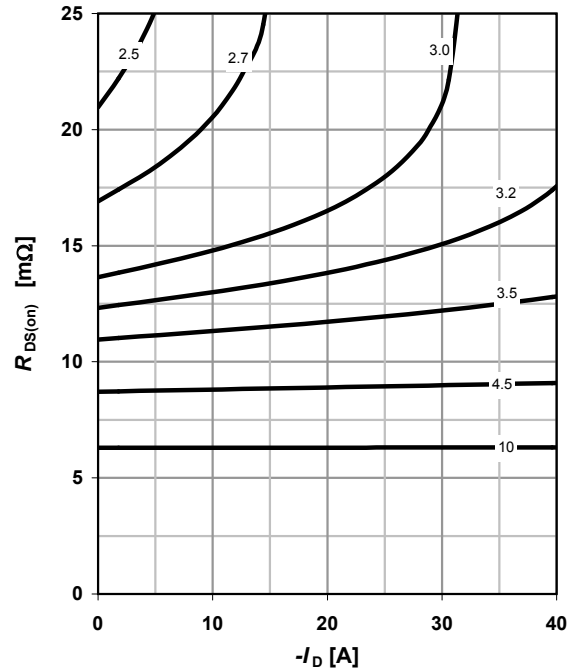
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

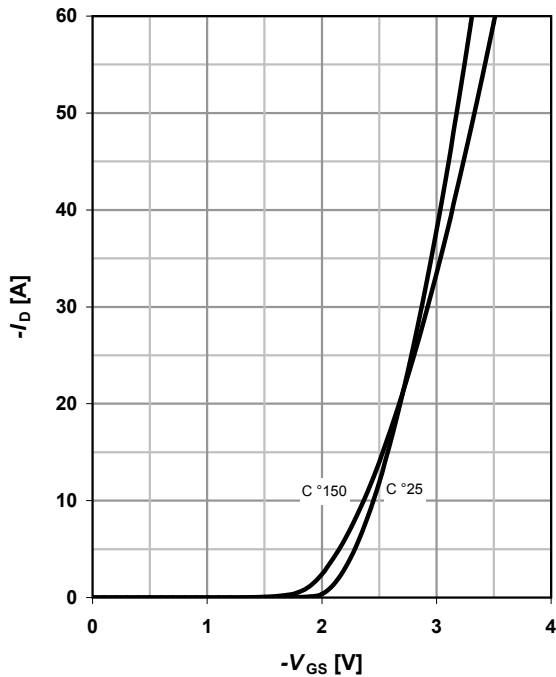
parameter: V_{GS}



7 Typ. transfer characteristics

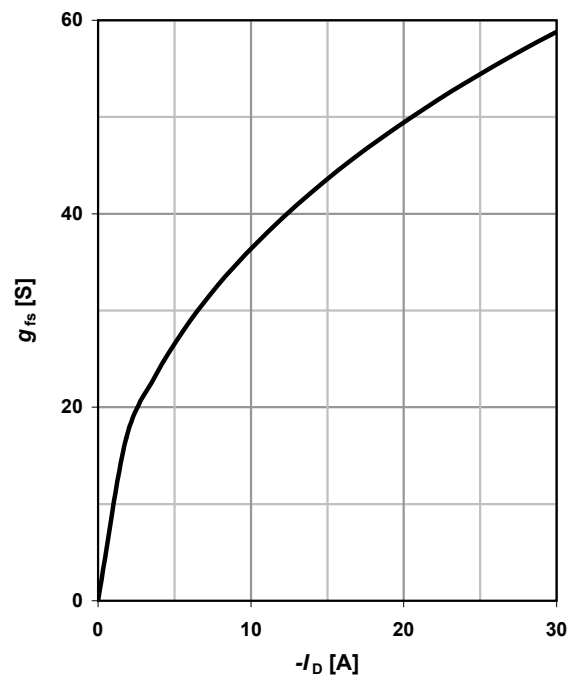
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



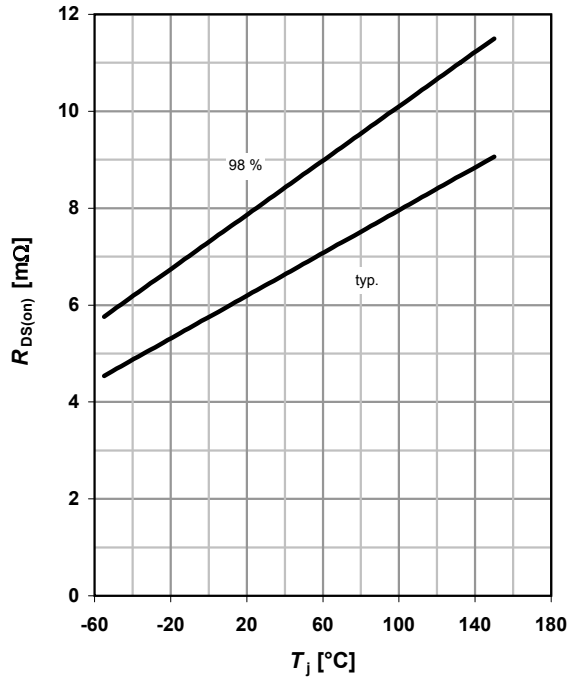
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



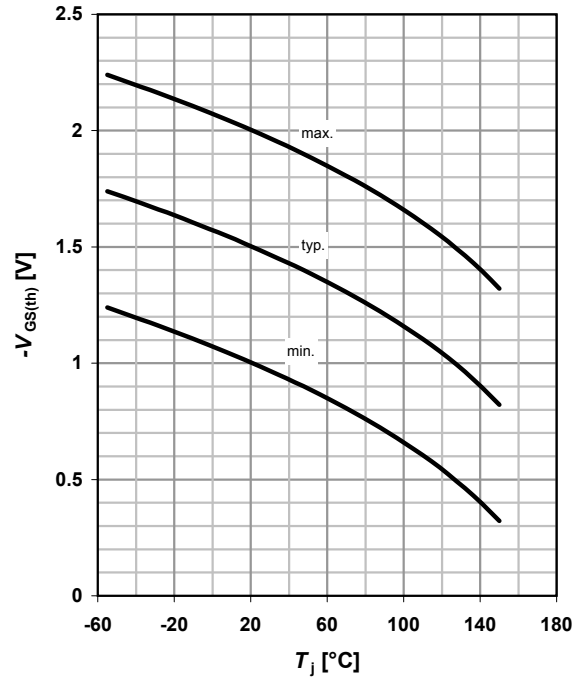
9 Drain-source on-state resistance

$R_{DS(on)} = f(T_j); I_D = -14.9 \text{ A}; V_{GS} = -10 \text{ V}$



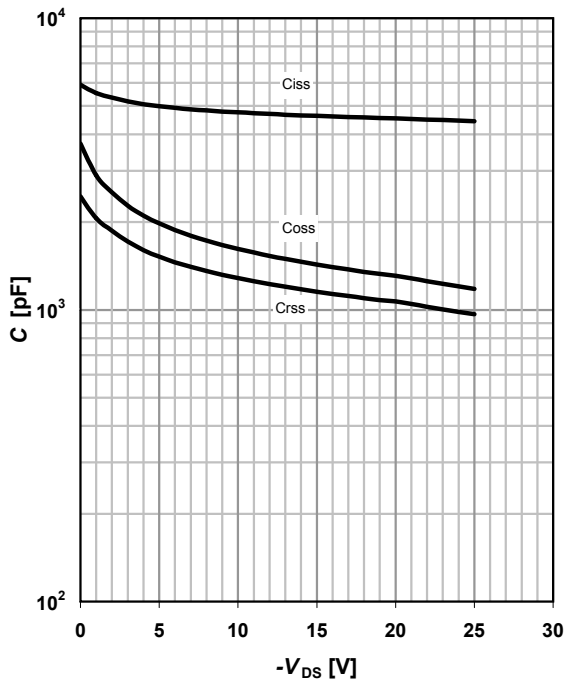
10 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = -250 \mu\text{A}$



11 Typ. capacitances

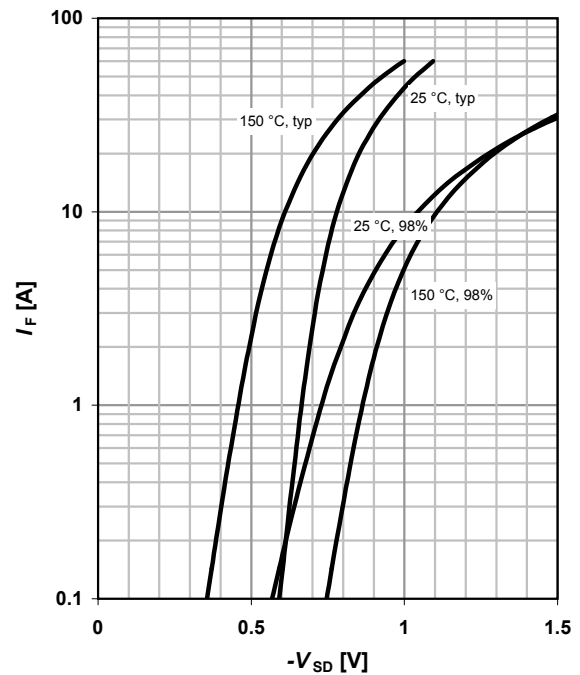
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

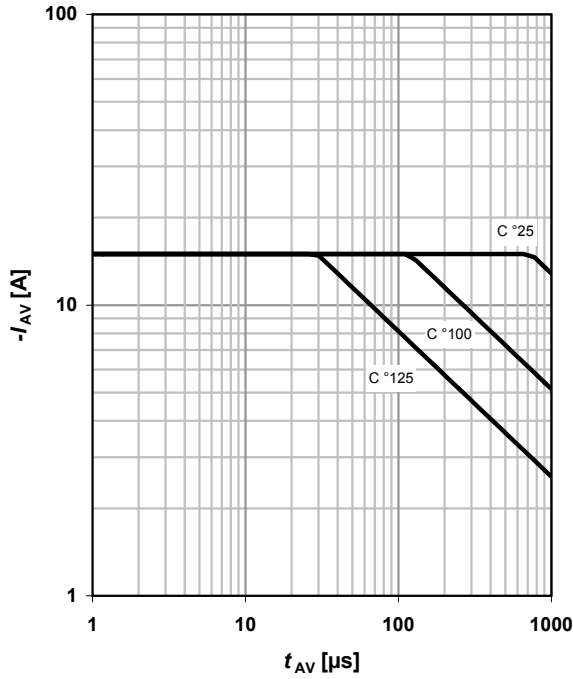
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

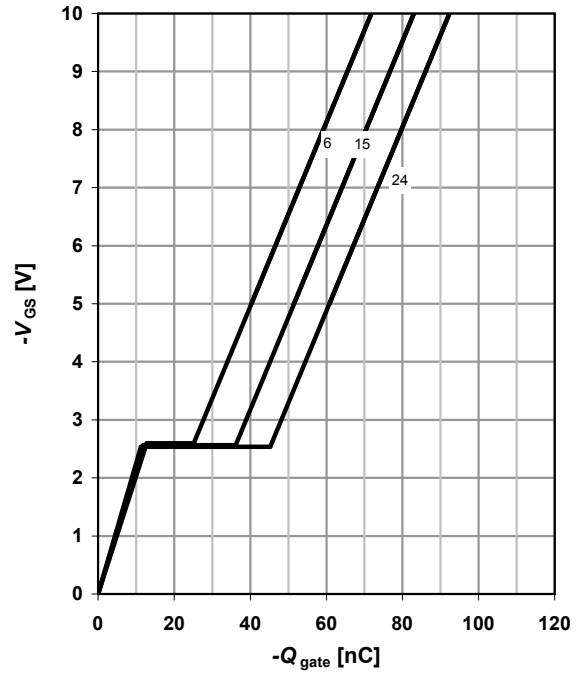
parameter: $T_{j(start)}$



14 Typ. gate charge

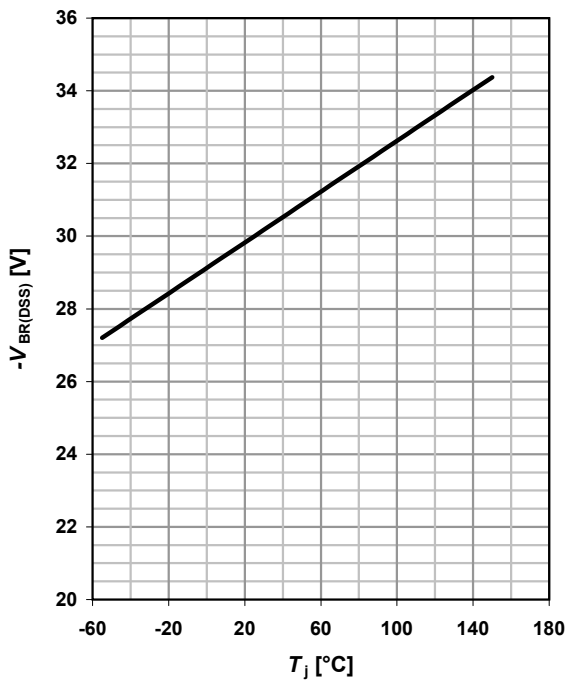
$V_{GS}=f(Q_{gate}); I_D=-14.9$ A pulsed

parameter: V_{DD}

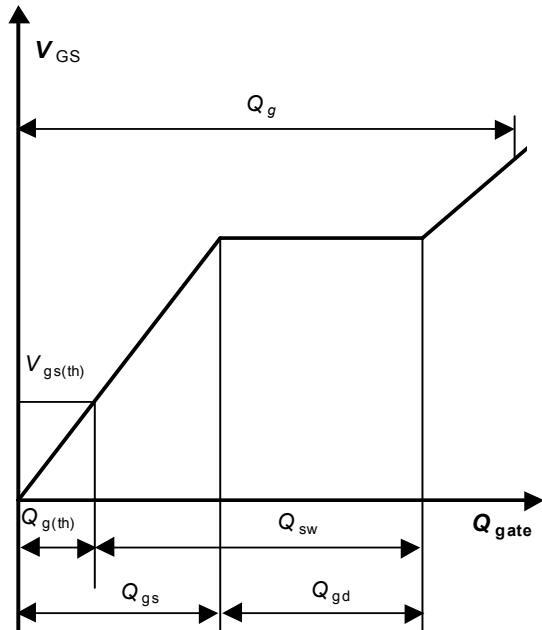


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=-250 \mu$ A

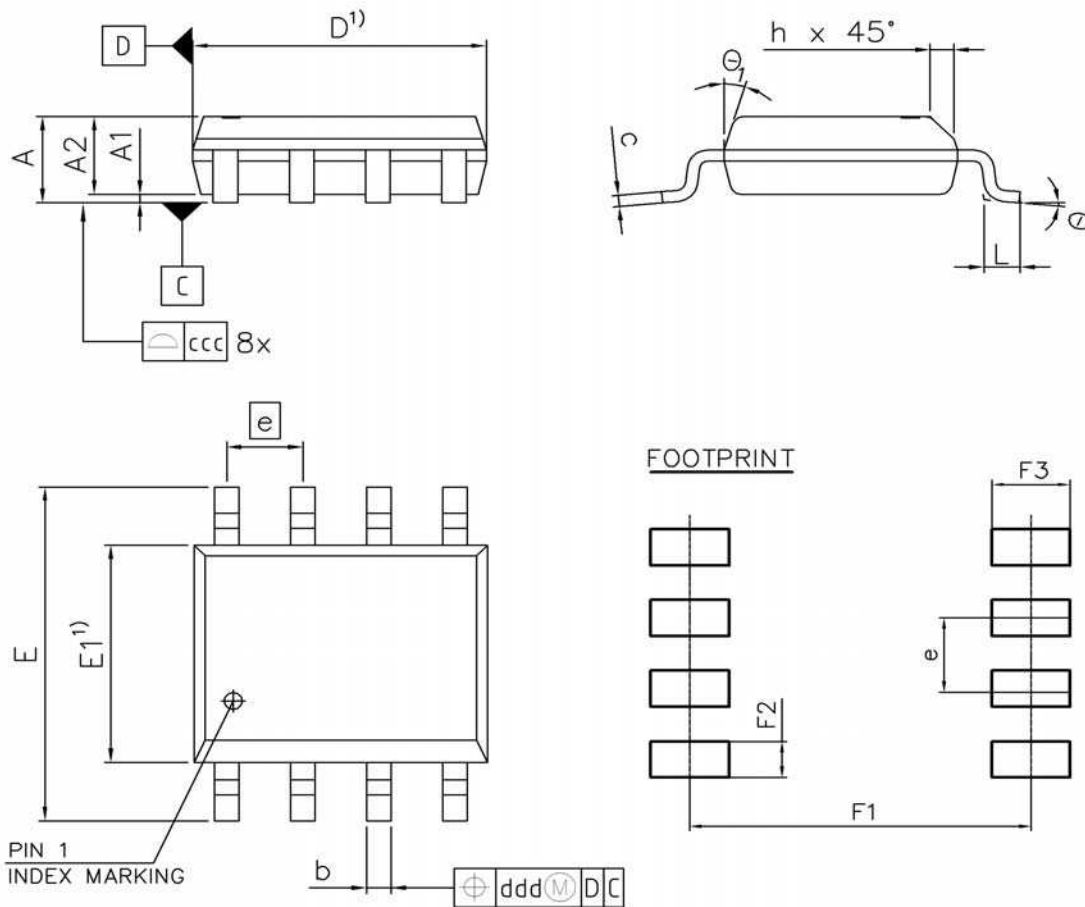


16 Gate charge waveforms



Package Outline

P-DSO-8: Outline



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ_1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

DOCUMENT NO.
Z8B00003333

SCALE

EUROPEAN PROJECTION

ISSUE DATE
09.01.2008

REVISION
02

Published by
Infineon Technologies AG
81726 Munich, Germany
© 2008 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.