

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CFDA Automotive

650V CoolMOS™ CFDA Power Transistor
IPx65R660CFDA

Data Sheet

Rev. 2.0
Final

Automotive

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFDA series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter, and cooler.

Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM $R_{ds(on)} \cdot Q_g$ and E_{oss}
- Easy to use/drive
- Qualified according to AEC Q101
- Green package (RoHS compliant), Pb-free plating, halogen free for mold compound

Applications

650V CoolMOS™ CFDA is designed for switching applications.

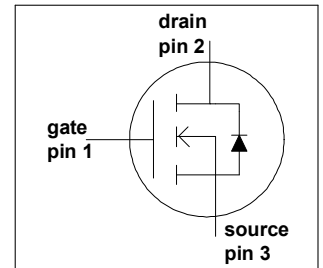
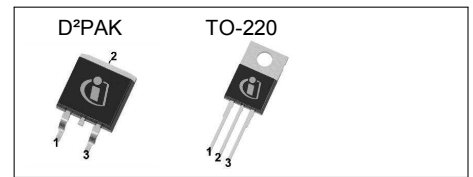


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	650	V
$R_{DS(on),max}$	0.66	Ω
Q_g,typ	20	nC
$I_D,pulse$	17	A
$E_{oss @ 400V}$	1.8	μJ
Body diode di/dt	900	A/ μs
Q_{rr}	0.2	μC
t_{rr}	65	ns
I_{rrm}	4.5	A

Type / Ordering Code	Package	Marking	Related Links
IPB65R660CFDA	PG-TO 263	65F6660A	-
IPP65R660CFDA	PG-TO 220		

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			6	A	$T_C = 25^\circ\text{C}$
				3.8		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			17	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			115	mJ	$I_D = 1.2\text{A}$, $V_{DD} = 50\text{V}$ (see table 19)
Avalanche energy, repetitive	E_{AR}			0.21	mJ	$I_D = 1.2\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			1.2	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation (non FullPAK, SMD) TO-220, D ² PAK	P_{tot}			62.5	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-40		150	$^\circ\text{C}$	
Mounting torque (non FullPAK) TO-220				60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S			6	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			17	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$ (see table 17)
Maximum diode commutation speed	di _f /dt			900	A/ μs	

¹⁾ Limited by $T_{j\text{ max}}$.

²⁾ Pulse width t_p limited by $T_{j\text{ max}}$

³⁾ Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics TO-220

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			2	K/W	
Thermal resistance, junction - ambient	R_{thJA}			62	K/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sld}			260	°C	1.6 mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics D²PAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			2	K/W	
Thermal resistance, junction - ambient ¹⁾	R_{thJA}			62	K/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm ² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sld}			260	°C	reflow MSL

¹⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage ¹⁾	$V_{(BR)DSS}$	650			V	$V_{GS} = 0V$, $I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	$V_{DS} = V_{GS}$, $I_D = 0.2mA$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 650V$, $V_{GS} = 0V$, $T_j = 25^\circ\text{C}$
			100			$V_{DS} = 650V$, $V_{GS} = 0V$, $T_j = 150^\circ\text{C}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20V$, $V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		0.594	0.66	Ω	$V_{GS} = 10V$, $I_D = 3.2A$, $T_j = 25^\circ\text{C}$
			1.544			$V_{GS} = 10V$, $I_D = 3.2A$, $T_j = 150^\circ\text{C}$
Gate resistance	R_G		6.5		Ω	$f = 1MHz$, open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		543		pF	$V_{GS} = 0V$, $V_{DS} = 100V$, $f = 1MHz$
Output capacitance	C_{oss}		32		pF	
Effective output capacitance, energy related ²⁾	$C_{o(er)}$		24		pF	$V_{GS} = 0V$, $V_{DS} = 0 \dots 400V$
Effective output capacitance, time related ³⁾	$C_{o(tr)}$		97		pF	$I_D = \text{constant}$, $V_{GS} = 0V$, $V_{DS} = 0 \dots 400V$
Turn-on delay time	$t_{d(on)}$		9		ns	$V_{DD} = 480V$, $V_{GS} = 13V$, $I_D = 3.2A$, $R_G = 6.8\Omega$ (see table 18)
Rise time	t_r		8		ns	
Turn-off delay time	$t_{d(off)}$		40		ns	
Fall time	t_f		10		ns	

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		3.5		nC	$V_{DD} = 480V$, $I_D = 3.2A$, $V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	Q_{gd}		11		nC	
Gate charge total	Q_g		20		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

¹⁾ For applications with applied blocking voltage > 65% of the specified blocking voltage, we recommend to evaluate the impact of the cosmic radiation effect in early design phase. For assessment please contact local Infineon sales office.

²⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

³⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V, I_F = 3.2A, T_j = 25^{\circ}C$
Reverse recovery time	t_{rr}		65		ns	$V_R = 400V, I_F = 3.2A,$ $di_F/dt = 100A/\mu s$ (see table 17)
Reverse recovery charge	Q_{rr}		0.2		μC	
Peak reverse recovery current	I_{rrm}		4.5		A	

5 Electrical characteristics diagrams

Table 9

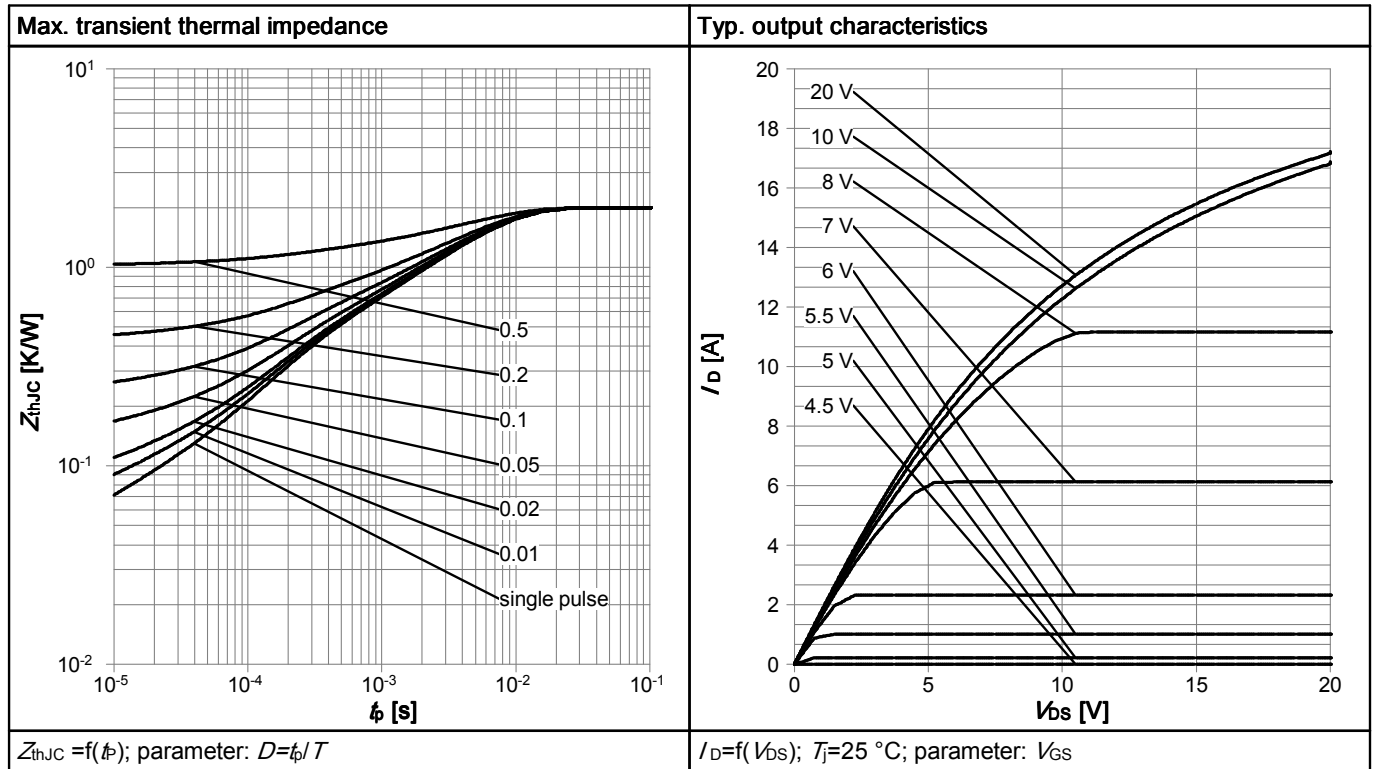


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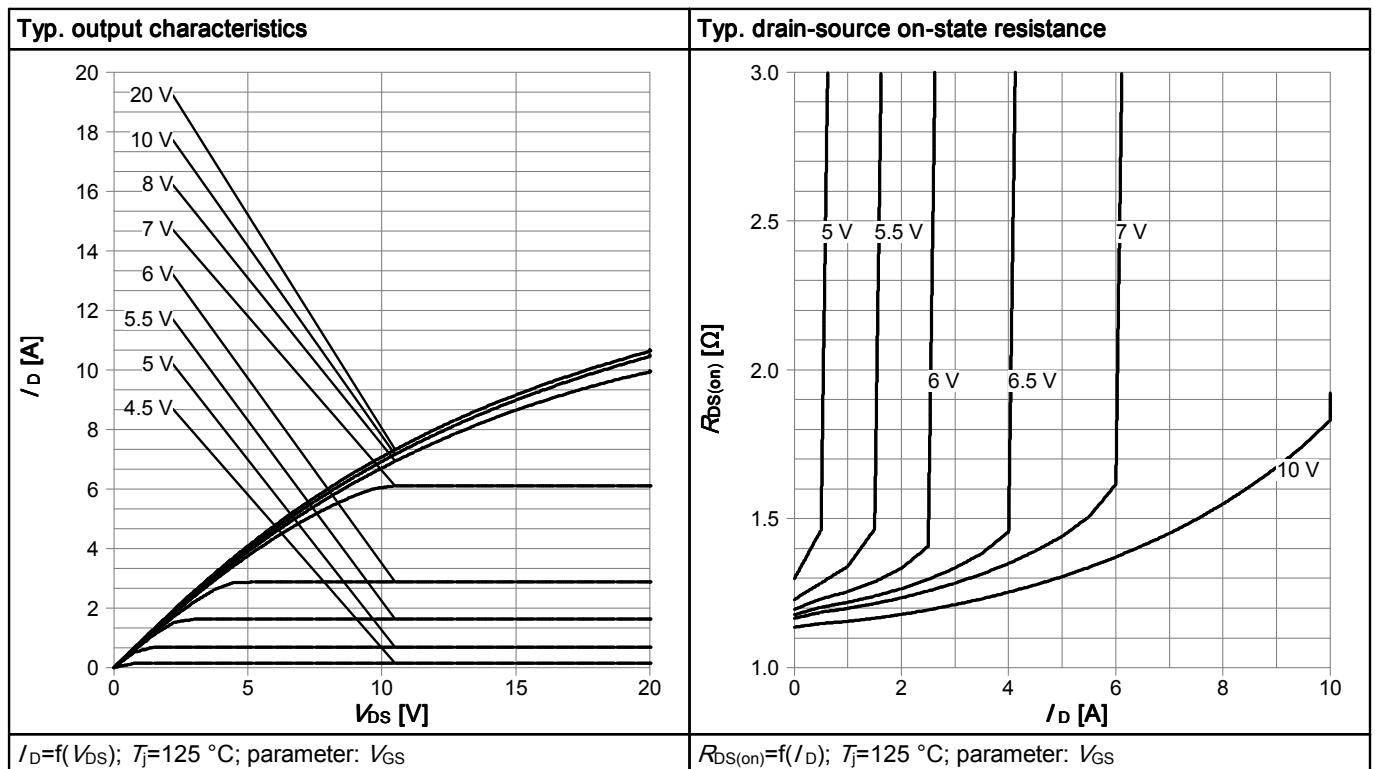


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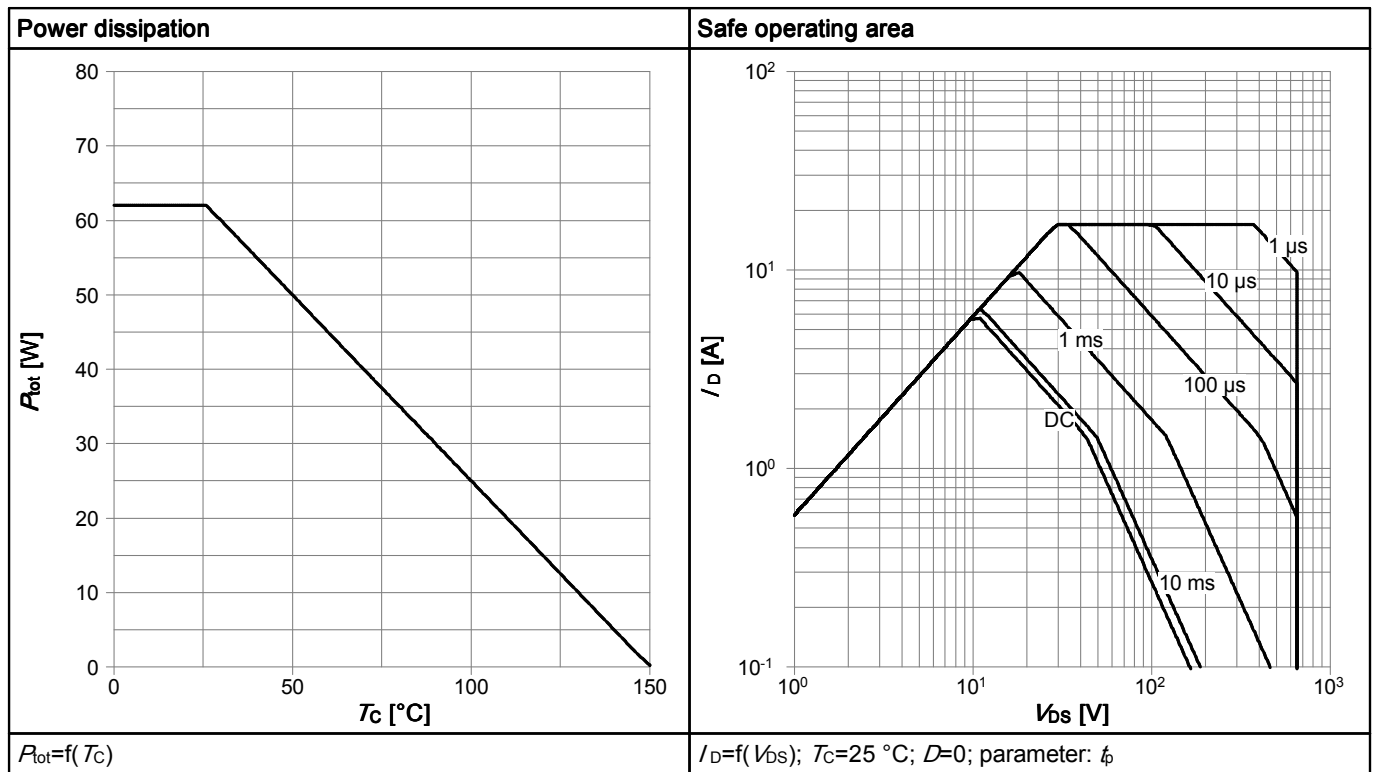


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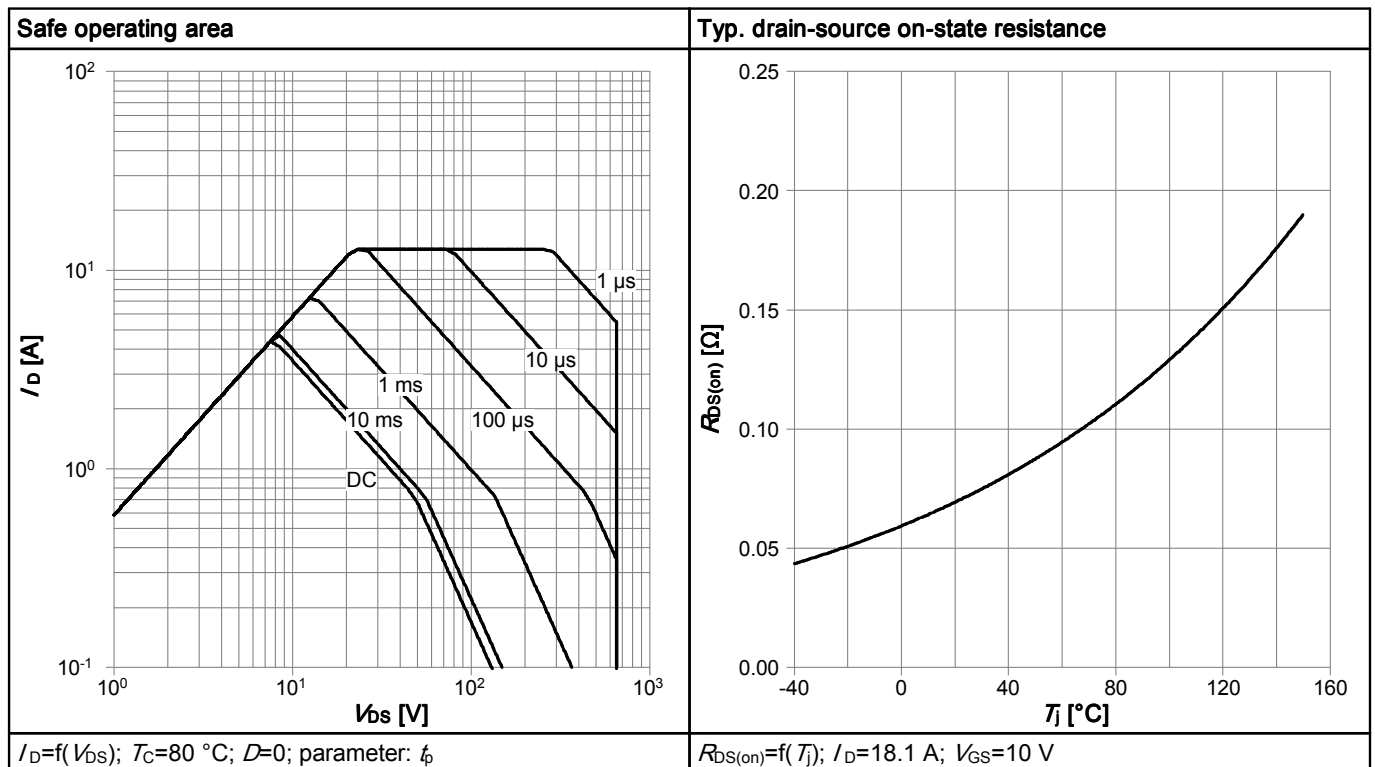


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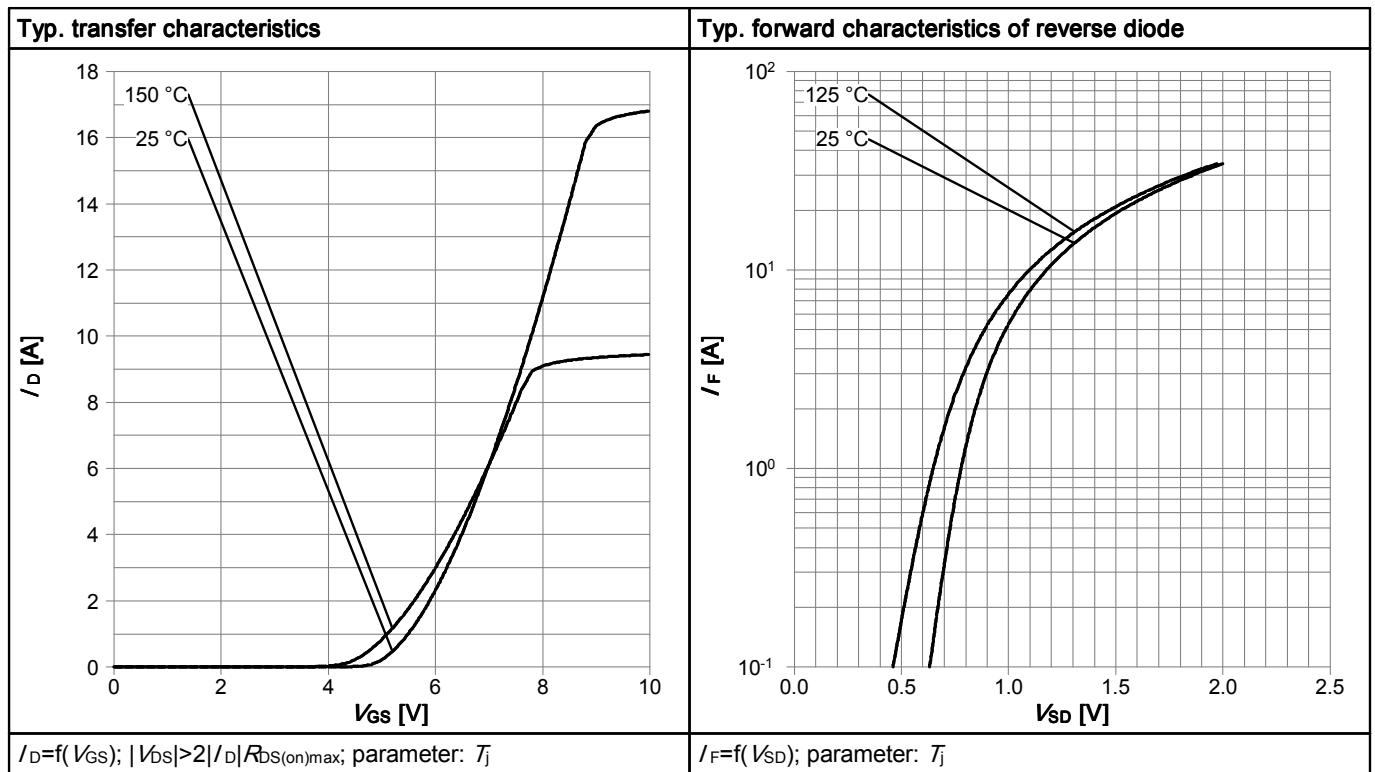


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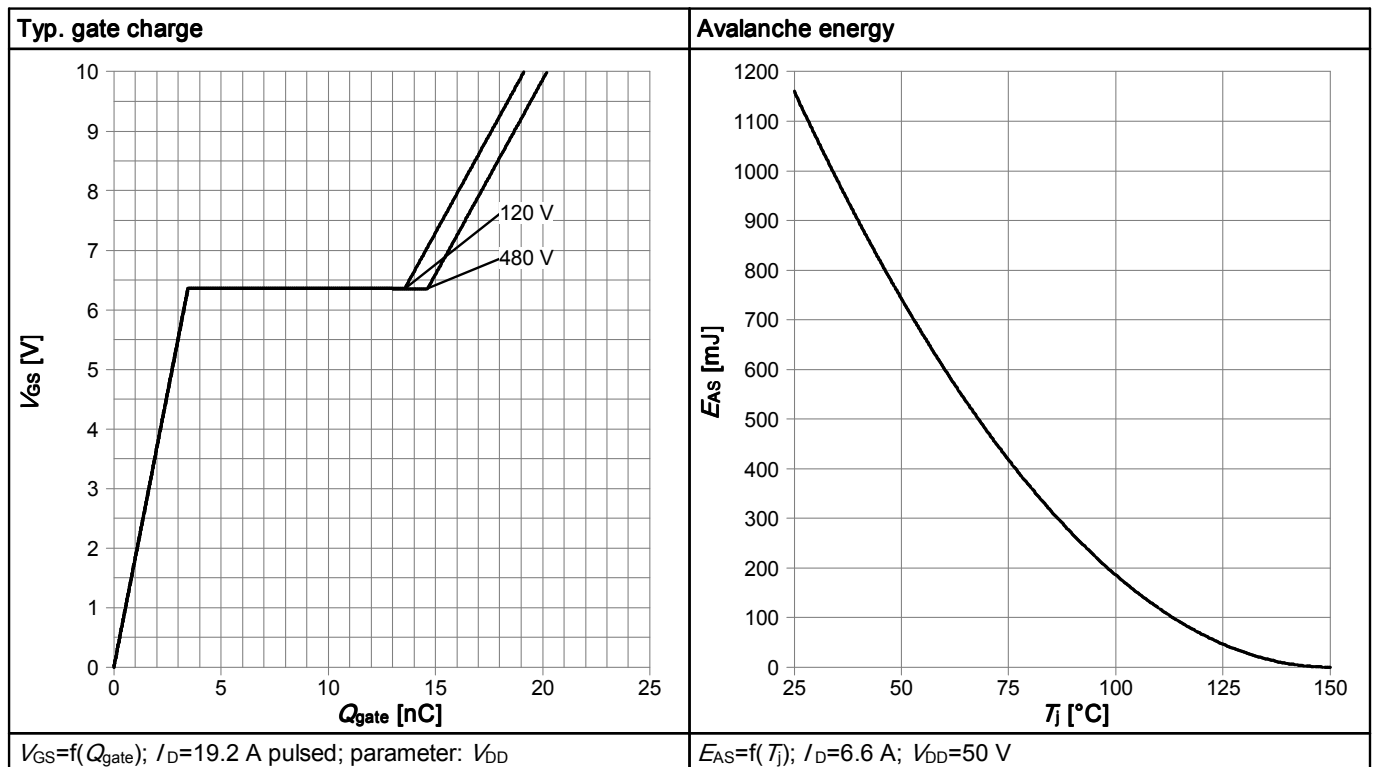


Table 15

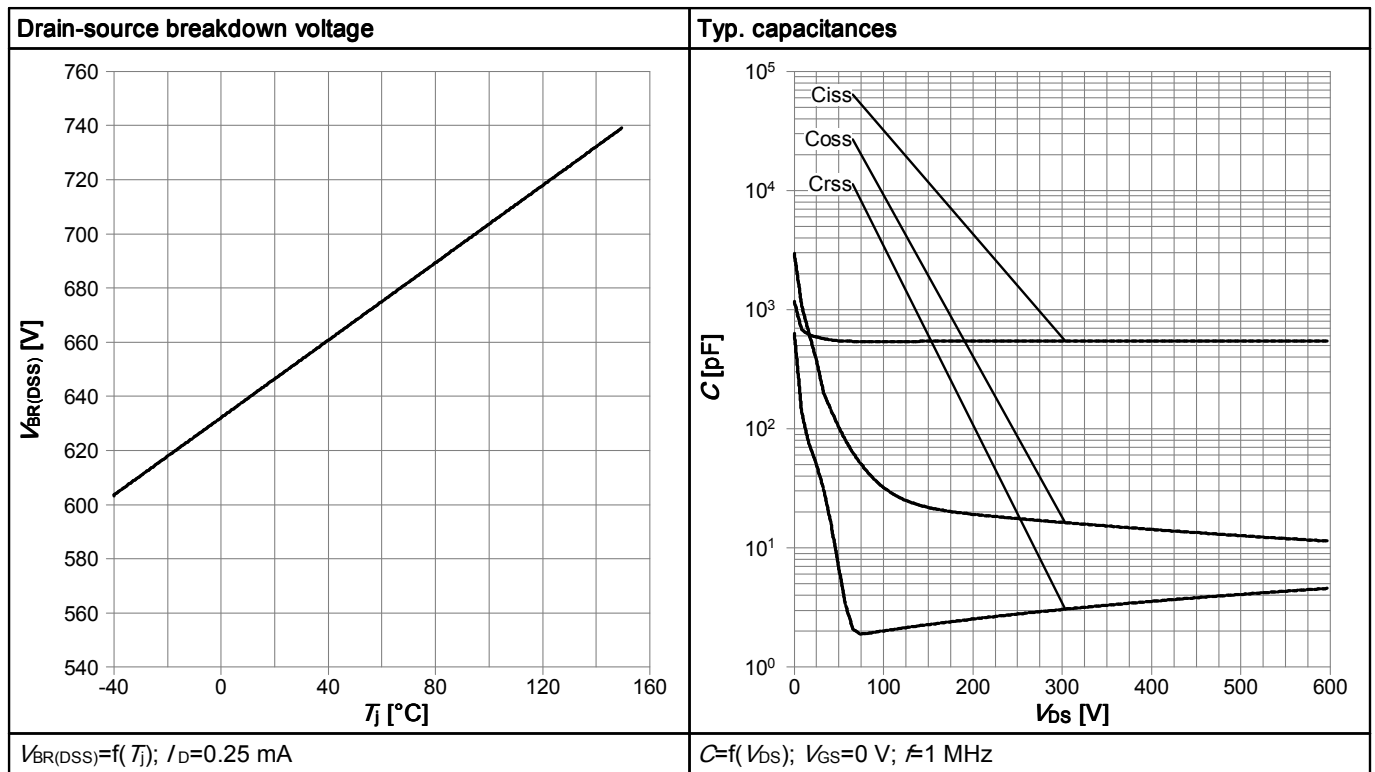
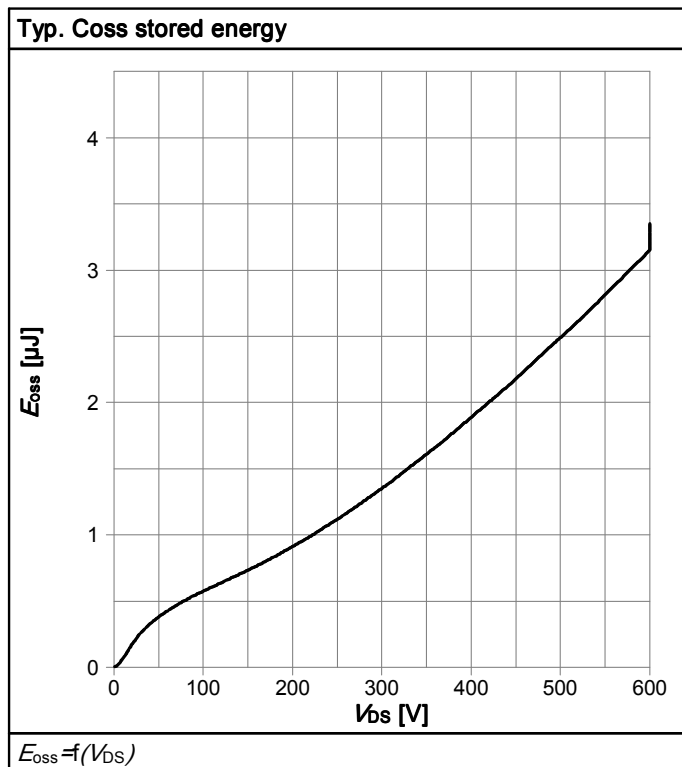


Table 16



6 Test Circuits

Table 17 Diode characteristics

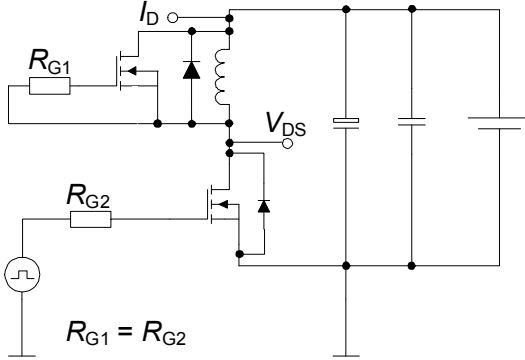
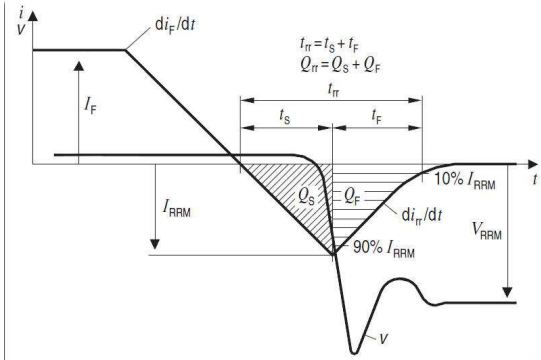
Test circuit for diode characteristics	Diode recovery waveform
 The test circuit shows a MOSFET switching an inductive load. The MOSFET gate is driven by a pulse generator through a resistor R_{G1}. The drain is connected to the inductive load and a DC supply V_{DS}. The MOSFET source is connected to ground through a resistor R_{G2}. The condition $R_{G1} = R_{G2}$ is specified. The drain current is labeled I_D.	 The waveform shows the current i and voltage V during diode recovery. Key parameters include: forward current I_F, reverse current I_{RRM}, reverse recovery time t_{rr} (divided into storage time t_s and fall time t_f), and reverse recovery charge Q_{rr} (divided into storage charge Q_s and fall charge Q_f). The total reverse recovery time is $t_{rr} = t_s + t_f$ and the total reverse recovery charge is $Q_{rr} = Q_s + Q_f$. The di/dt slope is indicated during both forward and reverse conduction. The voltage V shows the reverse recovery voltage V_{RRM} and the reverse recovery voltage V_{RRM} at 10% and 90% of I_{RRM}.

Table 18 Switching times

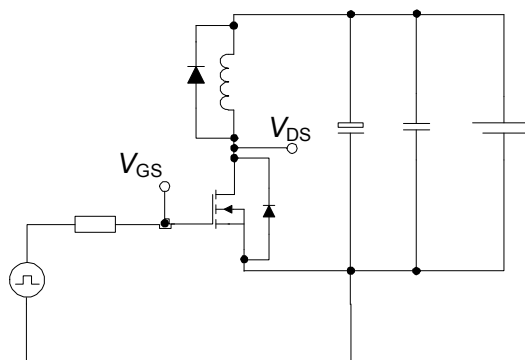
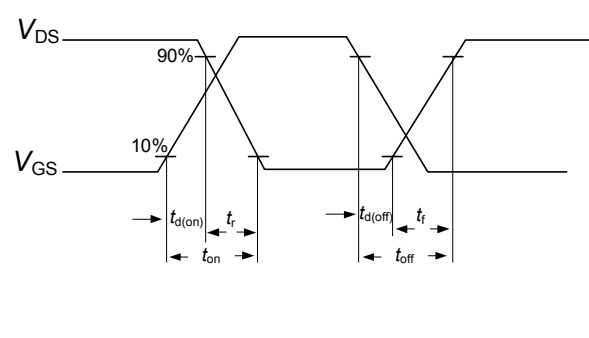
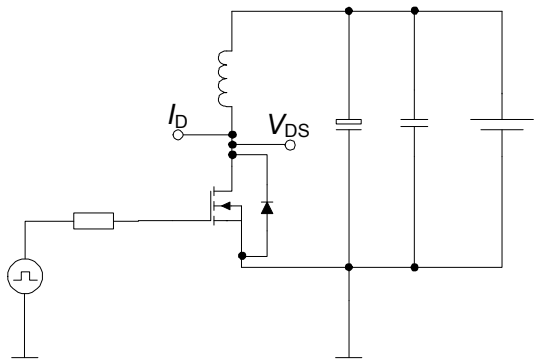
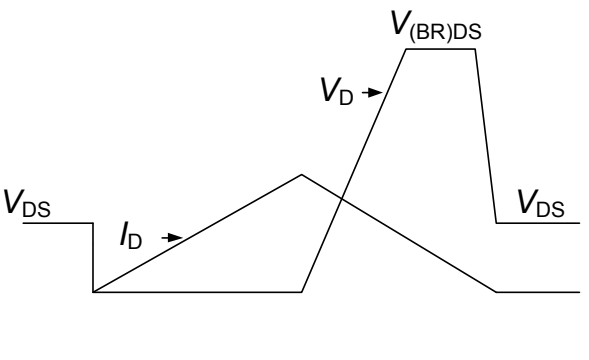
Switching times test circuit for inductive load	Switching times waveform
 The test circuit shows a MOSFET switching an inductive load. The MOSFET gate is driven by a pulse generator through a resistor. The drain is connected to the inductive load and a DC supply V_{DS}. The MOSFET source is connected to ground. The gate-source voltage is labeled V_{GS}.	 The waveform shows the switching times for the MOSFET. Key parameters include: turn-on time $t_{d(on)}$, rise time t_r, turn-off time $t_{d(off)}$, and fall time t_f. The gate-source voltage V_{GS} and drain-source voltage V_{DS} are shown. The turn-on and turn-off times are defined at 10% and 90% of the voltage levels.

Table 19 Unclamped inductive

Unclamped inductive load test circuit	Unclamped inductive waveform
 The test circuit shows a MOSFET switching an inductive load. The MOSFET gate is driven by a pulse generator through a resistor. The drain is connected to the inductive load and a DC supply V_{DS}. The MOSFET source is connected to ground. The drain current is labeled I_D.	 The waveform shows the unclamped inductive load. Key parameters include: drain-source voltage V_{DS}, drain current I_D, and the unclamped inductive voltage $V_{(BR)DS}$. The voltage V_{DS} is shown rising to $V_{(BR)DS}$ during the turn-off transient.

7 Package Outlines

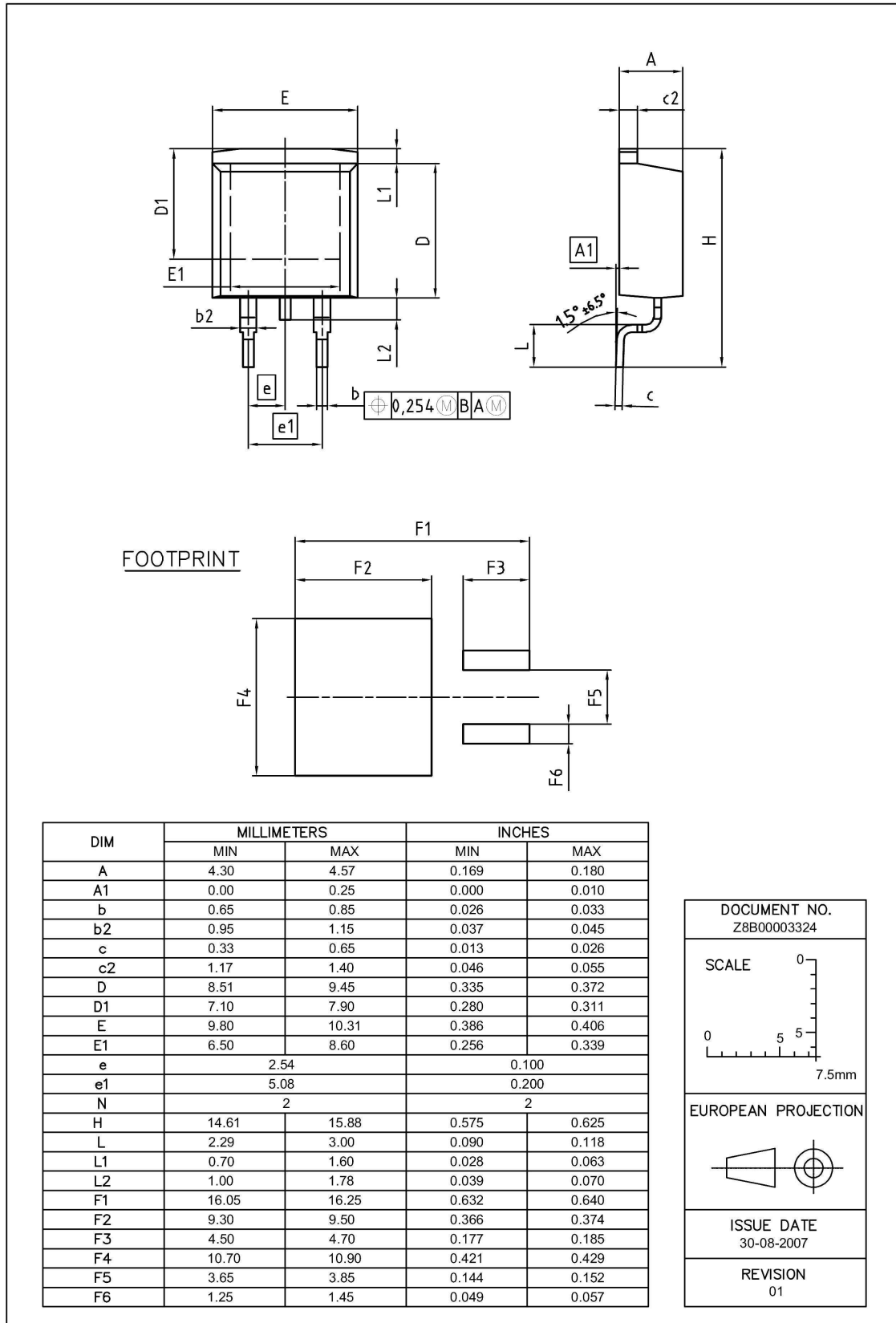


Figure 1 Outline PG-TO 263, dimensions in mm/inches

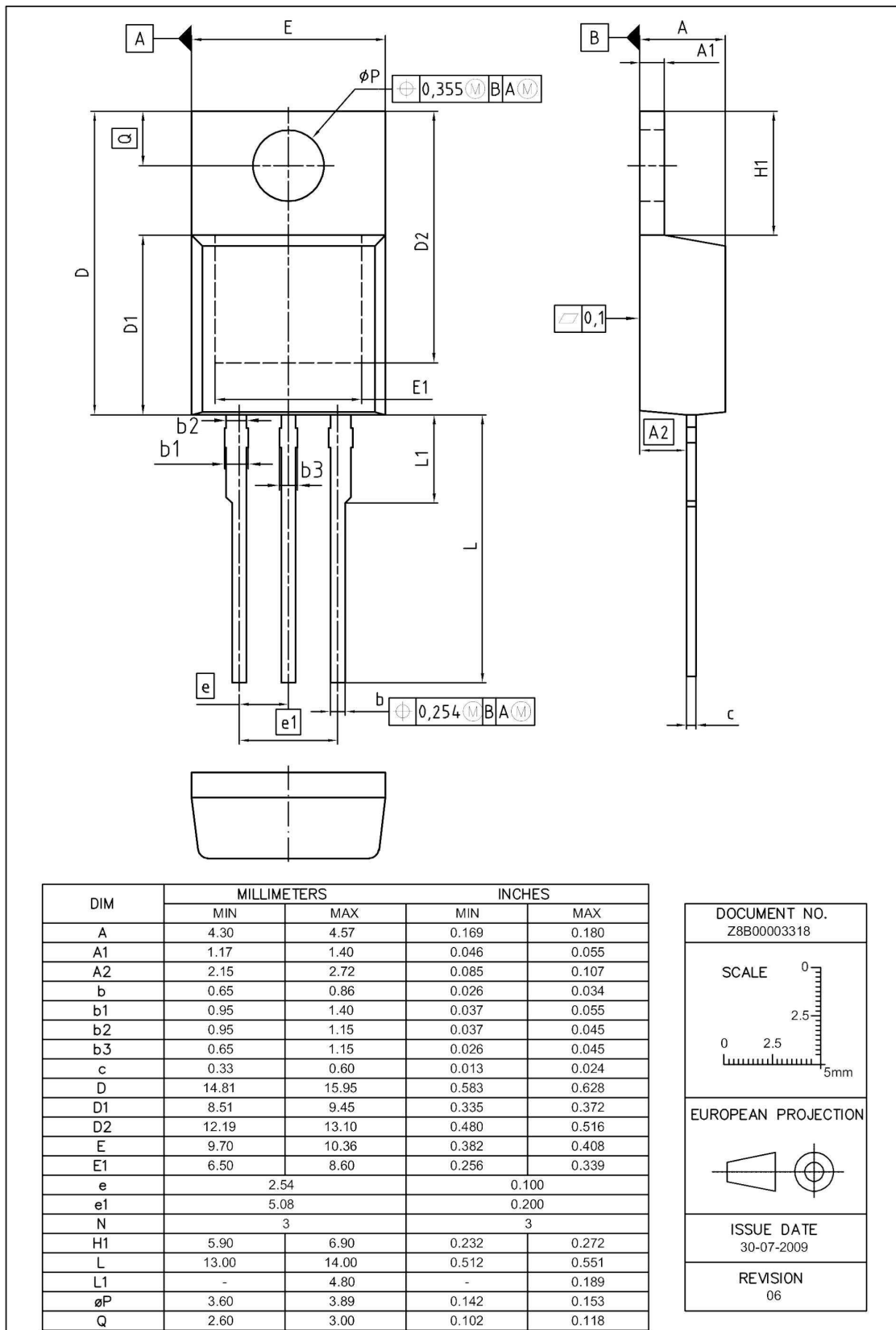


Figure 2 Outline PG-TO 220, dimensions in mm/inches

Revision History

IPB65R660CFDA, IPP65R660CFDA

Revision: 2012-03-28, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2012-03-28	Final datasheet

Disclaimer ATV

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