SmartLEWIS™ TRX

TDA5340

High Sensitivity Multi-Channel Transceiver

Data Sheet

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Wireless Sense & Control

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Revision History	
Page or Item	**Subjects (major changes since previous revisions)**
Revision 1.2, 13.06.2012	
Page 62	Package Outline Information added
Revision 1.1, 30.05.2012	
Page 40	Voltage at PA Pin changed to **Peak Voltage at pin RFOUT** with max 10% TX Duty Cycle
Page 40	Inserted maximum **Peak Voltage at pin RFOUT** with TX Duty Cycle above 10%
Page 40	Inserted maximum **DC Voltage at pin RFOUT**
Page 54	Inserted Definition for reception parameters

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1 Product Description

1.1 Overview

The IC is a low power ASK/FSK/GFSK Transceiver for the frequency bands 300-320, 415-495, 863-960 MHz. Bi-phase modulation schemes, like Manchester, bi-phase mark, bi-phase space and differential Manchester as well as NRZ are supported.

The chip offers a high level of integration and needs only a few external components, like a crystal, several blocking capacitors and the necessary matching elements. The IF-filter is integrated but depending on the performance requirements an external ceramic IF-filter can be used. For low cost applications an external passive antenna switch configuration can be used.

The device is qualified according to automotive quality standards and operates between -40 and +110 °C at supply voltage ranges of 3.0-3.6 Volts or 4.5-5.5 Volts.

A fully integrated Sigma-Delta Fractional-N PLL Synthesizer, with high frequency resolution and a crystal oscillator as reference, generates the necessary frequencies for the power amplifier or down conversion mixers. The on-chip temperature sensor may be utilized for temperature drift compensation of the crystal oscillator.

The receiver portion is realized as a double down conversion super-heterodyne / low-IF architecture each with image rejection supplemented by digital signal processing in the baseband. This architecture enables outstanding sensitivity performance in combination with very good blocking performance values.

The transmitter section comprises a class C/E power amplifier with a high efficiency and an output power level of up to 14 dBm. A tuning feature for the output power is possible via several switchable parallel output stages, of course matching to lower power levels is always possible. For higher power applications an external power amplifier can be used and the internal PA serves as a power driver. For ASK modulation a programmable data shaping is provided. With the fractional-N PLL synthesizer and a selectable Gaussian data shaping filter a very accurate and precise FSK modulation is achieved. The transmit data can be either stored in a separate FIFO data buffer or directly provided via the bus interface.

The receiver portion is able to scan autonomuosly for incoming data by using the self polling feature while the host micro controller can stay in power down mode, which reduces the system current consumption significanty.

The digital baseband processing unit together with the high performance downconverter is the key element for the exceptional sensitivity performance of the device which take it close to the theoretical top-performance limits. It comprises signal and noise detectors, matched data filter, clock and data recovery, data slicer and a format decoder. It demodulates the received ASK or FSK data stream and recovers the data clock out of the received data with very fast synchronziation times which can then be either accessed via separate pins or used for further processing like frame synchronization and intermediate storage in the on-chip FIFO.

The RSSI output signal is converted to the digital domain with an ADC. All these signals are accessible via the 4-wire SPI interface bus.

Up to 4 pre-configured telegram formats with different data rates and filter bandwidths can be stored into the device offering independent pre-processing of the received and transmitted data. The downconverter can be also configured to single-conversion mode at moderately reduced selectivity and image rejection performance but at the advantage of saving the external IF filter.

1.2 Key Features

Transceiver

- Multiband / Multichannel (300-320 MHz, 415-495 MHz, 863-960 MHz)
- High receiver sensitivity better than -116 dBm
- Power amplifier with up to 14 dBm output power
- Very Low Current consumption:
  - Receive Mode: 12 mA (typ)
  - Transmit Mode at 10 dBm and 434 MHz: 12 mA (typ)
  - Sleep Mode (XTAL ON): 40 uA (typ)
  - Deep Sleep Mode (XTAL OFF): 7 µA (typ)
  - Power down Mode: 0.9 uA (typ)
- ASK and FSK capability with programmable Gaussian data shaping
- 20 dB programable output power range
- On-chip IF filter with selectable bandwidth (optional an external CER-filter is possible)
- Sigma-delta fractional-N PLL synthesizer with high resolution
- Automatic Frequency Control function (AFC) for offset carrier frequency

Digital Baseband

- Multi protocol handling: Up to 4 parallel parameter sets for autonomous scanning and receiving from different sources
- Integrated data and clock recovery
- Autonomous receive functionality: Frame synchronisation, format decoding, message ID screening
- 288 Bit RX/TX-FIFO for receive and transmit data
- Wake-up generator and polling timer unit
- Ultra-fast wake-up on RSSI
- Supports all bi-phase format schemes and NRZ

General

- Operating temperature range -40 to +110°C
- Supply voltage range 3.0 to 3.6 V or 4.5 to 5.5 V
- Brownout detector
- Integrated 4-wire SPI bus interface
- 32-bit wide Unique ID on chip
- On-chip temperature sensor
- ESD protection +/- 2 kV on all pins (HBM)
- PG-TSSOP-28 package

1.3 Target Applications

- Remote keyless entry (RKE)
- Remote start applications
- Passive Keyless Entry (PKE)
- Security Alarm Systems
- Automatic Meter Reading (AMR) and Infrastructure (AMI)
- Home Automation
- Remote Control
- Sensor Networks
- Short range radio data transmission

1.4 Application Example

The Application examples within this section where optimezed for performance and sytem costs. Of course there exists several steps inbetween which can be realized by the customer to fullfill the application specific needs.

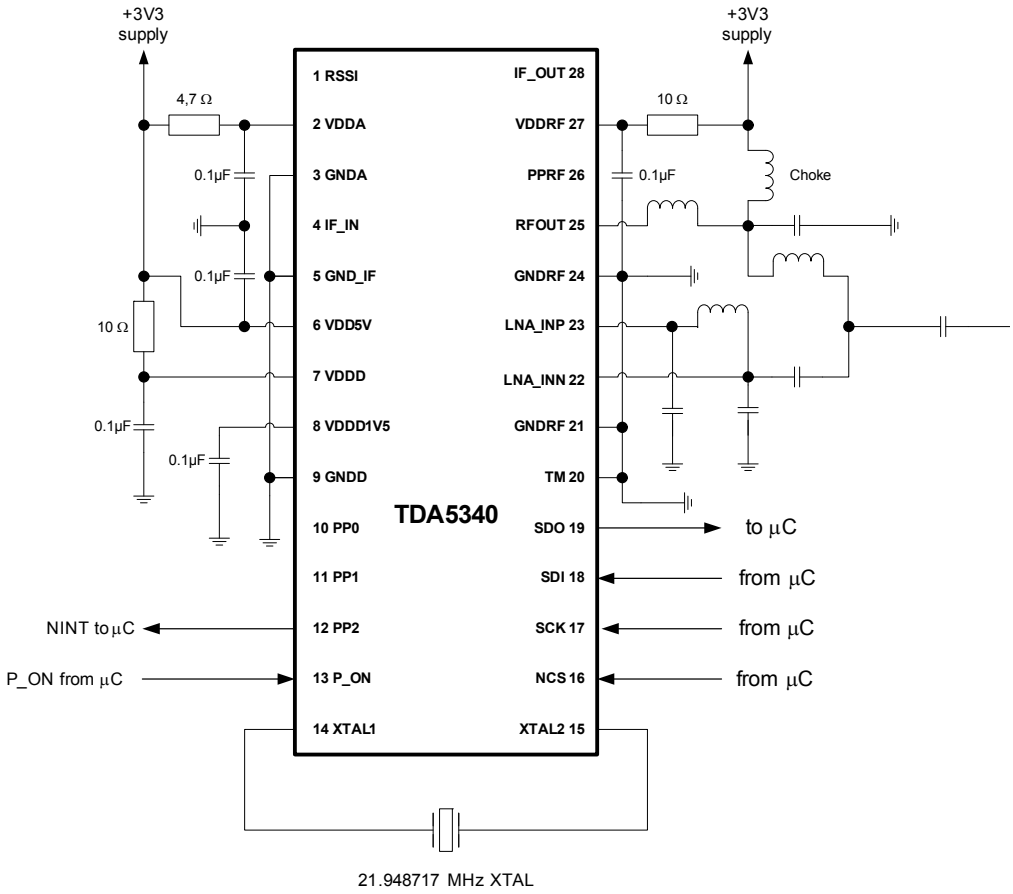


Figure 1 Application Example optimized for System Costs (3V3 Supply)

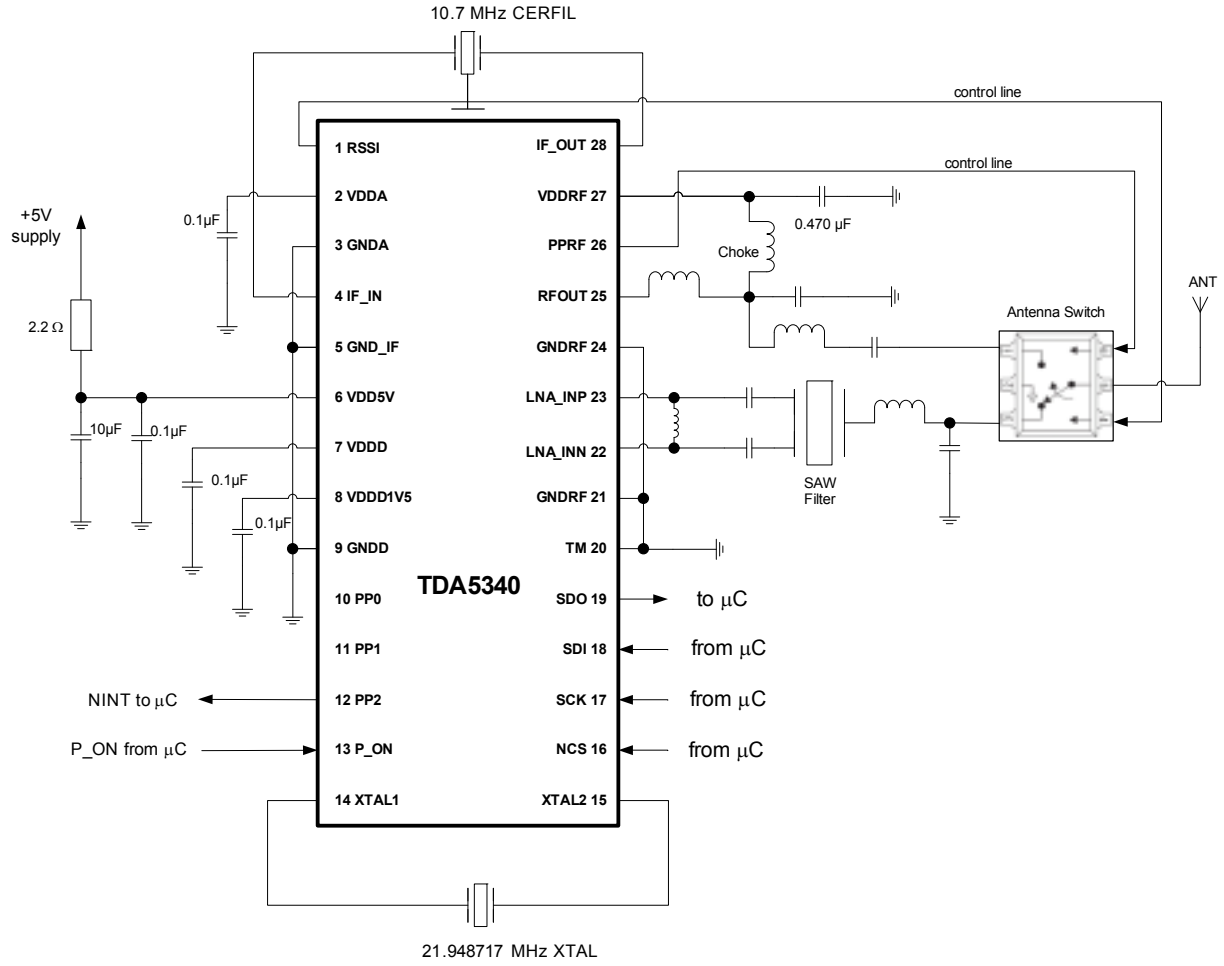


Figure 2 Application Example optimized for RF performance (5V Supply)

2 Functional Overview

2.1 Pin Configuration

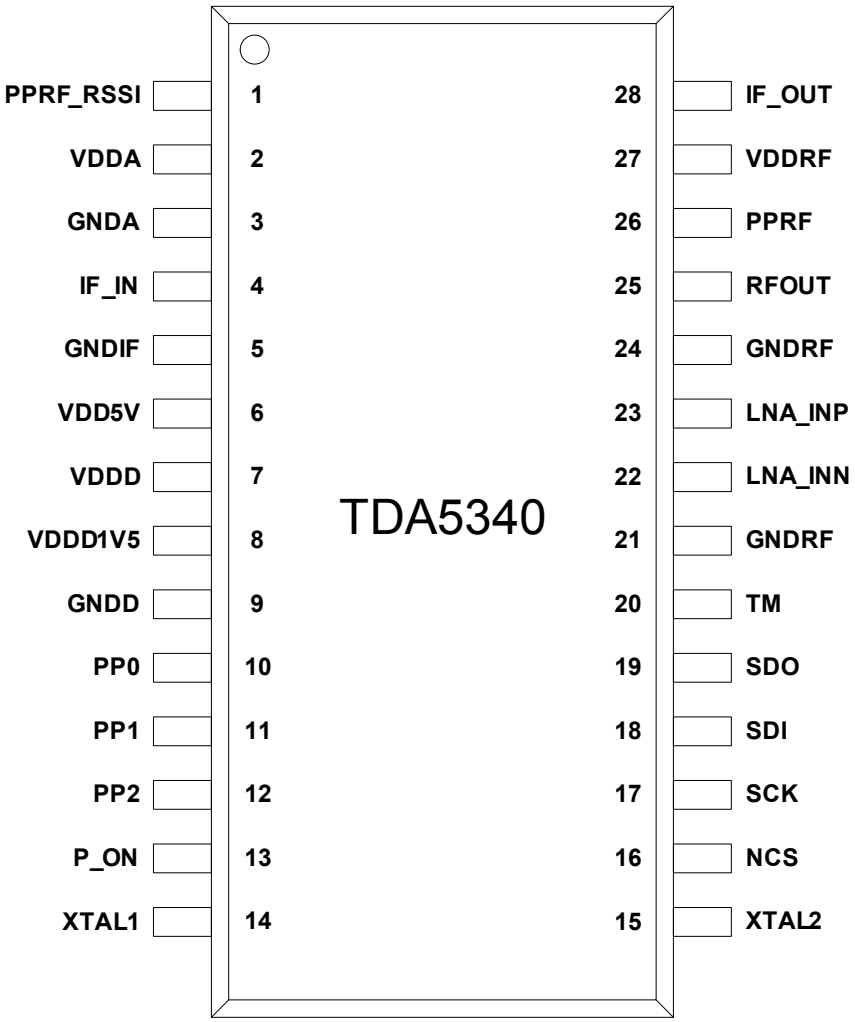


Figure 3 Pin-Out

2.1.1 Pin Definition

Table 1 Pin Definition and Function

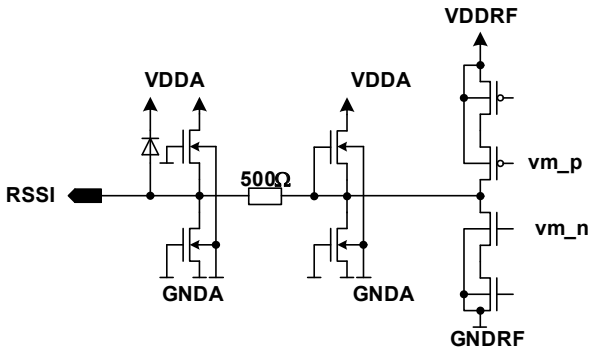
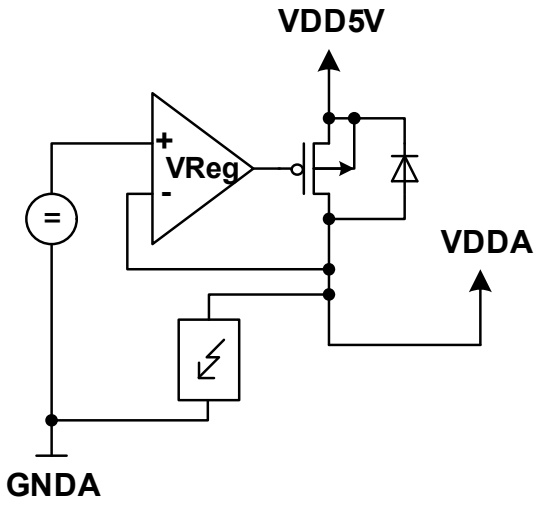
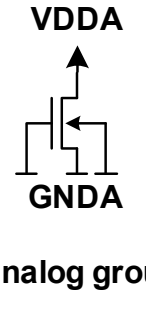
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
1	PPRF_RSSI		Analog output Digital output with weak driver capability, always in 3V domain CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: TRISTATE
2	VDDA		Analog input Analog supply
3	GNDA		Analog Ground

Table 1 Pin Definition and Function

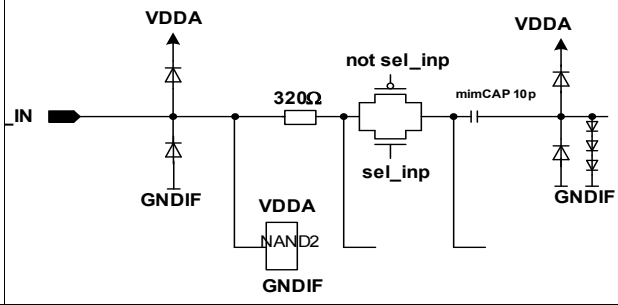
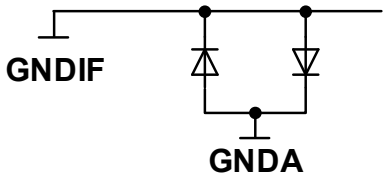
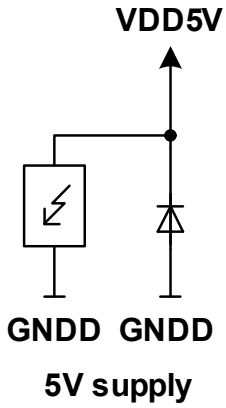
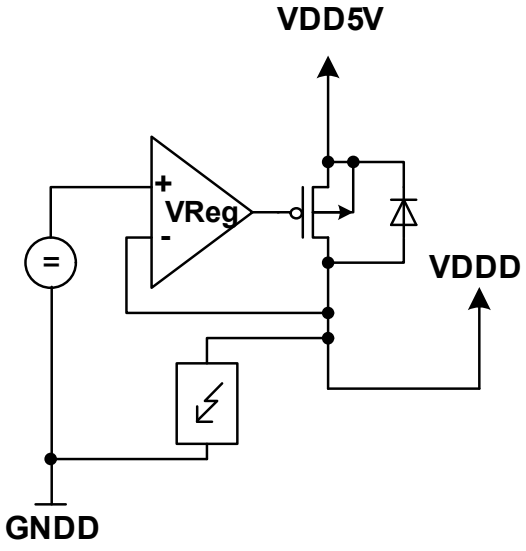
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
4	IF_IN		Analog input IF mixer input
5	GND_IF		Analog Ground
6	VDD5V		Analog input 5 Volt supply input
7	VDDD		Analog input digital supply input

Table 1 Pin Definition and Function

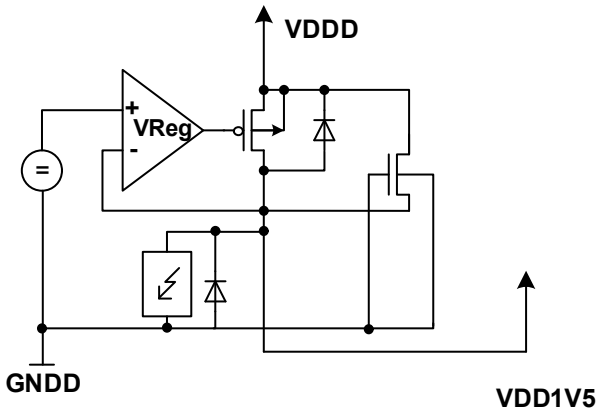
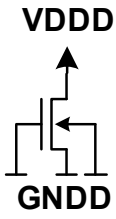
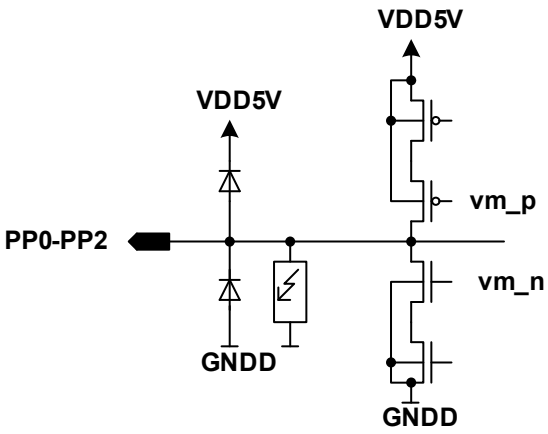
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
8	VDDD1V5		Analog output 1.5V regulator
9	GNDD		Digital ground
10	PP0		Digital output CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: CLK_OUT
11	PP1	same as PP0	Digital output CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: DATA

Table 1 Pin Definition and Function

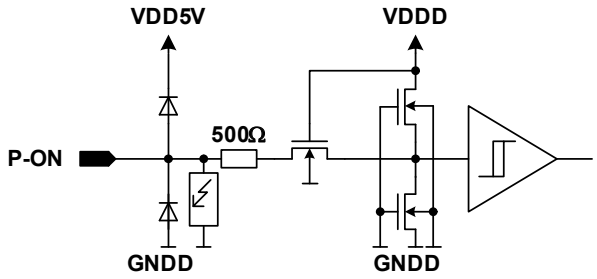
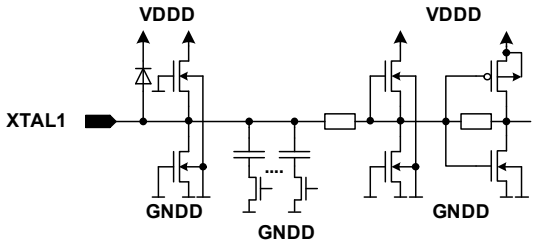
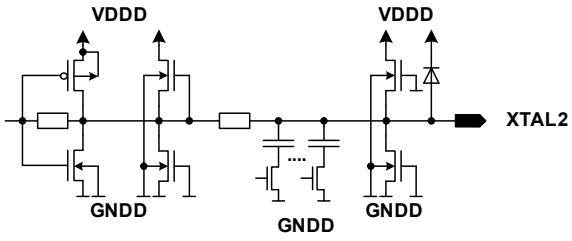
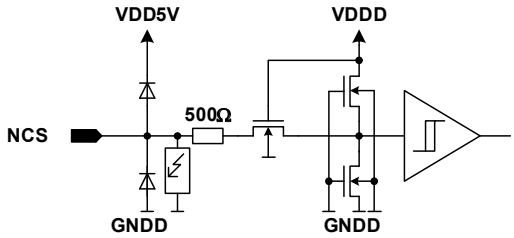
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
12	PP2	same as PP0	Digital output CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: NINT
13	P_ON		Digital input power-on reset
14	XTAL1		Analog input crystal oscillator input
15	XTAL2		Analog output crystal oscillator output
16	NCS		Digital input SPI Not Chip select

Table 1 Pin Definition and Function

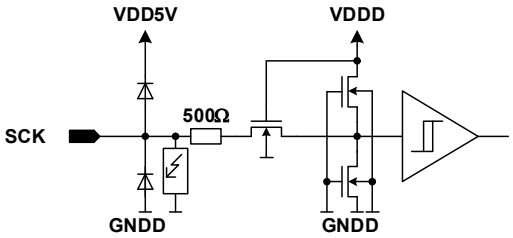
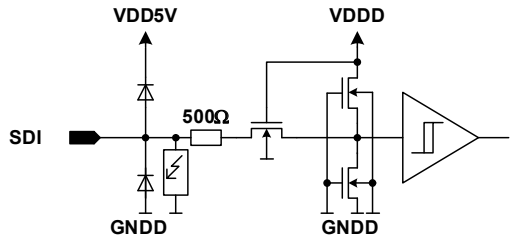
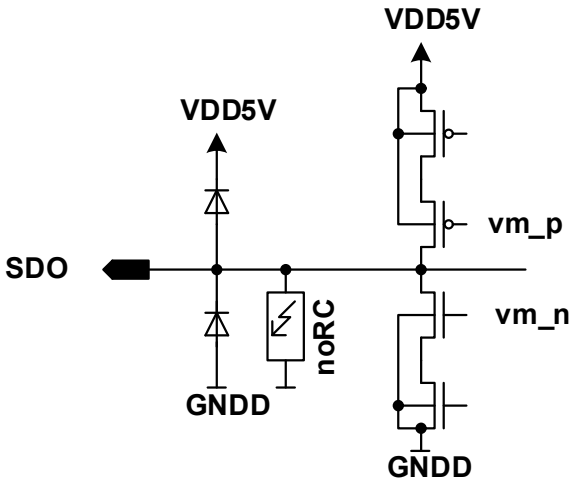
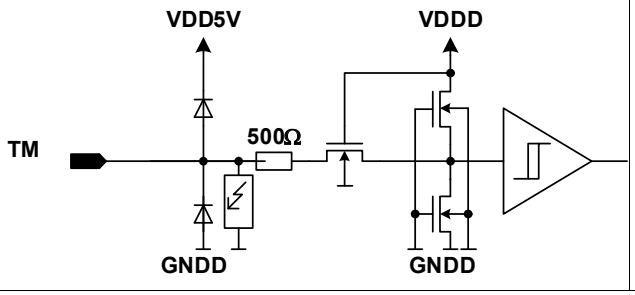
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
17	SCK		Digital input SPI clock
18	SDI		Digital input SPI data in
19	SDO		Digital output SPI data out
20	TM		Digital input connect to digital ground

Table 1 Pin Definition and Function

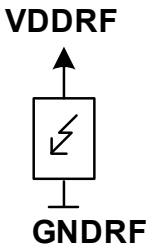
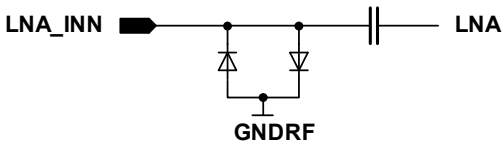
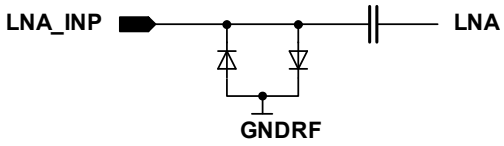
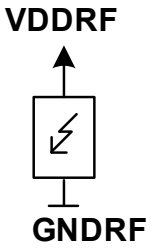
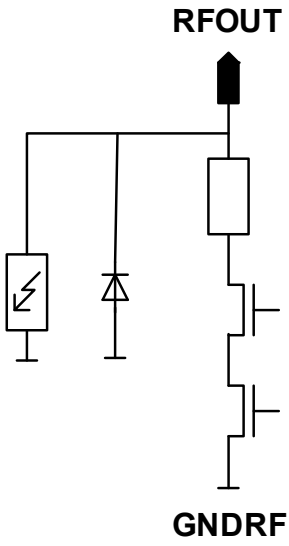
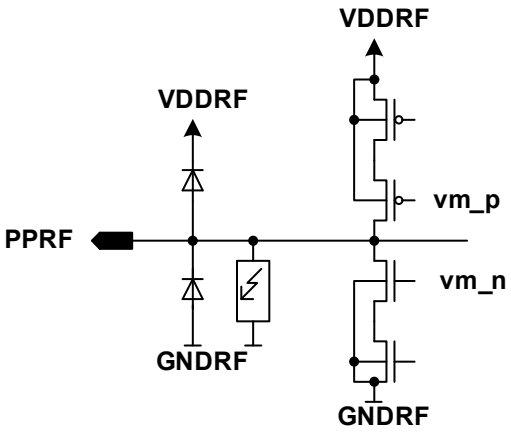
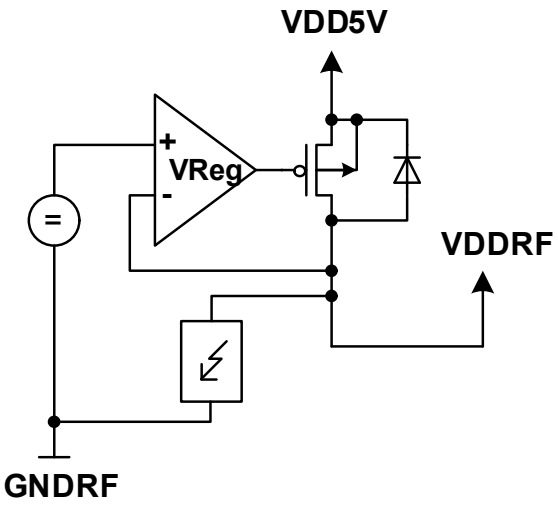
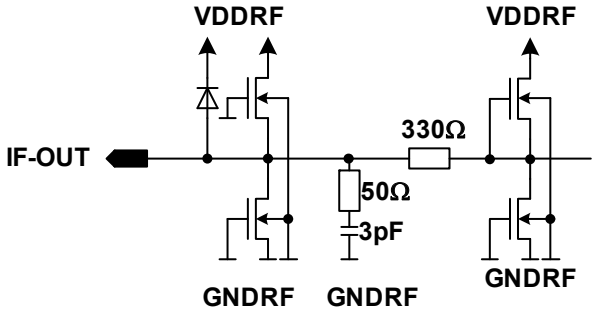
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
21	GNDRF		Analog ground
22	LNA_INN		Analog input - RF input
23	LNA_INP		Analog input +RF input
24	GNDRF		Analog ground
25	RFOUT		Analog output power amplifier output

Table 1 Pin Definition and Function

Pin Nr	Pad Name	Equivalent I/O Schematic	Function
26	PPRF		Digital output always in 3V domain CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: TRISTATE
27	VDDRF		Analog input RF supply
28	IF_OUT		Analog output Mixer output

2.2 Functional Block Diagram

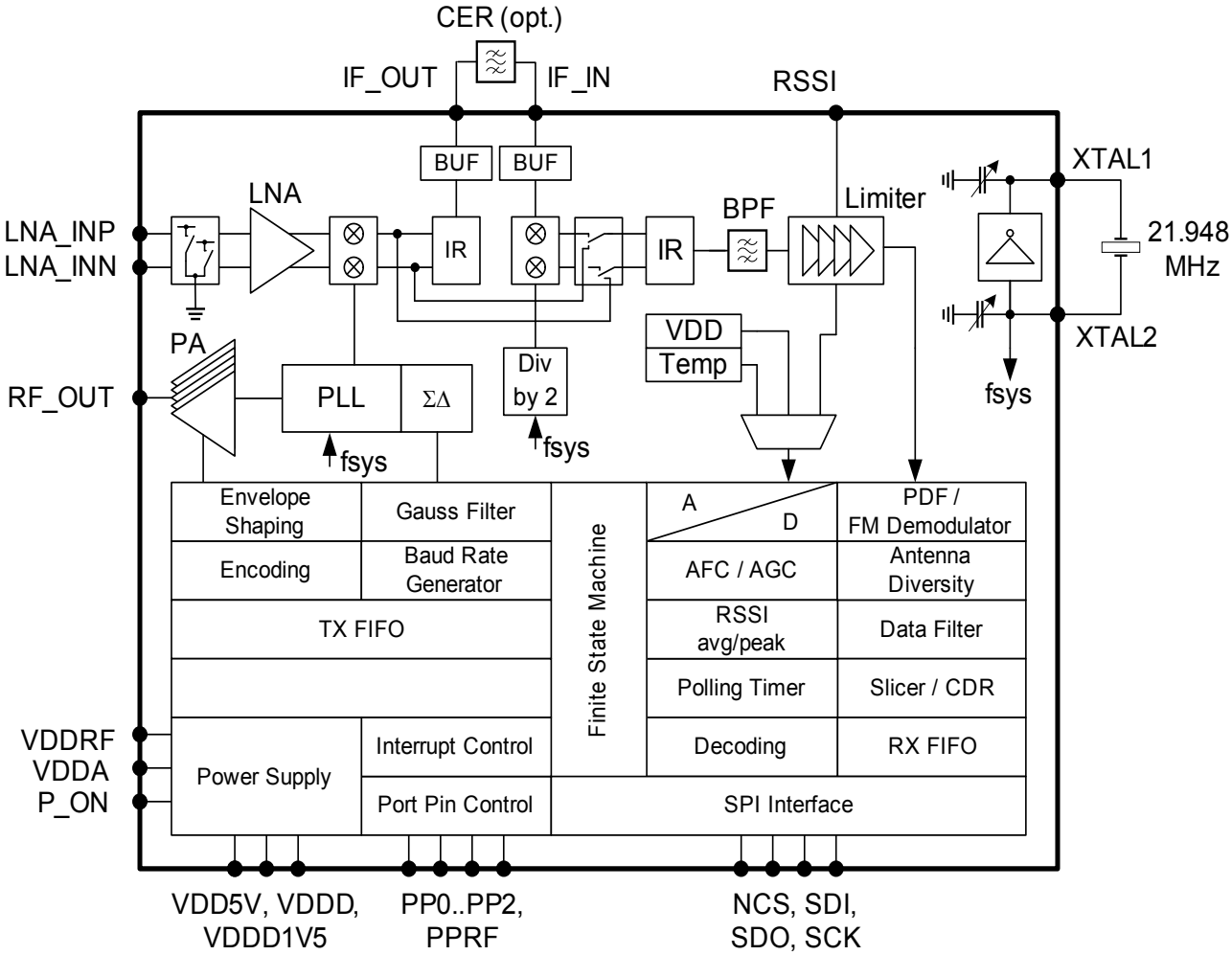


Figure 4 TDA5340 Block Diagram

2.3 Architecture Overview

A fully integrated Sigma-Delta Fractional-N PLL Synthesizer covers the frequency bands 300-320 MHz, 415-495 MHz, 860-960 MHz with a high frequency resolution, using only one VCO running at around 3.6 GHz. This makes the IC most suitable for Multi-Band/Multi-Channel applications. For Multi-Channel applications a very good channel separation is essential. To achieve the necessary high sensitivity and selectivity a double down conversion super-heterodyne architecture is used. The first IF frequency is located at 10.7 MHz and the second IF frequency at 274 kHz. For both IF frequencies an adjustment-free image frequency rejection feature is realized. In the second IF domain the filtering is done with an on-chip third order bandpass polyphase filter. A multi-stage bandpass limiter completes the RF/IF path of the receiver. For Single-Channel applications with relaxed requirements to selectivity, a single down conversion low-IF scheme can be selected.

A highly efficient Class C/E Power amplifier with an output level of +14dBm combined with a Gaussian Filter for GFSK and amplitude ramping functions for shaped ASK is implemented. A high resolution power adjustment can be done to trim the output power for highest system power savings. The data can be either shifted out of a on-chip transmit FIFO or directly provided on an input pin.

An RSSI generator delivers a DC signal proportional to the applied input power and is also used as an ASK demodulator. Via an anti-aliasing filter this signal feeds an ADC with 10 bits resolution. The limiter output signal

feeds a digital FSK demodulator. This block demodulates the FSK data and delivers an AFC signal which controls the divider factor of the PLL synthesizer. A digital receiver, which comprises RSSI peak detectors, a matched data filter, a clock and data recovery, a data slicer, a frame synchronization and a data FIFO, decodes the received ASK or FSK data stream. The recovered data and clock signals are accessible via 2 separate pins. The FIFO data buffer is accessible via the SPI bus interface.The crystal oscillator serves as the reference frequency for the PLL phase detector, the clock signal of the Sigma-Delta modulator and divided by two as the 2nd local oscillator signal. To accelerate the start up of the crystal oscillator two modes are selectable: a Low Power Mode (with lower precision) and a High Precision Mode.

2.4 Block Overview

The TDA5340 is separated into the following main blocks:

- RF / IF Receiver
- Power Amplifier
- Crystal Oscillator and Clock Divider
- Sigma-Delta Fractional-N PLL Synthesizer
- ASK / FSK Demodulator incl. AFC and AGC
- RSSI Peak Detector
- Digital Baseband Receiver
- Digital Baseband Transmitter
- Power Supply Circuitry
- System Interface
- System Management Unit

2.5 Operating Modes

The transceiver has three different power saving modes, two receive modes and a transmit mode. The different operating modes are used to adjust the transceiver functionality to the needs of the application. Depending on the used communication protocols the appropriate power saving mode can be selected. In the table below all different modes are listed and corresponding to the modes the active blocks and current consumptions are shown.

Table 2 Operating Modes

Operating Mode	Transceiver Blocks								typ. Current Consumption
	Dig. Vreg	Ana. Vreg	XTAL	SFR	SPI	PLL	PA	RX	
Power Down	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0.9 µA
Deep Sleep	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	7 µA
Sleep	ON	OFF	ON[1)]	ON	ON	OFF	OFF	OFF	40 µA[2)]
Sleep ADC enabled	ON	ON	ON[1)]	ON	ON	OFF	OFF	OFF	1 mA
Transmit Ready	ON	ON	ON	ON	ON	ON	OFF	OFF	5.8 mA
Transmit Idle	ON	ON	ON	ON	ON	OFF	OFF	OFF	<3 mA
Transmit	ON	ON	ON	ON	ON	ON	ON	OFF	12.5 mA[3)]
Receive	ON	ON	ON	ON	ON	ON	OFF	ON	11 mA[4)]

1) selectable between XTAL in high or low precision mode
2) XTAL in low precision mode
3) 10dBm Output power at 434MHz
4) single down conversion Mode (no external CER Filter used)

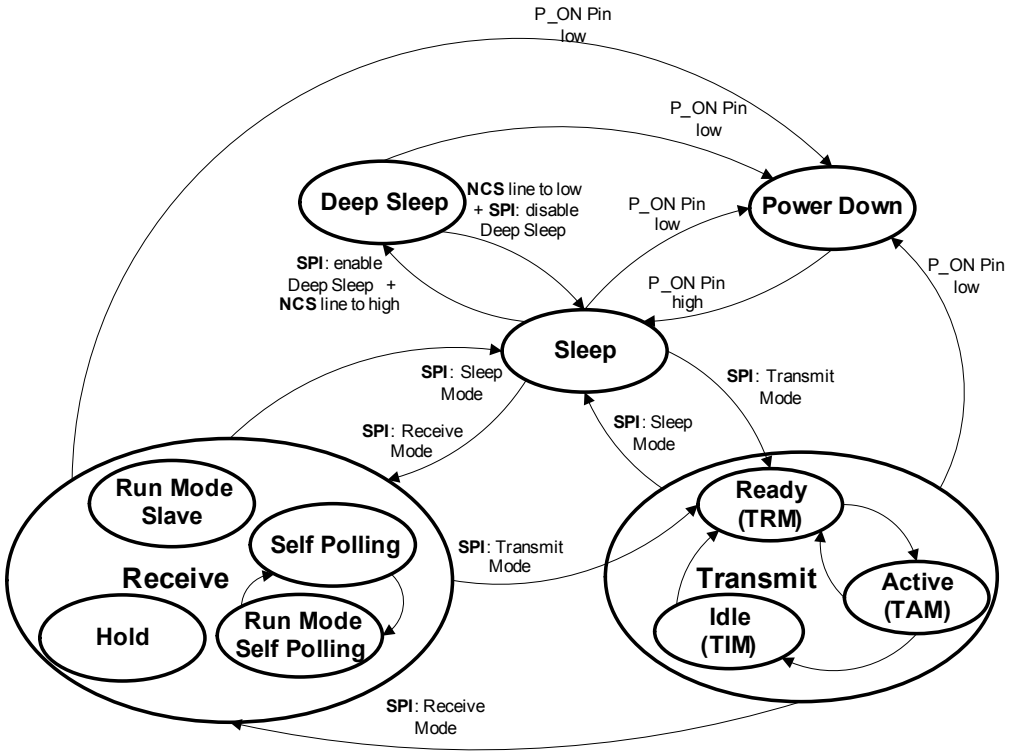


Figure 5 Main State Diagram

2.6 Block Description

2.6.1 Power Supply Circuitry

The chip may be operated within a 5 Volts or a 3.3 Volts environment.

For operation within a 5 Volts environment (supply voltage range 1), the chip is supplied via the VDD5V pin. In this configuration the digital I/O pads are supplied via VDD5V and a 5 V to 3.3 V voltage regulator supplies the analog/RF section (only active in Run Modes). When operating within a 3.3 Volts environment (supply voltage range 2), the VDD5V, VDDA, VDDD and VDDRF pins must be supplied. The 5 V to 3.3 V voltage regulators are inactive in this configuration.The internal digital core is supplied by an additional 3.3 V to 1.5 V regulator.The regulators for the digital section are controlled by the signal at P_ON (Power On) pin. A low signal at P_ON disables all regulators and set the IC in Power Down Mode. A low to high transition at P_ON enables the regulators for the digital section and initiates a power on reset. The regulator for the analog section is controlled by the Master Control Unit and is active only when the RF section is active.To provide data integrity within the digital units, a brownout detector monitors the digital supply. In case a voltage drop of VDDD below approximately 2.45 V is detected a RESET will be initiated. A typical power supply application for a 3.3 Volts and a 5 Volts environment is shown in the figure below.

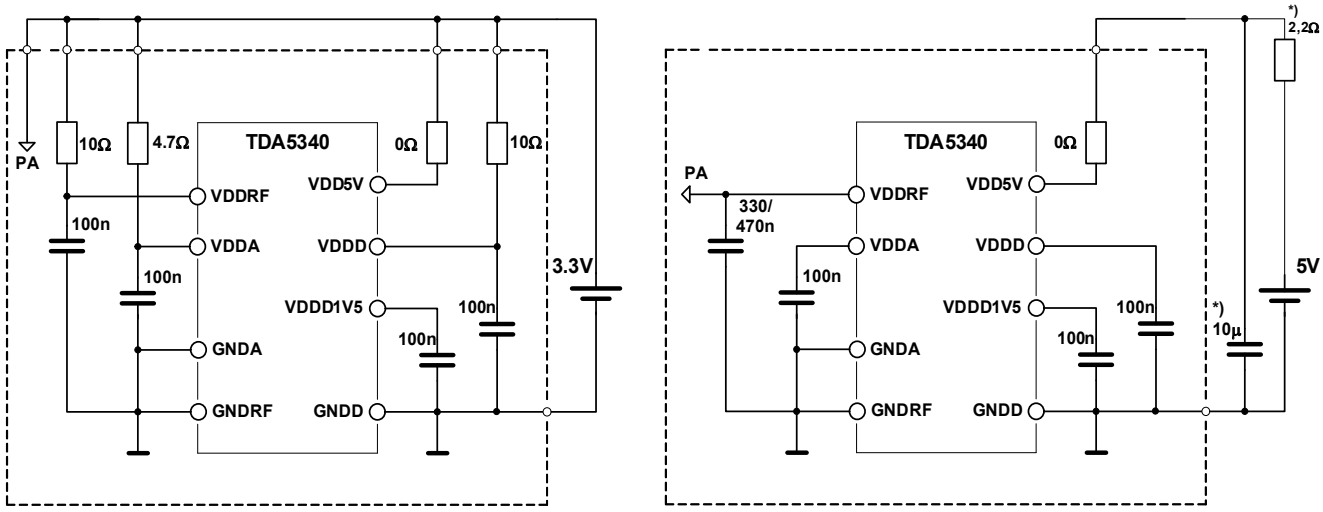


Figure 6 3.3 Volts and 5 Volts Applications

2.6.2 Chip Reset

Power down and power on are controlled by the P_ON pin. A LOW at this pin keeps the IC in Power Down Mode. All voltage regulators and the internal biasing are switched off. A high transition at P_ON pin activates the appropriate voltage regulators and the internal biasing of the chip. A power up reset is generated at the same time.

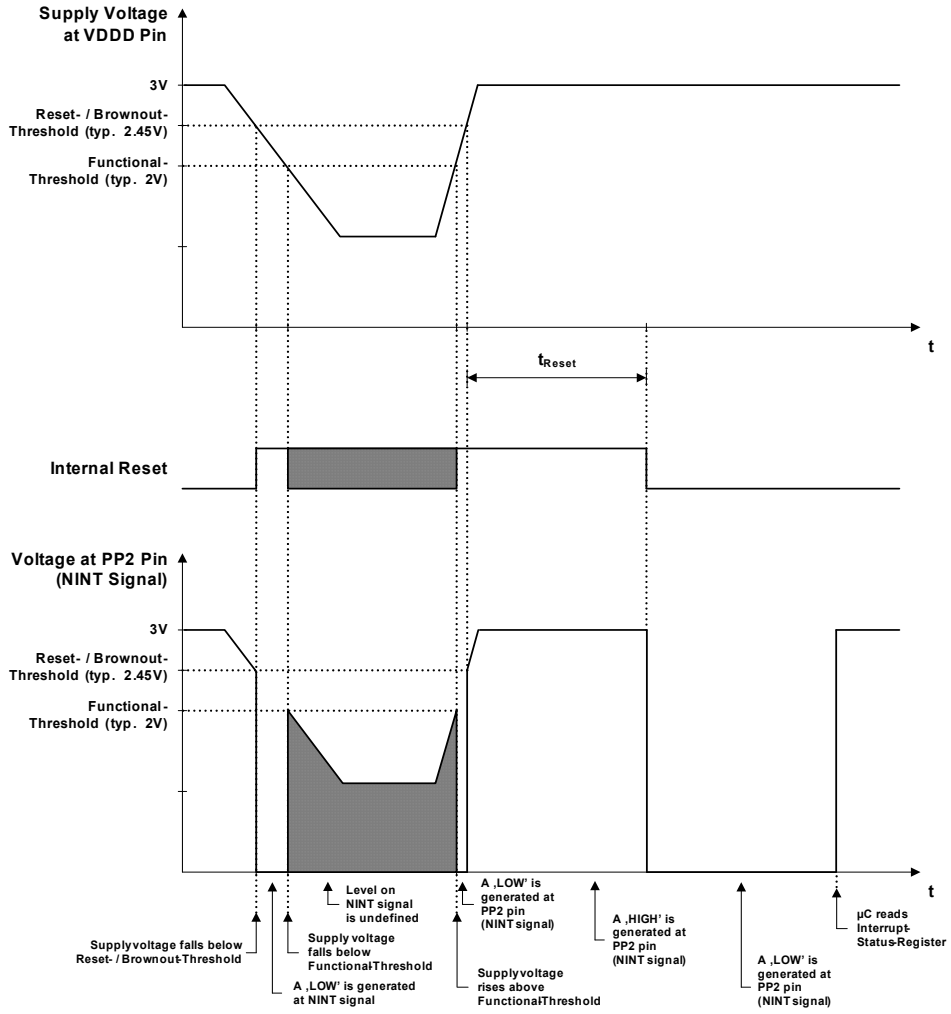


Figure 7 Reset Behavior

A second source that can trigger a reset is a brownout event. Whenever the integrated brownout detector measures a voltage drop below the brownout threshold on the digital supply, the integrity of the stored data and configuration can no longer be guaranteed; thus a reset is generated. While the supply voltage stays between the brownout and the functional threshold of the chip, the NINT signal is forced to low. When the supply voltage drops below the functional threshold, the levels of all digital output pins are undefined. When the supply voltage raises above the brownout threshold, the IC generates a high pulse at NINT and remains in the reset state for the duration of the reset time. When the IC leaves the reset state, the Interrupt Status registers are set to 0xFF and the NINT signal is forced to low. Now, the IC starts operation in the SLEEP Mode, ready to receive commands via the SPI interface. The NINT signal will go high, when one of the Interrupt Status registers is read for the first time.

2.6.3 RF / IF Receiver

The receiver path uses a double down conversion super-heterodyne/low-IF architecture, where the first IF frequency is located at 10.7 MHz and the second IF frequency at 274 kHz. For the first IF frequency an adjustment-free image frequency rejection is realized by means of two I/Q-mixers followed by a second order passive polyphase filter centered at 10.7 MHz (PPF). The I/Q-oscillator signals for the first down conversion are delivered from the PLL synthesizer. The frequency selection in the first IF domain is done by an external CER filter. For moderate or low performance applications, this ceramic filter can be substituted by a simple LC Pi-filter or completely by-passed using the receiver as a single down conversion low-IF scheme with 274 kHz IF frequency.

The down conversion to the second IF frequency is done by means of two high-side injected I/Q-mixers together with an on-chip third order bandpass polyphase filter (PPF2 + BPF). The I/Q-oscillator signals for the second down conversion are directly derived by division of two from the crystal oscillator frequency. The bandwidth of the bandpass filter (BPF) can be selected from 50 kHz to 300 kHz in 5 steps. For a frequency offset of 150 kHz to 120 kHz, the AFC (Automatic Frequency Control) function is mandatory. Activated AFC option might require a longer preamble sequence in the receive data stream.

The receiver enable signal (RX_RUN) can be offered at each of the port pins to control external components. Whenever the receiver is active, the RX_RUN output signal is active. Active high or active low is configurable via PPCFG2 register.

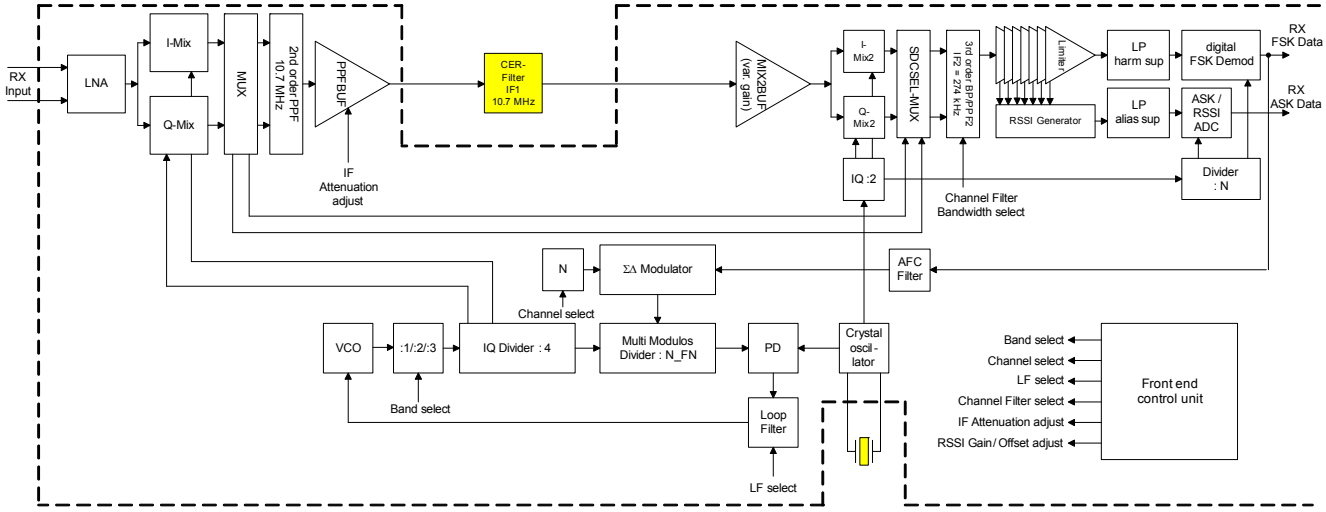


Figure 8 Block Diagram RF Receiver Section

2.6.4 Transmitter

A highly efficient Class C/E Power amplifier with output levels of +14 dBm combined with a Gaussian Filter for GFSK and amplitude ramping functions for shaped ASK is implemented. A high resolution power adjustment can be done to trim the output power for highest system power savings. The data can be either shifted out of a on-chip transmit FIFO or directly provided on an input pin.

2.6.5 Crystal Oscillator and Clock Divider

The crystal oscillator is a Pierce type oscillator. An automatic amplitude regulation circuitry allows the oscillator to operate with minimum current consumption. In SLEEP Mode, where the current consumption should be as low as possible, the load capacitor must be small and the frequency is slightly detuned, therefore all internal trim capacitors are disconnected. The internal capacitors are controlled by the crystal oscillator calibration registers XTALCALx. With a binary weighted capacitor array the necessary load capacitor can be selected.

Whenever a XTALCALx register value is updated, the selected trim capacitors are automatically connected to the crystal so that the frequency is precise at the specified value. Step size is 1 pF. The SFR control bit XTALHPMS can be used to activate the High Precision Mode also during SLEEP Mode.

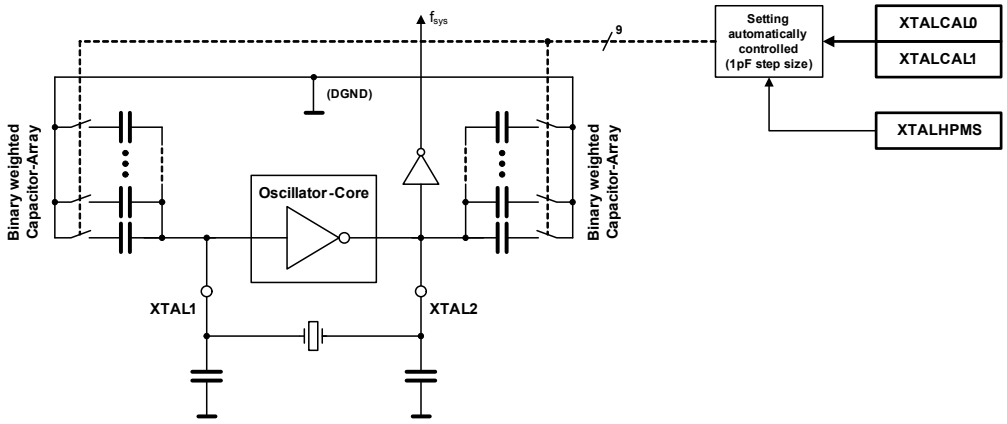


Figure 9 Crystal Oscillator

External Clock Generation Unit

A built-in programmable frequency divider can be used to generate an external clock source out of the crystal reference. The 20 bit wide division factor is stored in the registers CLKOUT0, CLKOUT1 and CLKOUT2. The minimum value of the programmable frequency divider is 1. This programmable divider is followed by an additional divider by 2, which generates a 50% duty cycle of the CLK_OUT signal. So the maximum frequency at the CLK_OUT signal is the crystal frequency divided by 4. The minimum CLK_OUT frequency is the crystal frequency divided by 2^{21}.

To save power, this programmable clock signal can be disabled by the SFR control bit CLKOUTEN. In this case the external clock signal is set to low.

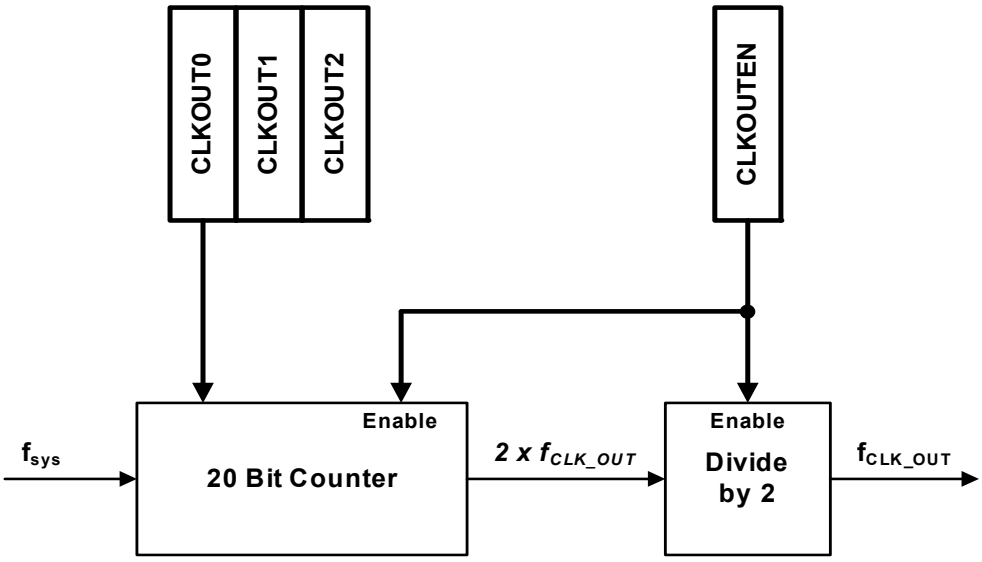


Figure 10 External Clock Generation Unit

2.6.6 Sigma-Delta Fractional-N PLL Block

The Sigma-Delta Fractional-N PLL is fully integrated on chip. The Voltage Controlled Oscillator (VCO) with on-chip LC-tank runs at approximately 3.6 GHz and is first divided with a band select divider by 1, 2 or 3 and then with an I/Q-divider by 4 which provides an orthogonal local oscillator signal for the first image reject mixer with the necessary high accuracy.

The multi-modulus divider determines the channel selection and is controlled by a 3rd order Sigma-Delta Modulator (SDM). A type IV phase detector, a charge pump with programmable current and an on-chip loop filter closes the phase locked loop.

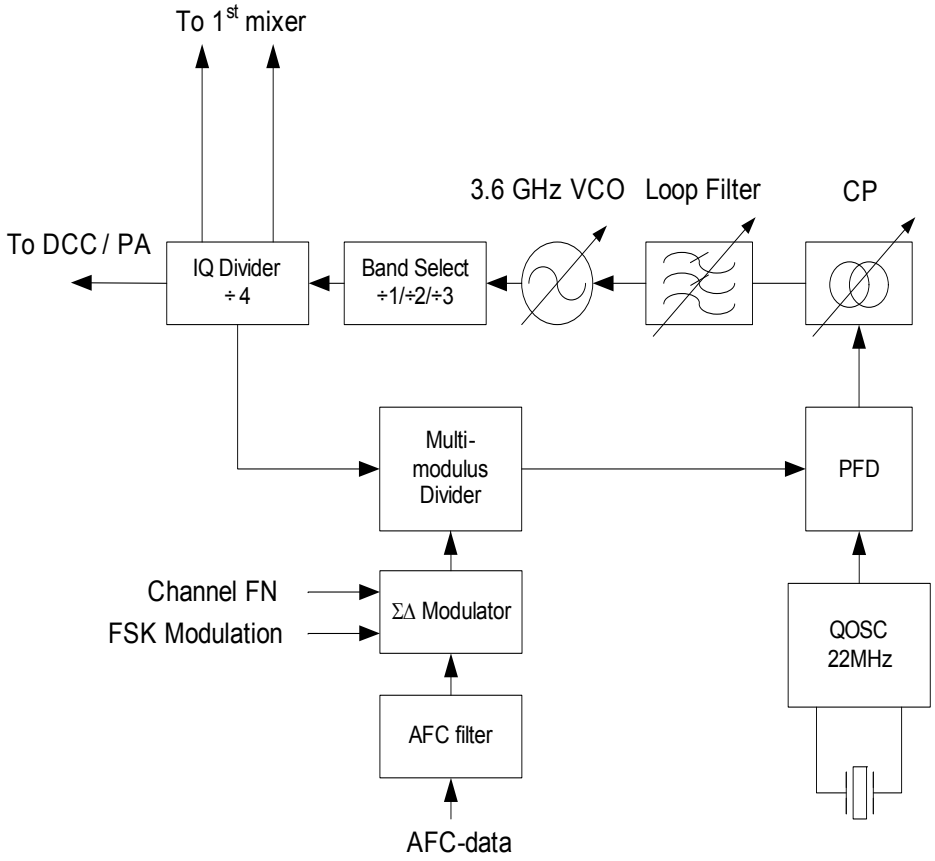


Figure 11 Synthesizer Block Diagram

2.6.6.1 PLL Dividers

The divider chain consists of a band select divider 1/2/3, an I/Q-divider by 4 which provides an orthogonal 1st local oscillator signal for the first image reject mixer with the necessary high accuracy and a multi-modulus divider controlled by the Sigma-Delta Modulator. With the band select divider, the wanted frequency band is selected. Divide by 1 selects the 915 MHz and 868 MHz band, divide by 2 selects the 434 MHz band and divide by 3 selects the 315 MHz band. The ISM band selection is done via bit group BANDSEL in x_PLLINTC1 register.

2.6.6.2 Digital Modulator

The 3rd order Sigma-Delta Modulator (SDM) has a 22 bit wide input word, however the LSB is always high, and is clocked by the XTAL oscillator. This determines the achievable frequency resolution.

The Automatic Frequency Control (AFC) Unit filters the actual frequency offset from the FSK demodulator data and calculates the necessary correction of the divider factor to achieve the nominal IF center frequency.

2.6.7 Decoding/Encoding Modes

The IC supports the following Bi-phase encodings:

- Manchester code
- Differential Manchester code

- Bi-phase space code
- Bi-phase mark code
- Miller code (TX only)
- NRZ

The encoding mode is set and enabled by bit group CODE in x_DIGRXC (receiver) and x_TXCFG (transmitter) configuration register.

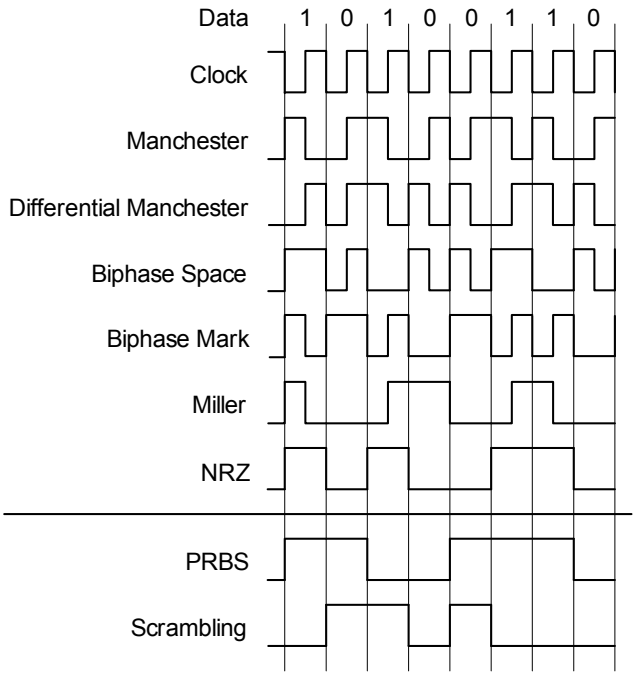


Figure 12 Encoding/Decoding Schemes

2.6.8 ASK and FSK Demodulator

The IC comprises two separate demodulators for ASK and FSK.

After combining FSK and ASK data path, a sampling rate adaptation follows to meet an output oversampling between 8 and 16 samples per chip. Finally, an oversampling of 8 samples per chip can be achieved using a fractional sample rate converter (SRC) with linear interpolation

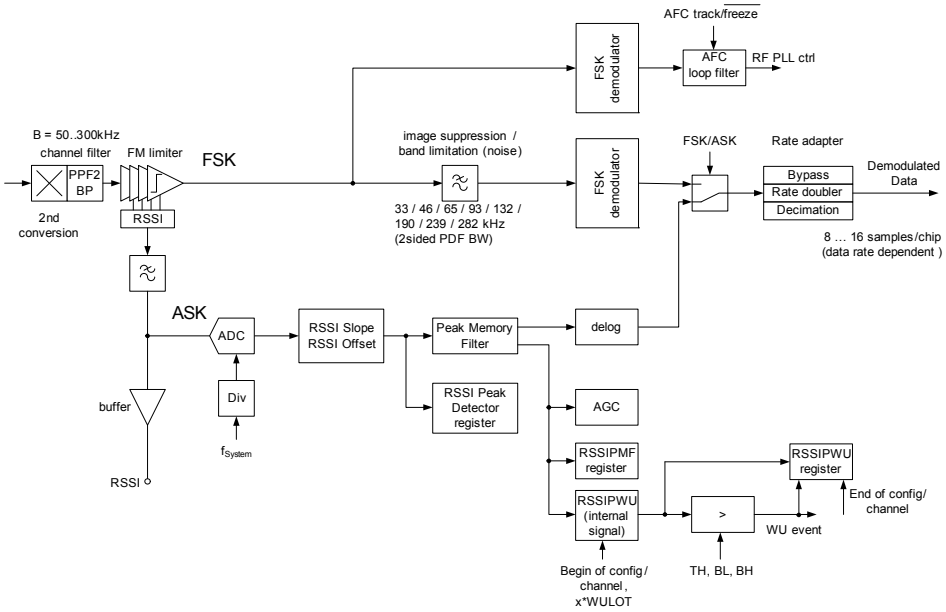


Figure 13 Functional Block Diagram ASK/FSK Demodulator

2.6.8.1 ASK Demodulator

The RSSI generator delivers a DC signal proportional to the applied input power at a logarithmic scale (dBm) and is also used as an ASK demodulator. Via a programmable anti-aliasing filter this signal is converted to the digital domain by means of a 10-bit ADC. For the AM demodulation a signal proportional to the linear power is required. Therefore a conversion from logarithmic scale to linear scale is necessary. This is done in the digital domain by a nonlinear filter together with an exponential function. The analog RSSI signal after the anti-aliasing filter is available at the RSSI pin via a buffer amplifier. To enable this buffer the SFR control bit RSSIMONEN must be set. The anti-aliasing filter can be by-passed for visualization on the RSSI pin (see AAFBYP control bit).

2.6.8.2 FSK Demodulator

The limiter output signal, which has a constant amplitude over a wide range of the input signal, feeds the FSK demodulator. There is a configurable lowpass filter in front of the FSK demodulation to suppress the down conversion image and noise/limiter harmonics (FSK Pre-Demodulation Filter, PDF). This is realized as a 3rd order digital filter. The sampling rate after FSK demodulation is fixed and independent from the target data rate.

2.6.8.3 Automatic Frequency Control Unit (AFC)

In front of the image suppression filter a second FSK demodulator is used to derive the control signal for the Automatic Frequency Control Unit, which is actually the DC value of the FSK demodulated signal. This makes the AFC loop independent from signal path filtering and allow so a wider frequency capture range of the AFC. The derivation of the AFC control signal is preferably done during the DC-free preamble and is then frozen for the rest of the datagram.

Since the digital FSK demodulator determines the exact frequency offset between the received input frequency and the programmed input center frequency of the receiver, this offset can be corrected through the sigma delta control of the PLL.

2.6.8.4 Digital Automatic Gain Control Unit (AGC)

Automatic Gain Control (AGC) is necessary mainly because of the limited dynamic range of the on-chip bandpass filter (BPF). The BPF dynamic range reduces to less than 60dB in case of minimum BPF bandwidth.

AGC is used to cover the following cases:

- 1. ASK demodulation at large input signals
- 2. RSSI reading at large input signals
- 3. Improve IIP3 performance in either FSK or ASK mode

The 1st IF buffer can be fine tuned "manually" by means of 4 bits thus optimizing the overall gain to the application (attenuation of 0dB to -12dB by means of IFATT0 to IFATT15). This buffer allows the production spread of external components to be trimmed.

The gain of the 2nd IF path is set to three different values by means of an AGC algorithm. Depending on whether the receiver is used in single down conversion or in double down conversion mode the gain control in the 2nd IF path is either after the 2nd poly-phase network or in front of the 2nd mixer.

The AGC action is illustrated in the RSSI curve below:

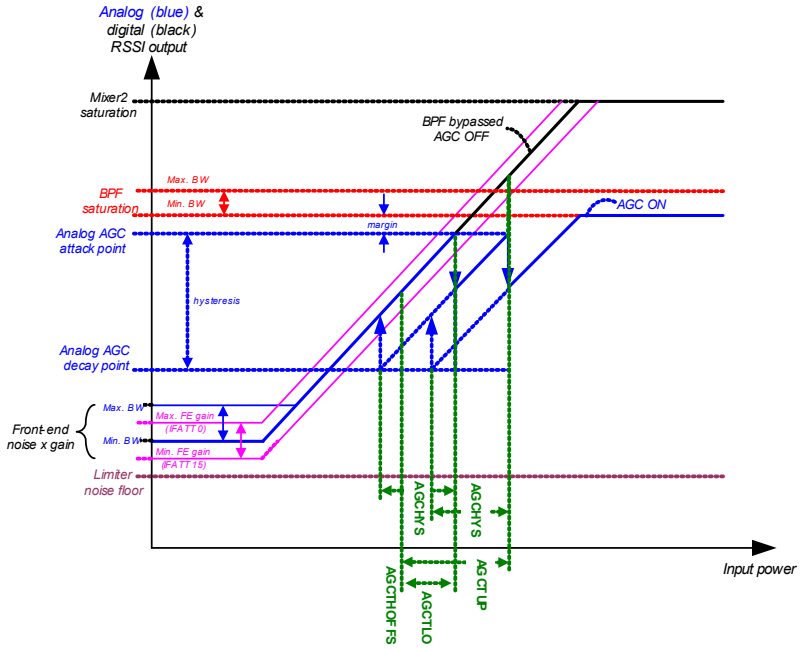


Figure 14 Analog RSSI output curve with AGC action ON (blue) vs. OFF (black)

2.6.8.5 Digital Baseband (DBB) Receiver

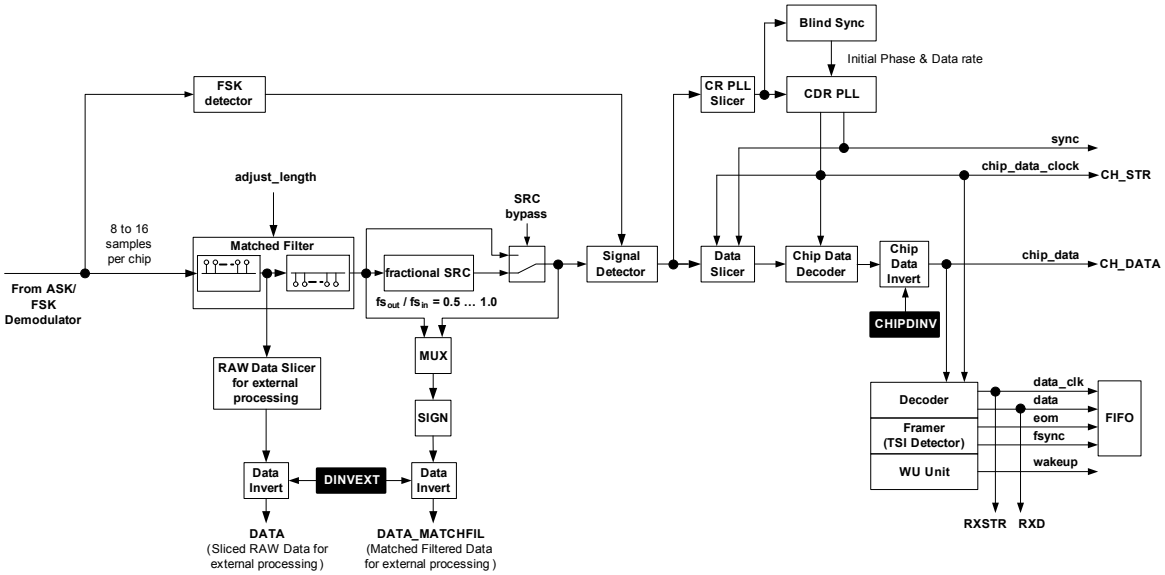


Figure 15 Functional Block Diagram Digital Baseband Receiver

The digital baseband receiver comprises a matched data filter, a clock and data recovery, a data slicer, a line decoder, a wake-up generator, a frame synchronization and a data FIFO. The recovered data and clock signals are accessible via 2 separate pins. The FIFO data buffer is accessible via the SPI bus interface.

2.6.8.6 Clock and Data Recovery (CDR)

An all-digital PLL (ADPLL) recovers the data clock from the incoming data stream. The second main function is the generation of a signal indicating symbol synchronization. Synchronization on the incoming data stream generally occurs within the first 4 bits of a telegram.

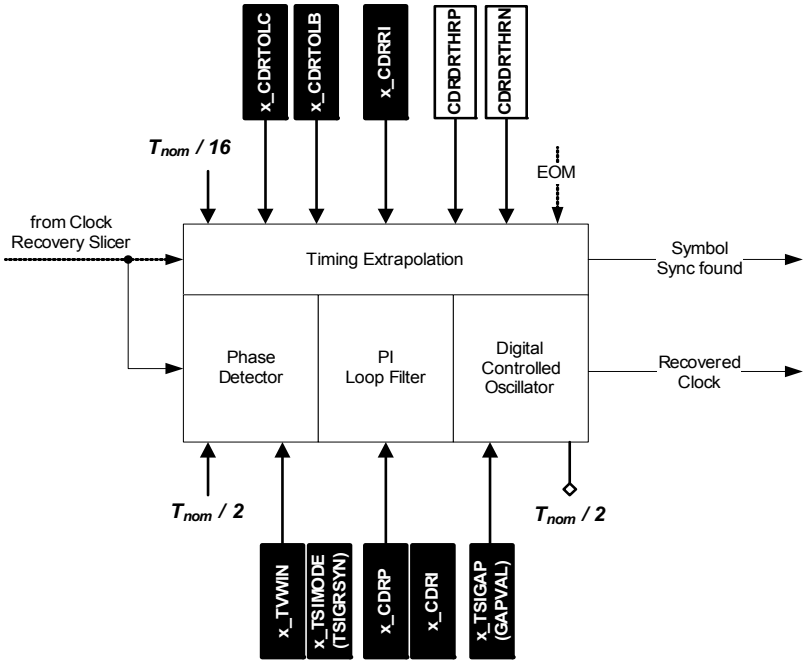


Figure 16 Clock Recovery (ADPLL)

Clock Recovery is implemented as standard ADPLL PI regulator with Timing Extrapolation Unit for fast settling. In the unlocked state, the Timing Extrapolation Unit calculates the frequency offset for the incoming data stream. If the defined number of Bi-phase encoded bits are detected (the RUNIN length can be set in the x_CDRRI register), the I-part and the PLL oscillator will be set and the PLL will be locked. When x_CDRRI.RUNLEN is set to small values, then the I-part is less accurate (residual error) and can lead to a longer needed PLL settling time and worse performance in the first following bits. Therefore the selected default value is a good compromise between fast symbol synchronization and accuracy/performance. Duty cycle and data rate acceptance limits are adjustable via registers. After locking, the clock must be stable and must follow the reference input. Therefore, a rapid settling procedure (Timing Extrapolation Unit) and a slow PLL are implemented. If the PLL is locked, the reference signal from the Clock Recovery Slicer is used in the phase detector block to compute the actual error. The error is used in the PI loop filter to set the digital controlled oscillator running frequency. For the P, I and Timing Extrapolation Unit settings, the default values for the x_CDRP and x_CDRI control registers are recommended.The PLL will be unlocked, if a code violation of more than the defined length is detected, which is set in the x_TVWIN control register. Another criterion for PLL resynchronization is an End Of Message (EOM) signalled by the Framer block. The PLL oscillator generates the chip clock frequency is equal to 2 times the data rate.

2.6.8.7 Wake-Up Generator

A wake-up generation unit is used only in the Self Polling Mode for the detection of a predefined wake-up criterion in the received pattern. There are two groups of configurable wake-up criteria:

- Wake-up on Level criteria
- Wake-up on Data criteria

The search for the wake-up data criterion is started if data chip synchronization has occurred within the predefined number of symbols, otherwise the wake-up search is aborted. Several different wake-up patterns, like random bit, equal bit, bit pattern or bit synchronization, are programmable.Additional level criterion fulfilment for RSSI or Signal Recognition can lead to a fast wake-up and to a change to Run Mode Self Polling. Whenever one of these Wake-up Level criteria is enabled and exceeds a programmable threshold, a wake-up has been detected.The Wake-up Level criterion can be used very effectively in combination with the Ultrafast Fall Back to SLEEP Mode for further decreasing the needed active time of the autonomous receive mode. A configurable observation time for Wake-up on Level can be set in the x_WULOT register.

2.6.8.8 Frame Synchronization

The Frame Synchronization Unit (Framer) synchronizes to a specific pattern to identify the exact start of a payload data frame within the data stream. This pattern is called Telegram Start Identifier (TSI).There are different TSI modes selectable via the configuration:

- 16-Bit TSI Mode, supporting a TSI length of up to 16 bits or 32 chips
- 8-Bit Parallel TSI Mode, supporting two independent TSI pattern of up to 8 bits length each. Different payload length is possible for these two TSI pattern.
- 8-Bit Extended TSI Mode, identical to 8-Bit Parallel TSI Mode, but identifies which pattern matches by adding a single bit at the beginning of the data frame
- 8-Bit TSI Gap Mode, supporting two independent TSI pattern separated by a discontinuity

All SFRs configuring the Frame Synchronization Unit support the Multi-Configuration capability (Config A, B, C and D). The Framer starts working in Run Mode Slave after Symbol Sync found and in Self Polling Mode after wake-up found and searches for a frame until TSI is found or synchronization is lost. The input of the Framer is a sequence of Bi-phase encoded data (chips). Basically the Framer consists of two identical correlators of 16 chips in length. It allows a Telegram Start Identifier (TSI) to be composed of Bi-phase encoded “Zeros” and “Ones”. The active length of each of the 16 chips correlators is defined independently in the x_TSILENA and x_TSILENB registers. The pattern to match is defined as a sequence of chips in the x_TSIPTA0, x_TSIPTA1, x_TSIPTB0 and x_TSIPTB1 registers.

2.6.8.9 Message ID Scanning

This unit is used to define an ID or special combination of bits in the payload data stream, which identifies the pattern. All SFRs configuring the Message ID Scanning Unit feature the Multi-Configuration capability. Furthermore, it is available in the Slave and Self Polling Mode. The MID Unit can be mainly configured in two modes: 4-Byte and 2-Byte organized Message ID. For each configuration there are 20 8-bit registers designed for ID storage. SFRs are used to configure the MID Unit: Enabling of the MID scanning, setting of the ID storage organization, the starting position of the comparison and number of bytes to scan. When the Message ID Scanning Unit is activated, the incoming data stream is compared bit-wise serially with all stored IDs. If the Scan End Position is reached and all received data have matched the observed part of at least one MID the Message ID Scanning Unit indicates a successful MID scanning to the Master FSM, which generates an MID interrupt. Please note that the default register value of the MID registers is set to 0x00. All MID registers must be set to a pattern value to avoid matching to default value 0x00.If the MID Unit finishes ID matching without success, the data receiving is stopped and the FSM waits again for a Frame Start criterion. The received bits are still stored in the FIFO.

2.6.8.10 RUNIN, Synchronization Search Time and Inter-Frame Time

The functionality of the Digital Baseband Receiver is divided into four consecutive data processing stages; the data filter, clock and data recovery, data slicer and frame synchronization unit. The architecture of the Digital Baseband Receiver is optimized for processing bi-phase coded data streams.The basic structure of a payload frame is shown in **Figure 17**. The protocol starts with a so called RUNIN. The RUNIN with the minimum length of four bi-phase coded symbols is used for internal filter settling and frequency adjustment. The TSI (Telegram Start Identifier), which is used as framing word, follows the RUNIN sequence. The payload contains the effective data. The length of the valid payload data is defined as the length itself or additional criteria (e.g. loss of Sync). Please note that almost all transmitted protocols send a wake-up sequence before the payload frame. This wake-up sequence allows a very fast decision, whether there is a suitable message available or not.

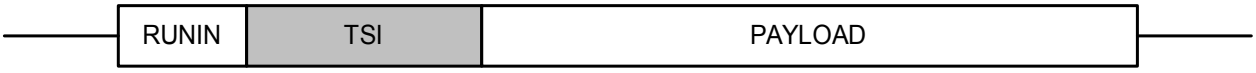


Figure 17 Structure of Payload Frame

2.6.9 Application Interface

Transparent Mode

The TDA5340 supports two levels of integration. In the most elementary fashion, it provides a rather rudimentary interface.

The incoming RF signal is demodulated and the corresponding data is made available to the Application Controller. Optionally, a chip clock is generated by the TDA5340.

The Application Controller can provide the baseband data to a single input pin which is modulated and amplified via the PLL and Power amplifier.

Since the data signal is always directly the baseband representation of the RF signal, we call this mode the Transparent Mode.

Packet Oriented Mode

Alternatively, the TDA5340 features the so-called Packet Oriented Mode which supports the autonomous reception and transmission of data telegrams. The Packet Oriented Mode provides a high-level System Interface which greatly simplifies the integration of the transceiver in data-centric applications. In Packet Oriented Mode, the data interface is based on chunks of synchronous data which are received in packets. In the easiest way, the Application Controller only reacts on the synchronous data it receives. The receiver autonomously handles the line decoding and the deframing of these data, and supports the timed reception of packets. Data is buffered in a receive FIFO and can be read out via the data interface. Further, the receiver provides support for the identification of wake-up signals.

2.6.9.1 Digital Control (4-wire SPI Bus)

The control interface used for device control and data transmission is a 4-wire SPI interface.

- NCS - select input, active low
- SDI - data input
- SDO - data output
- SCK - clock input:

Data bits on SDI are read in at rising SCK edges and written out on SDO at falling SCK edges.

Level Definition:

logic 0 = low voltage

level logic 1 = high voltage level

Note: It is possible to send multiple frames while the device is selected. It is also possible to change the access mode while the device is selected by sending a different instruction.Note: In all bus transfers MSB is sent first, except for the received data read from the FIFO. There the bit order is given as first bit received is first bit transferred via the bus.

Table 3 Instruction Set

Instruction	Description	Instruction Format
WRB	Write to chip in Burst mode	0x01
WR	Write to chip	0x02
RD	Read from chip	0x03
RDF	Read FIFO from chip	0x04
RDB	Read from chip in Burst mode	0x05

Table 3 Instruction Set

Instruction	Description	Instruction Format
WRF	Write FIFO	0x06
WRT0	Write transparent transmit data with starting low data	0x08
WRT1	Write transparent transmit data with starting high data	0x07

Burst Write Command

To write to the device in Burst mode, the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte and the start address byte have been transferred to the SPI slave (MSB first) the successive data bytes will be stored into the automatically addressed registers.To verify the SPI Burst Write transfer, the current address (start address, start address + 1, etc.) is stored in register SPIAT and the current data field of the frame is stored in register SPIDT. At the end of the Burst Write frame the latest address as well as the latest data field can be read out to verify the transfer. Note that some error in one of the intermediate data bytes can not be detected by reading SPIDT. Driving the NCS line to high will end the Burst frame.A single SPI Burst Write command can be applied very efficiently for data transfer either within a register block of configuration dependent registers or within the block of configuration independent registers.

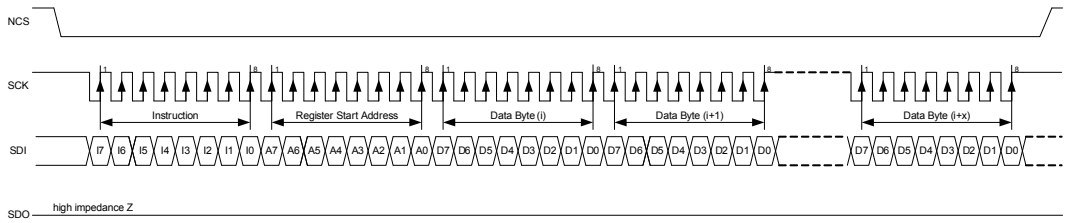


Figure 18 Burst Write Registers

Write Command

To write to the device, the SPI master has to select the SPI slave unit first. Therefore, the master must set the NCS line to low. After this, the instruction byte and the address byte are shifted in on SDI and stored in the internal instruction and address register. The following data byte is then stored at this address. After completing the writing operation, either the master sets the NCS line to high or continues with another SPI command.Additionally the received address byte is stored into the register SPIAT and the received data byte is stored into the register SPIDT. These two trace registers are readable.Therefore, an external controller is able to check the correct address and data transmission by reading out these two registers after each write instruction. The trace registers are updated at every write instruction, so only the last transmission can be checked by a read out of these two registers.

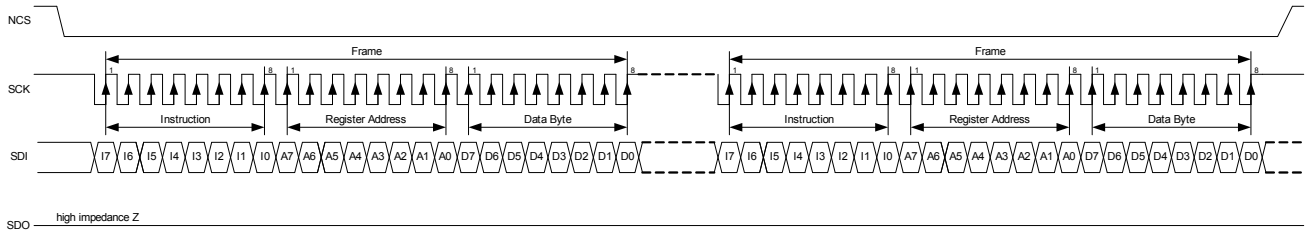


Figure 19 Write Register

Read Command

To read from the device, the SPI master has to select the SPI slave unit first. Therefore, the master must set the NCS line to low. After this, the instruction byte and the address byte are shifted in on SDI and stored in the internal instruction and address register. The data byte at this address is then shifted out on SDO. After completing the read operation, either the master sets the NCS line to high or continues with another SPI command.

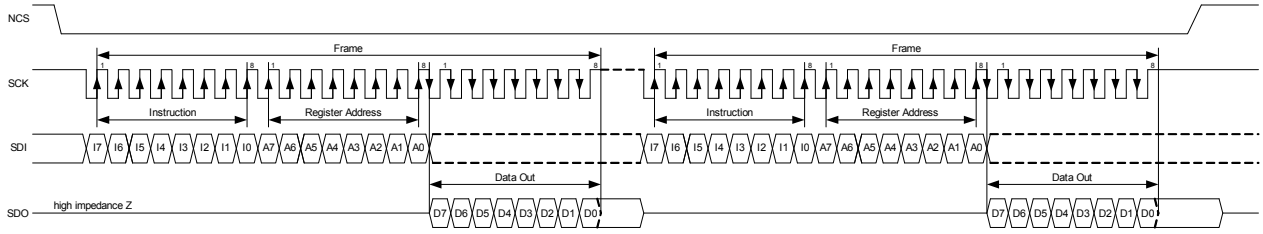


Figure 20 Read Register

Burst Read Command

To read from the device in Burst mode, the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte and the start address byte have been transferred to the SPI slave (MSB first), the slave unit will respond by transferring the register contents beginning from the given start address (MSB first). Driving the NCS line to high will end the Burst frame.

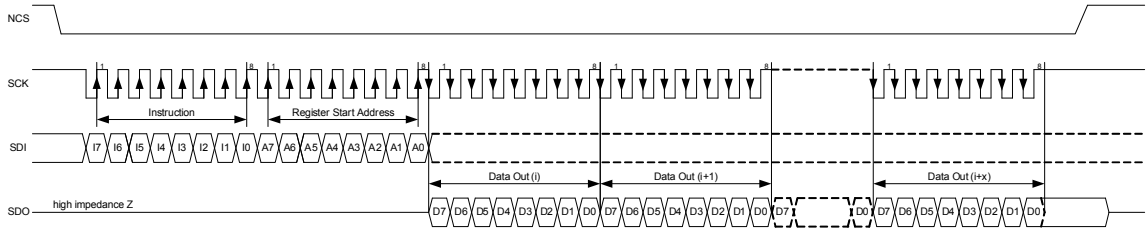


Figure 21 Burst Read Registers

Read FIFO Command

To read the FIFO, the SPI master has to select the SPI slave unit first. Therefore, the master must set the NCS line to low. After this, the instruction byte is shifted in on SDI and stored in the internal instruction register. The data bits of the FIFO are then shifted out on SDO. The following byte is a status word that contains the number of valid bits in the data packet. After completing the read operation, either the master sets the NCS line to high or continues with a other SPI command.

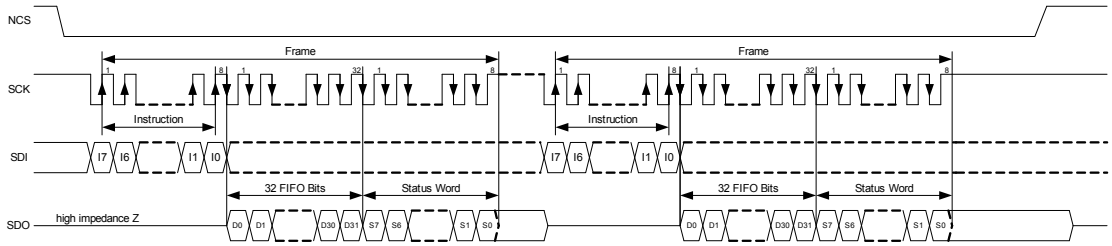


Figure 22 Read FIFO

Write FIFO Command

To write to the TX FIFO the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte (MSB first) the next byte contains the number of data items (chip or bit) minus 1 to be transferred to the FIFO. Therefore 0x00 means a single data item, whereas 0xFF means 256 data items. Successive data bytes contain the data items to be stored into the FIFO. Only the number of data items specified in the 2nd byte of the instruction will be stored into the FIFO. Other bits are skipped. At the end of the access frame the master has to deselect the slave unit by driving the NCS line to high.

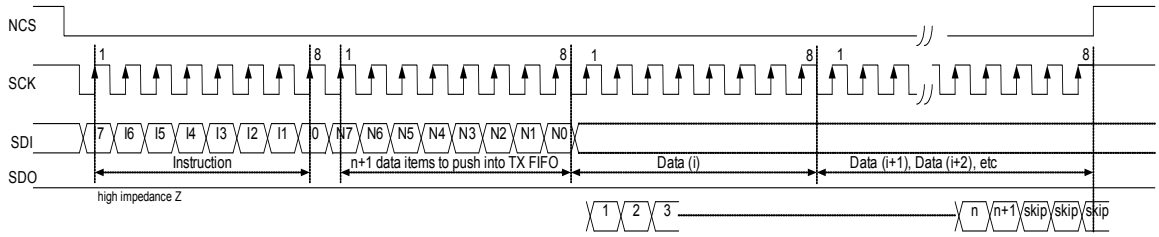


Figure 23 Write TX FIFO

Transparent TX Command

To transfer data items (chip/bit) via SPI in transparent TX mode the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte (MSB first) the SCK should stay static to reduce noise during transmit.

Note that there are 2 versions of the same command available. They differ only in the LSB of the instruction. The intent of this is to pre-set the level of the SDI line to the level of the first TX data item (chip/bit). A new data item is asserted every “k” Gaussian Filter strobes (depends on the configuration, k strobes per chip).

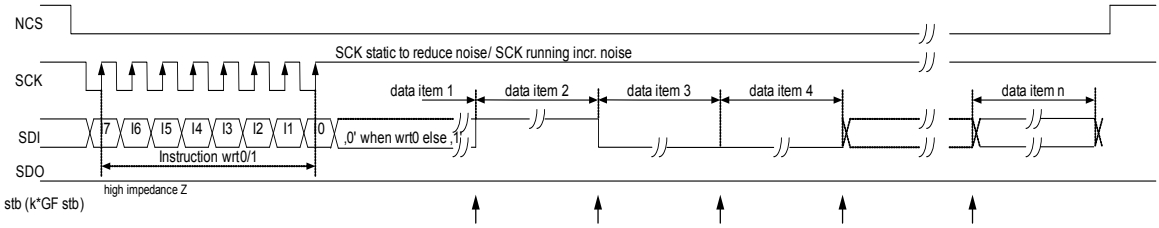


Figure 24 Transparent TX Command

SPI Check Sum

The SPI also includes a safety feature by which the checksum is calculated with an XOR operation from the address and the data when writing SFR registers content. The checksum is in fact an XOR of the data 8-bitwise after every 8 bits of the SPI write command. The calculated checksum value is automatically written in the SPICHKSUM register and can be compared with the expected value. After the SPICHKSUM register is read, its value is cleared. In case of an SPI Burst Write and Write FIFO frame, a checksum is calculated from the SPI start address and consecutive data fields.

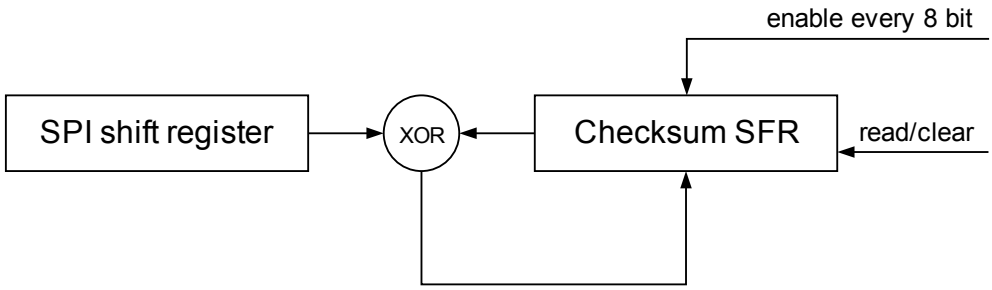


Figure 25 SPI Checksum Generation

2.6.10 Chip Serial Number

Every device contains a unique, preprogrammed 32-bit wide serial number. This number can be read out from SN3, SN2, SN1 and SN0 registers via the SPI interface. The TDA5340 always has SN0.6 set to 1 and SN0.5 is reserved.

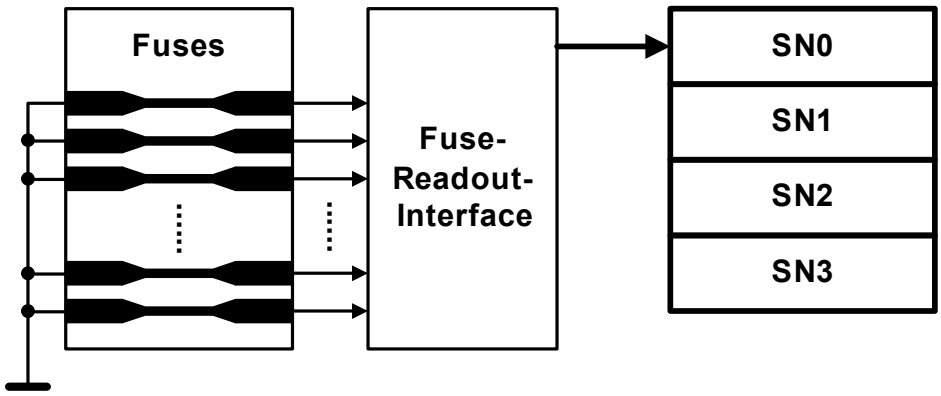


Figure 26 Chip Serial Number

3 Reference

3.1 Electrical Data

3.1.1 Absolute Maximum Ratings

■ not subject to production test - verified by characterization/design

Attention: The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Voltage at VDD5V pin	V_{smax}	-0.3		+6	V		■	1.1
Supply Voltage at VDDD, VDDA, VDDRF pin	V_{smax}	-0.3		+4	V		■	1.2
Voltage between VDD5V vs VDDD , VDD5V vs VDDA and VDD5V vs VDDRF	V_{smax}	-0.3		+4	V		■	1.3
Junction Temperature	T_j	-40		+125	°C		■	1.4
Storage Temperature	T_S	-40		+150	°C		■	1.5
Thermal resistance junction to air	$R_{th(ja)}$			110	K/W		■	1.6
Total power dissipation at Tamb = 105°C	P_{tot}			135	mW		■	1.7
ESD HBM integrity (all pins except RFOUT pin)	V_{HBMRF}	-2		2	kV	According to AEC Q100-002 /JEDEC JESD22/A114	■	1.8
ESD HBM integrity (RFOUT pin)	V_{HBMRF_PA}	-4		4	kV	According to AEC Q100-002 /JEDEC JESD22/A114	■	1.8.1
ESD CDM / SDM integrity (All pins except corner pins)	V_{SDM}	-500		500	V	According to ANSI / ESD SP5.3.2.-2008	■	1.9
ESD CDM / SDM integrity (All corner pins)	V_{SDM}	-750		750	V	According to ANSI / ESD SP5.3.2.-2008	■	1.10
Latch up	I_{LU}	100			mA	JEDEC JESD78	■	1.11

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Maximum input voltage at digital input pins	V_{inmax}	-0.3		VDD5V+0.5 or 6.0	V	whichever is lower	■	1.12
Maximum current into digital input and output pins	I_{IOmax}			4	mA	except PPRF_RSSI pin	■	1.13

3.1.2 Operating Range

■ not subject to production test - verified by characterization/design

Table 5 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Voltage at pin VDD5V	V_{DD5V}	4.5		5.5	V	Supply Voltage Range 1	■	2.1
Supply Voltage at pin VDD5V = VDDD = VDDA = VDDRF	V_{DD3V3}	3.0		3.6	V	Supply Voltage Range 2	■	2.2
Peak Voltage at pin RFOUT	V_{RFOUT_peak}			8	V	TX duty cycle <= 10%[1)]	■	2.2.1
				6.5	V	TX duty cycle > 10%[1)]	■	2.2.2
DC Voltage at pin RFOUT	V_{RFOUT_DC}			3.6	V		■	2.2.3
Ambient temperature	T_{amb}	-40		110	°C	upper and lower limit tested		2.3

1) TX duty cycle defines the on time of the power amplifier compared to all other modes of the TDA5340

3.1.3 AC/DC Characteristics

Supply voltage VDD5V = 4.5 to 5.5 Volt or VDD5V = VDDA = VDDD = VDDRF = 3.0 to 3.6 Volt, Ambient temperature Tamb = -40...110°C, Tamb = +25°C for typical parameters, unless otherwise specified.

Values of AC/DC characteristics are with combined matching network using internal antenna switch not including matching variation.

■ not subject to production test - verified by characterization/design

Table 6 General Transceiver Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Current: Transmit Mode								
315 MHz Band	$I_{TX,10dBm}$		12	14	mA	Continuous wave measured in a 50 Ω Load	■	3.1
434 MHz Band	$I_{TX,10dBm}$		12.5	15	mA	Continuous wave measured in a 50 Ω Load / measured @ 433,92 MHz	■	3.1.1
315 / 434 MHz Band	$I_{TX,13dBm}$		18	21	mA	Continuous wavemeasured in a 50 Ω Load / measured and test @ 433,92 MHz		3.2
868 /915 /954 MHz Band	$I_{TX,10dBm}$		17	20	mA	Continuous wave measured in a 50 Ω Load	■	3.3
868 /915 MHz Band	$I_{TX,13dBm}$		22.5	26	mA	Continuous wave measured in a 50 Ω Load / test at 868 MHz		3.4
Supply Current: Receive Mode								
Double Down Conversion Mode	$I_{Run,Double}$		12.5	15.5	mA	ASK or FSK mode Pin < -50 dBm		3.5
Single Down Conversion Mode	$I_{Run,Single}$		11.5	14.5	mA	ASK or FSK mode Pin < -50 dBm		3.6
Supply Current: Sleep Mode								
Tamb = 25 °C	$I_{sleep_low,25°C}$		40	50	µA	1)		3.7
Tamb = 85 °C	$I_{sleep_low,85°C}$		70	130	µA	1)	■	3.8
Tamb = 110 °C	$I_{sleep_low,110°C}$		110	180	µA	1)		3.9
Sleep Mode Supply current High Precision:	I_{sleep_high}		100		µA	2)	■	3.10

Table 6 General Transceiver Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply current: clock generator	I_{clock}		12	18	µA	$f_{clockout}$ = 1 kHz C_{load} = 10 pF	■	3.11
Supply Current: Deep Sleep Mode								
Tamb = 25 °C	$I_{Deep_sleep_low,25°C}$		7	14	µA			3.11.1
Tamb = 85 °C	$I_{Deep_sleep_low,85°C}$		30	80	µA		■	3.11.2
Tamb = 110 °C	$I_{Deep_sleep_low,110°C}$		70	140	µA			3.11.3
Supply current: Power Down Mode								
Tamb = 25 °C 3,3V	$I_{PDN,25°C,3V3}$		0.9	1,9	µA			3.12
Tamb = 85 °C 3,3V	$I_{PDN,85°C,3V3}$		5	15	µA		■	3.13
Tamb = 110 °C 3,3V	$I_{PDN,110°C,3V3}$		13,5	31	µA			3.14
Tamb = 25 °C 5V	$I_{PDN,25°C,5V}$		2	3	µA			3.14.1
Tamb = 85 °C 5V	$I_{PDN,85°C,5V}$		5,5	15	µA		■	3.14.2
Tamb = 110 °C 5V	$I_{PDN,110°C,5V}$		12,5	31	µA			3.14.3
General								
Data Rate ASK	DR_{ASK}	0.5		40	kchips/s		■	3.15
Data Rate FSK	DR_{FSK_TX}	0.5		112	kchips/s		■	3.16
	DR_{FSK_RX}	0.5		112	kchips/s		■	3.17
FSK Deviation	f_{dev}	+/-1		+/-64	kHz		■	3.18
Modulation index	m_{ASK}	50		100	%		■	3.19
	m_{FSK}	0.5					■	3.20
Transceiver reset time	t_{RESET}	1	1.8	3	ms	Time from Power Down Mode to Sleep Mode		3.21
Transceiver startup time: deep sleep to sleep mode	$t_{DSstartup}$		0.35	1.3	ms	Time from DeepSleep Mode to Sleep Mode; XTAL see **Table 12**		3.21.1
Transceiver startup time: receive mode	$t_{startupRX}$	469	469	469	µs	Time from Sleep Mode to Receive Mode[3)4)]	■	3.22

Table 6 General Transceiver Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Transceiver startup time: transmit mode	$t_{startupTX}$	403	403	403	µs	Time from Sleep Mode to Transmit Mode[3)4)]	■	3.23
RX/TX switch time	$t_{RX/TX}$	133	133	133	µs	Time from transmit mode to receive mode[4)]	■	3.24
TX/RX switch time	$t_{TX/RX}$	470	470	470	µs	Time from receive mode to transmit mode[4)]	■	3.25
RF Channel / Configuration Hop Latency Time	t_{ChHop}	110	110	110	µs	Time to switch RF PLL between different RF Channels [4)5)]	■	3.26
P_ON LOW pulse width	t_{P_ON}	15			µs	Minimal necessary pulse width to reset the chip	■	3.27
NINT pulse length	t_{NINT_Pulse}		11.7		µs	Pulse width of interrupt	■	3.28
Brownout detector threshold	V_{BOR}	2.3	2.45	2.6	V			3.29

1) crystal oscillator in Low Power Mode; clock generator off; valid for SLEEP Mode and during SPM Off time
2) crystal osscillator in High Precision Mode C_{load} = 25 pF; clock generator off; valid for SLEEP Mode and during SPM Off time
3) comprises time required to switch crystal oscillator from Low Power Mode to High Precision Mode
4) default RX/TX PLL startup time
5) does not include settling of Data Clock Recovery

Table 7 Receive Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Overall noise figure	NF		6	8	dB	RF input matched to 50 Ω @ Tamb = 25 °C	■	4.1
3rd order intercept IIP3	P_{IIP3}	-16	-15		dBm	IFATT = 7;[1)]	■	4.2
1 dB compression point CP1dB	P_{CP1dB}	-27	-25		dBm	IFATT = 7;[1)]	■	4.3
1st IF image rejection	d_{image1}	30	40		dB	1st IF = 10.7 MHz Double Down Conversion Mode only		4.4
2nd IF image rejection	d_{image2}	30	35		dB	2nd IF = 274 kHz single Down Conversion Mode;		4.5

Table 7 Receive Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
3dB Overall analog Bandwidth	BW_{ana}	230	250		kHz	LNA input to Limiter output, excluding external CER Filter, 2nd IF BW = 300 kHz	■	4.6
FSK 3dB Sensitivity BW	SBW_{FSK}		120		kHz	10kBit/s; Δf = 40 kHz; 2nd IF BW = 300 kHz PDF = 283 kHz	■	4.7
		180	200		kHz	10kBit/s; Δf = 40 kHz; 2nd IF BW = 300 kHz PDF = 283 kHz AFC active	■	4.8
ASK 3dB Sensitivity BW	SBW_{ASK}	230	250		kHz	2nd IF BW = 300 kHz	■	4.9
Sensitivity variation due to temperature (-40...+110°C)	ΔP_{in_temp}			3	dB	relative to Tamb = 25 °C;[2)]	■	4.10
Sensitivity improvement in case of pure RX matching	$\Delta P_{in_315/434}$		1		dB		■	4.10.1
	$\Delta P_{in_868/915}$		2		dB		■	4.10.2
Data rate tol.	R_{data_tol}	-10		+10	%		■	4.11
Duty cycle ASK	T_{chip}/T_{data}	35		55	%	see Definition C in User Manual	■	4.12
Duty cycle FSK	T_{chip}/T_{data}	45		55	%	see Definition B in User Manual	■	4.13
ASK Demodulation								
Data Rate 0.5 kBit/s Manchester Coding	$SASK1_{MER}$		-120	-117	dBm peak	m = 100% 2nd IF BW = 50 kHz	■	4.14
	$SASK2_{MER}$		-115	-112	dBm peak	m = 100% 2nd IF BW = 300 kHz [3)]	■	4.15
Data Rate 2 kBit/s Manchester Coding	$SASK3_{MER}$		-116	-113	dBm peak	m = 100% 2nd IF BW = 50 kHz	■	4.16
	$SASK4_{MER}$		-112	-109	dBm peak	m = 100% 2nd IF BW = 300 kHz [3)]	■	4.17

Table 7 Receive Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Data Rate 10 kBit/s Manchester Coding	$SASK5_{MER}$		-111	-108	dBm peak	m = 100% 2nd IF BW = 50 kHz	■	4.18
	$SASK6_{MER}$		-108	-105	dBm peak	m = 100% 2nd IF BW = 300 kHz 3)	■	4.19
Data Rate 16 kBit/s Manchester Coding	$SASK7_{MER}$		-109	-106	dBm peak	m = 100% 2nd IF BW = 80 kHz	■	4.20
	$SASK8_{MER}$		-107	-104	dBm peak	m = 100% 2nd IF BW = 300 kHz 3)	■	4.21
FSK Demodulation								
Data Rate 2 kBit/s; Δf =4kHz Manchester Coding	$SFSK1_{MER}$		-116	-113	dBm	2nd IF BW = 50 kHz PDF = 33 kHz 4)	■	4.22
	$SFSK2_{MER}$		-108	-105	dBm	2nd IF BW = 300 kHz PDF = 282 kHz;5)	■	4.23
Data Rate 2 kBit/s; Δf =10kHz Manchester Coding	$SFSK2.1_{MER}$		-118		dBm	2nd IF BW = 50 kHz PDF = 33 kHz 4)	■	4.23.1
Data Rate 10 kBit/s; Δf = 14 kHz Manchester Coding	$SFSK3_{MER}$		-114	-111	dBm	2nd IF BW = 50 kHz PDF = 65 kHz 4)	■	4.24
	$SFSK4_{MER}$		-106	-103	dBm	2nd IF BW = 300kHz PDF = 282 kHz;5)	■	4.25
Data Rate 10 kBit/s; Δf = 40 kHz Manchester Coding	$SFSK5_{MER}$		-112	-109	dBm	2nd IF BW = 125 kHz PDF = 132 kHz 4)	■	4.26
	$SFSK6_{MER}$		-110	-107	dBm	2nd IF BW = 300kHz PDF = 282 kHz;5)	■	4.27
Data Rate 50 kBit/s; Δf = 50 kHz Manchester Coding	$SFSK7_{MER}$		-105	-102	dBm	2nd IF BW = 300 kHz; PDF = 239 kHz 4)	■	4.28

1) input matched to 50 Ω; Insertion loss of input matching network = 1dB
2) temperature coefficient of crystal not considered
3) Note: min 3dB sensitivity loss @ foffset = +/-100 kHz
4) AFC off
5) Note: min 3dB sensitivity loss @ foffset=+/-90kHz; AFC ON

Table 8 Transmit Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Output Power	P_{TXmax}		+14		dBm	measured at 50 Ω Load / test at 868 MHz		5.1
Number of output power steps	$\#P_{step}$		31			not linear	■	5.3
TX output Power Variation vs. Production	P_{TX_P}	-1.5		+1.5	dB	test at +13 dBm and 868 MHz		5.10
TX output Power Variation vs. Voltage	P_{TX_V}	-1.5		+1.5	dB	test at +13 dBm and 868 MHz		5.11
TX output Power Variation vs. Temp.	P_{TX_temp}	-2		+1.5	dB		■	5.12
Modulation Filtering	B*T		0.5			programmable	■	5.13
Optimal load impedance, matched to 10 dBm output power at 50 Ohm	Z_{opt1}		490+j227			315 MHz	■	5.14
	Z_{opt2}		420+j136			434 MHz	■	5.15
	Z_{opt3}		280+j65			868 MHz	■	5.16
	Z_{opt4}		223+j40			915 MHz	■	5.17
	Z_{opt5}		251+j36			954 MHz	■	5.18
Optimal load impedance, matched to 13 dBm output power at 50 Ohm	Z_{opt1}		220+j217			315 MHz	■	5.19
	Z_{opt2}		215+j150			434 MHz	■	5.20
	Z_{opt3}		140+j60			868 MHz	■	5.21
	Z_{opt4}		153+j40			915 MHz	■	5.22
	Z_{opt5}		156+j36			954 MHz	■	5.23
PPRF output current	I_{PPRF}			4	mA		■	5.24

(Unless otherwise noted, all values apply for the specified frequency ranges)

Table 9 Synthesizer Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
TRX Frequency Bands								
Range 1	f_{band_1}	300		320	MHz	1)		6.1
Range 2	f_{band_2}	415		495	MHz	1)2)		6.2
Range 3	f_{band_3}	863		960	MHz	1)		6.3
Frequency step of Sigma-Delta PLL	f_{step}	10.5			Hz	$f_{step} = f_{XTAL} / 2^{21}$	■	6.6
PLL loop Bandwidth TX	PLLBWTX	75	130		kHz		■	6.7

Table 9 Synthesizer Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
PLL Phase Noise								
f_{LO}= 315 MHz PLLBWTX = 130kHz	d_{SSB_LO}		-87	-79	dBc/Hz	@ f_{offset} = 10 kHz[3)]	■	6.8
			-91	-80	dBc/Hz	@ f_{offset} = 100 kHz[3)]	■	6.9
			-124	-115	dBc/Hz	@ f_{offset} = 1 MHz[3)]	■	6.10
			-140	-129	dBc/Hz	@ f_{offset} =>10 MHz[3)]	■	6.11
f_{LO}= 434 MHz PLLBWTX = 130kHz	d_{SSB_LO}		-87	-78	dBc/Hz	@ f_{offset} = 10 kHz[3)]	■	6.12
			-89	-81	dBc/Hz	@ f_{offset} = 100 kHz[3)]	■	6.13
			-123	-115	dBc/Hz	@ f_{offset} = 1 MHz[3)]	■	6.14
			-140	-131	dBc/Hz	@ f_{offset} =>10 MHz[3)]	■	6.15
fLO = 868.95 MHz PLLBWTX = 130kHz	d_{SSB_LO}		-82	-70	dBc/Hz	@ f_{offset} = 10 kHz[3)]	■	6.16
			-86	-78	dBc/Hz	@ f_{offset} = 100 kHz[3)]	■	6.17
			-120	-112	dBc/Hz	@ f_{offset} = 1 MHz[3)]	■	6.18
			-135	-128	dBc/Hz	@ f_{offset} = 6 MHz[3)]	■	6.19
			-138	-128	dBc/Hz	@ f_{offset} = =>10 MHz[3)]	■	6.20
f_{LO}= 960 MHz PLLBWTX = 130kHz	d_{SSB_LO}		-80	-70	dBc/Hz	@ f_{offset} = 10 kHz[3)]	■	6.20.1
			-86	-79	dBc/Hz	@ f_{offset} = 100 kHz[3)]	■	6.25
			-118	-110	dBc/Hz	@ f_{offset} = 1 MHz[3)]	■	6.28
			-138	-128	dBc/Hz	@ f_{offset} = =>10 MHz[3)]	■	6.29

Table 9 Synthesizer Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
fLO = 960MHz PLLBWTX = 70kHz	d_{SSB_LO}		-74	-67	dBc/Hz	@ f_{offset} = 10 kHz[3]	■	6.30
			-90	-82	dBc/Hz	@ f_{offset} = 100 kHz[3]	■	6.31
			-119	-111	dBc/Hz	@ f_{offset} = 1 MHz[3]	■	6.32
			-138	-128	dBc/Hz	@ f_{offset} = =>10 MHz[3]	■	6.33

1) except: $|f_{TX} - k*f_{XTAL}| < 500$ kHz where k is an integer value
2) for f > 485MHz high side injection in receive mode not alllowed
3) unmodulated TX carrier

Table 10 Receiver Frontend Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
FE voltage conversion gain	$AV_{FE,max}$	34	36	38	dB	min. IF attenuation (IFATT = 0)[1]		7.1
FE voltage conversion gain	AV_{FE_7}	29	31	33	dB	IF attenuation (IFATT = 7)[1]		7.2
FE voltage conversion gain	$AV_{FE,min}$	22	24	26	dB	max. IF attenuation (IFATT = 15)[1]		7.3
FE voltage conversion gain step			0.8		dB	Double Down Conversion: 16 gain steps; Single Down Conversion: 7 gain steps		7.4
FE output impedance	R_{out_IF}	290	330	370	Ω	f_{IF} = 10.7 MHz	■	7.5
LNA input impedance								
fRF = 315 MHz	R_{in_p}		672		Ω	[2]	■	7.6
	C_{in_p}		1.075		pF	[2]	■	7.7
fRF = 434MHz	R_{in_p}		534		Ω	[2]	■	7.8
	C_{in_p}		0.835		pF	[2]	■	7.9
fRF = 868MHz	R_{in_p}		462		Ω	[2]	■	7.10
	C_{in_p}		0.665		pF	[2]	■	7.11
fRF = 915MHz	R_{in_p}		460		Ω	[2]	■	7.12
	C_{in_p}		0.66		pF	[2]	■	7.13

1) input matched to 50 Ω; Insertion loss of input matching network = 1dB; Rload_IF = 330Ω ; tested at 433.92MHz

2) differential parallel equivalent input between LNA_INP and LNA_INN

Table 11 Receiver 2nd IF Mixer, RSSI and Filter Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Mixer input impedance	R_{in_IF}	290	330	370	Ω	fIF = 10...12 MHz	■	8.1
RSSI								
Dynamic range	DR_{RSSI1}	-110		-30	dBm	applies for digital RSSI	■	8.2
	DR_{RSSI2}	-115		-60	dBm	applies for analog RSSI @ 50 kHz BPF, AGC off	■	8.3
	DR_{RSSI3}	-110		-50	dBm	applies for analog RSSI @ 300 kHz BPF, AGC off	■	8.4
Linearity	DR_{LIN}	-1		+1	dB	-95 dBm ....-35 dBm; applies for digital RSSI	■	8.5
Temperature drift within linear dynamic range	DR_{TEMP}	-2.5		+1.5	dB	-95 dBm...-35 dBm; applies for digital RSSI	■	8.6
Output voltage dynamic range	V_{RSSI+}	0.8	1.0	2	V		■	8.7
analog RSSI error, untrimmed	$DRSSI_{ana}$	-4		+2.5	dB	at RSSI pin		8.8
analog RSSI slope, untrimmed	dV_{RSSI}/dV_{mix_in}	8	10	12	mV/dB	at RSSI pin; typical 600 mV/60 dB = 10 mV/dB		8.9
digital RSSI error, untrimmed	$DRSSI_{dig_u}$	-3		+3	dB	RSSI register readout		8.10
digital RSSI error, user trimmed via SFRs RSSISLOPE and RSSIOFFS	$DRSSI_{dig_t}$	-1		+1	dB	RSSI register readout	■	8.11
digital RSSI slope,untrimmed	dV_{RSSI}/dV_{mix_in}	8	10	12	LSB/dB	RSSI register readout; typical 600 mV/60 dB = 10 mV/dB, 1mV = 1 LSB		8.12

Table 11 Receiver 2nd IF Mixer, RSSI and Filter Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
digital RSSI slope,user trimmed via SFRs RSSISLOPE and RSSIOFFS	dV_{RSSI}/dV_{mix_in}	9.5	10	10.5	LSB/dB	RSSI register readout; typical 600 mV/60 dB = 10 mV/dB, 1 mV = 1 LSB	■	8.13
Resistive load at RSSI pin	$R_{L,RSSImax}$	100			kΩ		■	8.14
Capacitive load at RSSI pin	$C_{L,RSSI}$			20	pF		■	8.15
2nd IF Filter (3rd order Bandpass Filter)								
Center frequency	f_{center}	262	274	288	kHz	Asymmetric BPF corners: f_center=sqrt(flow * fhigh); Use AFC for more symmetry	■	8.16
-3 dB BW	BW_{-3dB}		50 / 80 125 / 200 300		kHz	selectable	■	8.17
-3 dB BW tolerance	tol_BW_{-3dB}	-5		+5	%	BW=125, 200, 300 kHz	■	8.18
-3 dB BW tolerance	tol_BW_{-3dB}	-6		+6	%	BW=50,80 kHz	■	8.19

Table 12 Crystal Oscillator Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Frequency range	f_{XTAL}		21.948717		MHz			9.1
Crystal parameters								
Motional capacitance	C_1		4		fF		■	9.2
Motional resistance	R_1			60	Ω		■	9.3
Shunt capacitance	C_0		1.2		pF		■	9.4
Load capacitance	C_{Load}		12		pF	nominal value	■	9.5

Table 12 Crystal Oscillator Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Initial frequency tolerance	f_{XTAL_Tol}	-30		+30	ppm	oscillator untrimmed (trim capacitor default settings, usage of recommended crystal); not including crystal tolerances	■	9.6
Frequency trimming range	Δf_{XTAL}	-30		+50	ppm	using only internal load C, larger trimming range possible via SD PLL		9.7
Frequency trimming range	Δf_{XTAL}	-50		+50	ppm	using external load C (2 x 3.9pF), larger trimming range possible via SD PLL	■	9.7.1
Clock output frequency at PPx pin	f_{clock_out}	12		5.5M	Hz	10 pF load	■	9.8
Crystal oscillator settling time (switching from Low Power to High Precision Mode)	$t_{XOSCsettle}$		300	330	µs		■	9.9

Table 13 Digital Input/Output Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
High level input voltage	V_{In_High}	0.7*VDD5 V		VDD5V+0 .1	V		■	10.1
High level input leakage current	I_{In_High}			5	µA			10.2
Low level input voltage (except P_ON pin)	V_{In_Low}	0		0.8	V		■	10.3
Low level input voltage (at P_ON pin)	$V_{In_Low_PON}$	0		0.5	V		■	10.4
Low level input leakage current	I_{In_Low}	-5			µA			10.5

Table 13 Digital Input/Output Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
High level output voltage 1	V_{Out_High1}	VDD5V - 0.4		VDD5V	V	IOH=-500 µA, static driver capability; Normal Pad Mode		10.6
Low level output voltage 1	V_{Out_Low1}	0		0.4	V	IOL=500 µA, static driver capability; Normal Pad Mode		10.7
High level output voltage 2	V_{Out_High2}	VDD5V-0.8		VDD5V	V	IOH=-4 mA, static driver capability; High Power Pad Mode		10.8
Low level output voltage 2	V_{Out_Low2}	0		0.8	V	IOL=4 mA, static driver capability; High Power Pad Mode		10.9

Table 14 Timing SPI-Bus Charcteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Clock frequency	f_{clock}			2.2	MHz		■	11.1
Clock High time	t_{CLK_H}	200			ns		■	11.2
Clock Low time	t_{CLK_L}	200			ns		■	11.3
Active setup time	t_{setup}	200			ns		■	11.4
Not active setup time	t_{not_setup}	200			ns		■	11.5
Active hold time	t_{hold}	200			ns		■	11.6
Not active hold time	t_{not_hold}	200			ns		■	11.7
Deselect time	$t_{Deselect}$	200			ns		■	11.8
SDI setup time	t_{SDI_setup}	100			ns		■	11.9
SDI hold time	t_{SDI_hold}	100			ns		■	11.10
Clock low to SDO valid	t_{CLK_SDO}			145	ns	@ Cload = 80 pF High Power Pad not enabled (Normal Mode)	■	11.11
Clock low to SDO valid	t_{CLK_SDO}			40	ns	@ Cload = 10 pF High Power Pad not enabled (Normal Mode)	■	11.12
SDO rise time	t_{SDO_r}			90	ns	@ Cload = 80 pF	■	11.13

Table 14 Timing SPI-Bus Charcteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
SDO fall time	t_{SDO_f}			90	ns	@ Cload = 80 pF	■	11.14
SDO rise time	t_{SDO_r}			15	ns	@ Cload = 10 pF	■	11.15
SDO fall time	t_{SDO_f}			15	ns	@ Cload = 10 pF	■	11.16
SDO disable time	$t_{SDO_disable}$			25	ns		■	11.17

Definitions

Unless explicitly otherwise noted, the following test conditions apply to the given specification values in **Table 7** of **ASK Demodulation** and **FSK Demodulation**:

* Hardware: TDA5340 Platform Testboard V1.3
* Combined low cost Matching for 315.0 MHz / 433.92 MHz / 868.3 MHz / 915.0 MHz
* RF input matched to 50 Ohm; Insertion loss of input matching network = 1dB
* Receive Frequency 315.0 MHz / 433.92 MHz / 868.3 MHz / 915.0 MHz; Lo-Side LO-Injection
* Reference Clock: XTAL=21.948717 MHz

* IF-Gain: Attenuation set to 0 dB (IFATT = 0)
* Double Down Conversion
* 1 IF-Filter: Center=10.7MHz; BW=330kHz; Connected between IF_OUT and IFBUF_IN
* Received Signal at zero Offset to IF Center Frequency
* RSSI trimmed
* FSK Pre-Demodulation Filter (PDF) BW: Depending on Data Rate and FSK Deviation
* No SPI-traffic during telegram reception, CLK_OUT disabled
* AFC and AGC are OFF, unless otherwise noted
* Specification values are in respect to Manchester-coded Infineon-Reference Pattern 1
(7 Bits '0', 1 Bit ’1', 1 Bits '0', 1 Bit ’1', 1 Bits '0', 1 Bit ’1', PRBS5 (31 Bit), 1 Bit 'M') however a Code Violation is not used as EOM criterion.

MER sensitivity measurements use Receive Mode - Packet oriented FIFO Mode)

* DC ... Duty Cycle
* MER ... Message Error Rate
[MER = 1 - (number_of_correctly_received_messages / number_of_transmitted messages)]
* FAR ... False Alarm Rate
[FAR = number_of_mistakenly_wake_ups / number_of_periods_searching_for_data_on_channel]
* MMR ... Missed Message Rate
[MMR = number_of_mistakenly_missed_wake_up_patterns /
number_of_periods_with_wake_up_pattern_transmitted_and_searching_for_wake_up_pattern]
* BER ... Bit Error Rate (using a PRBS9 Pseudo-Random Binary Sequence)
[BER = 1 - (number_of_correctly_received_bits / number_of_transmitted bits)]

Measurement Results

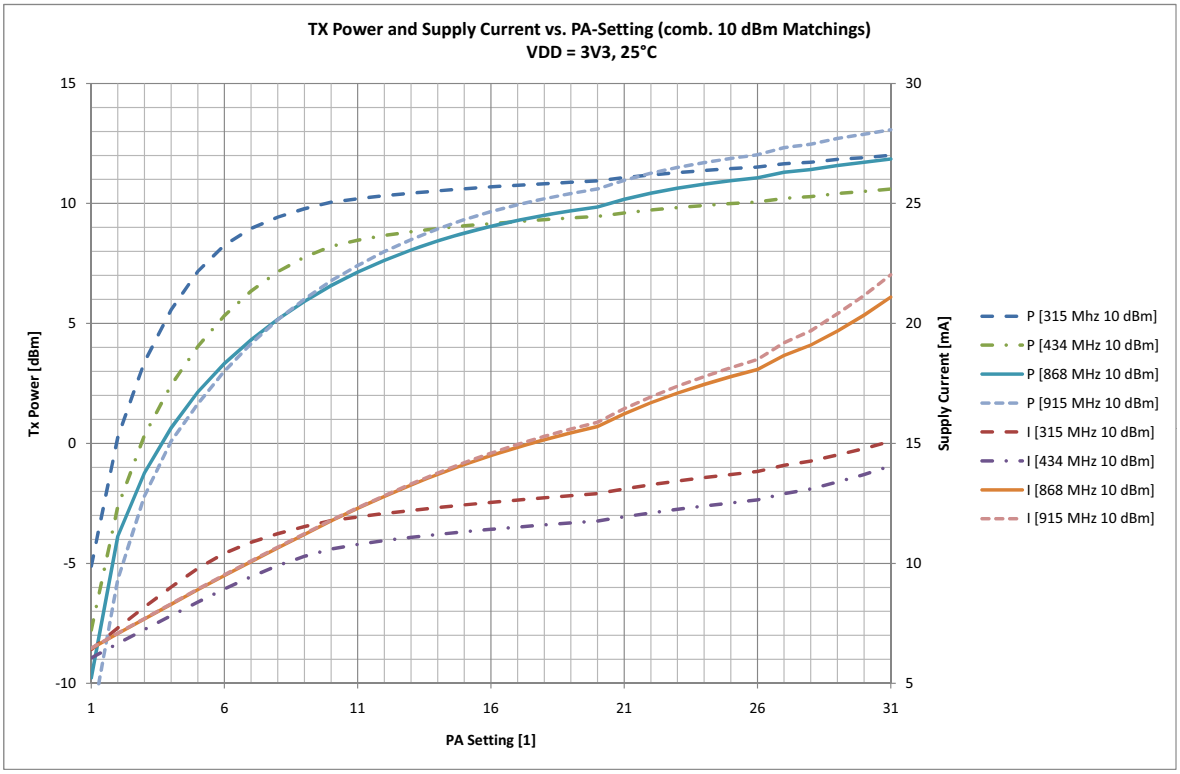


Figure 27 10dBm Matching, Output Power and Supply Current in TX vs. Output power stages

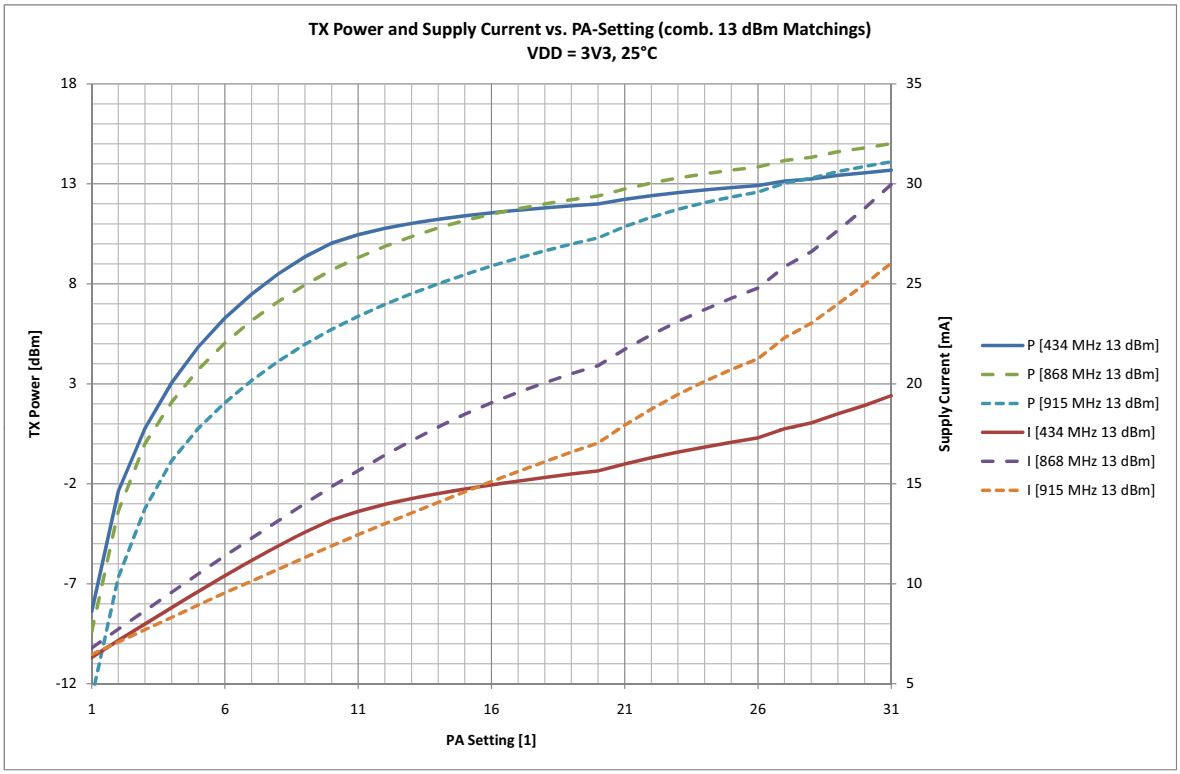


Figure 28 13dBm Matching, Output Power and Supply Current in TX vs. Output power stages

3.2 Test Circuitry Evaluation Board V1.3

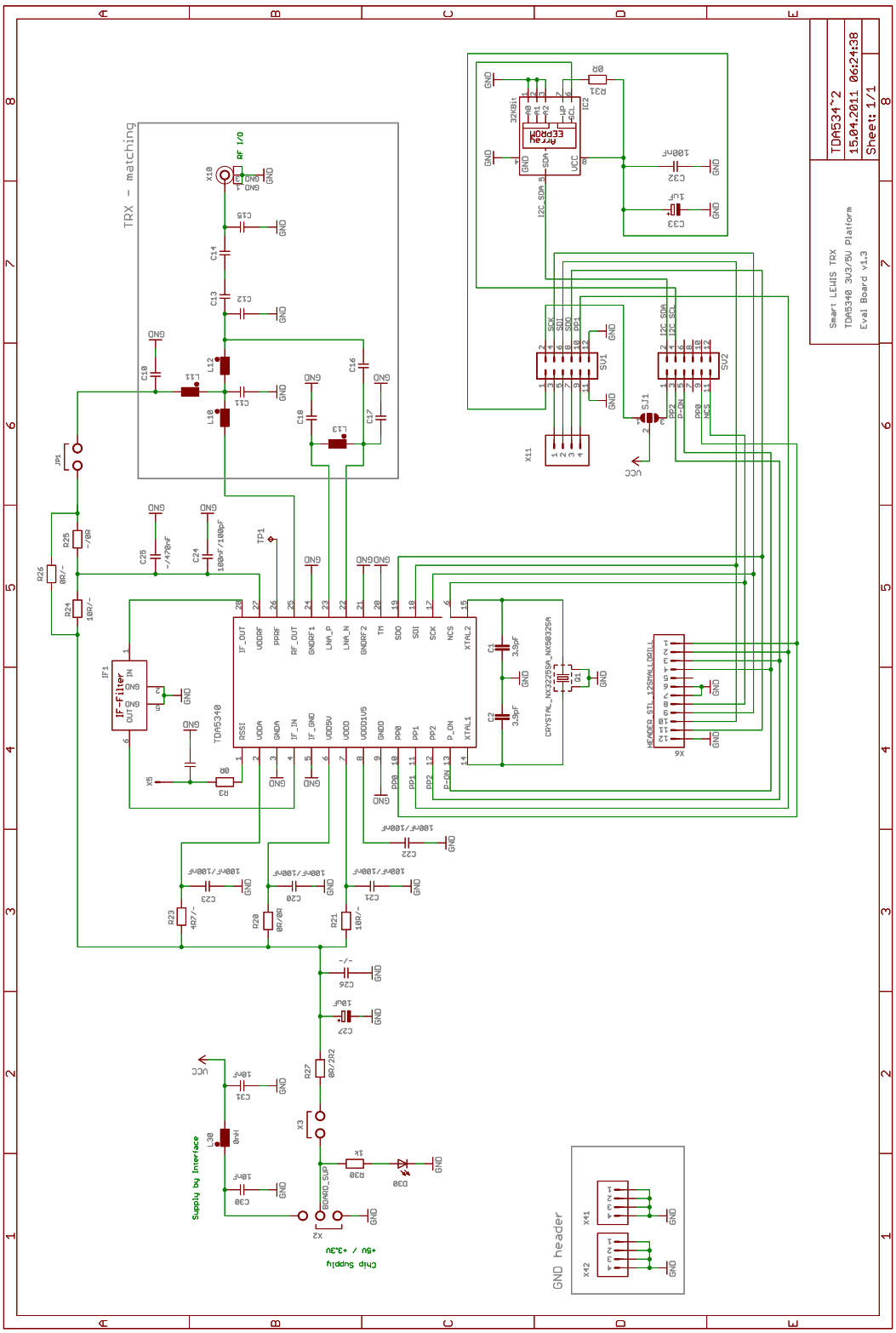


Figure 29 Test CircuitSchematic

3.3 Test Board Layout, Evaluation Board V1.3

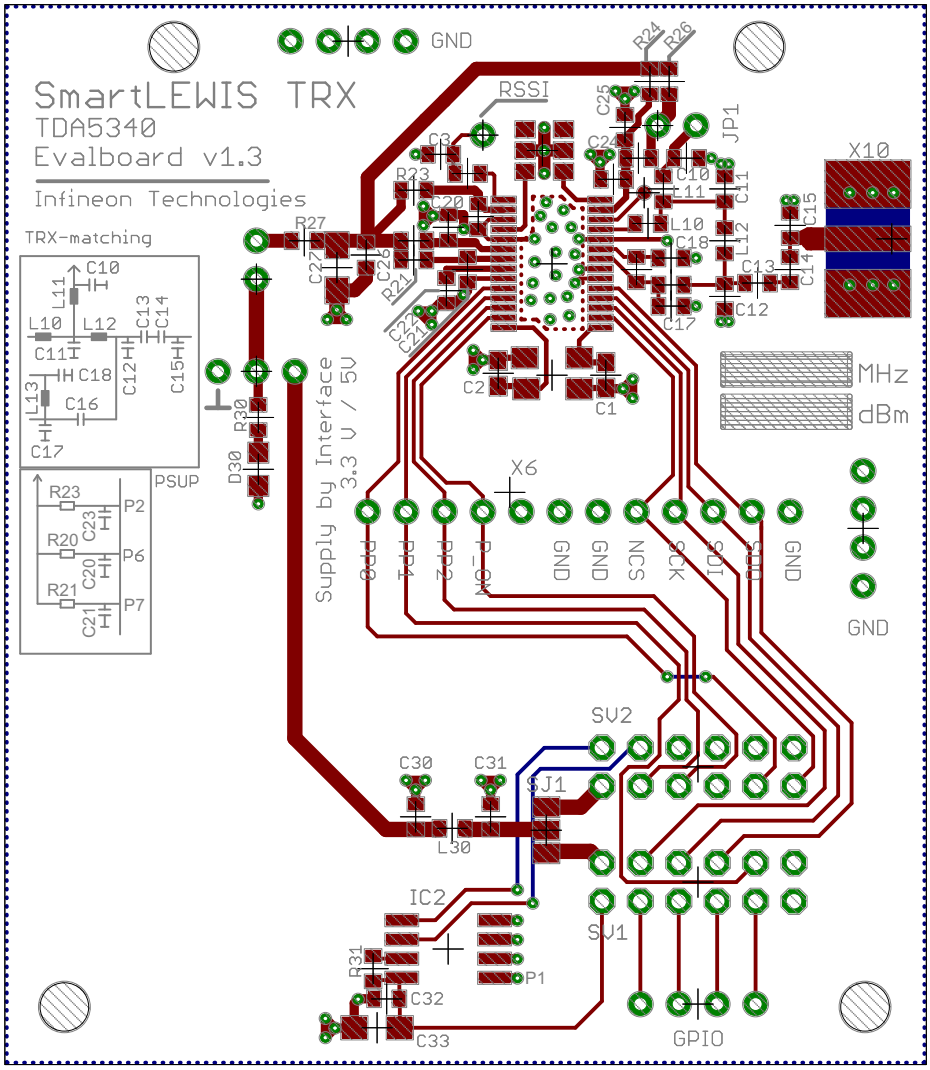


Figure 30 Test Board Layout

3.4 Bill of Material

Table 15 BOM

Part	Value	Unit	Package	Tolerance	Manufacturer	Device / Type	Voltage	Pout	Frequency Info
IC1	TDA5340		PG-TSSOP-28		Infineon				
C10	2,2	nF	0603	+/- 10%		COG or XR7			

Table 15 BOM

Part	Value	Unit	Package	Tolerance	Manufacturer	Device / Type	Voltage	Pout	Frequency Info
C11	15	pF	0603	+/- 1%		COG		10 dBm	315 MHz
	12	pF	0603	+/- 1%		COG		10 dBm	434 MHz
	3,9	pF	0603	+/- 0.1pF		COG		13 dBm	868 MHz
	3,9	pF	0603	+/- 0.1pF		COG		13 dBm	915 MHz
	3,9	pF	0603	+/- 0.1pF		COG		10 dBm	954 MHz
C12	18	pF	0603	+/- 1%		COG		10 dBm	315 MHz
	10	pF	0603	+/- 0.1pF		COG		10 dBm	434 MHz
	open	pF	0603			COG		13 dBm	868 MHz
	1	pF	0603	+/- 0.1pF		COG		13 dBm	915 MHz
	0,5	pF	0603	+/- 0.1pF		COG		10 dBm	954 MHz
C13	82	pF	0603	+/- 1%		COG		10 dBm	315 MHz
	47	pF	0603	+/- 1%		COG		10 dBm	434 MHz
	12	pF	0603	+/- 1%		COG		13 dBm	868 MHz
	100	pF	0603	+/- 1%		COG		13 dBm	915 MHz
	12	pF	0603	+/- 1%		COG		10 dBm	954 MHz
C14	82	pF	0603	+/- 1%		COG		10 dBm	315 MHz
	47	pF	0603	+/- 1%		COG		10 dBm	434 MHz
	12	pF	0603	+/- 1%		COG		13 dBm	868 MHz
	12	pF	0603	+/- 1%		COG		13 dBm	915 MHz
	12	pF	0603	+/- 1%		COG		10 dBm	954 MHz
C15	open	pF	0603			COG		10 dBm	315 MHz
	open	pF	0603			COG		10 dBm	434 MHz
	open	pF	0603			COG		13 dBm	868 MHz
	open	pF	0603			COG		13 dBm	915 MHz
	open	pF	0603			COG		10 dBm	954 MHz
C16	4.7	pF	0603	+/- 0.1pF		COG		10 dBm	315 MHz
	3.9	pF	0603	+/- 0.1pF		COG		10 dBm	434 MHz
	1.8	pF	0603	+/- 0.1pF		COG		13 dBm	868 MHz
	2.2	pF	0603	+/- 0.1pF		COG		13 dBm	915 MHz
	2.7	pF	0603	+/- 0.1pF		COG		10 dBm	954 MHz
C17	5.6	pF	0603	+/- 0.1pF		COG		10 dBm	315 MHz
	1.8	pF	0603	+/- 0.1pF		COG		10 dBm	434 MHz
	2.7	pF	0603	+/- 0.1pF		COG		13 dBm	868 MHz
	3.3	pF	0603	+/- 0.1pF		COG		13 dBm	915 MHz
	3.3	pF	0603	+/- 0.1pF		COG		10 dBm	954 MHz

Table 15 BOM

Part	Value	Unit	Package	Tolerance	Manufacturer	Device / Type	Voltage	Pout	Frequency Info
C18	12	pF	0603	+/- 1%		COG		10 dBm	315 MHz
	6.8	pF	0603	+/- 0.1pF		COG		10 dBm	434 MHz
	4.7	pF	0603	+/- 0.1pF		COG		13 dBm	868 MHz
	3.3	pF	0603	+/- 0.1pF		COG		13 dBm	915 MHz
	2.2	pF	0603	+/- 0.1pF		COG		10 dBm	954 MHz
C20	100	nF	0603	+/-10%		X7R or COG	3V3		
	100	nF	0603	+/-10%		X7R or COG	5V		
C21	100	nF	0603	+/-10%		X7R or COG	3V3		
	100	nF	0603	+/-10%		X7R or COG	5V		
C22	100	nF	0603	+/-10%		X7R or COG	3V3		
	100	nF	0603	+/-10%		X7R or COG	5V		
C23	100	nF	0603	+/-10%		X7R or COG	3V3		
	100	nF	0603	+/-10%		X7R or COG	5V		
C24	100	nF	0603	+/-10%		X7R or COG	3V3		
	100	nF	0603	+/-10%		X7R or COG	5V		
C25	open		0603			X7R or COG	3V3		
	470	nF	0603	+/-10%		X7R or COG	5V		
C26	open		0603			X7R or COG	3V3		
	open		0603			X7R or COG	5V		
C27	10	µF	SMC	+/-10%		Tantal	3V3		
	10	µF	SMC	+/-10%		Tantal	5V		
L10	56	nH	0603	+/-2%	CoilCraft	1608		10dBm	315 MHz
	39	nH	0603	+/-2%	CoilCraft	1608		10dBm	434 MHz
	12	nH	0603	+/-2%	CoilCraft	1608		13dBm	868 MHz
	12	nH	0603	+/-2%	CoilCraft	1608		13dBm	915 MHz
	5.6	nH	0603	+/-2%	CoilCraft	1608		10dBm	954 MHz
L11	220	nH	0603	+/-2%	CoilCraft	1608		10dBm	315 MHz
	82	nH	0603	+/-2%	CoilCraft	1608		10dBm	434 MHz
	220	nH	0603	+/-2%	CoilCraft	1608		13dBm	868 MHz
	100	nH	0603	+/-2%	CoilCraft	1608		13dBm	915 MHz
	220	nH	0603	+/-2%	CoilCraft	1608		10dBm	954 MHz
L12	18	nH	0603	+/-2%	CoilCraft	1608		10dBm	315 MHz
	12	nH	0603	+/-2%	CoilCraft	1608		10dBm	434 MHz
	8.2	nH	0603	+/-2%	CoilCraft	1608		13dBm	868 MHz
	8.2	nH	0603	+/-2%	CoilCraft	1608		13dBm	915 MHz
	4.7	nH	0603	+/-2%	CoilCraft	1608		10dBm	954 MHz

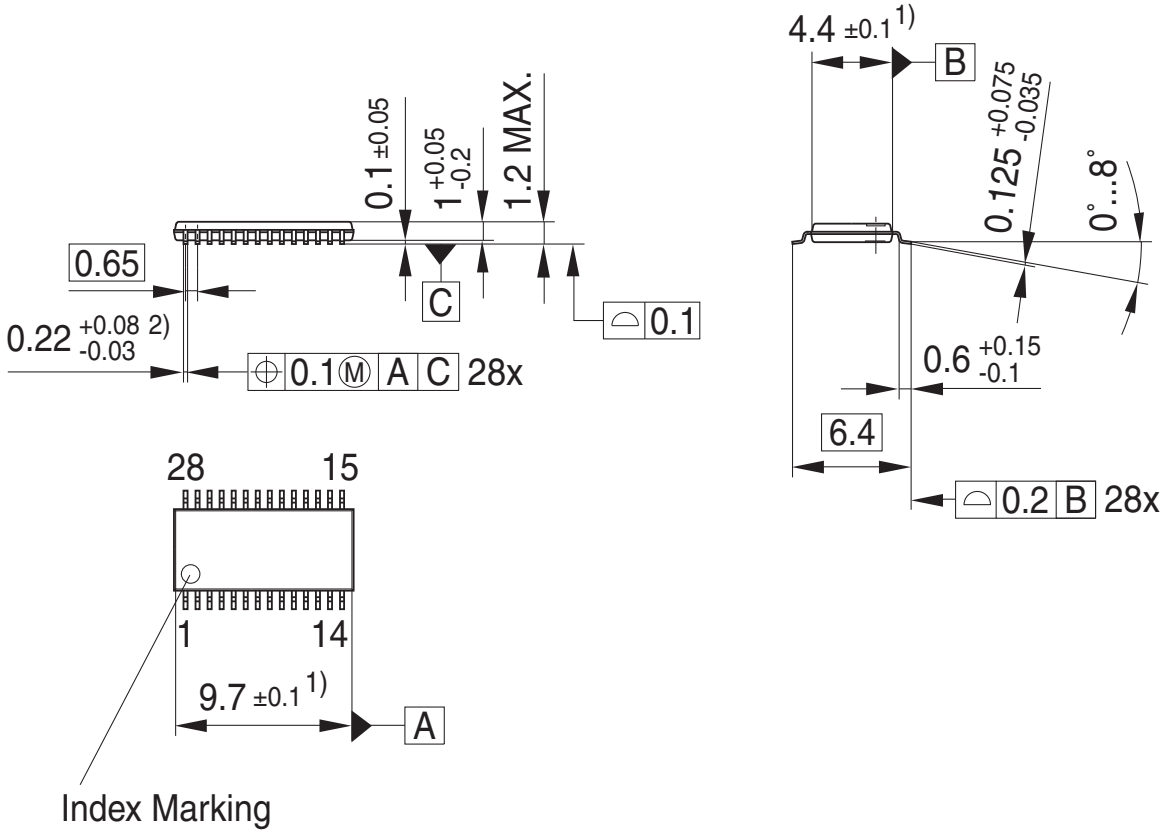
Table 15 BOM

Part	Value	Unit	Package	Tolerance	Manufacturer	Device / Type	Voltage	Pout	Frequency Info
L13	33	nH	0603	+/-2%	CoilCraft	1608		10dBm	315 MHz
	27	nH	0603	+/-2%	CoilCraft	1608		10dBm	434 MHz
	8.2	nH	0603	+/-2%	CoilCraft	1608		13dBm	868 MHz
	8.2	nH	0603	+/-2%	CoilCraft	1608		13dBm	915 MHz
	8.2	nH	0603	+/-2%	CoilCraft	1608		10dBm	954 MHz
R20	0	Ω	0603				3V3		
	0	Ω	0603				5V		
R21	10	Ω	0603	+/- 5%			3V3		
	open	Ω	0603				5V		
R23	4.7	Ω	0603	+/- 5%			3V3		
	open	Ω	0603				5V		
R24	10	Ω	0603	+/- 5%			3V3		
	open	Ω	0603				5V		
R25	open	Ω	0603				3V3		
	0	Ω	0603				5V		
R26	0	Ω	0603				3V3		
	open	Ω	0603				5V		
R27	0	Ω	0603				3V3		
	2.2	Ω	0603	+/- 5%			5V		
Q1	21.948717 MHz		NX3225SA		NDK; Frischer Electronics	CL = 12pF			
IF1	SFECF10?M7EA00				Murata	BW = 330kHz			
Interface components / optional									
IC2	AT24C32C-SH-B or? AT24C512		SOIC8			EEPROM / Board detection			
C1	open								
C2	open								
C3	open								
C30	open								
C31	open								
C32	100	nF	0603	+/-10%		X7R or COG			
C33	open								
L30	0	Ω	0603						
D30	LED					status indication LED			

Table 15 BOM

Part	Value	Unit	Package	Tolerance	Manufacturer	Device / Type	Voltage	Pout	Frequency Info
R3	0	Ω	0603						
R30	1	kΩ	0603	+/- 5%					
R31	open								
SJ1	connect to SV2					Supply from UWLINK main board	3V3		
	connect to SV2 and SV1						5V		
JP1	2 pins					Power amplifier current			
SV1	2x6 pin					UWLINK connector			
SV2	2x6 pin					UWLINK connector			
X2	3 pin					Supply selection / ext or UWLINK			
X3	2 pin					Chip supply current			
X5	1 pin					analog RSSI test point			
X6	12 pin					Digital Chip I/O			
X10	SMA socket				SAMTEC	RF Input / Output			
X11	4 pin					GND Pin Header			
X41	4 pin					GND Pin Header			
X42	4 pin					GND Pin Header			

4 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Figure 31 PG-TSSOP-28 Package Outline (green package)

Table 16 Ordering Information

Type	Ordering Code	Package
TDA5340	SP000803722	PG-TSSOP-28

You can find all of our packages, sorts of packaging and other on our Infinion Internet Page”Products”: **http://www.infineon.com/products**

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