PTFA192001E
PTFA192001F

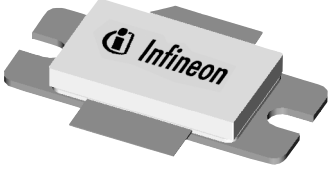
green Product

Thermally-Enhanced High Power RF LDMOS FETs
200 W, 1930 – 1990 MHz

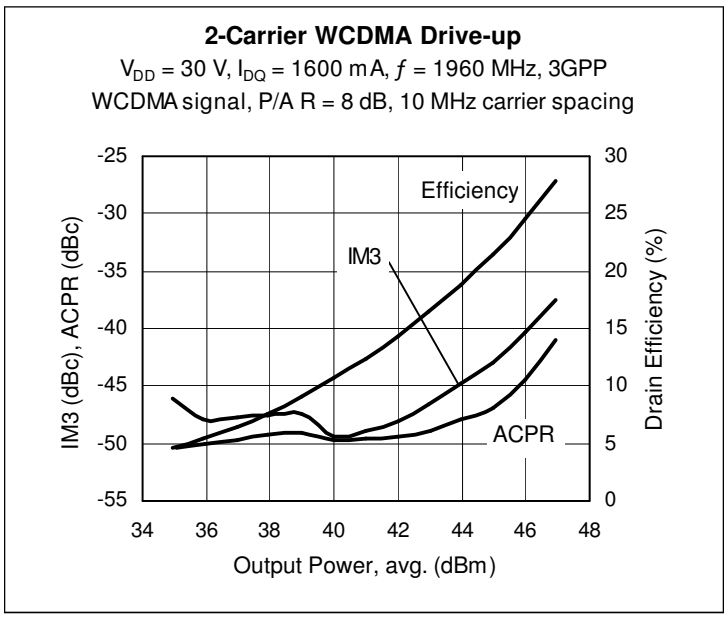
Description

The PTFA192001E and PTFA192001F are 200-watt LDMOS FETs intended for single- and two-carrier WCDMA and CDMA applications from 1930 to 1990 MHz. Features include input and output matching, and thermally-enhanced packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA192001E
Package H-36260-2



PTFA192001F
Package H-37260-2



Features

- Pb-free, RoHS-compliant and thermally-enhanced packages
- Broadband internal matching
- Typical two-carrier WCDMA performance at 1990 MHz, 30 V
  - Average output power = 47.0 dBm
  - Linear Gain = 15.9 dB
  - Efficiency = 27%
  - Intermodulation distortion = –36 dBc
  - Adjacent channel power = –41 dBc
- Typical single-carrier WCDMA performance at 1960 MHz, 30 V, 3GPP signal, P/AR = 7.5 dB
  - Average output power = 48.5 dBm
  - Linear Gain = 15.9 dB
  - Efficiency = 34%
  - Intermodulation distortion = –37 dBc
  - Adjacent channel power = –40 dBc
- Typical CW performance, 1960 MHz, 30 V
  - Output power at P–1dB = 240 W
  - Efficiency = 57%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 5:1 VSWR @ 30 V, 200 W (CW) output power

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics

WCDMA Measurements (tested in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 1.8 A, P_{OUT} = 50 W average
f_1 = 1985 MHz, f_2 = 1995 MHz, 3GPP signal, channel bandwidth = 3.84 MHz , peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	15.3	15.9	—	dB
Drain Efficiency	η_D	26.5	27	—	%
Intermodulation Distortion	IMD	—	–36	–34	dBc

Two-tone Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 1.6 A, P_{OUT} = 200 W PEP, f = 1960 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	15.9	—	dB
Drain Efficiency	η_D	—	41	—	%
Intermodulation Distortion	IMD	—	–30	—	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
Drain Leakage Current	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.05	—	Ω
Operating Gate Voltage	V_{DS} = 30 V, I_{DQ} = 1.8 A	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	625	W
Above 25°C derate by		3.57	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 200 W CW)	$R_{\theta JC}$	0.28	°C/W

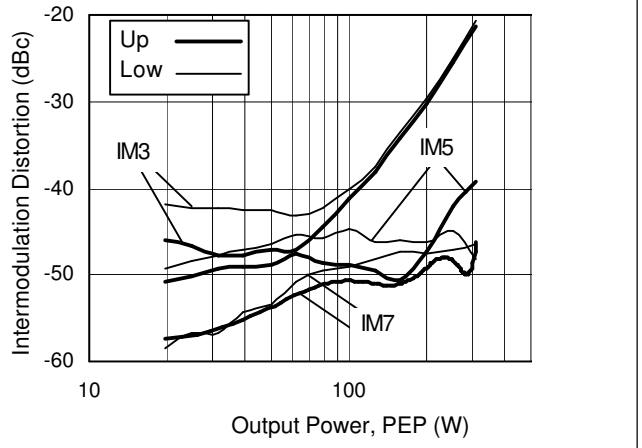
Ordering Information

Type and Version	Package Type	Package Description	Marking
PTFA192001E V4	H-36260-2	Thermally-enhanced slotted flange, single-ended	PTFA192001E
PTFA192001F V4	H-37260-2	Thermally-enhanced earless flange, single-ended	PTFA192001F

Typical Performance (data taken in a production test fixture)

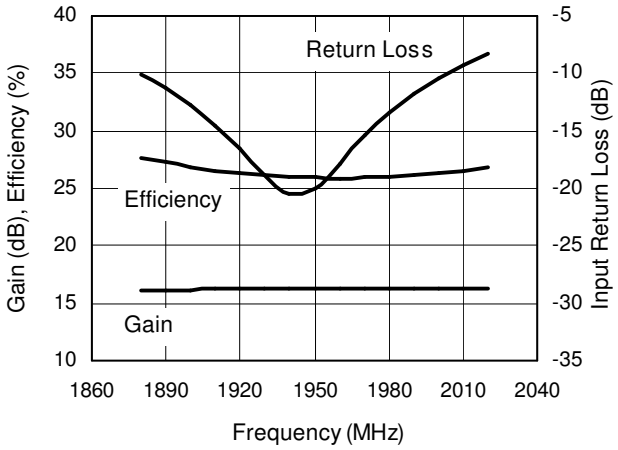
Intermodulation Distortion Products v. Output Power

V_{DD} = 30 V, I_{DQ} = 1600 mA,
f_1 = 1957.5 MHz, f_2 = 1962.5 MHz



Broadband Performance

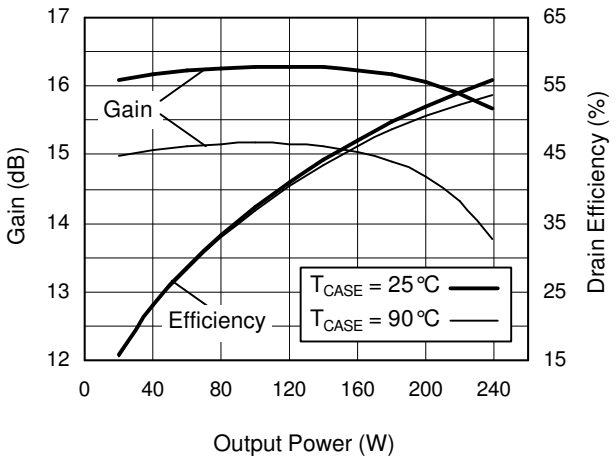
V_{DD} = 30 V, I_{DQ} = 1600 mA, P_{OUT} = 50 W



Typical Performance (cont.)

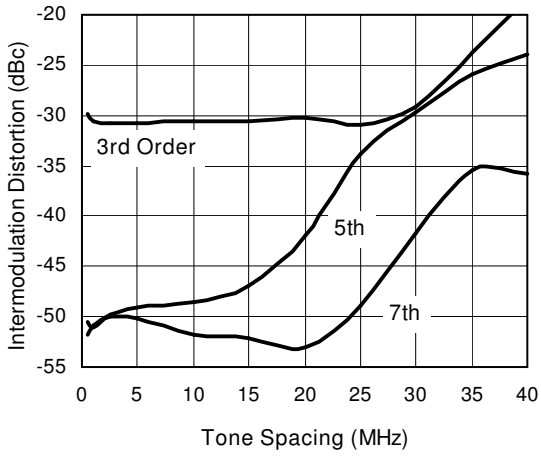
Power Sweep, CW Conditions

V_{DD} = 30 V, I_{DQ} = 1800 mA, f = 1990 MHz



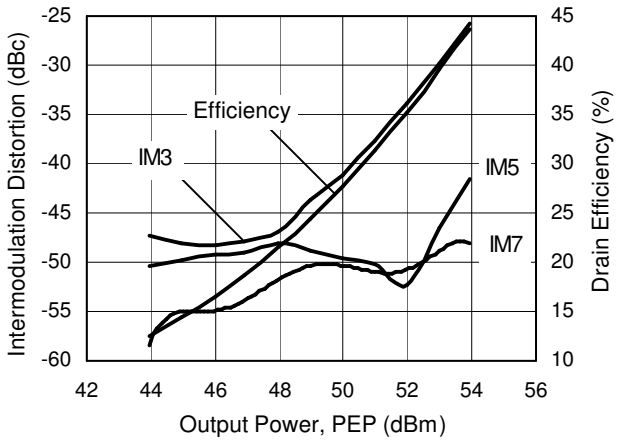
Intermodulation Distortion Products vs. Tone Spacing

V_{DD} = 30 V I_{DQ} = 1800 mA , f = 1960 MHz,
P_{OUT} = 53 dBm PEP



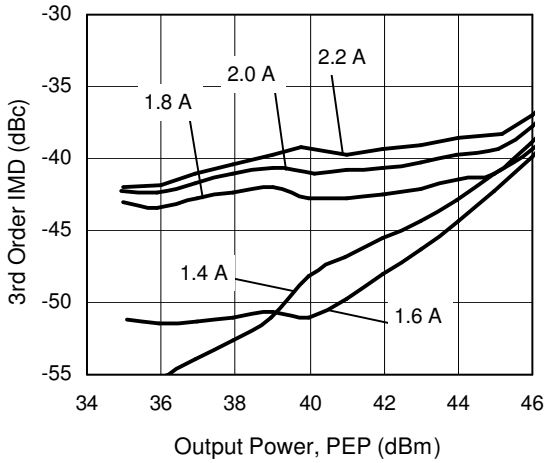
2-Tone Drive-up

V_{DD} = 30 V, I_{DQ} = 1600 mA,
f = 1960 MHz, tone spacing = 1 MHz



Two-carrier WCDMA at Selected Biases

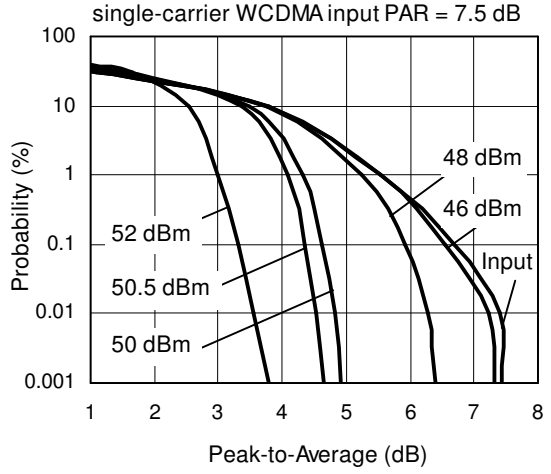
V_{DD} = 30 V, f = 1960 MHz, 3GPP WCDMA signal,
P/AR = 8 dB, 10 MHz carrier spacing, series show I_{DQ}



Typical Performance (cont.)

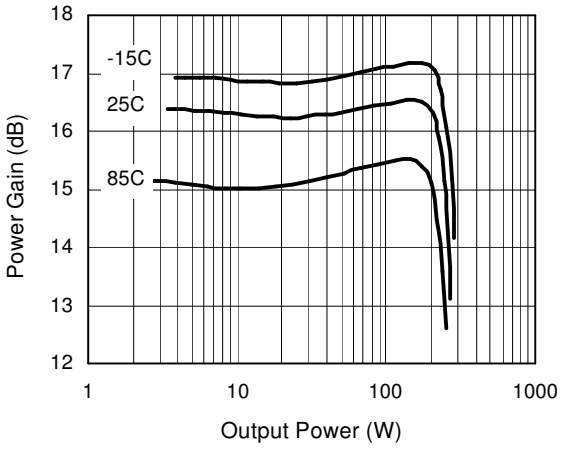
Output Peak-to-Average Ratio Compression (PARC) at various Power levels

V_{DD} = 30 V, I_{DQ} = 1500 mA, f = 1990 MHz, single-carrier WCDMA input PAR = 7.5 dB



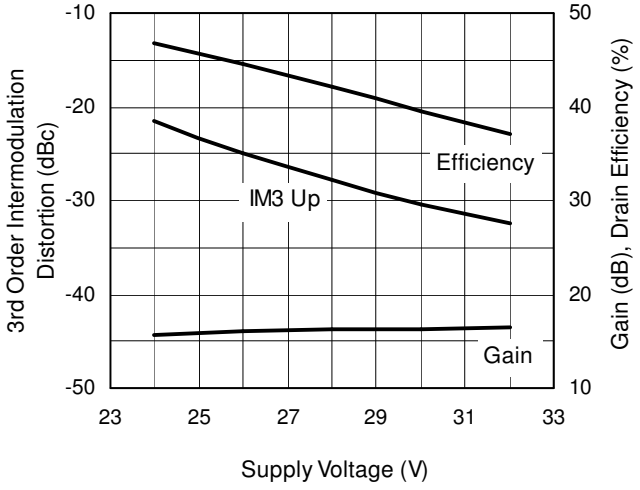
Power Gain vs. Power Sweep (CW) over Temperature

V_{DD} = 30 V, I_{DQ} = 1500 mA, f = 1990 MHz



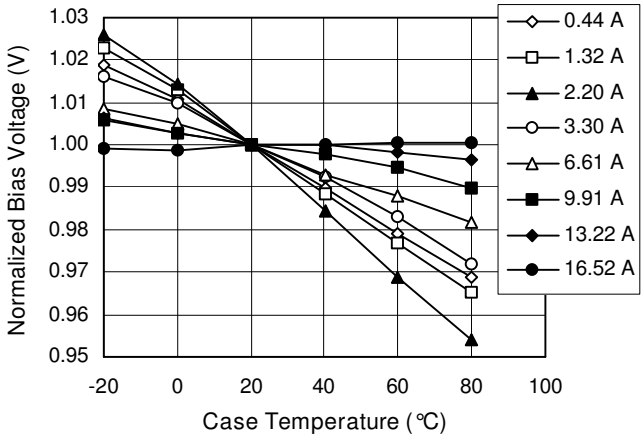
Voltage Sweep

I_{DQ} = 1800 mA, f = 1960 MHz, tone spacing = 1 MHz, Output Power (PEP) = 53 dBm

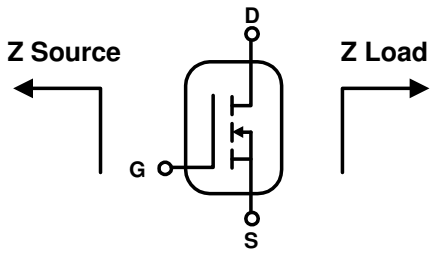


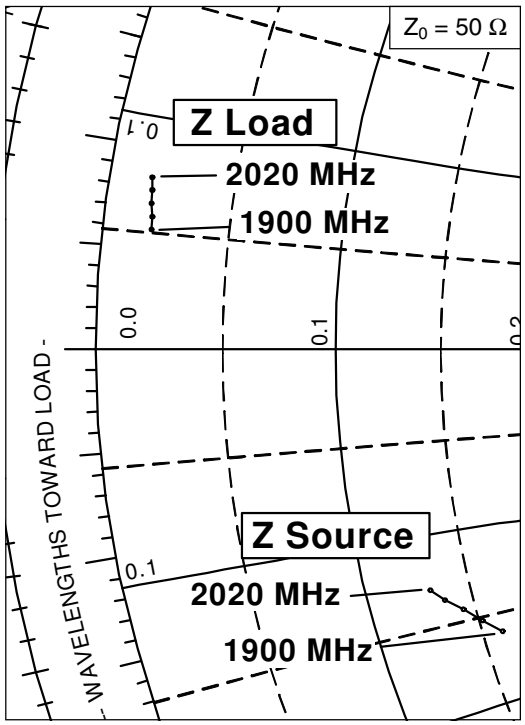
Bias Voltage vs. Temperature

Voltage normalized to typical gate voltage, series show current



Broadband Circuit Impedance

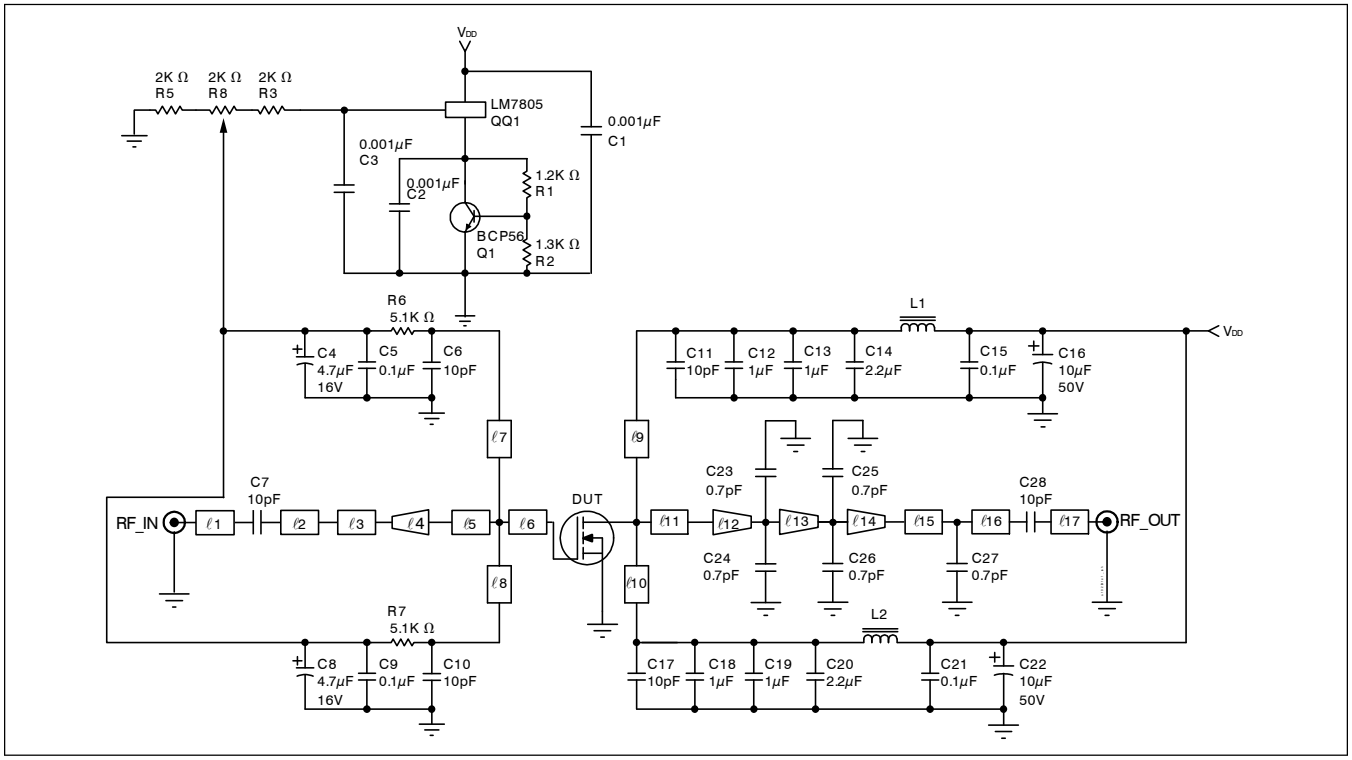




Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
1900	8.033	–8.054	0.943	2.60
1930	7.611	–7.612	0.932	2.87
1960	7.230	–7.197	0.886	3.15
1990	6.839	–6.839	0.863	3.44
2020	6.541	–6.496	0.829	3.71

See next page for circuit information

Reference Circuit



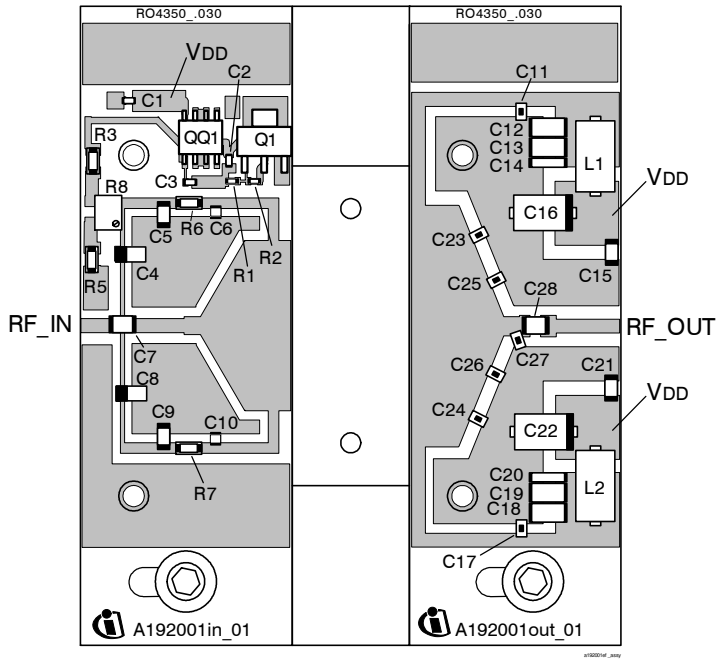
Reference circuit schematic for ƒ = 1960 MHz

Circuit Assembly Information			
DUT	PTFA192001E or PTFA192001F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 3.48	Rogers RO4350	1 oz. copper

Microstrip	Electrical Characteristics at 1960 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.038 λ, 50.0 Ω	3.51 x 1.70	0.138 x 0.067
ℓ2	0.071 λ, 50.0 Ω	6.60 x 1.70	0.260 x 0.067
ℓ3	0.022 λ, 43.0 Ω	2.01 x 2.16	0.079 x 0.085
ℓ4 (taper)	0.060 λ, 43.0 Ω / 6.9 Ω	5.28 x 2.16 / 20.32	0.208 x 0.085 / 0.800
ℓ5	0.040 λ, 6.9 Ω	3.33 x 20.32	0.131 x 0.800
ℓ6	0.026 λ, 6.9 Ω	2.21 x 20.32	0.087 x 0.800
ℓ7, ℓ8	0.123 λ, 60.0 Ω	11.48 x 1.24	0.452 x 0.049
ℓ9, ℓ10	0.258 λ, 50.9 Ω	23.88 x 1.65	0.940 x 0.065
ℓ11	0.067 λ, 5.0 Ω	5.59 x 28.91	0.220 x 1.138
ℓ12 (taper)	0.017 λ, 5.0 Ω / 7.2 Ω	1.42 x 28.91 / 19.51	0.056 x 1.138 / 0.768
ℓ13 (taper)	0.024 λ, 7.2 Ω / 12.3 Ω	2.08 x 19.51 / 10.67	0.082 x 0.768 / 0.420
ℓ14 (taper)	0.019 λ, 12.3 Ω / 41 Ω	1.78 x 10.67 / 2.29	0.070 x 0.420 / 0.090
ℓ15	0.009 λ, 41.0 Ω	0.79 x 2.29	0.031 x 0.090
ℓ16	0.021 λ, 41.0 Ω	1.85 x 2.29	0.073 x 0.090
ℓ17	0.096 λ, 50.0 Ω	8.99 x 1.70	0.354 x 0.067

[1]Electrical characteristics are rounded.

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4, C8	Capacitor, 4.7 µF, 16 V	Digi-Key	PCS3475CT-ND
C5, C9, C15, C21	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C6, C10	Ceramic capacitor, 10 pF	ATC	100A 100
C7, C28	Ceramic capacitor, 10 pF	ATC	100B 100
C11, C17	Capacitor, 10 pF	AVX	08051J100GBTTR
C12, C13, C18, C19	Ceramic capacitor, 1 µF	Digi-Key	445-1411-1-ND
C14, C20	Capacitor, 2.2 µF	Digi-Key	445-1447-2-ND
C16, C22	Tantalum capacitor, 10 µF, 50 V	Garrett Electronics	TPSE106K050R0400
C23, C24, C25, C26, C27	Capacitor, 0.7 pF	AVX	08051J0R7BBTTR
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infinion Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3, R5	Chip resistor 2 k-ohms	Digi-Key	P2KECT-ND
R6, R7	Chip resistor 5.1 k-ohms	Digi-Key	P5.1KECT-ND
R8	Potentiometer 2 k-ohms	Digi-Key	3224W-202ETR-ND

**Gerber files for this circuit available on request*

Package Outline Specifications

Package H-36260-2

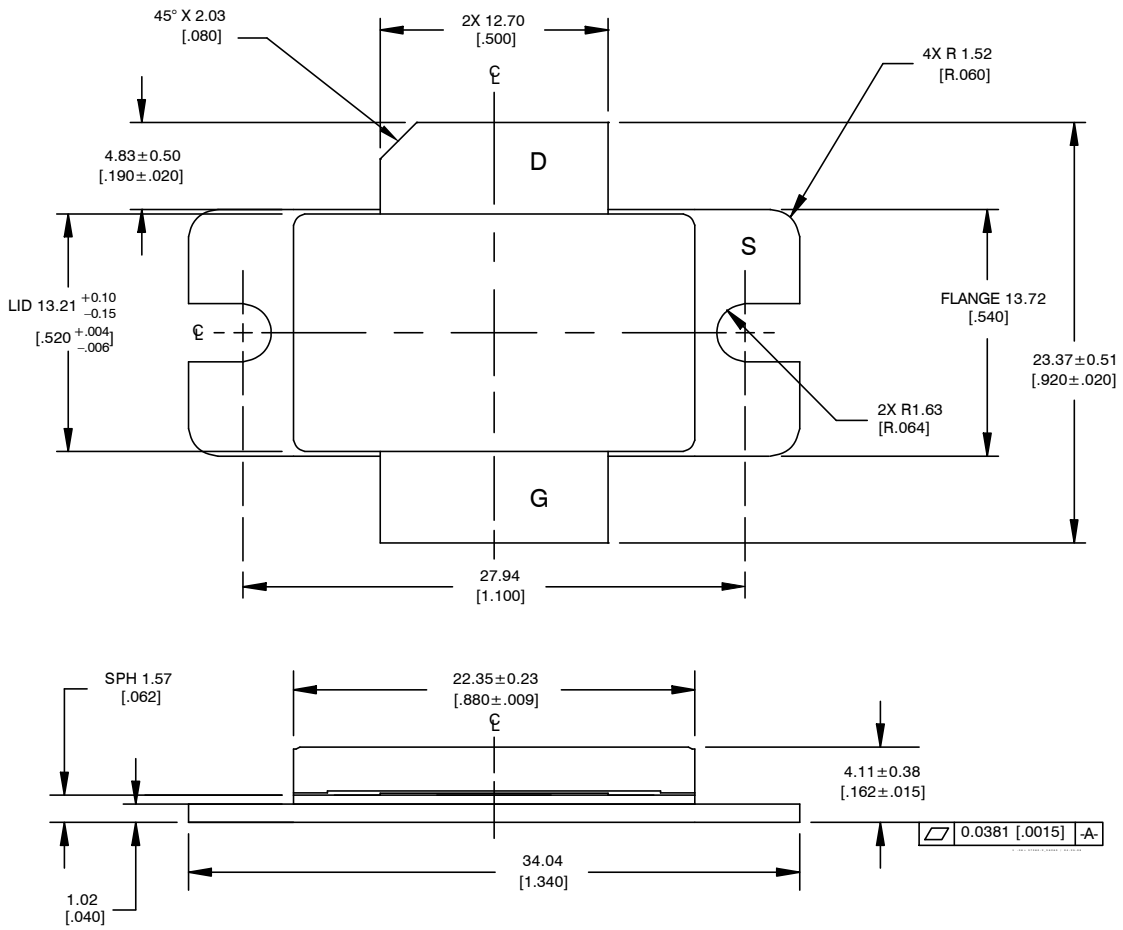


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Pins: D = drain, S = source, G = gate.
3. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
4. Gold plating thickness:
   S, D, G - flange & leads: 1.14 ± 0.38 micron [45 ± 15 microinch]
5. All tolerances ± 0.25 [0.01] / ± 0.127 [.005] unless specified otherwise.
6. Primary dimensions are mm. Alternate dimensions are inches.

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Package Outline Specifications (cont.)

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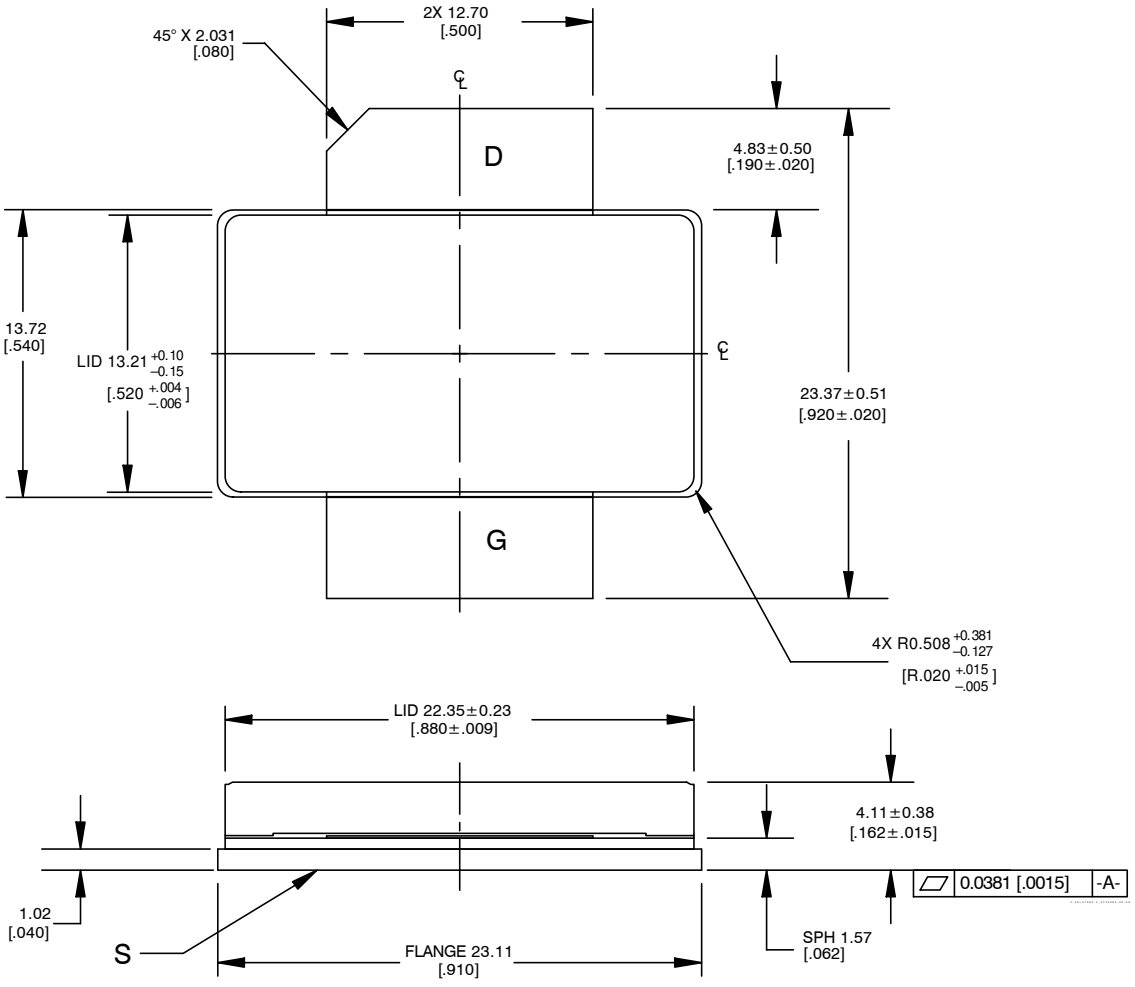

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Revision History:	2008-05-15	Data Sheet
Previous Version:	2007-12-06, Data Sheet	

Page	**Subjects (major changes since last revision)**
1, 3, 9, 10	Update to product V4. Update package outline diagrams.
1, 2	Update specifications.

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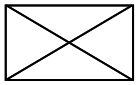

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