

Thermally-Enhanced High Power RF LDMOS FETs 100 W, 1930 – 1990 MHz

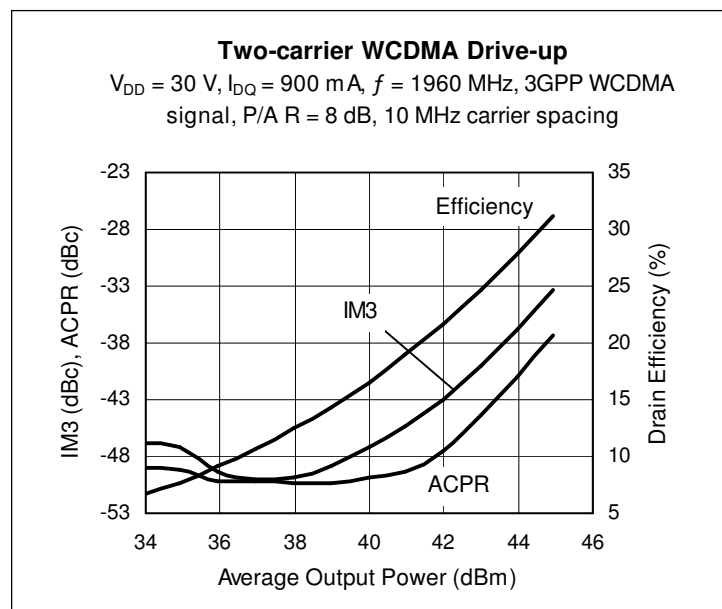
Description

The PTFA191001E and PTFA191001F are thermally-enhanced, 100-watt, internally-matched LDMOS FETs intended for WCDMA, IS-95 and CDMA2000 applications. They are characterized for single- and two-carrier WCDMA operation from 1930 to 1990 MHz. Thermally-enhanced packaging provides the coolest operation available.

PTFA191001E
 Package H-36248-2



PTFA191001F
 Package H-37248-2



Features

- Thermally-enhanced packages, Pb-free and RoHS-compliant
- Broadband internal matching
- Typical two-carrier WCDMA performance at 1960 MHz, 30 V
 - Average output power = 25 W
 - Linear Gain = 17.0 dB
 - Efficiency = 27.5%
 - Intermodulation distortion = -37 dBc
 - Adjacent channel power = -41.0 dBc
- Typical two-carrier IS-95 performance at 1930 MHz, 30 V
 - Average output power = 25 W
 - Efficiency = 28%
 - Intermodulation distortion = -35 dBc @ 1.2288
 - Adjacent channel power = -51 dBm
- Typical CW performance, 1960 MHz, 30 V
 - Output power at P-1dB = 130 W
 - Efficiency = 56%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 30 V, 100 W (CW) output power

All published data at $T_{CASE} = 25^{\circ}\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics

WCDMA Measurements (tested in Infineon test fixture)

$V_{DD} = 30\text{ V}$, $I_{DQ} = 900\text{ mA}$, $P_{OUT} = 44\text{ dBm}$ average

$f_1 = 1955\text{ MHz}$, $f_2 = 1965\text{ MHz}$, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	16	17.0	—	dB
Drain Efficiency	η_D	26	28	—	%
Intermodulation Distortion	IMD	—	-37	-35	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
On-State Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.08	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}$, $I_{DQ} = 900\text{ mA}$	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA

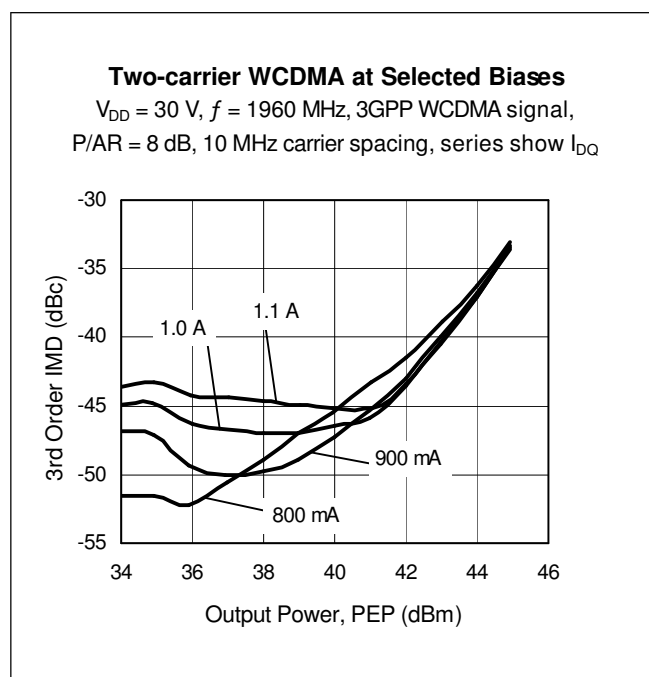
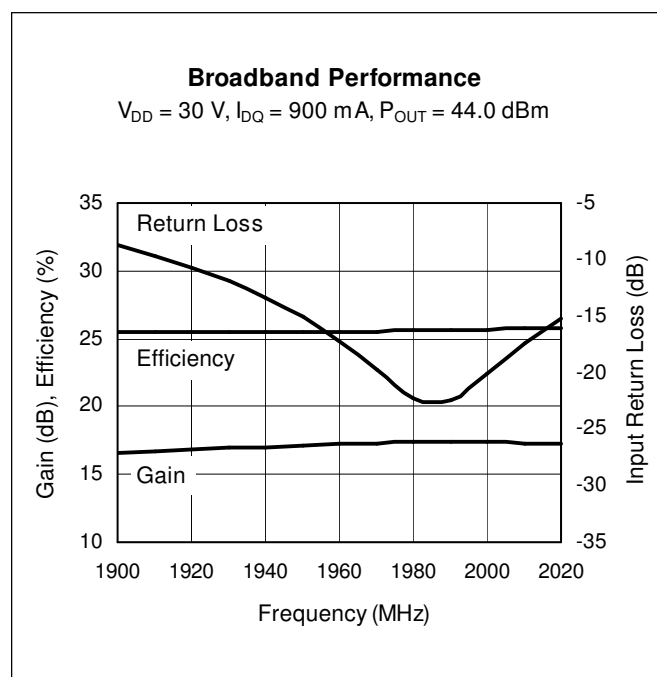
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	-0.5 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Total Device Dissipation Above 25 $^{\circ}\text{C}$ derate by	P_D	417	W
		2.38	W/ $^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$, 100 W CW)	$R_{\theta JC}$	0.42	$^{\circ}\text{C/W}$

Ordering Information

Type and Version	Package Type	Package Description	Marking
PTFA191001E V4	H-36248-2	Thermally-enhanced slotted flange, single-ended	PTFA191001E
PTFA191001F V4	H-37248-2	Thermally-enhanced earless flange, single-ended	PTFA191001F

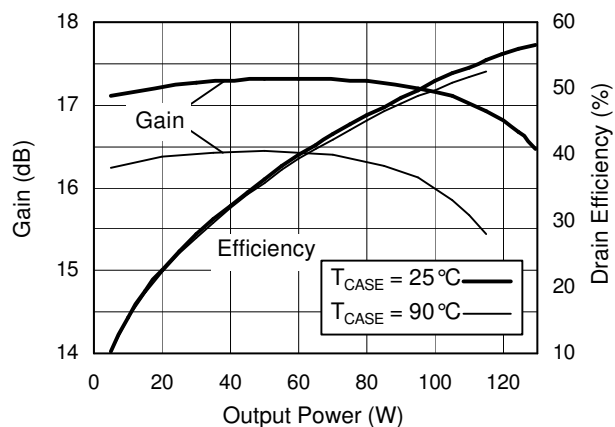
Typical Performance (data taken in a production test fixture)



Typical Performance (cont.)

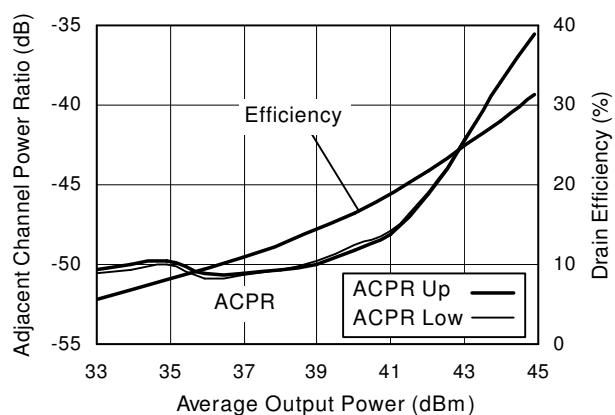
Power Sweep, CW Conditions

$V_{DD} = 30\text{ V}$, $I_{DQ} = 900\text{ mA}$, $f = 1960\text{ MHz}$



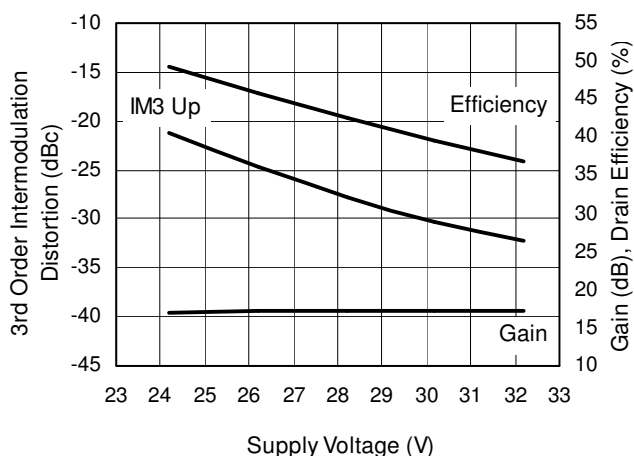
Single-carrier WCDMA Drive-up

$V_{DD} = 30\text{ V}$, $I_{DQ} = 900\text{ mA}$, $f = 1960\text{ MHz}$,
3GPP WCDMA signal, TM1 w/16 DPCH, 67% clipping,
PAR = 8.5 dB, 3.84 MHz BW



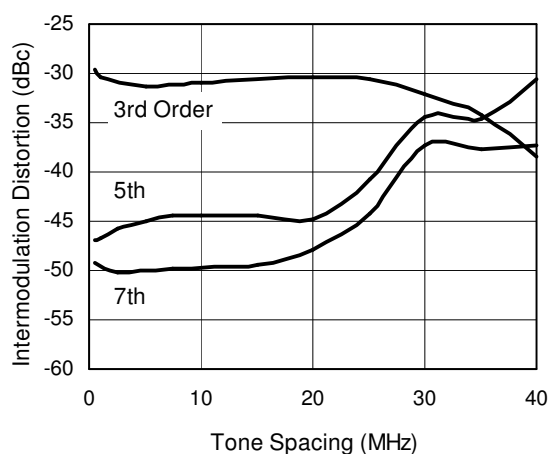
Voltage Sweep

$I_{DQ} = 900\text{ mA}$, $f = 1960\text{ MHz}$,
tone spacing = 1 MHz, P_{OUT} (PEP) = 50 dBm

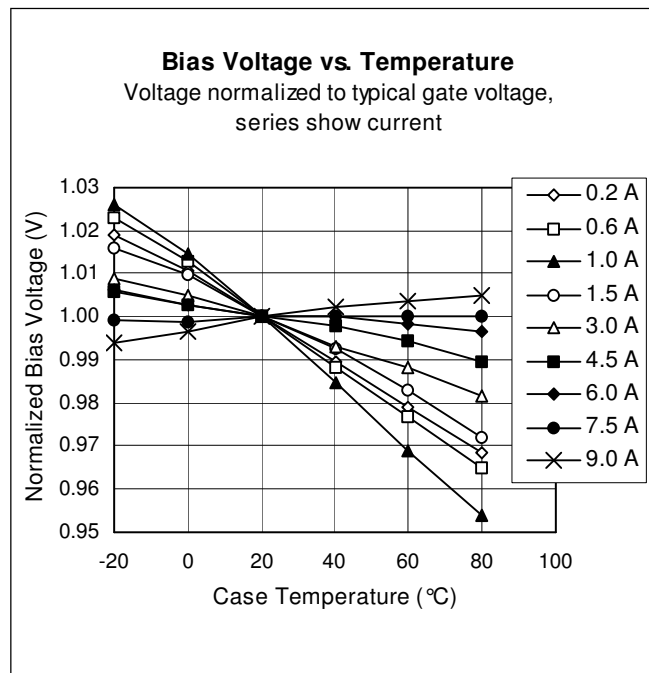
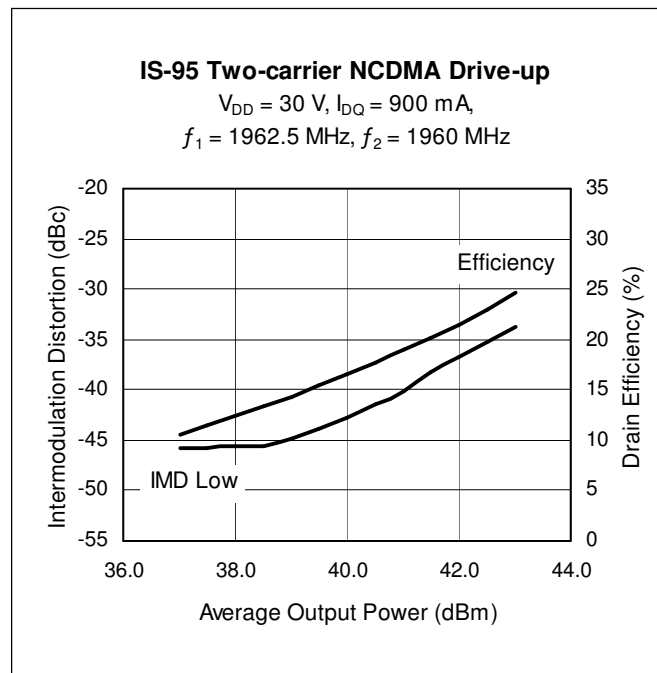


Intermodulation Distortion Products vs. Tone Spacing

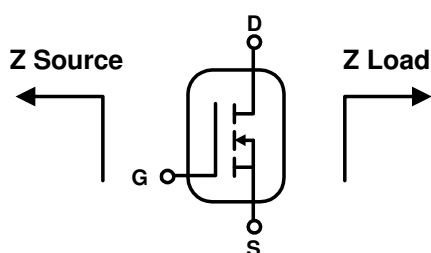
$V_{DD} = 30\text{ V}$, $I_{DQ} = 900\text{ mA}$, $f = 1960\text{ MHz}$,
 $P_{OUT} = 49.5\text{ dBm PEP}$



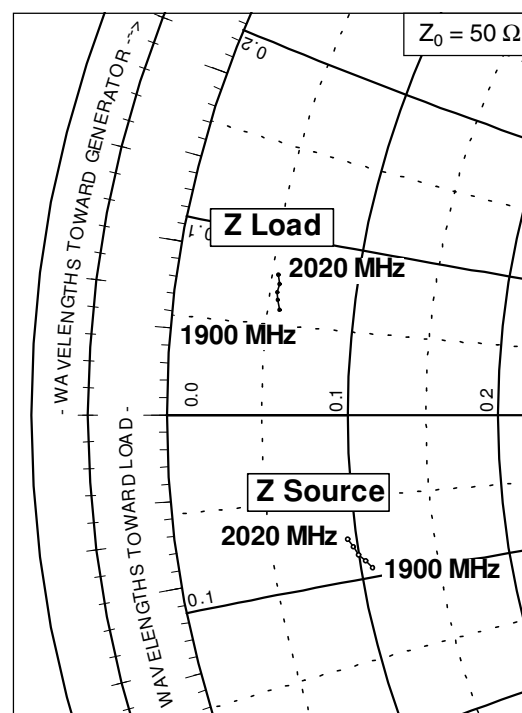
Typical Performance (cont.)



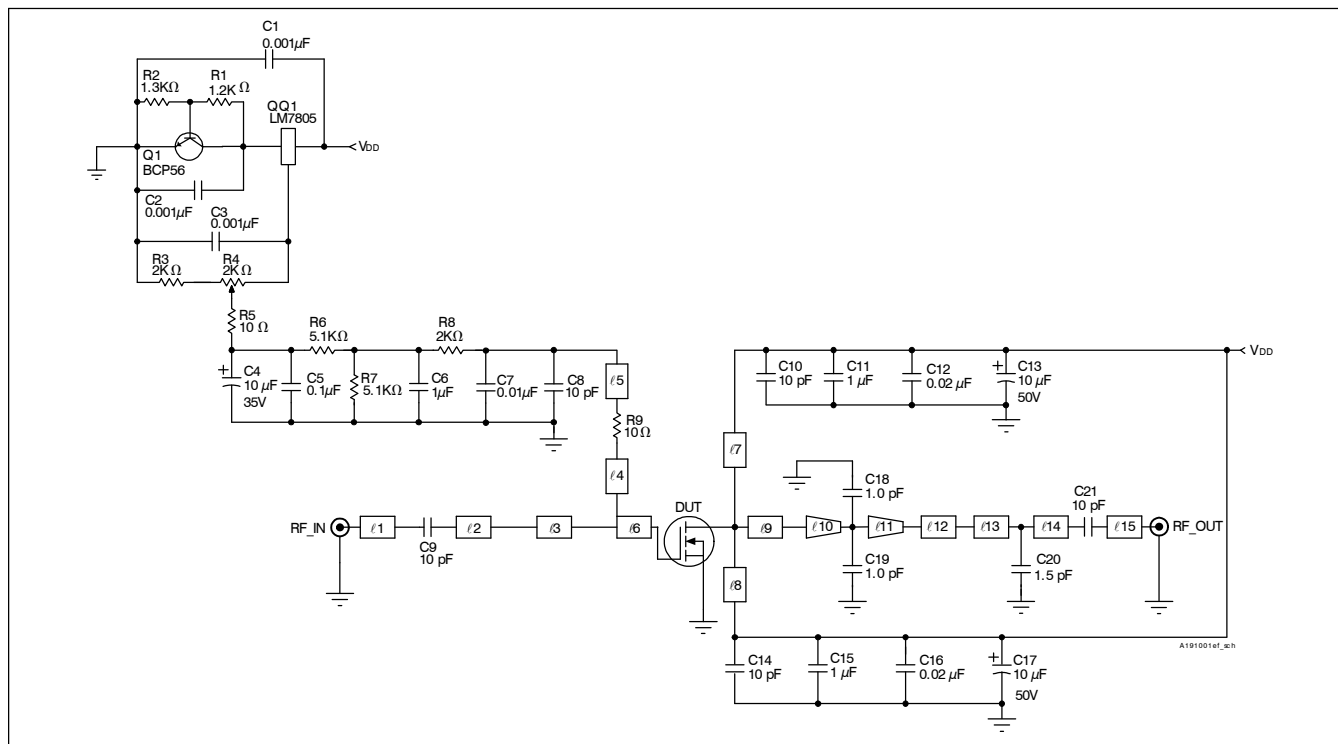
Broadband Circuit Impedance



Frequency MHz	Z Source Ω		Z Load Ω	
	R	jX	R	jX
1900	5.41	-4.79	2.88	2.91
1930	5.23	-4.54	2.81	3.18
1960	5.05	-4.32	2.77	3.39
1990	4.92	-4.06	2.80	3.63
2020	4.79	-3.81	2.73	3.89



Reference Circuit



Reference circuit schematic for $f = 1960 \text{ MHz}$

Circuit Assembly Information

DUT	PTFA191001E or PTFA191001F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, $\epsilon_r = 4.5$	Rogers TMM4	2 oz. copper

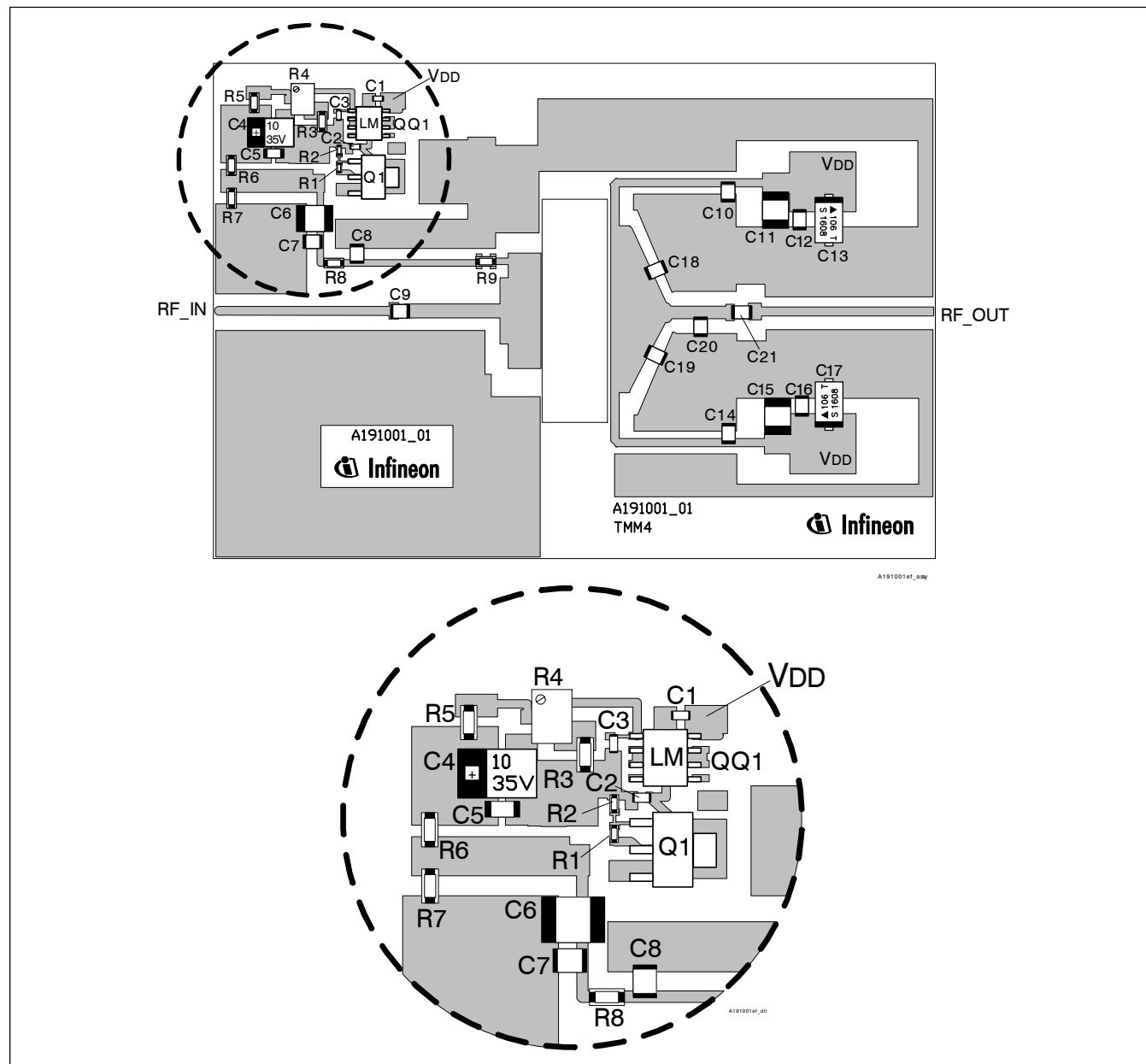
Microstrip	Electrical Characteristics at 1960 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ_1	0.352λ , 50.4Ω	29.31 x 1.42	1.154 x 0.056
ℓ_2	0.183λ , 38.0Ω	14.86 x 2.16	0.585 x 0.085
ℓ_3	0.016λ , 11.4Ω	1.22 x 10.19	0.048 x 0.401
ℓ_4	0.026λ , 60.0Ω	2.16 x 0.99	0.085 x 0.039
ℓ_5	0.213λ , 60.0Ω	18.03 x 0.99	0.710 x 0.039
ℓ_6	0.069λ , 6.9Ω	5.11 x 17.86	0.201 x 0.703
ℓ_7	0.289λ , 54.5Ω	24.16 x 1.24	0.951 x 0.049
ℓ_8	0.289λ , 54.5Ω	24.16 x 1.24	0.951 x 0.049
ℓ_9	0.040λ , 5.0Ω	2.95 x 25.40	0.116 x 1.000
ℓ_{10} (taper)	0.050λ , $5.0 \Omega / 11.8 \Omega$	3.81 x 25.40 / 9.80	0.150 x 1.000 / 0.386
ℓ_{11} (taper)	0.027λ , $11.8 \Omega / 31.0 \Omega$	2.18 x 9.80 / 2.84	0.086 x 0.386 / 0.112
ℓ_{12}	0.009λ , 31.0Ω	0.76 x 2.87	0.030 x 0.113
ℓ_{13}	0.034λ , 41.0Ω	2.82 x 1.91	0.111 x 0.075
ℓ_{14}	0.086λ , 41.0Ω	7.06 x 1.91	0.278 x 0.075
ℓ_{15}	0.364λ , 50.4Ω	30.33 x 1.42	1.194 x 0.056

Reference Circuit (cont.)

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 μ F	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 μ F, 35 V	Digi-Key	PCS6106TR-ND
C5	Capacitor, 0.1 μ F	Digi-Key	PCC104BCT-ND
C6, C11, C15	Capacitor, 1.0 μ F	Digi-Key	920C 105
C7	Capacitor, 0.01 μ F	Digi-Key	200B 103
C8, C9, C10, C14, C21	Capacitor (ceramic), 10 pF	ATC	100B 100
C12, C16	Capacitor, 0.02 μ F	Digi-Key	200B 203
C13, C17	Tantalum capacitor, 10 μ F, 50 V	Garrett Electronics	TPS106K050R0400
C18, C19	Capacitor (ceramic), 1.0 pF	ATC	100B 1R0
C20	Capacitor (ceramic), 1.5 pF	ATC	100B 1R5
Q1	Transistor	Infineon	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor, 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor, 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3, R8	Chip resistor, 2 k-ohms	Digi-Key	P2KECT-ND
R4	Potentiometer, 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5, R9	Chip resistor, 10 ohms	Digi-Key	P10ECT-ND
R6, R7	Chip resistor, 5.1 k-ohms	Digi-Key	P5.1KECT-ND

See next page for reference circuit assembly diagram

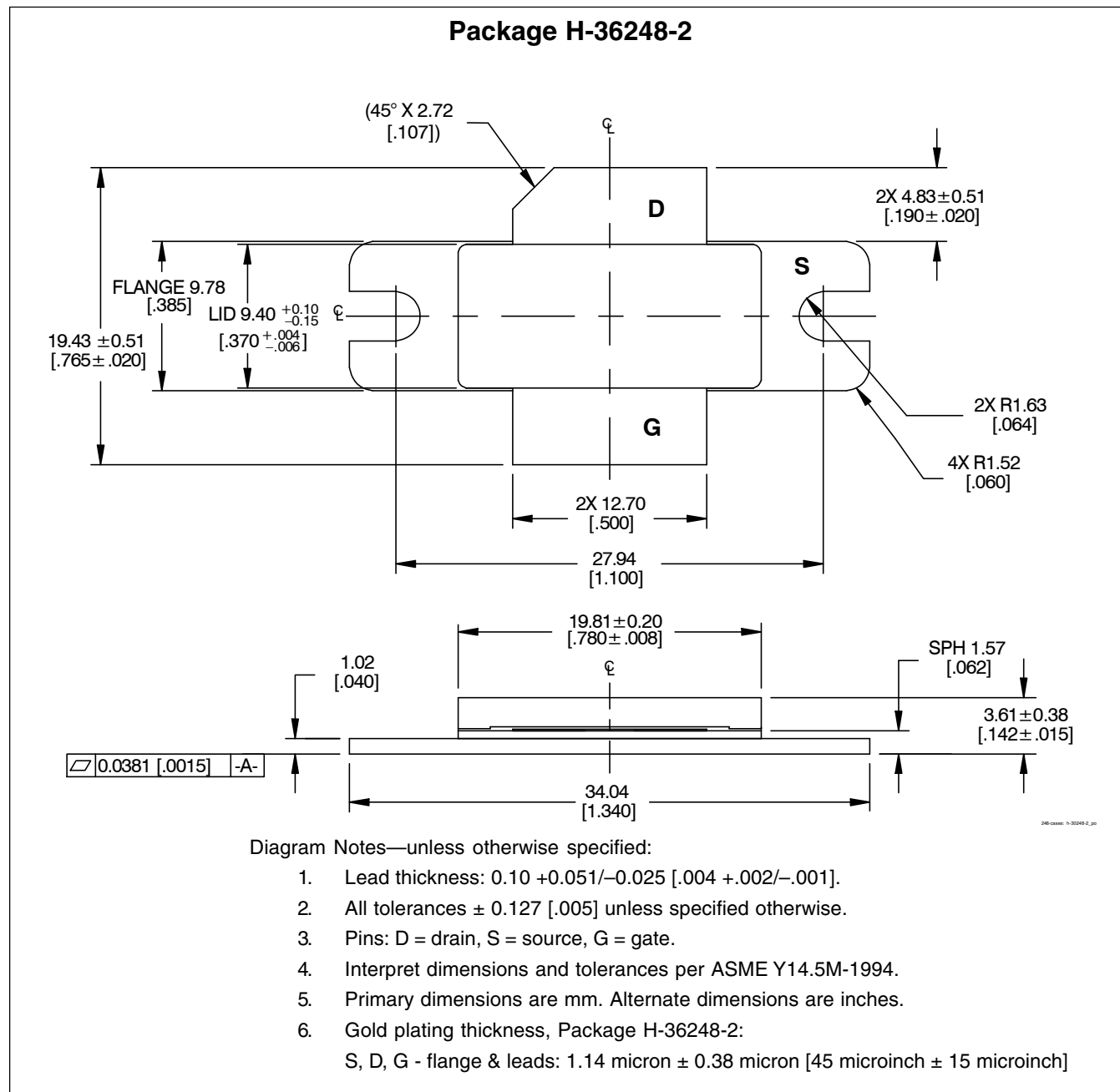
Reference Circuit (cont.)



Reference circuit assembly diagram* (not to scale)

*Gerber Files for this circuit available on request

Package Outline Specifications



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Package Outline Specifications (cont.)

Package H-37248-2

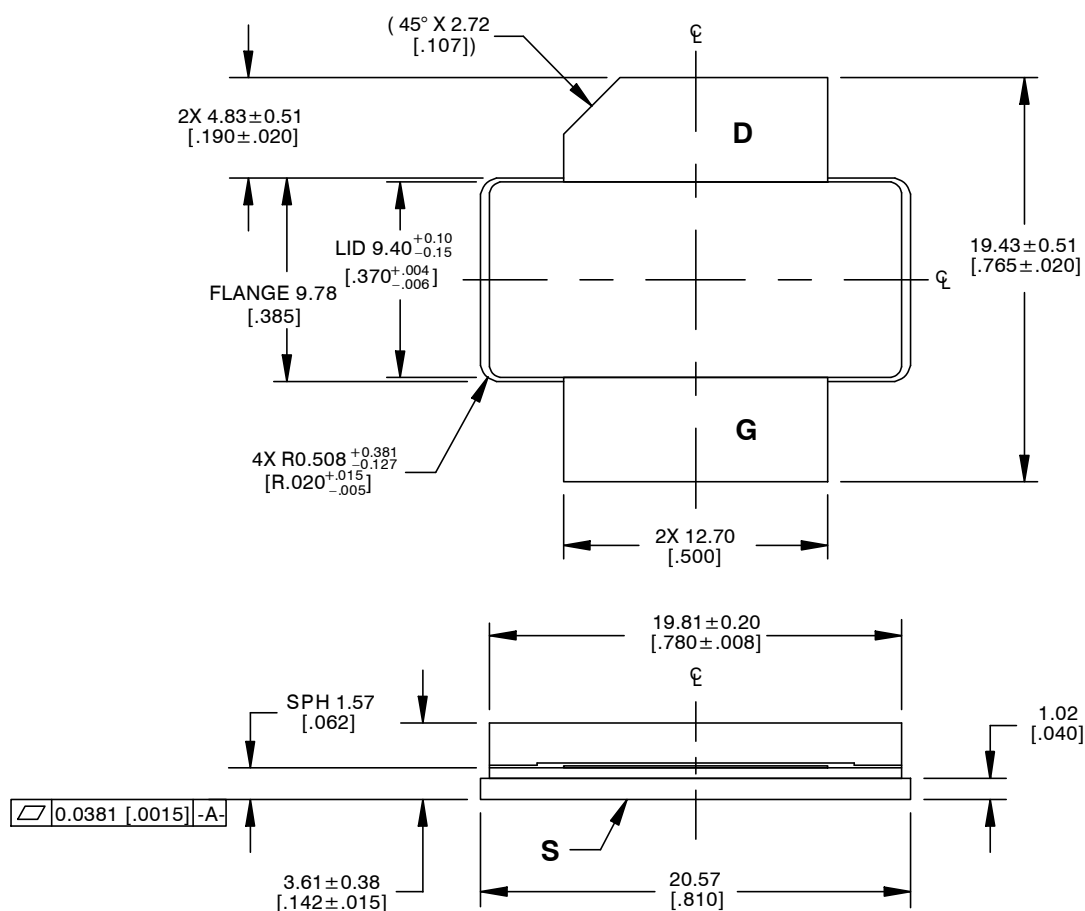


Diagram Notes—unless otherwise specified:

1. Lead thickness: $0.10^{+0.051}_{-0.025}$ [$.004^{+.002}_{-.001}$].
2. All tolerances ± 0.127 [$.005$] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
S, D, G - flange & leads: $1.14\ \mu\text{m} \pm 0.38\ \mu\text{m}$ [$45\ \mu\text{in} \pm 15\ \mu\text{in}$]

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Previous Version: Rev. 02, 2005-08-11, Data Sheet; Rev. 03, 2007-06-25

Page	Subjects (major changes since last revision)
1, 10	Update company information.
1, 3, 9, 10	Update to product V4, with new package technologies. Update package outline diagrams.

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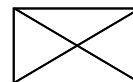
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