

Thermally-Enhanced High Power RF LDMOS FETs 170 W, 725 – 770 MHz

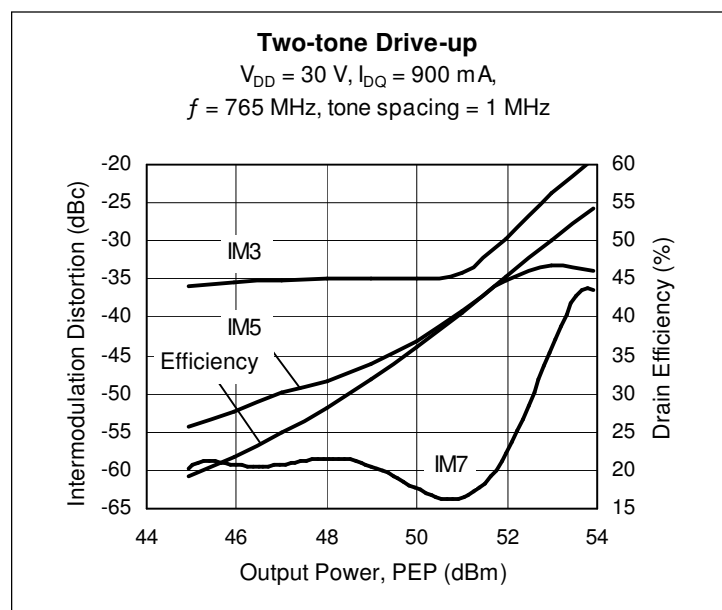
Description

The PTFA071701E and PTFA071701F are 170-watt, LDMOS FETs designed for use in cellular power amplifiers in the 725 to 770 MHz frequency band. Features include internal I/O matching, and thermally-enhanced, ceramic open-cavity packages. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA071701E
Package H-36248-2



PTFA071701F
Package H-37248-2



Features

- Thermally-enhanced packages, Pb-free and RoHS-compliant
- Broadband internal matching
- Typical CDMA2000 performance at 770 MHz, 30 V
 - Average output power = 35 W
 - Linear Gain = 18 dB
 - Efficiency = 34%
 - Adjacent channel power = -50 dBc
- Typical CW performance, 770 MHz, 30 V
 - Output power at P-1dB = 165 W
 - Efficiency = 62%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 30 V, 170 W (CW) output power

RF Characteristics

Two-carrier WCDMA Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

$V_{DD} = 30\text{ V}$, $I_{DQ} = 1.0\text{ A}$, $P_{OUT} = 40\text{ W}$ average,
 $f_1 = 760$, $f_2 = 770\text{ MHz}$, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8.1 dB at 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	18.5	—	dB
Drain Efficiency	η_D	—	32	—	%
Adjacent Channel Power Ratio	ACPR	—	-36	—	dBc

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

$V_{DD} = 30\text{ V}$, $I_{DQ} = 0.9\text{ A}$, $P_{OUT} = 150\text{ W PEP}$, $f = 765\text{ MHz}$, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	18.0	18.7	—	dB
Drain Efficiency	η_D	44	46	—	%
Intermodulation Distortion	IMD	—	-29.5	-28	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
On-State Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.07	—	Ω
Operating Gate Voltage	$V_{DS} = 30\text{ V}$, $I_{DQ} = 1.0\text{ A}$	V_{GS}	2.0	2.48	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA

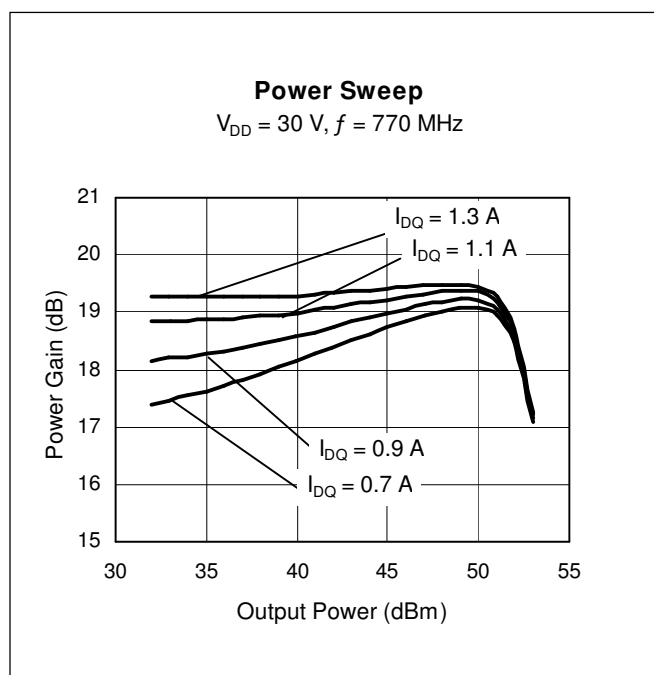
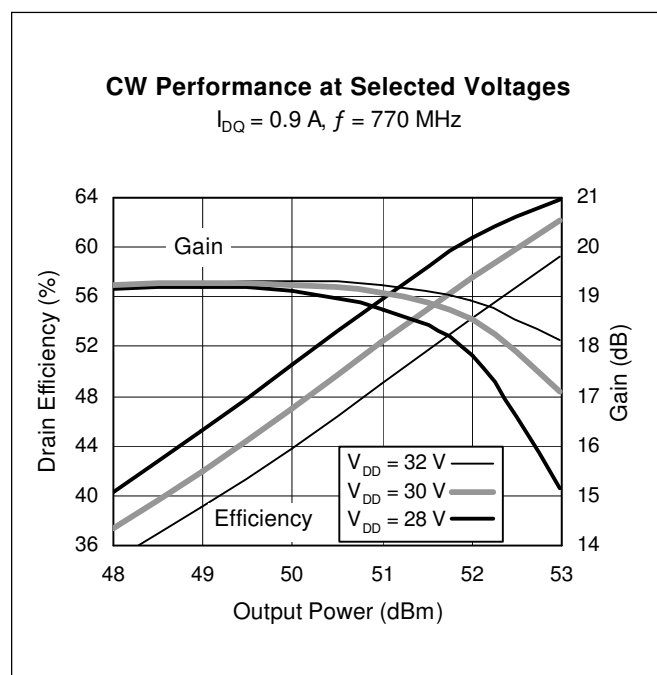
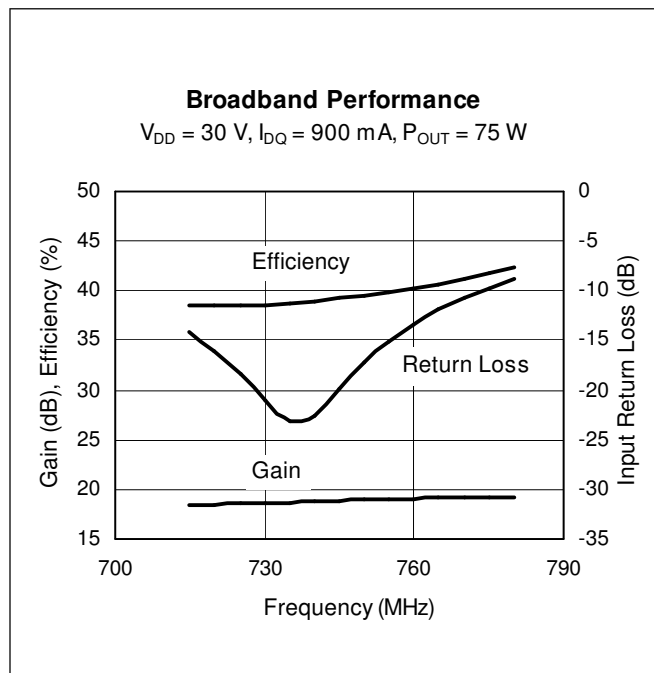
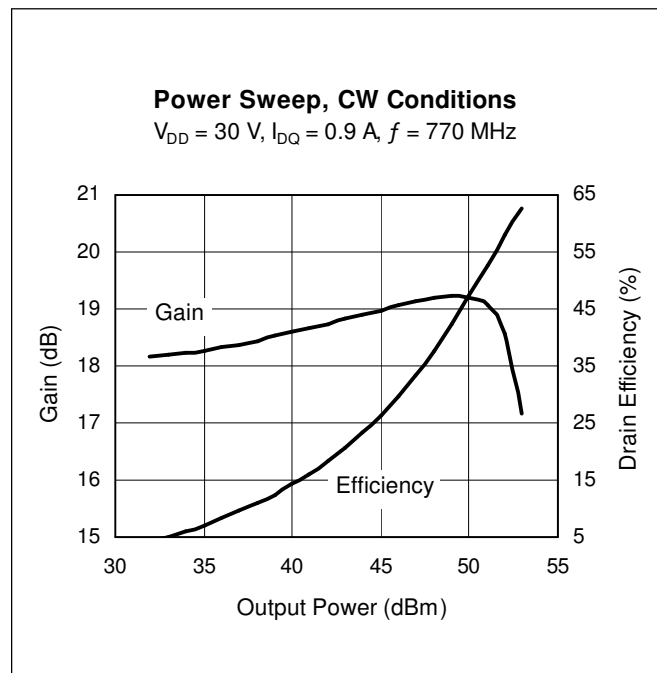
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	-0.5 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$, 170 W CW)	$R_{\theta JC}$	0.38	$^{\circ}\text{C/W}$

Ordering Information

Type and Version	Package Type	Package Description	Shipping
PTFA071701E V4	H-36248-2	Slotted flange, single-ended	Tray
PTFA071701E V4 R250	H-36248-2	Slotted flange, single-ended	Tape & Reel 250 pcs
PTFA071701F V4	H-37248-2	Earless flange, single-ended	Tray
PTFA071701F V4 R250	H-37248-2	Earless flange, single-ended	Tape & Reel 250 pcs

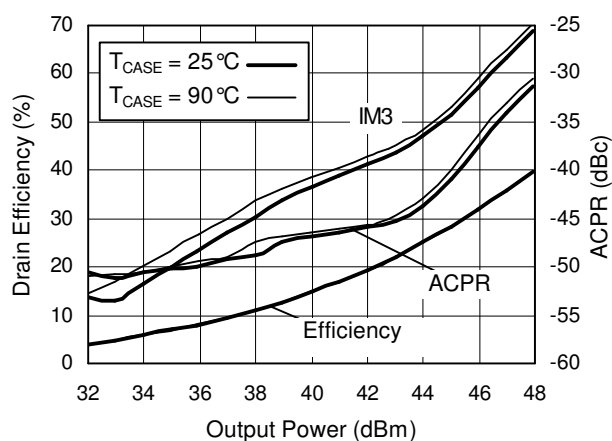
Typical Performance (data taken in a production test fixture)



Typical Performance (cont.)

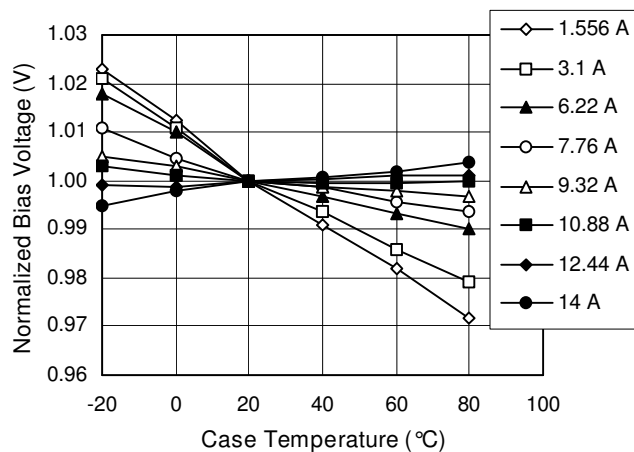
2-Carrier WCDMA Performance

$V_{DD} = 30\text{ V}$, $I_{DQ} = 1.0\text{ A}$, $f = 765\text{ MHz}$

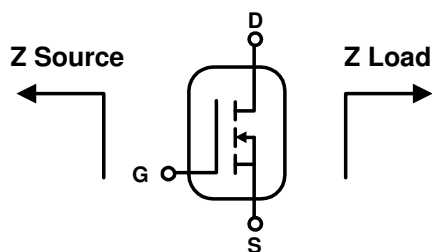


Bias Voltage vs. Temperature

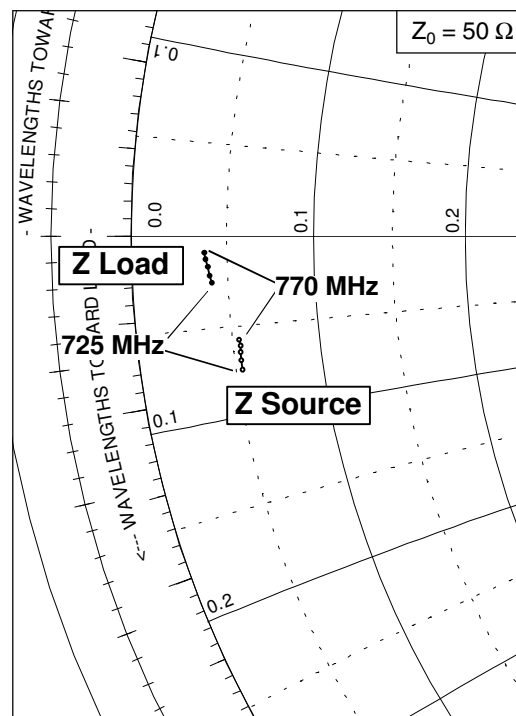
Voltage normalized to typical gate voltage, series show current



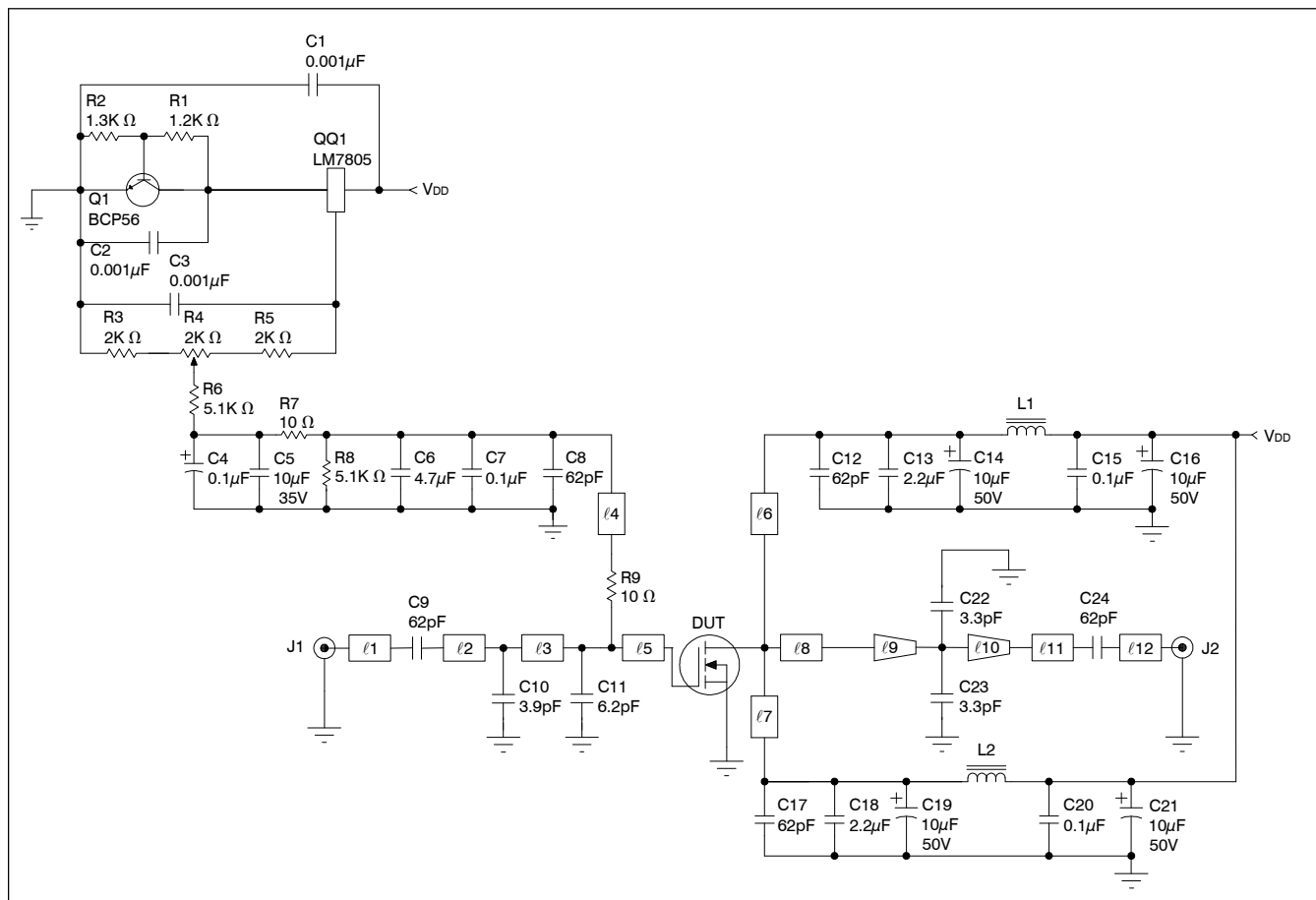
Broadband Circuit Impedance



Frequency MHz	Z Source Ω		Z Load Ω	
	R	jX	R	jX
725	2.690	-3.730	2.070	-1.27
736	2.680	-3.470	2.020	-1.08
748	2.700	-3.240	1.980	-0.84
759	2.720	-3.050	1.930	-0.64
770	2.690	-2.890	1.900	-0.46



Reference Circuit



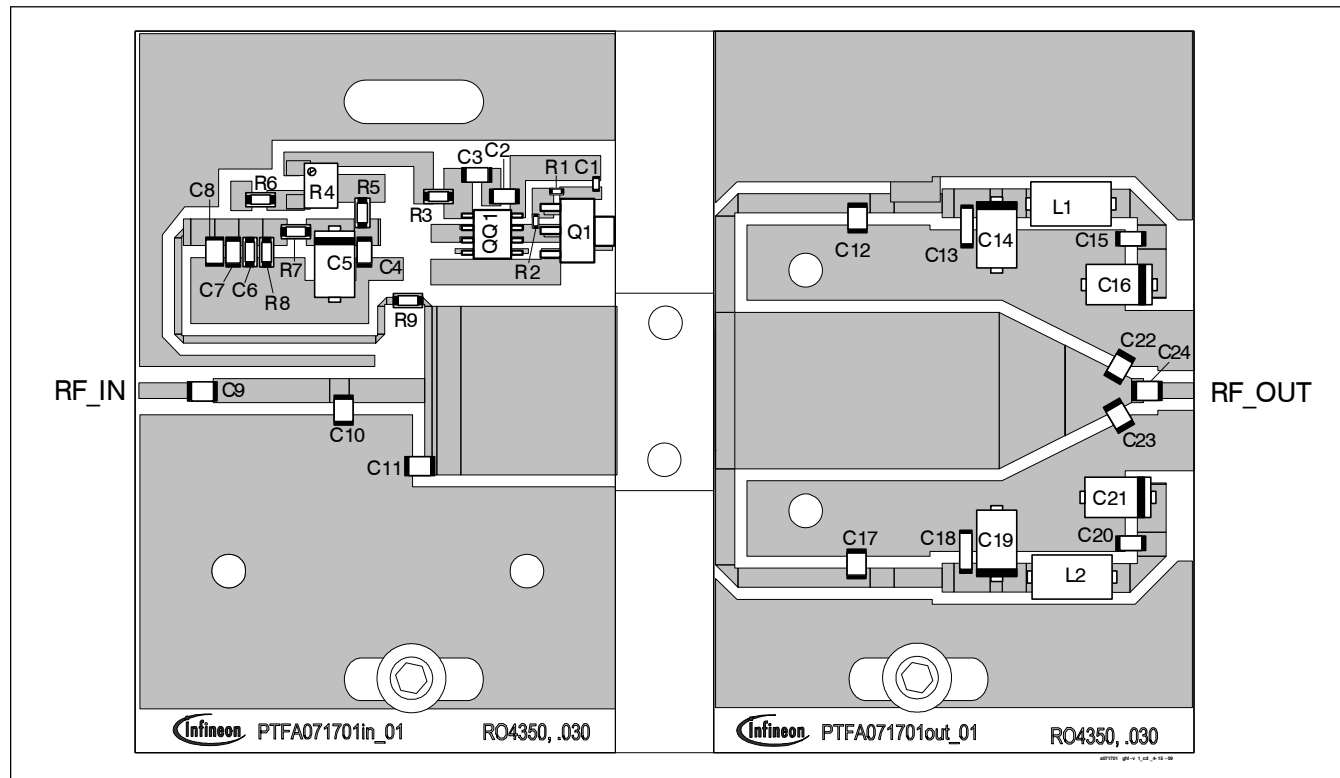
Reference circuit schematic for $f = 770 \text{ MHz}$

Circuit Assembly Information

DUT	PTFA071701E or PTFA071701F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, $\epsilon_r = 3.48$	Rogers RO4350	1 oz. copper

Microstrip	Electrical Characteristics at 770 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
$\ell 1$	0.025λ , 50.7Ω	5.84 x 1.65	0.230 x 0.065
$\ell 2$	0.053λ , 38.4Ω	12.32 x 2.54	0.485 x 0.100
$\ell 3$	0.035λ , 38.4Ω	8.00 x 2.54	0.315 x 0.100
$\ell 4$	0.148λ , 76.7Ω	35.94 x 0.76	1.415 x 0.030
$\ell 5$	0.094λ , 7.8Ω	20.32 x 17.78	0.800 x 0.700
$\ell 6, \ell 7$	0.103λ , 44.5Ω	24.13 x 2.03	0.950 x 0.080
$\ell 8$	0.139λ , 8.4Ω	29.97 x 16.51	1.180 x 0.650
$\ell 9$ (taper)	0.062λ , $8.4 \Omega / 33.8 \Omega$	13.46 x 16.51 / 3.05	0.530 x 0.650 / 0.120
$\ell 10$ (taper)	0.002λ , $33.8 \Omega / 38.4 \Omega$	0.51 x 3.05 / 2.54	0.020 x 0.120 / 0.100
$\ell 11$	0.005λ , 38.4Ω	1.27 x 2.54	0.050 x 0.100
$\ell 12$	0.016λ , 50.7Ω	3.76 x 1.65	0.148 x 0.065

Reference Circuit (cont.)

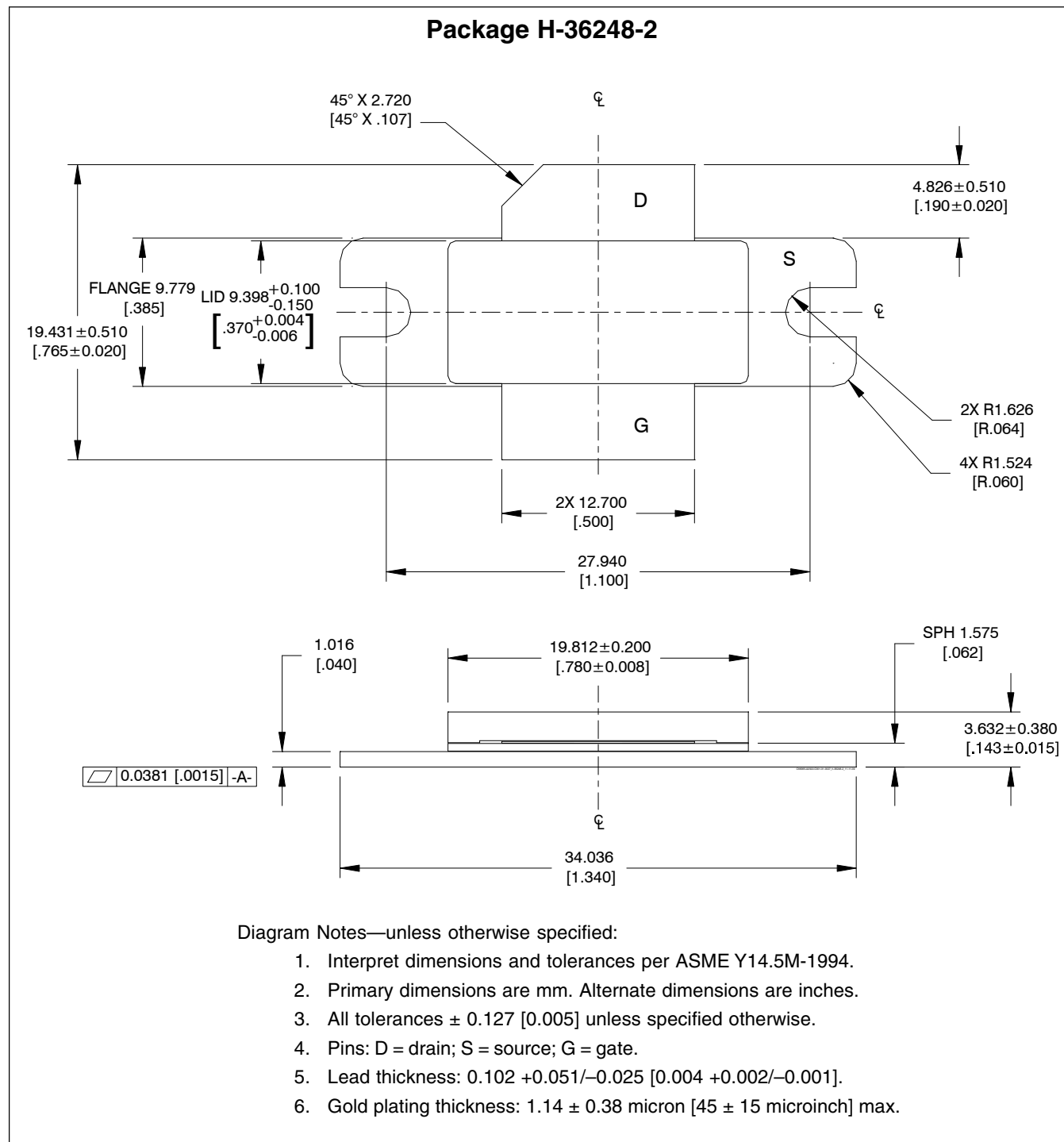


Reference circuit assembly diagram* (not to scale)

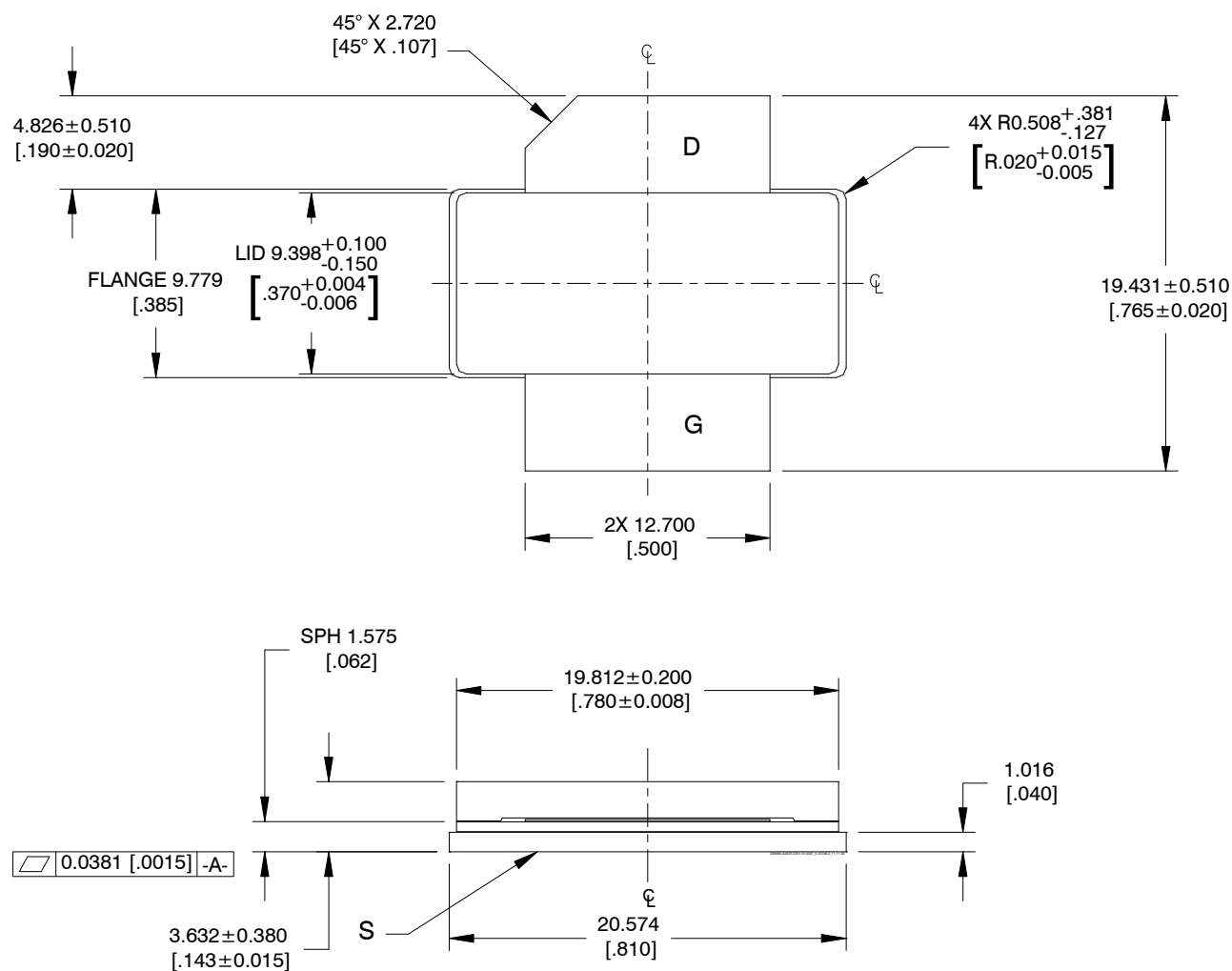
Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 μ F	Digi-Key	PCC1772CT-ND
C4, C7, C15, C20	Capacitor, 0.1 μ F	Digi-Key	PCC104BCT-ND
C6	Capacitor, 4.7 μ F, 16 V	Digi-Key	PCS3475CT-ND
C5	Tantalum capacitor, 10 μ F, 35 V	Digi-Key	399-1655-2-ND
C8, C9, C12, C17, C24	Ceramic capacitor, 62 pF	ATC	100B 620
C10	Ceramic capacitor, 3.9 pF	ATC	100B 3R9
C11	Ceramic capacitor, 6.2 pF	ATC	100B 7R5
C13, C18	Capacitor, 2.2 μ F	ATC	920C 202
C14, C16, C19, C21	Tantalum capacitor, 10 μ F, 50 V	Garrett Electronics	TPSE106K050R0400
C22, C23	Ceramic capacitor, 3.3 pF	ATC	100B 3R3
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor, 1.2k Ω	Digi-Key	P1.2KGCT-ND
R2	Chip resistor, 1.3k Ω	Digi-Key	P1.3KGCT-ND
R3, R5	Chip resistor, 2k Ω	Digi-Key	P2KECT-ND
R4	Potentiometer, 2k Ω	Digi-Key	3224W-202ETR-ND
R6, R8	Chip resistor, 5.1k Ω	Digi-Key	P5.1KECT-ND
R7, R9	Chip resistor, 10 Ω	Digi-Key	P10ECT-ND

*Gerber files for this circuit available on request

Package Outline Specifications



Package H-37248-2



1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [0.005] unless specified otherwise.
4. Pins: D = drain; S = source; G = gate.
5. Lead thickness: $0.102 +0.051/-0.025$ [0.004 +0.002/-0.001].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch] max.

Rev. 03, 2009-11-11

Revision History: 2009-11-11

Data Sheet

Previous Version: 2009-09-09, Preliminary Data Sheet

Page	Subjects (major changes since last revision)
All	Data Sheet now reflects released-product specifications
2	Updated maximum ratings
7,8	Updated package outline

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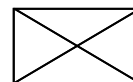
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