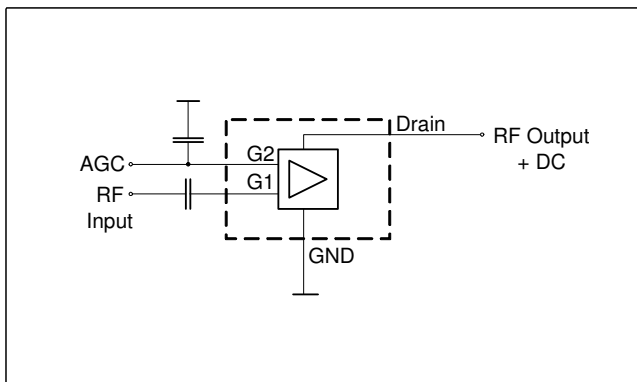
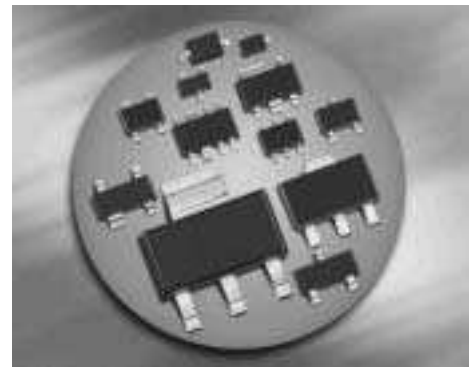


Silicon N-Channel MOSFET Tetrode

- For low noise, high gain controlled input stages up to 1 GHz
- Operating voltage 5 V
- Integrated biasing network
- Pb-free (RoHS compliant) package ¹⁾
- Qualified according AEC Q101



ESD (Electrostatic discharge) sensitive device, observe handling precaution!

Type	Package	Pin Configuration						Marking
BF1005S	SOT143	1=S	2=D	3=G2	4=G1	-	-	NZs
BF1005SR	SOT143R	1=D	2=S	3=G1	4=G2	-	-	NZs

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	8	V
Continuous drain current	I_D	25	mA
Gate 1/ gate 2-source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	3	V
Total power dissipation $T_S \leq 76^\circ\text{C}$	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	$^\circ\text{C}$
Channel temperature	T_{ch}	150	

¹⁾Pb-containing package may be available upon special request

Note:

It is not recommended to apply external DC-voltage on Gate 1 in active mode.

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point ¹⁾	R_{thchs}	≤ 370	K/W

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Drain-source breakdown voltage $I_D = 650\ \mu\text{A}$, $V_{G1S} = 0$, $V_{G2S} = 0$	$V_{(BR)DS}$	12	-	-	V
Gate1-source breakdown voltage $+I_{G1S} = 10\ \text{mA}$, $V_{G2S} = 0$, $V_{DS} = 0$	$+V_{(BR)G1SS}$	8	-	12	
Gate2 source breakdown voltage $\pm I_{G2S} = 10\ \text{mA}$, $V_{G1S} = 0$, $V_{DS} = 0$	$\pm V_{(BR)G2SS}$	8	-	13	
Gate1-source leakage current $V_{G1S} = 6\ \text{V}$, $V_{G2S} = 0$	$+I_{G1SS}$	-	100	-	μA
Gate 2 source leakage current $\pm V_{G2S} = 8\ \text{V}$, $V_{G1S} = 0$, $V_{DS} = 0$	$\pm I_{G2SS}$	-	-	50	nA
Drain current $V_{DS} = 5\ \text{V}$, $V_{G1S} = 0$, $V_{G2S} = 4\ \text{V}$	I_{DSS}	-	-	800	μA
Operating current (selfbiased) $V_{DS} = 5\ \text{V}$, $V_{G2S} = 4\ \text{V}$	I_{DSO}	8	13	16	mA
Gate2-source pinch-off voltage $V_{DS} = 5\ \text{V}$, $I_D = 100\ \mu\text{A}$	$V_{G2S(p)}$	-	1	-	V

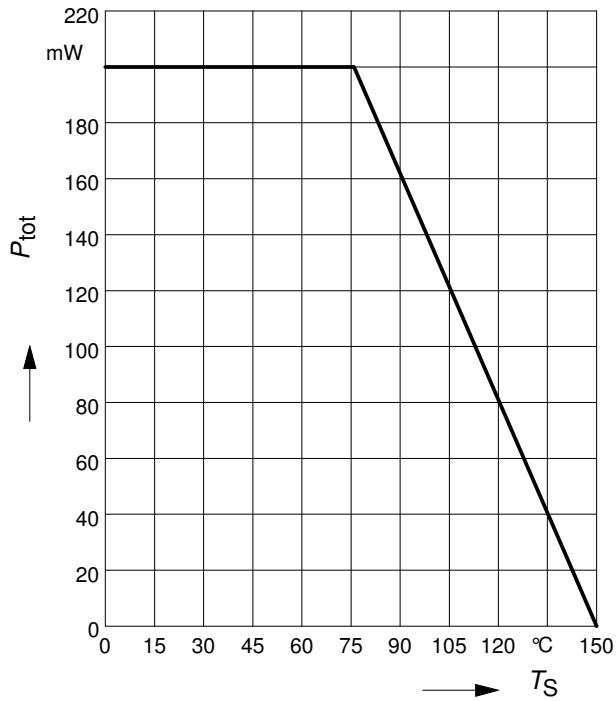
¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics (verified by random sampling)					
Forward transconductance $V_{DS} = 5\text{ V}$, $V_{G2S} = 4.5\text{ V}$	g_{fs}	26	30	-	mS
Gate1 input capacitance $V_{DS} = 5\text{ V}$, $V_{G2S} = 4\text{ V}$, $f = 1\text{ MHz}$	C_{g1ss}	-	2.4	2.7	pF
Output capacitance $V_{DS} = 5\text{ V}$, $V_{G2S} = 4\text{ V}$, $f = 100\text{ MHz}$	C_{dss}	-	1.3	-	
Power gain (self biased) $V_{DS} = 5\text{ V}$, $V_{G2S} = 4\text{ V}$, $f = 800\text{ MHz}$	G_p	20	22	-	dB
Noise figure $V_{DS} = 5\text{ V}$, $V_{G2S} = 4\text{ V}$, $f = 800\text{ MHz}$	F	-	1.6	2.1	dB
Gain control range $V_{DS} = 5\text{ V}$, $V_{G2S} = 4\text{ V} \dots 0\text{ V}$, $f = 800\text{ MHz}$	ΔG_p	40	50	-	

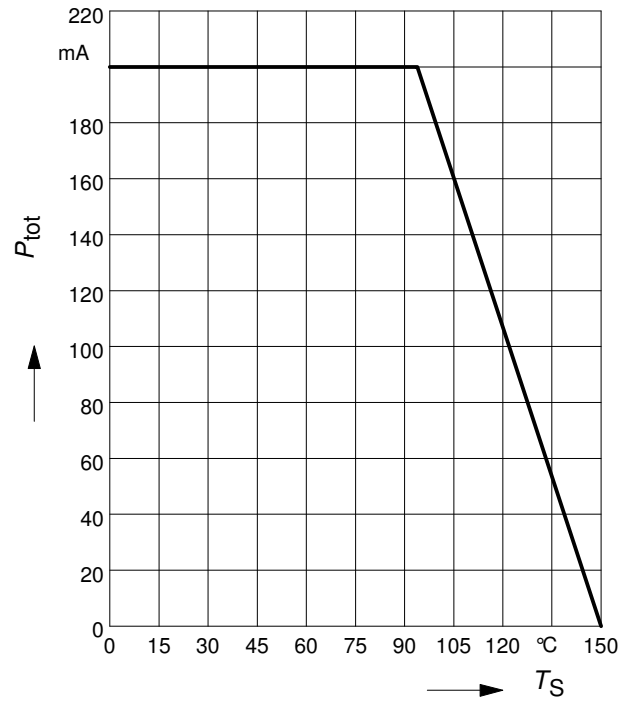
Total power dissipation $P_{\text{tot}} = f(T_S)$

BF1005S, BF1005SR

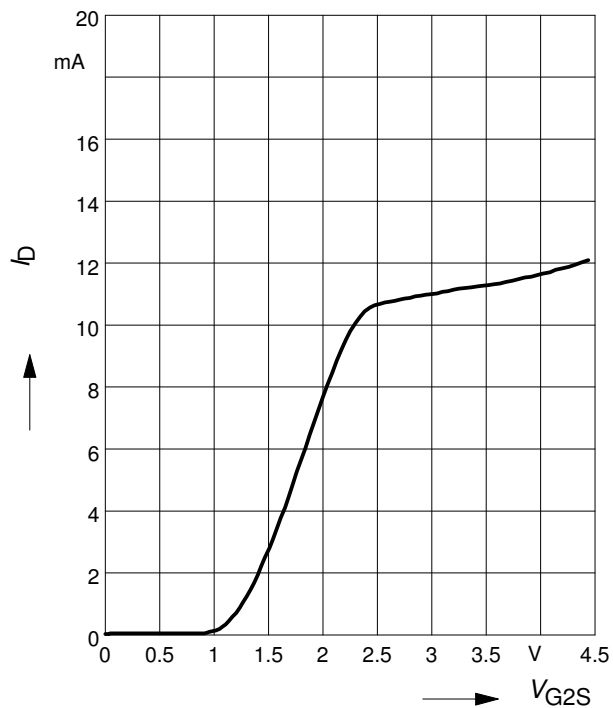


Total power dissipation $P_{\text{tot}} = f(T_S)$

BF1005SW

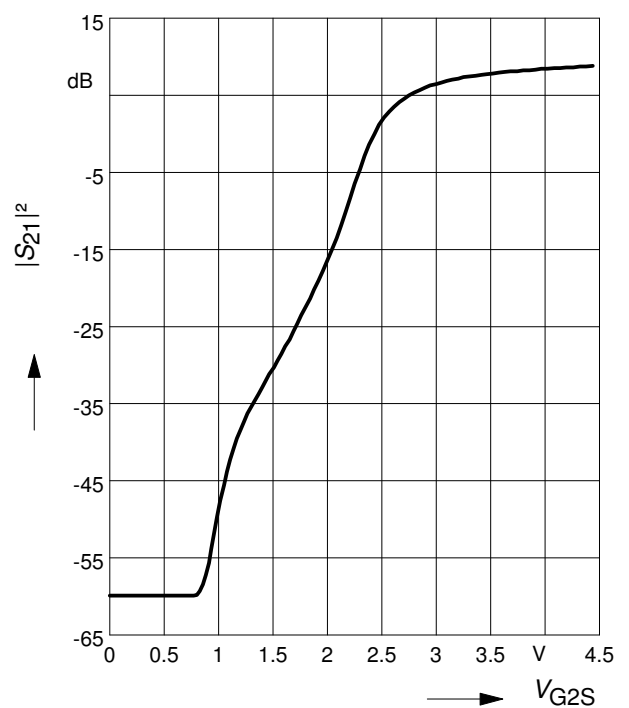


Drain current $I_D = f(V_{G2S})$



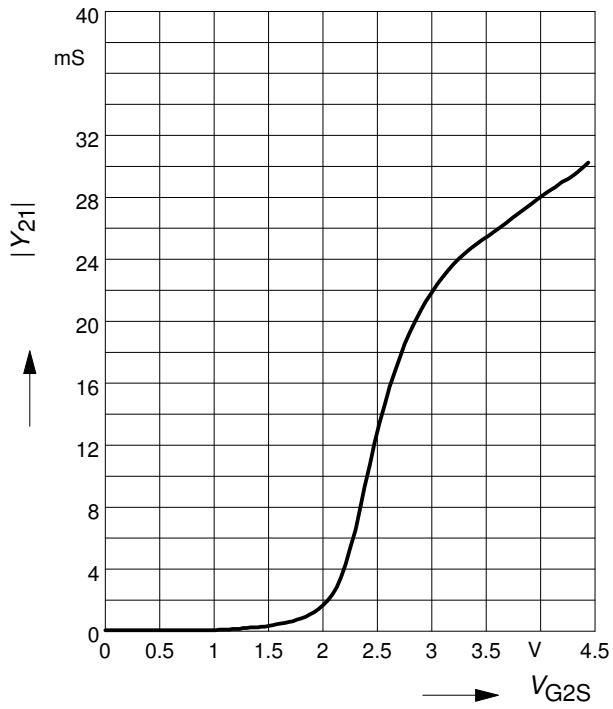
Insertion power gain

$|S_{21}|^2 = f(V_{G2S})$

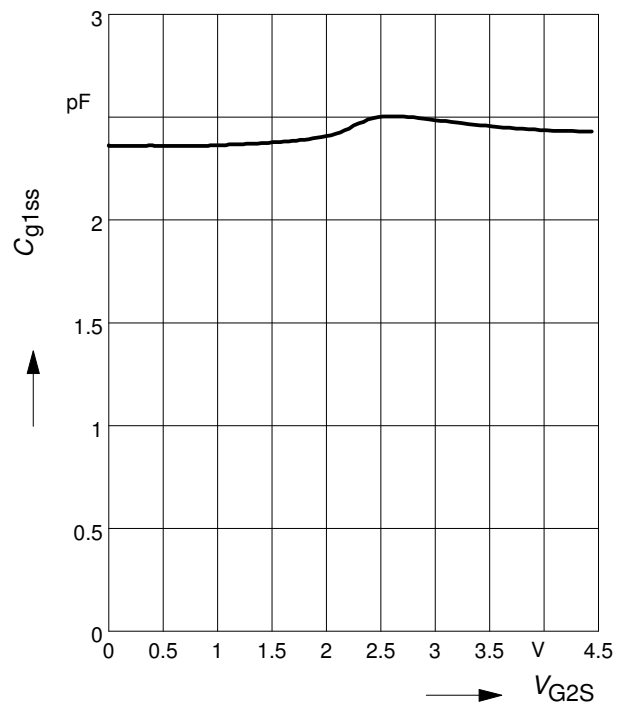


Forward transfer admittance

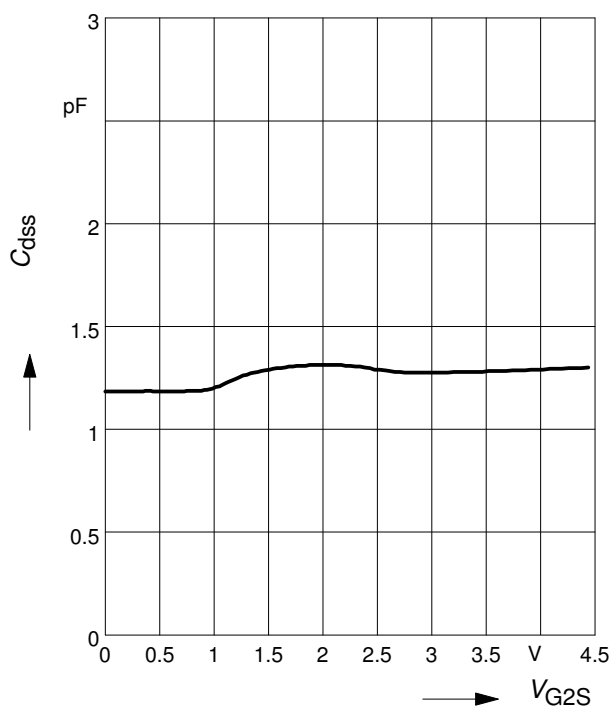
$$|Y_{21}| = f(V_{G2S})$$


Gate 1 input capacitance $C_{g1ss} = f(V_{G2S})$

$$f = 200\text{MHz}$$


Output capacitance $C_{dss} = f(V_{G2S})$

$$f = 200\text{MHz}$$



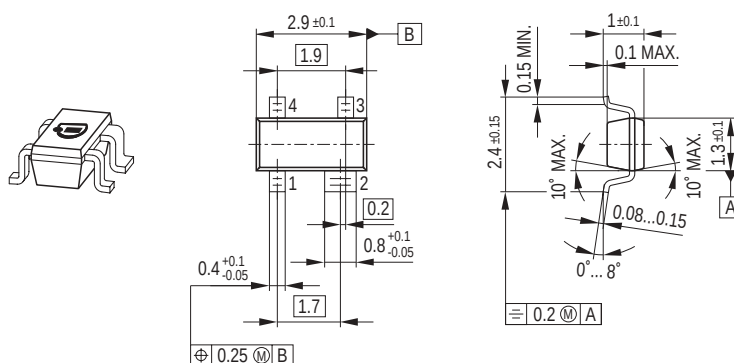
The diagram shows a top-down view of a BFP181 package. The marking area is a rectangle containing the text "RF S 56". Callouts point to various parts of the package and marking:

- Manufacturer:** Points to the Infineon logo.
- Date code (YM):** Points to the "56" in the marking.
- Type code:** Points to the "RF S" in the marking.
- Pin 1:** Points to the bottom-left pin.

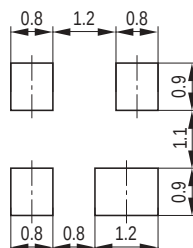
The technical drawing shows two views of a mechanical component:

- Top View:** A rectangular plate with overall dimensions of 4 units by 8 units. It features three rectangular slots along its length. The distance from the left edge to the first slot center is 3.15 units. The width of each slot is 2.6 units. There are circular holes at the ends of the plate.
- Side View:** Shows the profile of the plate with a total thickness of 0.2 units. One of the rectangular slots has a depth of 1.15 units.

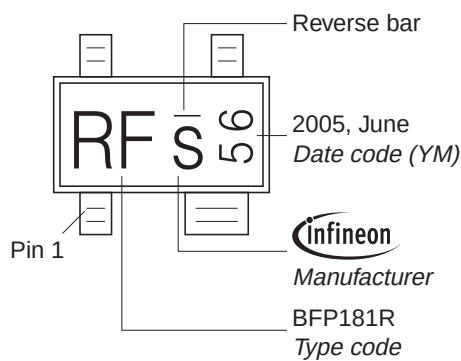
Package Outline



Foot Print

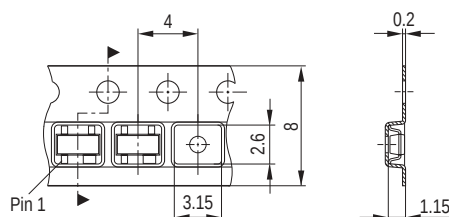


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



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