BGA915N7

Silicon Germanium GPS Low Noise Amplifier

Data Sheet

Revision 4.0, 2011-03-23

RF & Protection Devices

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 4.0, 2011-03-23	
all	“Preliminary” status removed
10, 11	Min/max limits specified for parameters I_{CC}, $\|S_{21}\|^2$ and NF
12, 13	Application Board: Board inductance specified, Cross-section drawing updated
Revision 3.0, 2010-12-07	
all	Preliminary data sheet
7	New marking code defined
10, 11	Electrical Characteristics specified for frequency range f = 1550 - 1615 MHz

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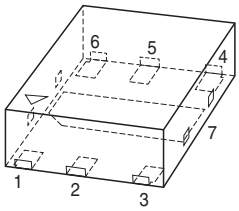
Features

- Insertion power gain: 15.5 dB
- High out of band input 3rd order intercept point: +10dBm
- High input 1 dB compression point: -5 dBm
- Low Noise Figure: 0.7 dB
- Low current consumption: 4.4 mA
- Operating frequencies: 1550 - 1615 MHz
- Supply voltage: 1.5 V to 3.6 V
- Digital on/off switch (1V logic high level)
- Very small TSNP-7-6 leadless package
- B7HF Silicon Germanium technology
- RF output internally matched to 50 Ω
- Only 3 external SMD components necessary
- 2 kV HBM ESD protection (including AI-pin)
- Pb-free (RoHS compliant) package



TSNP-7-6

RoHS

Application

- Suitable for all Global Navigation Satellite Systems (GNSS) like GPS, Galileo, GLONASS, COMPASS

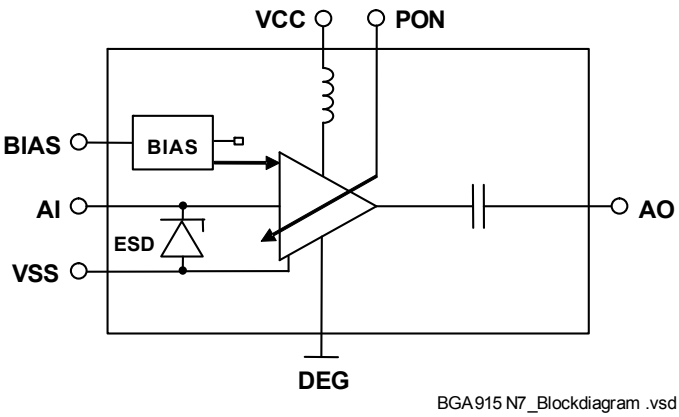


Figure 1 Block Diagram

Product Name	Marking	Package
BGA915N7	BC	TSNP-7-6

Description

The BGA915N7 is a front-end low noise amplifier for Global Navigation Satellite Systems (GNSS) from 1550 MHz to 1615 MHz like GPS, Galileo, GLONASS and COMPASS. The LNA provides 15.5 dB gain and 0.7 dB noise figure at a current consumption of 4.4 mA in the application configuration described in **Chapter 3**. The BGA915N7 is based upon Infineon Technologies' B7HF Silicon Germanium technology. It operates from 1.5 V to 3.6 V supply voltage.

Pin Definition and Function

Table 1 Pin Definition and Function

Pin No.	Name	Function
1	DEG	LNA emitter degeneration ground
2	AI	LNA input
3	BIAS	DC bias
4	AO	LNA output
5	VCC	DC Supply
6	PON	Power on control
7	VSS	Common on chip RF and DC ground

1 Maximum Ratings

Table 2 Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at pin VCC	V_{CC}	-0.3	–	3.6	V	1)
Voltage at pin AI	V_{AI}	-0.3	–	0.9	V	–
Voltage at pin BIAS	V_{BIAS}	-0.3	–	0.9	V	–
Voltage at pin AO	V_{AO}	-0.3	–	V_{CC} + 0.3	V	–
Voltage at pin PON	V_{PON}	-0.3	–	V_{CC} + 0.3	V	–
Voltage at pin VSS	V_{SS}	-0.3	–	0.3	V	–
Current into pin VCC	I_{CC}	–	–	20	mA	–
RF input power	P_{IN}	–	–	0	dBm	–
Total power dissipation, T_S < 129 °C2)	T_J	–	–	72	mW	–
Junction temperature	P_{tot}	–	–	150	°C	–
Ambient temperature range	T_A	-40	–	85	°C	–
Storage temperature range	T_{STG}	-65	–	150	°C	–
ESD capability all pins	V_{ESD_HBM}	–	–	2000	V	according to JESD22A-114
ESD capability all pins	V_{ESD_MM}	–	–	100	V	according to JESD22A-115

1) All voltages refer to VSS-Node unless otherwise noted

2) T_S is measured on the ground lead at the soldering point

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Thermal Resistance

Table 3 Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point1)	R_{thJS}	291	K/W

1) For calculation of R_{thJA} please refer to Application Note Thermal Resistance

2 Electrical Characteristics

Table 4 Electrical Characteristics:[1] T_A = 25 °C, V_{CC} = 2.8 V, $V_{PON,ON}$ = 2.8 V, $V_{PON,OFF}$ = 0 V, f = 1550 - 1615 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	–	3.6	V	–
Supply current	I_{CC}	3.3	4.4	5.7	mA	ON-mode
		–	0.2	3	µA	OFF-mode
Power On voltage	V_{pon}	1.0	–	Vcc	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{pon}	–	5	12	µA	ON-mode
		–	–	1	µA	OFF-mode
Insertion power gain	$\|S_{21}\|^2$	14.3	15.5	17.2	dB	
Noise figure[2]	NF	–	0.7	1.2	dB	Z_S = 50 Ω
Input return loss	RL_{in}	–	11	–	dB	
Output return loss	RL_{out}	–	16	–	dB	
Reverse isolation	$1/\|S_{12}\|^2$	–	20	–	dB	
Power gain settling time[3]	t_S	–	5	–	µs	OFF- to ON-mode
		–	5	–	µs	ON- to OFF-mode
Inband input 1 dB compression point	IP_{1dB}	–	-5	–	dBm	
Inband input 3rd order intercept point[4]	IIP_3	–	+2	–	dBm	f_1 = 1575 MHz f_2 = f_1 +/-1 MHz
Out of band input 3rd order intercept point[5]	IIP_{3oob}	–	+10	–	dBm	f_1 = 1712.7 MHz f_2 = 1850 MHz
Stability	k	–	> 1	–		f = 20 MHz ... 10 GHz

1) Based on the application described in chapter 3
2) PCB losses are subtracted
3) To be within 1 dB of the final gain OFF- to ON-mode; to be within 3 dB of the final gain ON- to OFF-mode
4) Input Power = -30 dBm for each tone
5) Input Power = -20 dBm for each tone

Table 5 Electrical Characteristics:[1] T_A = 25 °C, V_{CC} = 1.8 V, $V_{PON,ON}$ = 1.8 V, $V_{PON,OFF}$ = 0 V, f = 1550 - 1615 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	–	3.6	V	–
Supply current	I_{CC}	3.3	4.4	5.7	mA	ON-mode
		–	0.2	3	µA	OFF-mode
Gain switch control voltage	V_{pon}	1.0	–	Vcc	V	ON-mode
		0	–	0.4	V	OFF-mode
Gain switch control current	I_{pon}	–	5	12	µA	ON-mode
		–	–	1	µA	OFF-mode
Insertion power gain	$\|S_{21}\|^2$	14.3	15.5	17.2	dB	
Noise figure[2]	NF	–	0.7	1.2	dB	Z_S = 50 Ω
Input return loss	RL_{in}	–	11	–	dB	
Output return loss	RL_{out}	–	16	–	dB	
Reverse isolation	$1/\|S_{12}\|^2$	–	20	–	dB	
Power gain settling time[3]	t_S	–	5	–	µs	OFF- to ON-mode
		–	5	–	µs	ON- to OFF-mode
Inband input 1 dB compression point	IP_{1dB}	–	-8	–	dBm	
Inband input 3rd order intercept point[4]	IIP_3	–	+1	–	dBm	f_1 = 1575 MHz f_2 = f_1 +/-1 MHz
Out of band input 3rd order intercept point[5]	IIP_{3oob}	–	+10	–	dBm	f_1 = 1712.7 MHz f_2 = 1850 MHz
Stability	k	–	> 1	–		f = 20 MHz ... 10 GHz

1) Based on the application described in chapter 3
2) PCB losses are subtracted
3) To be within 1 dB of the final gain OFF- to ON-mode; to be within 3 dB of the final gain ON- to OFF-mode
4) Input Power = -30 dBm for each tone
5) Input Power = -20 dBm for each tone

3 Application Information

Application Board Configuration

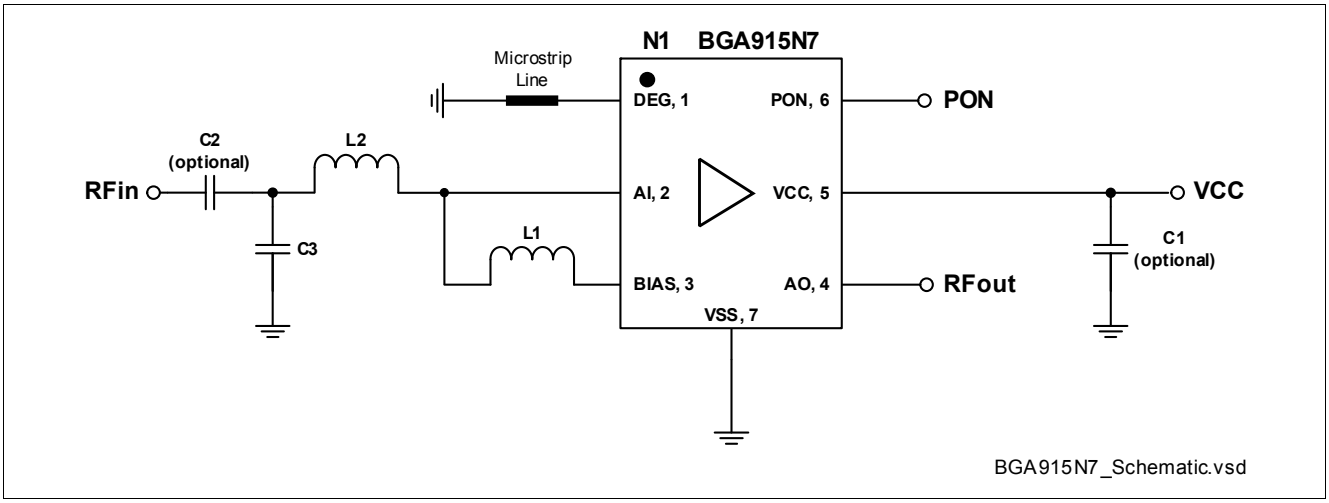


Figure 2 Application Schematic BGA915N7

Table 6 Bill of Materials

Name	Value	Package	Manufacturer	Function
C1 (optional)	1 uF	0402	Various	RF block
C2 (optional)	33 pF	0402	Various	DC block
C3	1 pF	0402	Various	Input matching
L1	82 nH	0402	Murata LQW type	Bias feed and RF choke
L2	7.3 nH	0402	Murata LQW type	Input matching
Microstrip Line	550pH[1)]	-	-	Board inductance from pin DEG to common GND
N1	BGA915N7	TSNP-7-6	Infineon	SiGe LNA

1) Total board inductance = inductance of the microstrip line (~500pH) + inductance of via (~50pH)
Please refer to application note AN258 for more details on “realization of small inductor values on a PCB by using microstriplines”.

A list of all application notes is available at **http://www.infineon.com/gpslna.appnotes**.

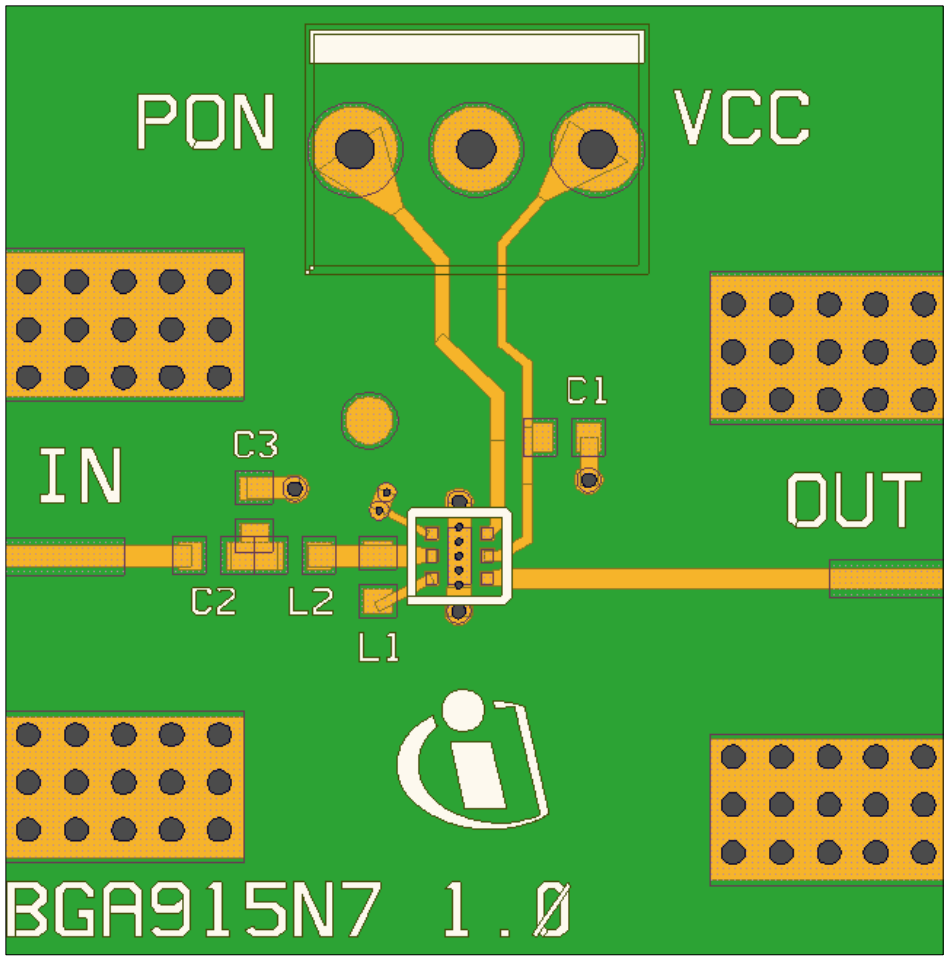


Figure 3 Drawing of Application Board

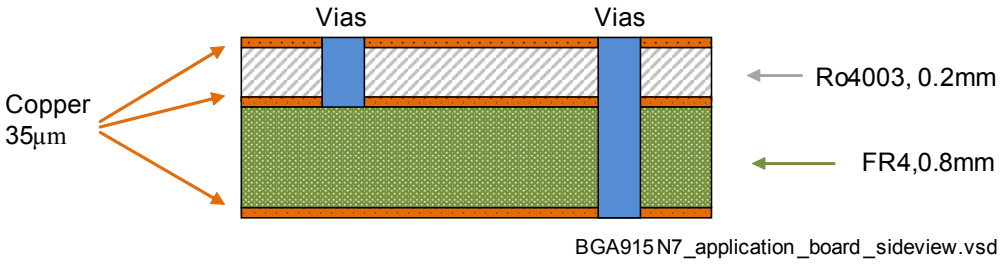


Figure 4 Cross-section of Application Board

4 Package Information

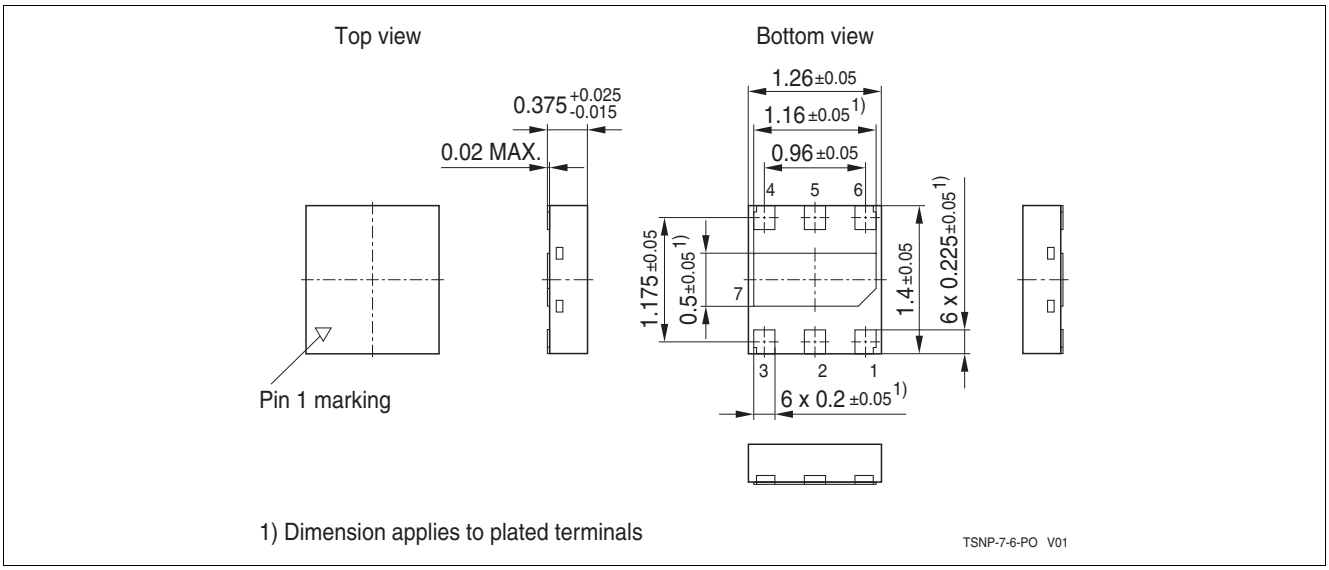


Figure 5 Package Outline TSNP-7-6

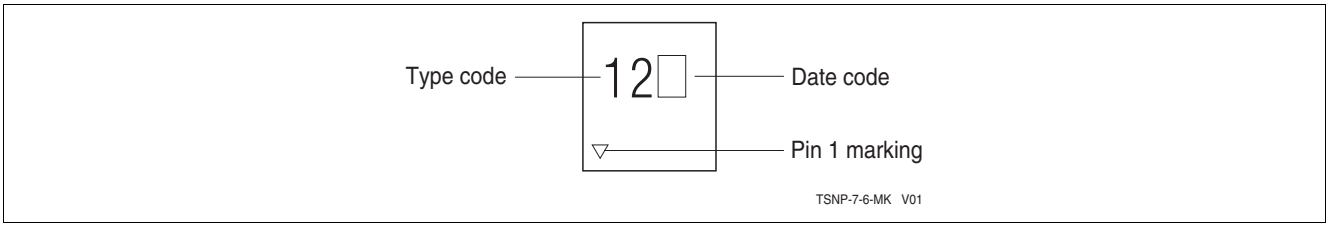


Figure 6 Marking Layout (top view)

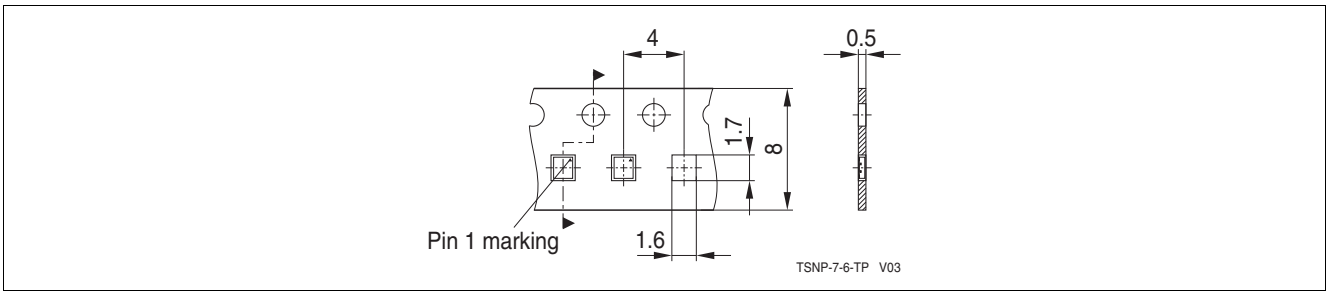


Figure 7 Tape & Reel Dimensions (Ø reel 180 mm, pieces/reel 7500)

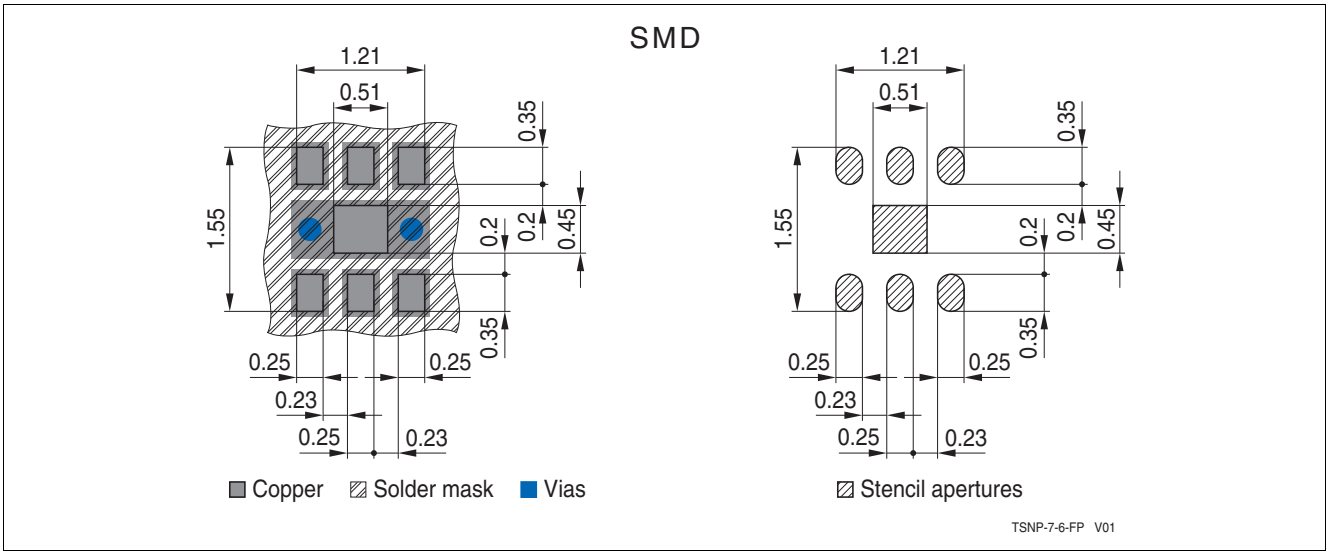


Figure 8 Footprint TSNP-7-6

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