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BGF137

Integrated Fuse and TVS Protection

BGF137

Data Sheet

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Final

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 3.1, 2011-08-09	
8, 9	**Table 3** updated
Revision 3.0, 2011-06-06	
all	Final data sheet
Revision 2.2, 2011-05-05	
4	marking updated

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1 Integrated Fuse and TVS Protection

1.1 Features

- 1 channel integrated fuse and TVS diode
- ESD protection according to IEC61000-4-2 up to 25 kV contact discharge on all IOs
- Wafer Level Package with SnAgCu solder balls
- RoHS and WEEE compliant package
- Very small form factor (0.75 mm x 0.75 mm)
- **Fuse**
  - 2 A fuse
  - Fast fusing time, t_F < 1 ms @ 5 A, 25 °C ambient
  - Very low fuse resistance, R < 50 mΩ
- **TVS**
  - Very high surge power capability
  - Operation voltage up to 12 V
  - Very accurate breakdown voltage with low temperature coefficient
  - Low clamping voltage

RoHS

1.2 Description

The BGF137 integrates a Fuse and TVS diode and is designed for transient voltage and power overstress suppression. All pins are protected against ESD pulses of ± 25 kV contact discharge according to IEC61000-4-2. The wafer level package is a green package with a size of only 0.75 x 0.75 mm² and a total height of 0.50 mm [2].

2 Product Description

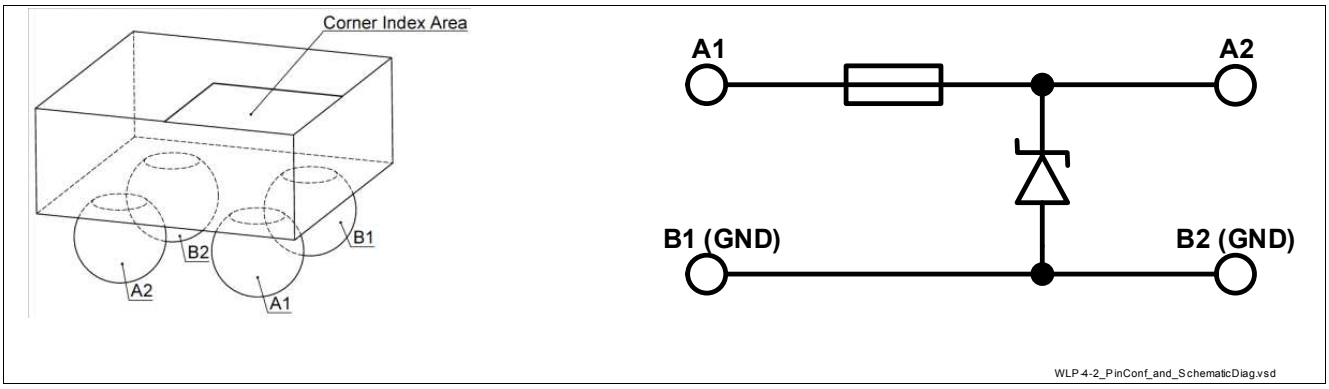

Figure 1 Schematic Diagram and Package Configuration

Table 1 Ordering Information

Type	Package	Chip	Marking code
BGF137	WLP-4-2	N0741	37

3 Characteristics

Table 2 **Maximum Rating** at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Voltage at all pins to GND	V_P	0	–	+12	V
Operating temperature range	T_{OP}	-30	–	+85	°C
Storage temperature	T_{STG}	-55	–	+150	°C
Electrostatic discharge according to IEC61000-4-2[1)] at all pins	V_{ESD}	-25	–	+25	kV

1) Contact discharge

3.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

Table 3 **DC Characteristics** at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fuse resistance	R	–	0.045	0.05	Ω	I = 200mA
Fusing time, no current through TVS from Pin A2 to B1/B2 ($I_{A2,B1/B2}$ = 0 A)						I = 5 A, A1 to A2
	t_F	–	1	–	ms	T_A = 25°C
		–	–	100		T_A = -30°C
Fusing time, no current through TVS from Pin A2 to B1/B2 ($I_{A2,B1/B2}$ = 0 A)						I = 3.2 A, A1 to A2
	t_F	–	0.7	–	h	T_A = 25°C
		–	1.2	24		T_A = 10°C, Max. at 100 ppm
		–	7	–		T_A = -30°C
Fuse lifetime, no current through TVS from Pin A2 to B1/B2 ($I_{A2,B1/B2}$ = 0 A)						I = 2 A, A1 to A2
	t_L	–	20000	–	h	T_A = 25°C
		1000	–	–		T_A = 25°C, Min. at 100 ppm
Fuse lifetime, no current through TVS from Pin A2 to B1/B2 ($I_{A2,B1/B2}$ = 0 A)						I = 1 A, A1 to A2
	t_L	–	14 x 10^6	–	h	T_A = 25°C
Insulation resistance post fusing	R_I	0.1	20	–	MΩ	5 A forced current, 14 V voltage compliance at A1[2]
Breakdown voltage of TVS diode, current forced from A1 to B1/B2						I_R = 20 mA
	V_{BR}	–	17	–	V	T_A = 25°C
		15.5	–	–		T_A = -30°C

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Leakage current of line to GND						V_R = 12 V
	I_R	–	100	–	nA	T_A = 85°C
		–	10	100		T_A = 25°C
		–	1	–		T_A = -30°C
Forward voltage of TVS diode, current forced from A1 to B1/B2[1)]						I_F = 850 mA
	V_F	–	1.05	1.1	V	T_A = 25°C
		–	–	1.15		T_A = -30°C

1) To avoid high temperature and possible disassembling of component from the board, DC current operation to be limited to few seconds [2]

Table 4 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance to GND	C_L	–	120	–	pF	V_R = 0 V, f = 1 MHz, V_{OSC} = 25 mV

Table 5 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1]						I_{PP} = 1 A,
	V_{CL}	–	18.9	19.5	V	T_A = 85°C from A2 to GND
		–	17.8	–		T_A = 25°C from A2 to GND
		–	17.0	–		T_A = -30°C from A2 to GND
Clamping voltage[2]						
	V_{CL}	–	25.0	–	V	+8 kV
		–	-2.5	–		-8 kV
		–	33.0	–		+15 kV
		–	-4.0	–		-15 kV
Clamping voltage[3]						
	V_{CL}	–	18.0	–	V	+8 kV
		–	-1.0	–		-8 kV
		–	22.0	–		+15 kV
		–	-1.6	–		-15 kV
Dynamic resistance[4]	R_{DYN}	–	0.14	–	Ω	from B1 to A1
		–	0.09	–		from B2 to A2
		–	0.66	–		from A1 to B1
		–	0.60	–		from A2 to B2

1) 8/20 µs pulse wafeform according to IEC61000-4-5

2) Clamping voltage after 30 ns according to IEC61000-4-2 (contact)

3) Clamping voltage after 100 ns according to IEC61000-4-2 (contact)

4) *TLP parameter: Z_0 = 50 Ω,* tp *= 100 ns,* tr *= 600 ps, averaging window:* t1 *= 30 ns to* t2 *= 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistic between* IPP1 *= 10 A and* IPP2 *= 40 A. The equivalent stress level* VIEC *according IEC 61000-4-2 (*R *= 330 Ω ,* C *= 150 pF) is calculated at the broad peak of the IEC waveform at* t *= 30 ns with 2 A / kV*

3.2 Typical Characteristics at T_A = 25 °C, unless otherwise specified

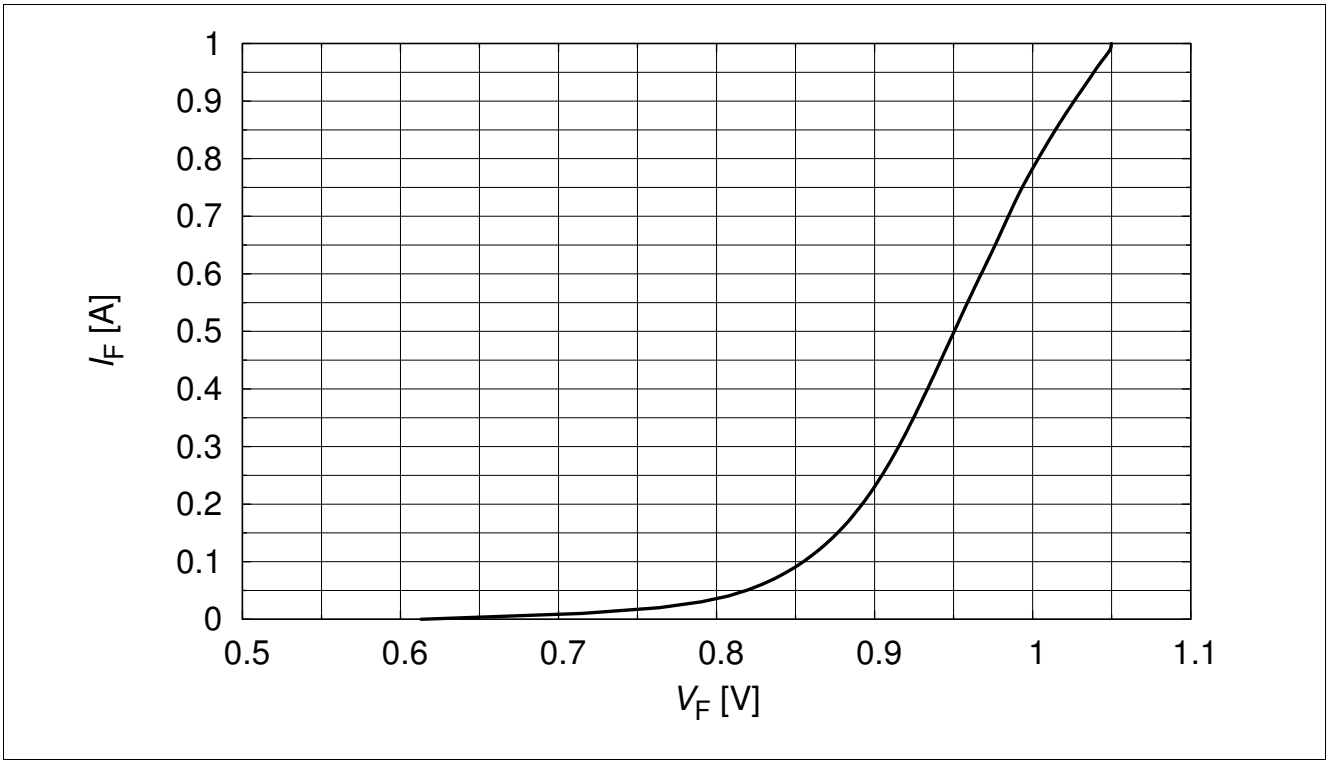

Figure 2 Forward characteristics, $I_F = f(V_F)$

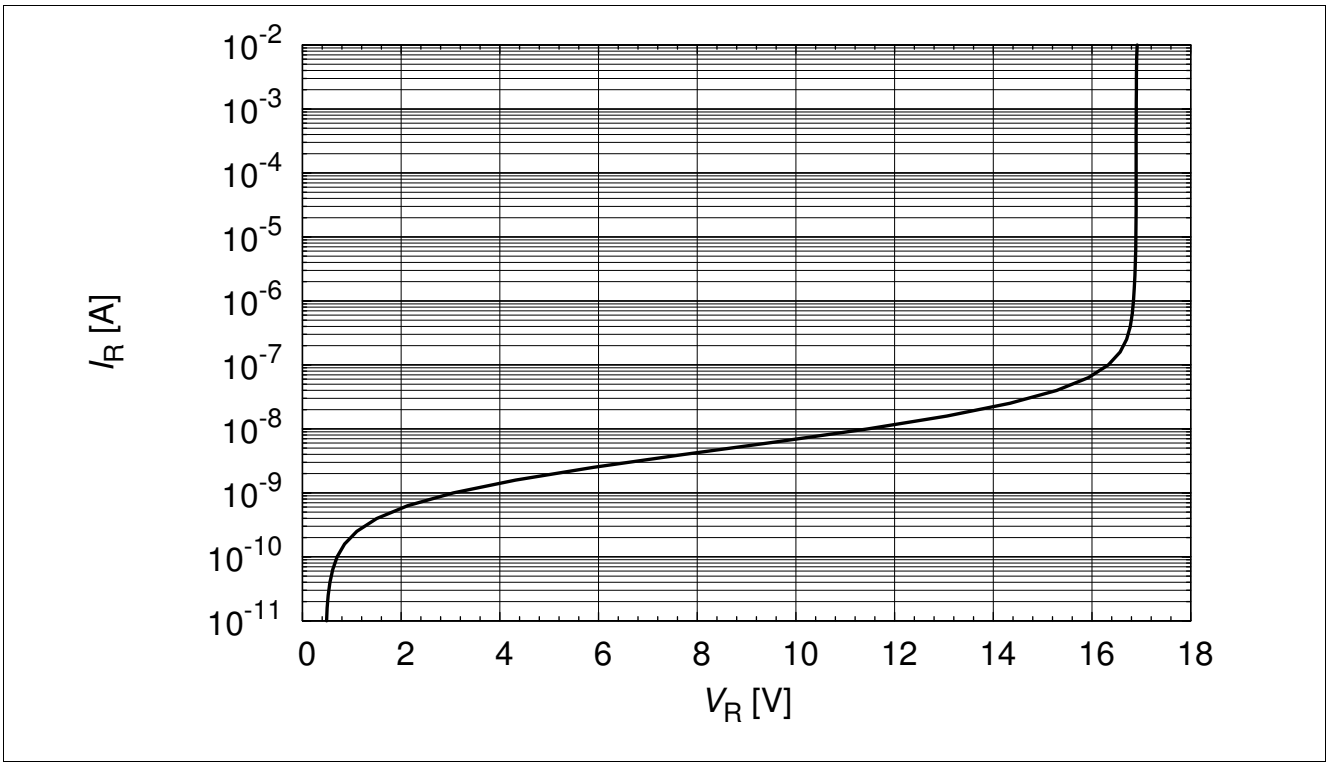

Figure 3 Reverse characteristics, $I_R = f(V_R)$

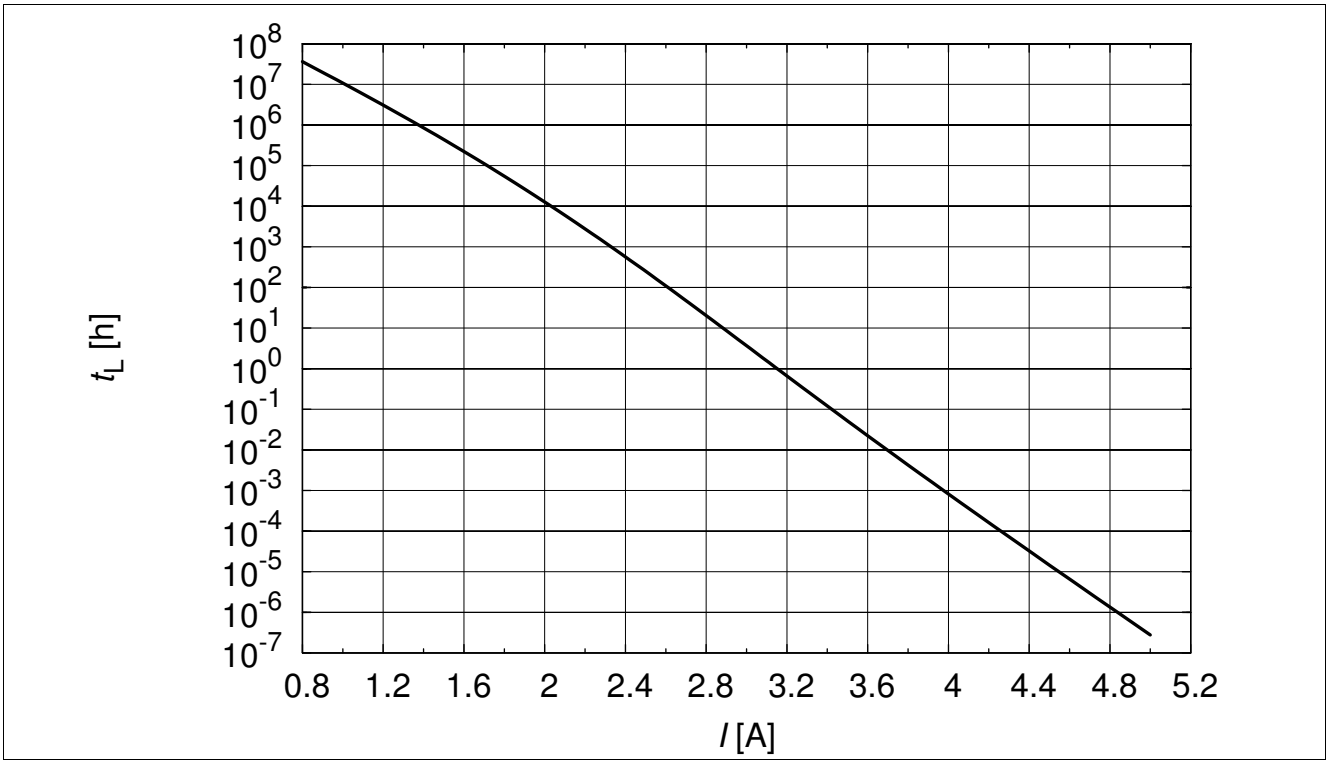

Figure 4 Fuse lifetime, $t_L = f(I)$

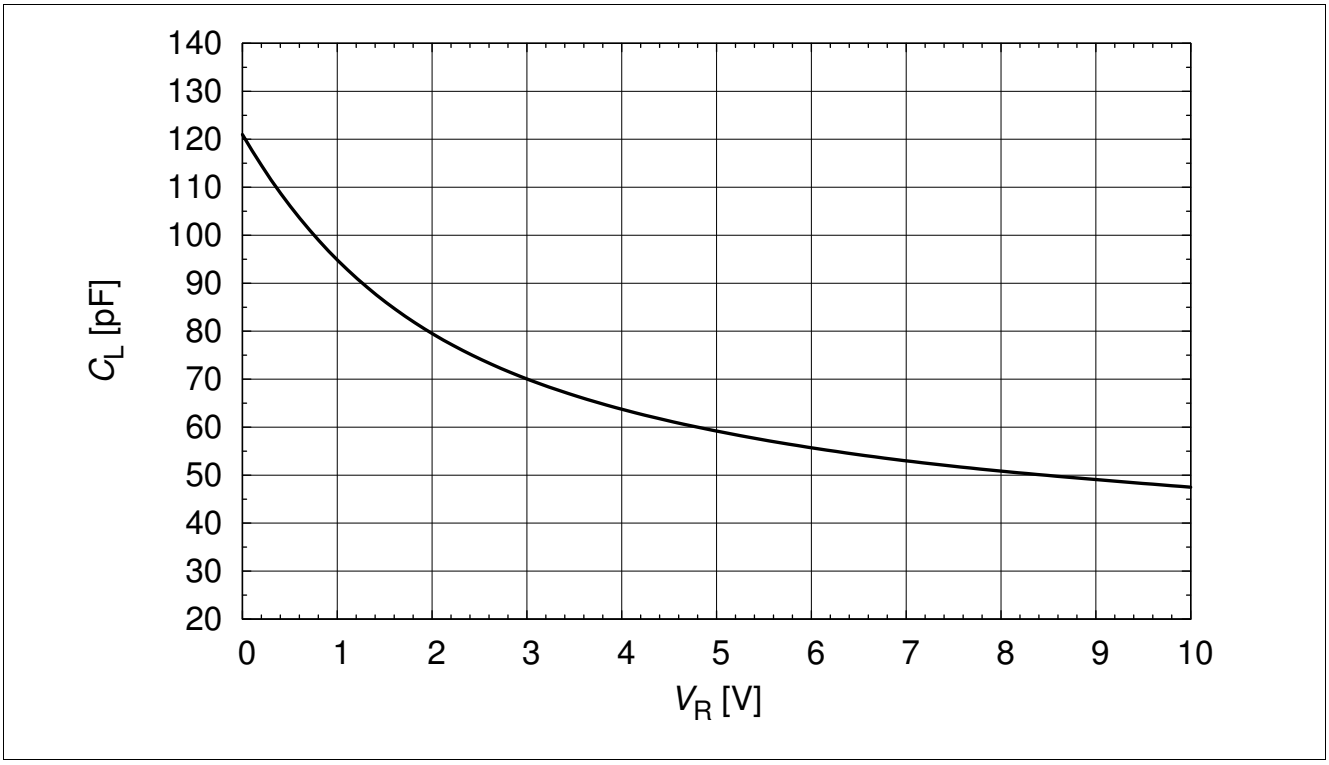

Figure 5 Line capacitance $C_L = f(V_R)$, f = 1 MHz

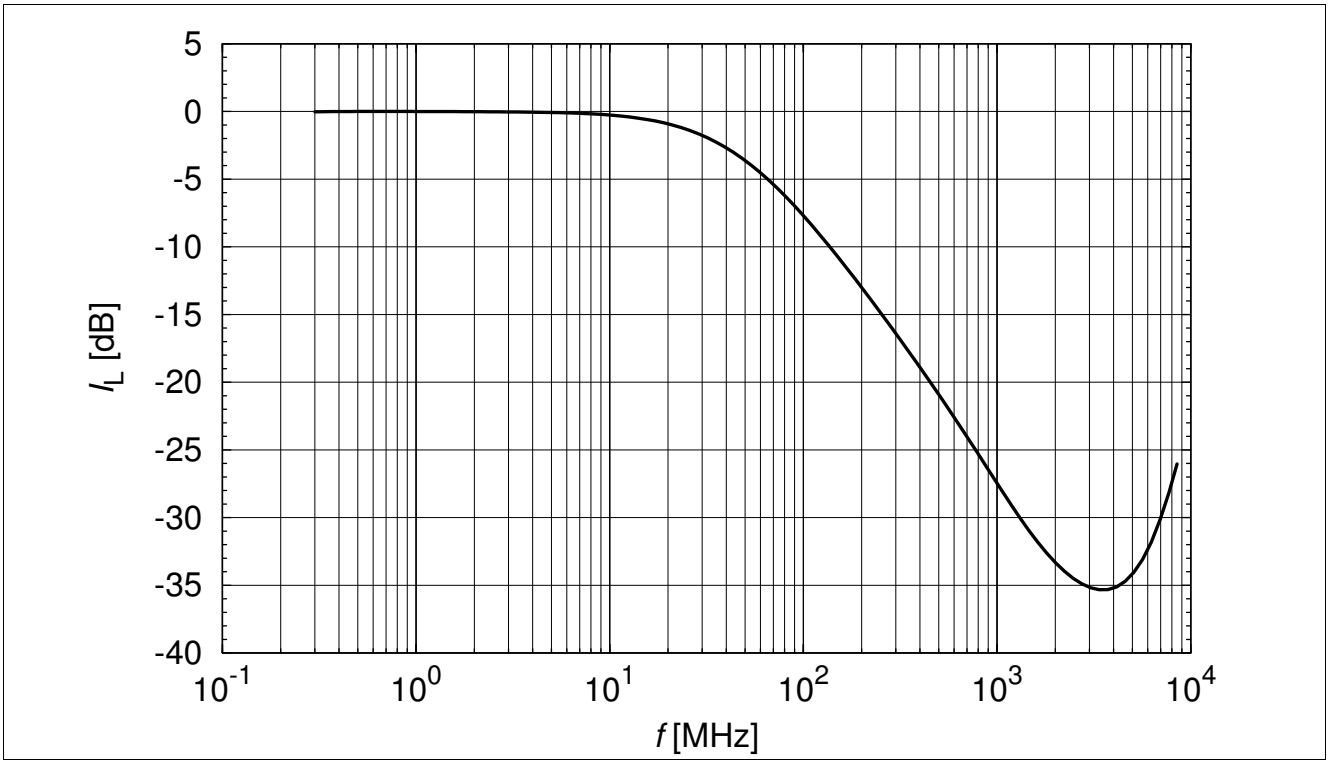

Figure 6 **Insertion loss $I_L = f(f)$, V_R = 0 V**

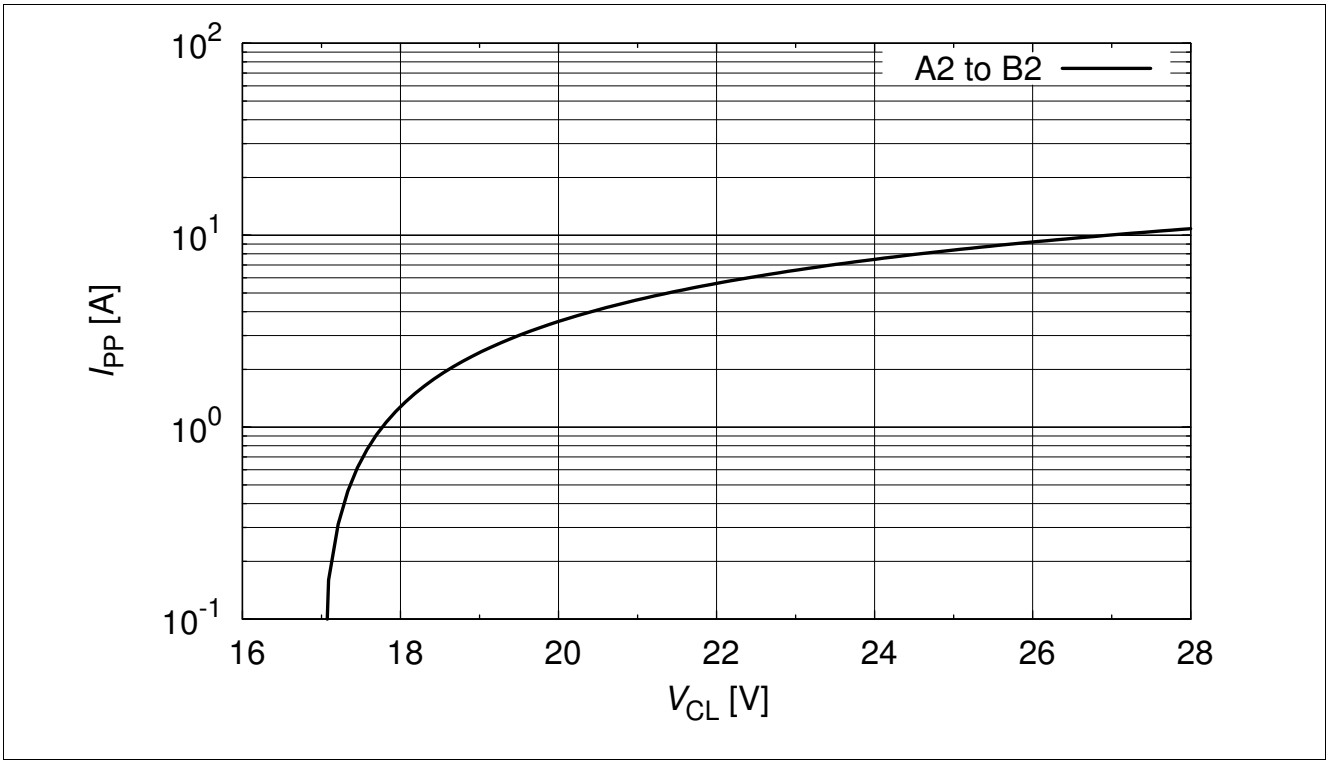

Figure 7 **Pulse reverse current (IEC61000-4-5) versus clamping voltage, $I_{PP} = f(V_{CL})$**

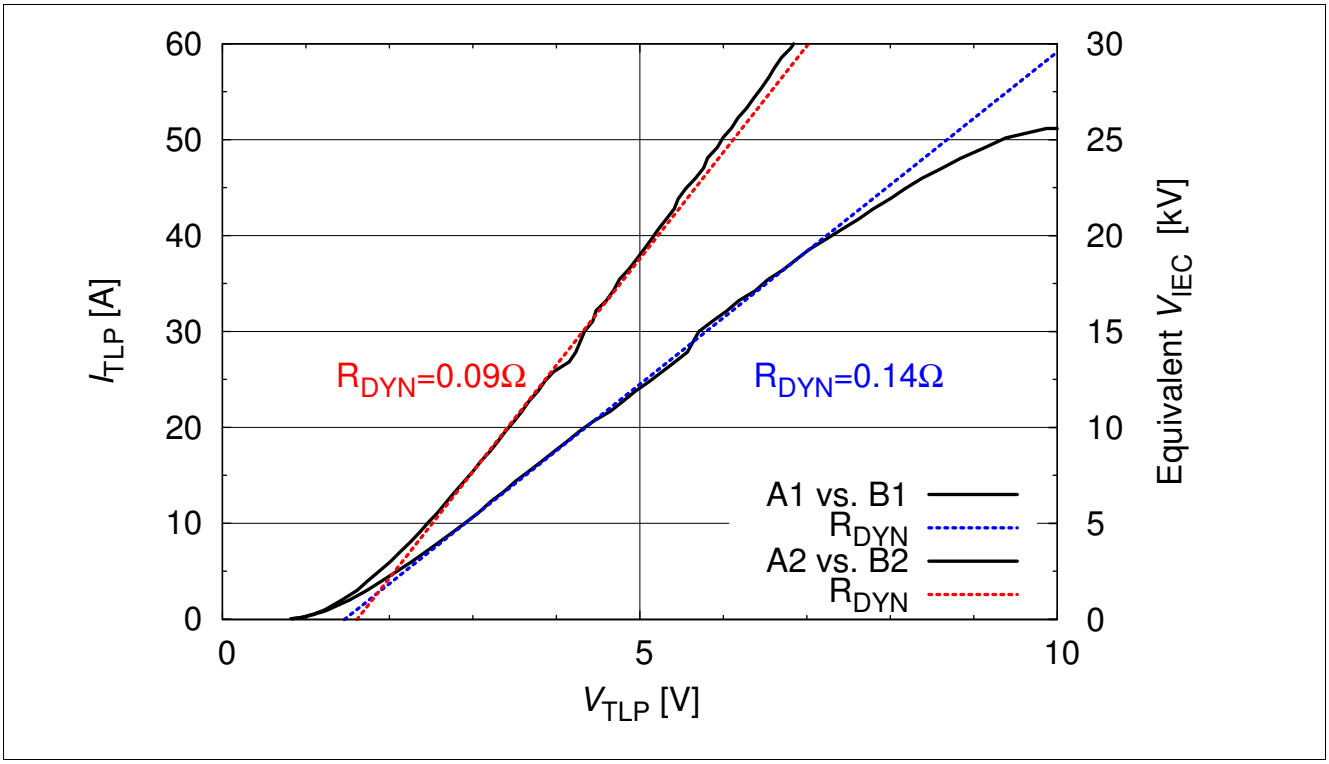

Figure 8 TLP characteristics, negative pulse Note: [1]

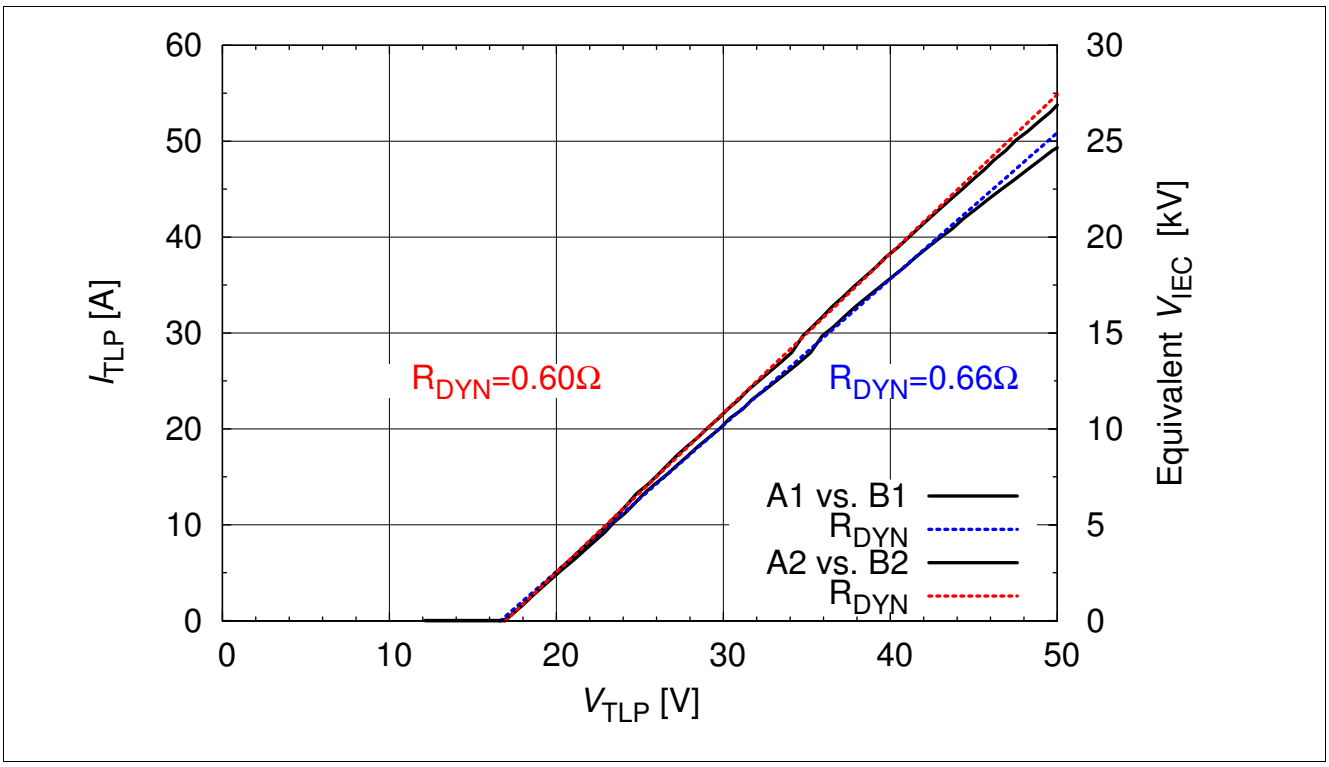

Figure 9 TLP characteristics, positive pulse Note: [1]

Note: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 600 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistic between I_{PP1} = 10 A and I_{PP2} = 40 A. The equivalent stress level V_{IEC} according IEC 61000-4-2 (R = 330 Ω, C = 150 pF) is calculated at the broad peak of the IEC waveform at t = 30 ns with 2 A / kV

4 Package Information

4.1 WLP-4-2 (in mm)

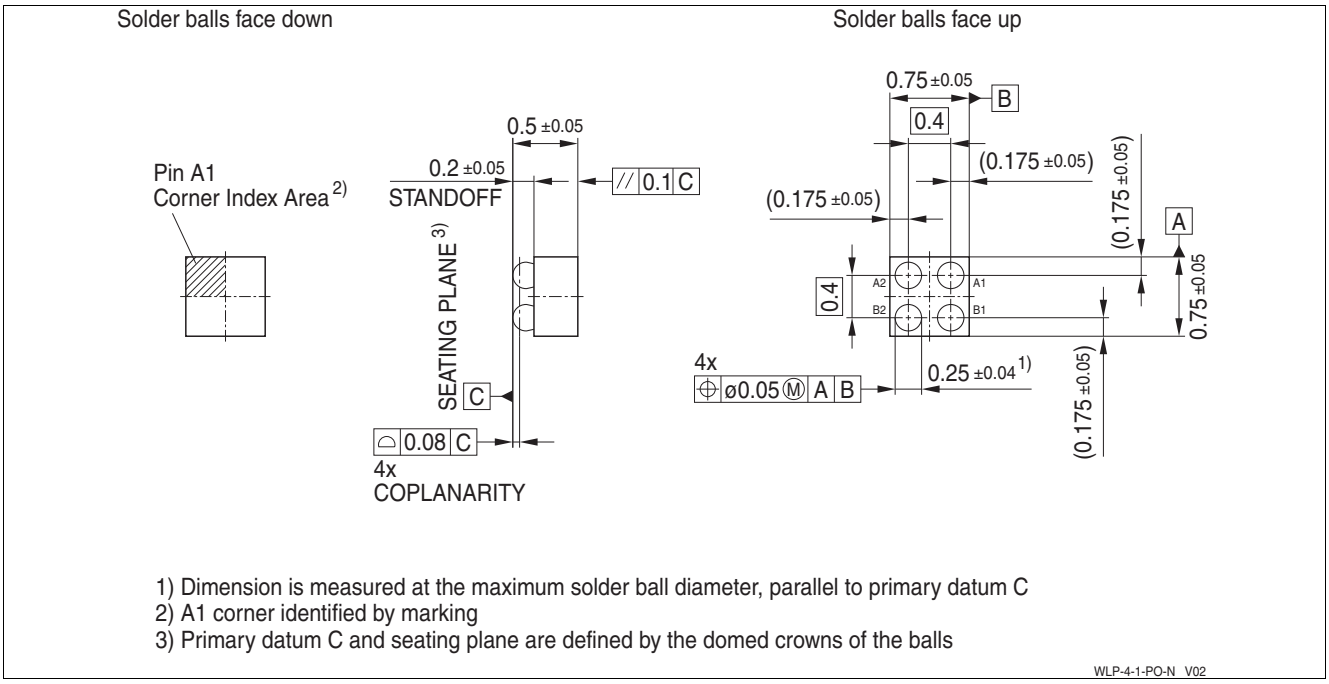

Figure 10 WLP-4-2: Package overview

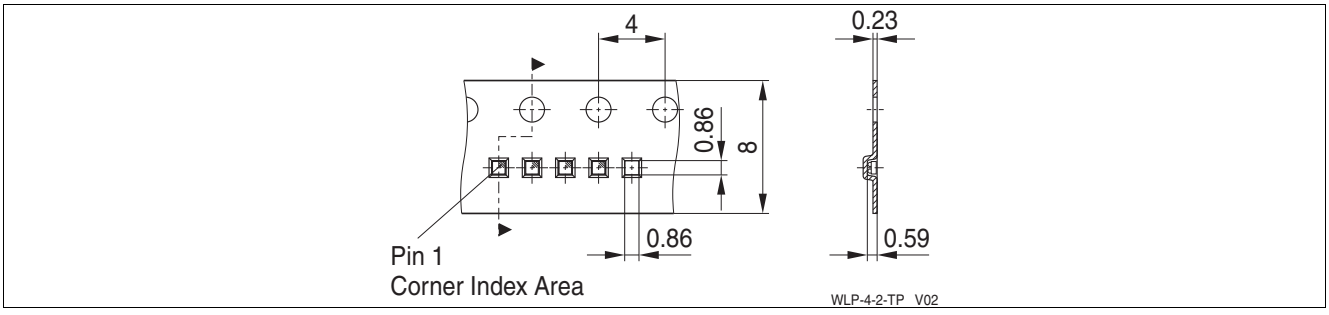

Figure 11 WLP-4-2: Packing

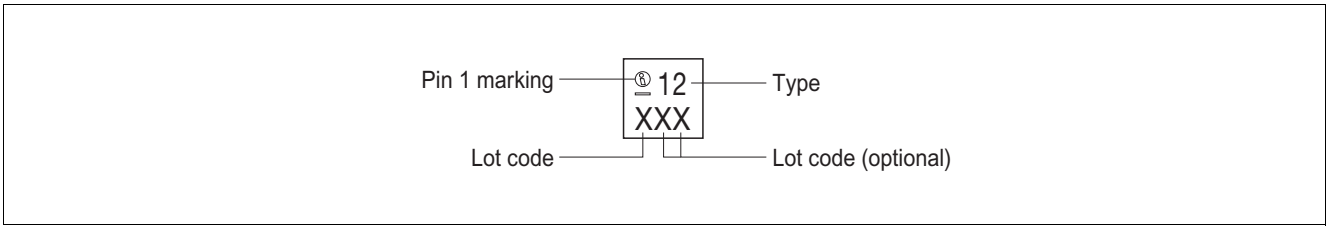

Figure 12 WLP-4-2: Marking (example)

References

[1] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

[2] Infineon Technologie AG - **Application Note AN260**: Hipac Protection Devices for EOS and ESD

Terminology

C_L	Line capacitance
ESD	Electrostatic Discharge
IEC	International Electrotechnical Commission
I_{PP}	Peak pulse current
I_R	Reverse current
R	Fuse resistance
R_{DYN}	Dynamic resistance
R_I	Insulation resistance
RoHS	Restriction of Hazardous Substances Directive
T_A	Ambient temperature
t_F	Fusing time
t_L	Fuse lifetime
TLP	Transmission Line Pulse
T_{OP}	Operation temperature
t_r	Pulse rise time
T_{STG}	Storage temperature
V_{CL}	Reverse clamping voltage
V_{ESD}	Electrostatic discharge
V_{FC}	Forward Clamping Voltage
V_{IEC}	Equivalent stress level according IEC61000-4-2 (R = 330 Ω , C = 150 pF)
V_{OSC}	Oscillator voltage
V_P	Voltage pins
V_R	Reverse voltage
WEEE	Waste Electronic and Electrical Equipment
Z_0	Impedance

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