

# SLE 78CX800P

16-bit Security Controller with “Integrity Guard”,  
optimized for Payment and Identification  
applications in 0.13  $\mu\text{m}$  CMOS technology  
80 kBytes E<sup>2</sup>PROM, 288 kBytes User ROM, 8 kBytes RAM

Crypto@2304T engine  
with register lengths of up to 2304 bits, certified RSA and ECC libraries  
Symmetric Crypto Processor (SCP)  
Triple-key-triple-DES and AES acceleration

## Short Product Overview

May 2010

<b>SLE 78CX800P Short Product Overview</b>		Ref.: Chip_Card_Product_Overview_11/09
<b>Revision History: Current Version 05.10</b>		
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**Important:** Further information is confidential and on request. Please contact:  
Infineon Technologies AG in Munich, Germany,  
Chip Card & Security  
E-Mail: [security.chipcard.ics@infineon.com](mailto:security.chipcard.ics@infineon.com)

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<b>Product name</b>	<b>SLE 78CX800P Secure <math>\mu</math>Slim EEPROM</b> 
<b>Product description</b>	Security cryptocontroller designed for high-security applications
<b>User-ROM</b>	288 kByte
<b>EEPROM</b>	80 kByte
<b>RAM</b>	8 kByte
<b>CPU</b>	Dual 16-bit
<b>Crypto coprocessors</b>	
<b>Symmetrical Cryptography</b>	3DES, AES up to 256 bit
<b>Asymmetrical Cryptography</b>	RSA up to 4096 bit, ECC up to 521 bit
<b>Clock (int.)</b>	1 - 33 MHz
<b>Clock (ext.)</b>	1-10MHz
<b>Operating voltage</b>	1.62 V - 5.5 V
<b>Max. supply current (at 5 MHz, 5 V)</b>	10 mA
<b>Max. sleep mode current (typical)</b>	100 $\mu$ A
<b>Ambient temperature</b>	-25 to +85°
<b>Write / erase time</b>	< 2.3 ms
<b>EEPROM page programming</b>	1 to 128 Byte
<b>Security features</b>	Integrity Guard Security System: Digital Full Error/Fault/ DFA Detection; Full CPU-, Memory-, Bus- and Cache-Encryption; Dual encrypted-calculation CPU; Active I2-Shield; MMU with Level Concept; DPA/SPA, DEMA/SEMA Countermeasures; Threshold Sensors: V, F, Light, Temperature; Intelligent Watchdog with Program Flow Check; Tamperproof Design; Chip ID; True RNG (AIS31, FIPS-140)
<b>Peripherals</b>	ICU/PEC, CRC, PLL, UART DF 8
<b>Delivery forms</b>	Module M5.1, MFC5.x, DSO-8, VQFN-8, die
<b>Typical applications</b>	Payment, EMV DDA, ePurse, Loyalty, Access Control, Health / Social Security, Digital Signature, ID-Card, GSM, UICC
<b>Certifications</b>	CC EAL5+ high, EMVCo

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