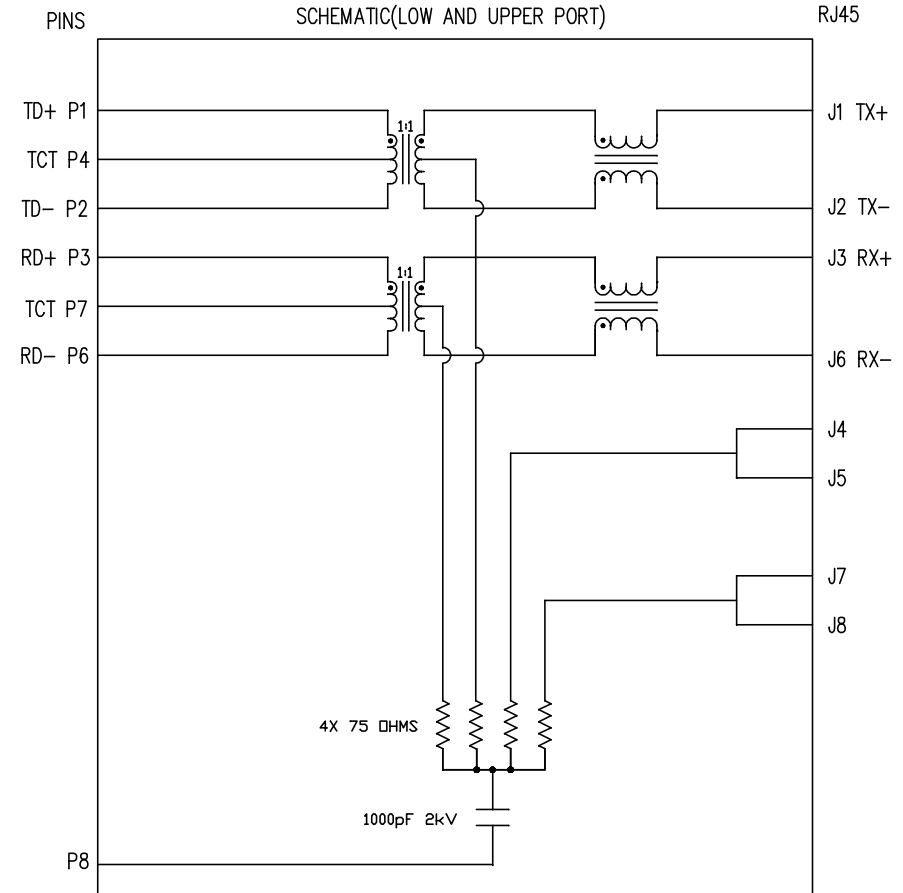




ELECTRICAL CHARACTERISTICS @ 25°C

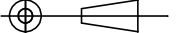
ELECTRICAL SPECIFICATIONS:

1.0	Turns Ratio: (P1-P4-P2) : (J1-J2)	: 1CT : 1 ±3%
	(P3-P7-P6) : (J3-J6)	: 1CT : 1 ±3%
2.0	Inductance: (P6-P3)	: 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias
	(P2-P1)	: 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias
3.0	Leakage Inductance: P6-P3 (WITH J6 AND J3 SHORT)	: 0.3uH MAX. @ 1MHz
	P2-P1 (WITH J2 AND J1 SHORT)	: 0.3uH MAX. @ 1MHz
4.0	Interwinding Capacitance: (P6,P7,P3) TO (J6,J3)	: 30pF MAX @ 1MHz
	(P2,P4,P1) TO (J2,J1)	: 30pF MAX @ 1MHz
5.0	DC Resistance: (J6-J3)=(J1-J2)	: 1.2 ohms Max.
	(P6-P3)	: .7 ohms Max.
	(P2-P1)	: .7 ohms Max.
6.0	Return Loss: 1MHz TO 30MHz	: 18dB MIN.
	60MHz TO 80MHz	: 12dB MIN.
7.0	Dielectric Withstand: (J1, J2) TO (P1, P2)	: 1500 VAC
	(J3, J6) TO (P3,P6)	: 1500 VAC
8.0	Insertion Loss: RS=RL=100 ohms	
	100KHz TO 100MHz	: 1.1 dB TYP
9.0	Rise Time: RS=100 OHMS AND RL = 100 OHMS	
	OUTPUT VOLTAGE = 1 V peak	: 3.0 nS MAX
	PULSE WIDTH= 112nS	: 3.0 nS MAX
10.0	Cross Talk: 1MHz TO 100MHz	: 40 dB TYP
11.0	Common to Common Mode Attenuation:	
	1MHz TO 100MHz	: 35dB TYP



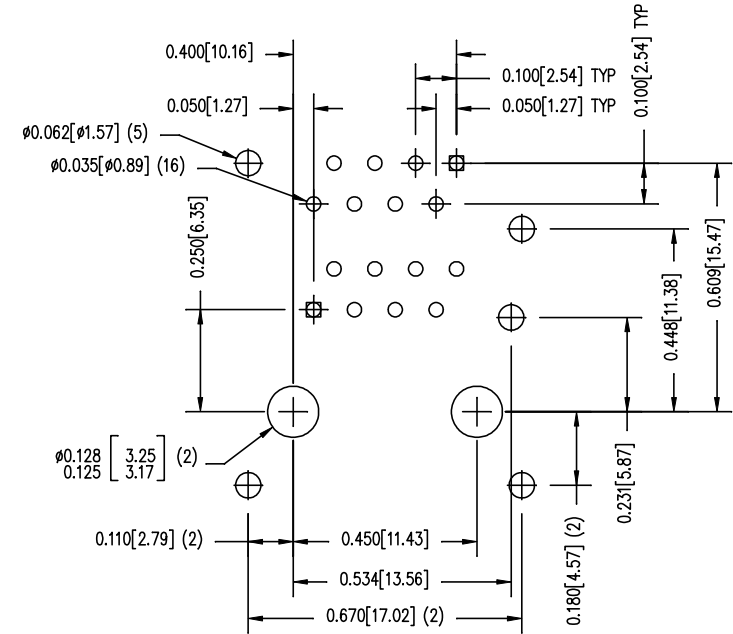
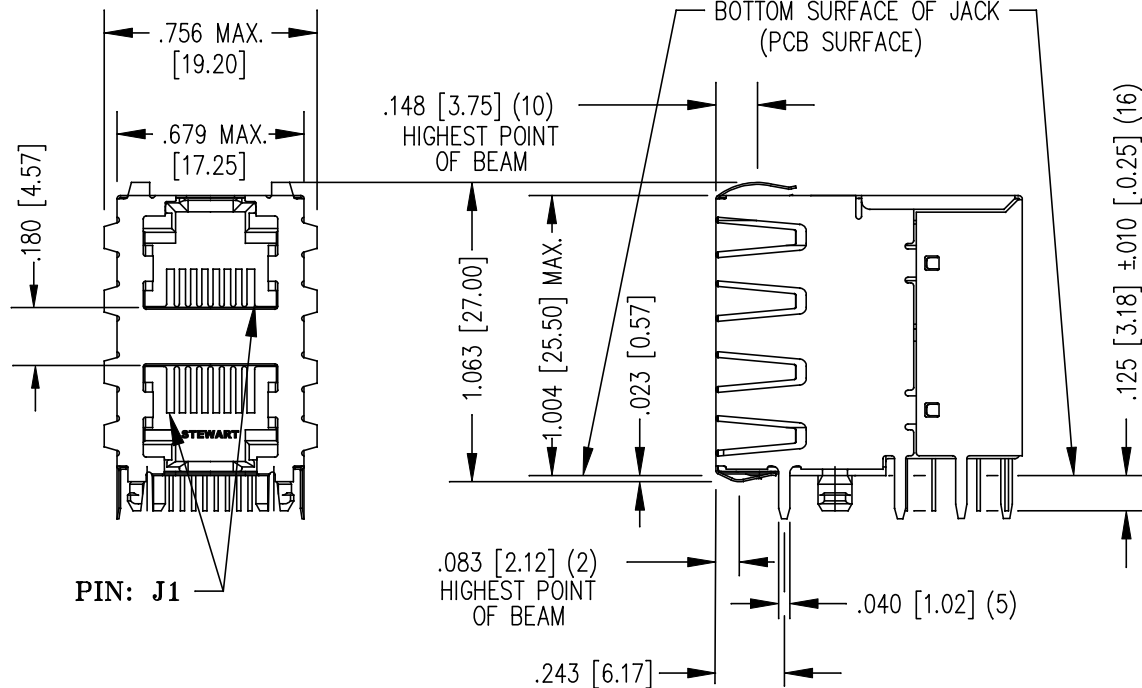
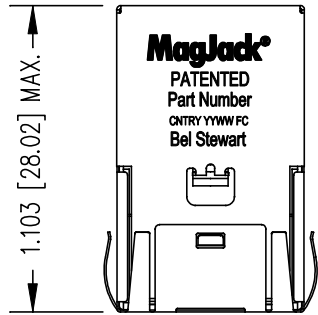
NOTES

1.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED.

ORIGINATED BY	DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM.	[] METRIC DIM. AS REFERENCE	
Zeng Xiao Chun	2011-08-18	 10/100BT STACK JACK, SHIELDED PATENTED	SI-30113-F	TOL. IN INCH	UNIT : INCH [mm]	REV. : A1
DRAWN BY	DATE		FILE NAME	.X	SCALE : N/A	SIZE : A4
Zhang Ru Sheng	2011-08-18		SI-30113-F.DWG	.XX		PAGE : 2
				.XXX		

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RoHS



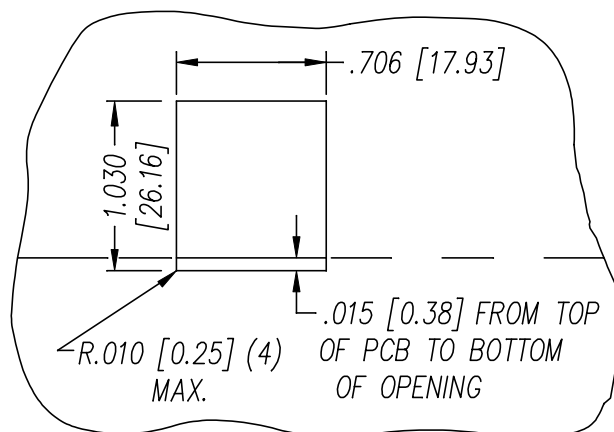
P.C.B. RECOMMENDED HOLE LAYOUT
SEEN FROM COMPONENT SIDE
ALL CENTERLINE DIMENSIONS ARE BASIC

NOTES:

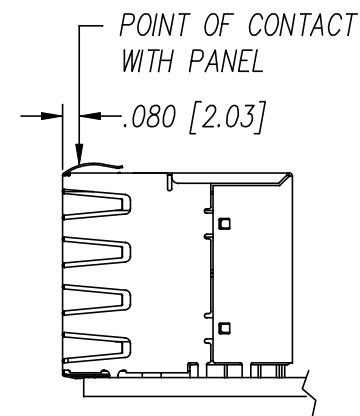
- CONNECTOR MATERIALS:
HOUSING: THERMOPLASTIC UL94 V-0
CONTACT/SHIELD: COPPER ALLOY
SHIELD PLATING: NICKEL OR TIN
CONTACT PLATING: SELECTIVE GOLD,
50 MICRO-INCHES MIN. IN CONTACT AREA.
- PIN NOT ELECTRICALLY CONNECTED MAYBE OMITTED.
SEE ELECTRICAL DRAWING FOR OMITTED PINS.
- TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS.
- ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE ± 0.005 [0.13]
- WAVE SOLDER COMPATIBLE - PREHEAT 125°C/90SECS.

ORIGINATED BY	DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM. TOL. IN INCH	[] METRIC DIM. AS REFERENCE	
Zeng Xiao Chun	2011-08-18	MagJack® 10/100BT STACK JACK, SHIELDED PATENTED	SI-30113-F FILE NAME SI-30113-F.DWG	.X	UNIT : INCH [mm]	REV. : A1
DRAWN BY	DATE			.XX	SCALE : N/A	SIZE : A4
Zhang Ru Sheng	2011-08-18			.XXX	±0.005	PAGE : 3





SUGGESTED PANEL OPENING
(N.T.S.)



1. THE SUGGESTED PANEL OPENING IS INTENDED TO GIVE THE USER THE ABILITY TO HAVE REASONABLE JACK / PANEL CLEARANCES YET MAINTAIN RELIABLE GROUNDING CAPABILITY.
2. ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE ± 0.005 [0.13]

ORIGINATED BY	DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM. TOL. IN INCH	[] METRIC DIM. AS REFERENCE	
Zeng Xiao Chun	2011-08-18	MagJack® 10/100BT STACK JACK, SHIELDED PATENTED	SI-30113-F		UNIT : INCH [mm]	REV. : A1
DRAWN BY	DATE		FILE NAME	.X	SCALE : N/A	SIZE : A4
Zhang Ru Sheng	2011-08-18		SI-30113-F.DWG	.XX		PAGE : 4
				.XXX		