1. Functional Description of the AMG-SO101

The AMG-SO101 is a universal photo IC that resolves various signal processing tasks.It incorporates an IR emitting diode driver/oscillator, a photo detector receiver with differential signal evaluation for position detecting, and a decision stage.The AMG-SO101 provides a linear output, a data output, and switching outputs with high driving capabilities.

2. Features

- ❑ Photo receiver front end
- ❑ Logic for independent switch function
- ❑ Analog + digital sensor output for MCU
- ❑ Adjustable Tx LED driver
- ❑ 2 open drain outputs (150mA each)
- ❑ Over current protection
- ❑ Over temperature shutdown
- ❑ 2.5V voltage reference
- ❑ 5V linear regulator
- ❑ 7V linear regulator
- ❑ Wide supply range: 9V...36V
- ❑ Industrial temperature: -25°C...90°C
- ❑ Package: QFN24 – Body size: 4mm x 4mm
- ❑ RoHS compliant

3. Application

The AMG-SO101 is suitable for:

- ❑ Optical proximity switch modules
- ❑ Distance and position sensors
- ❑ Data transmission

3.1. Application Circuit Drawing

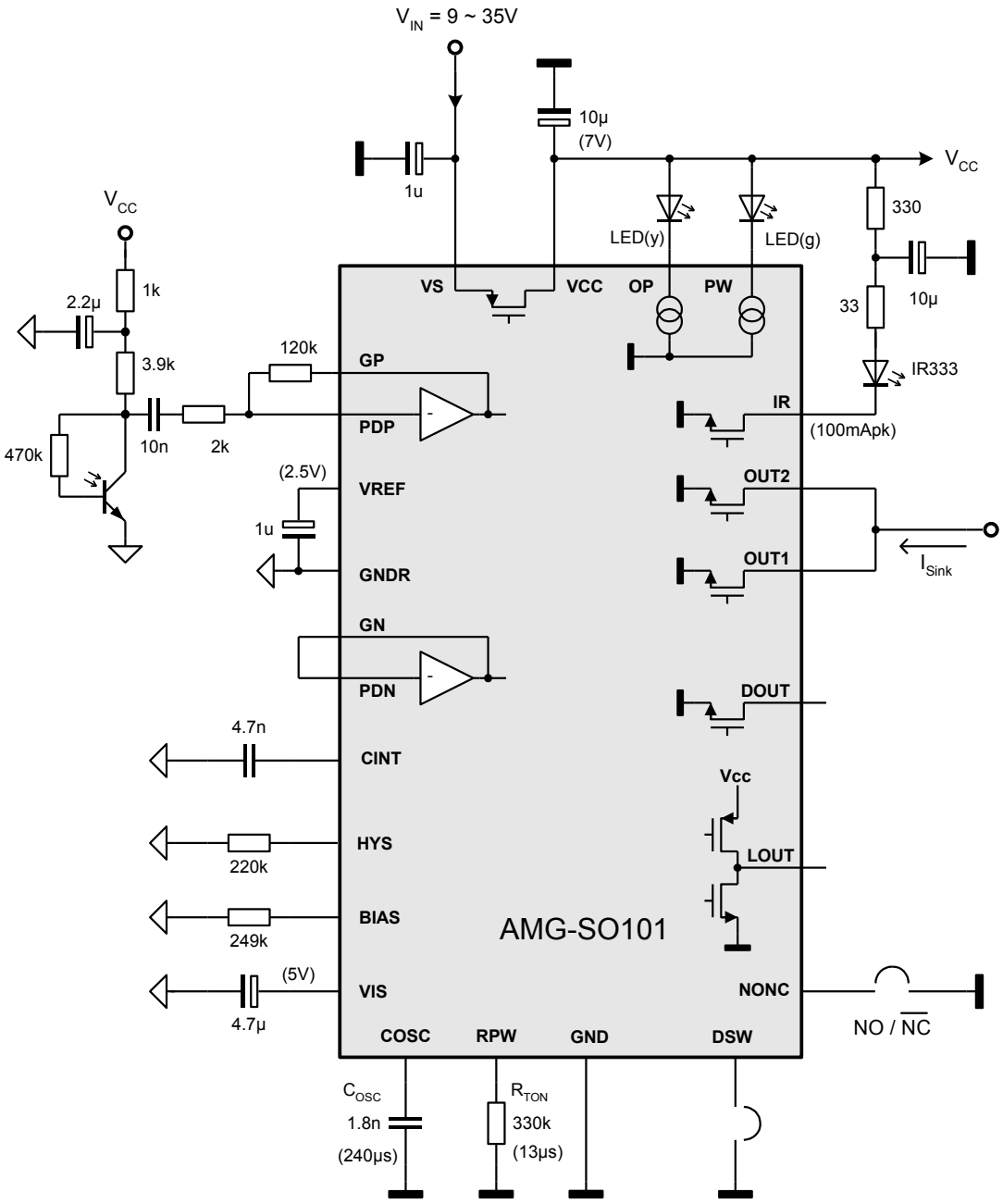


Figure 1: On-Off photo detector

3.2. Application Notes

Please refer to “Application Notes - AMG-AN-SO101”.

Table of Contents

4. Block Diagram

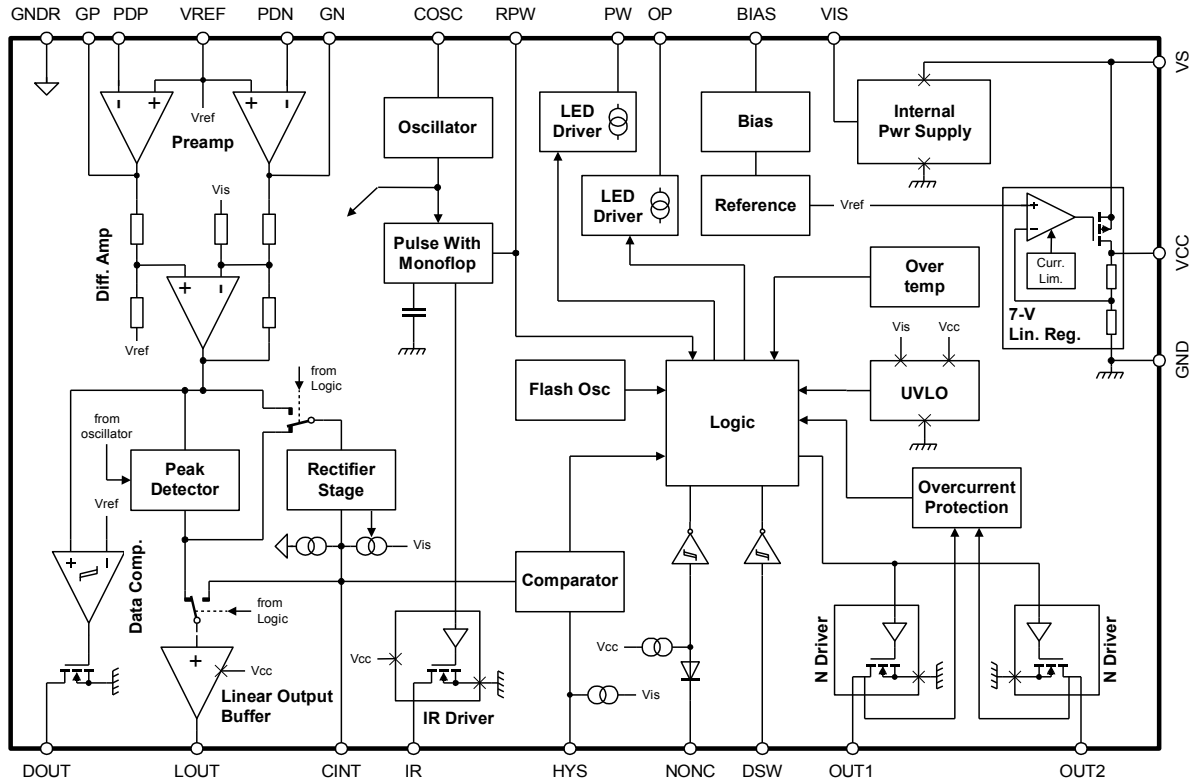


Figure 2: Simplified block diagram

5. Block Descriptions

Receiver Amplifier

The signal amplification is performed by two amplifier stages. External resistors are setting the gain of the preamplifier stage up to 60dB. The preamplifier is frequency compensated for a voltage gain of at least 10dB. The resistor between GP and PDP respectively GN and PDN should be greater than 50kΩ. The second amplifier stage has a fixed gain of 30dB. It also performs a shifting of the signal reference point from the reference voltage to the ground line.

a) Receiver amplifier with phototransistor input:

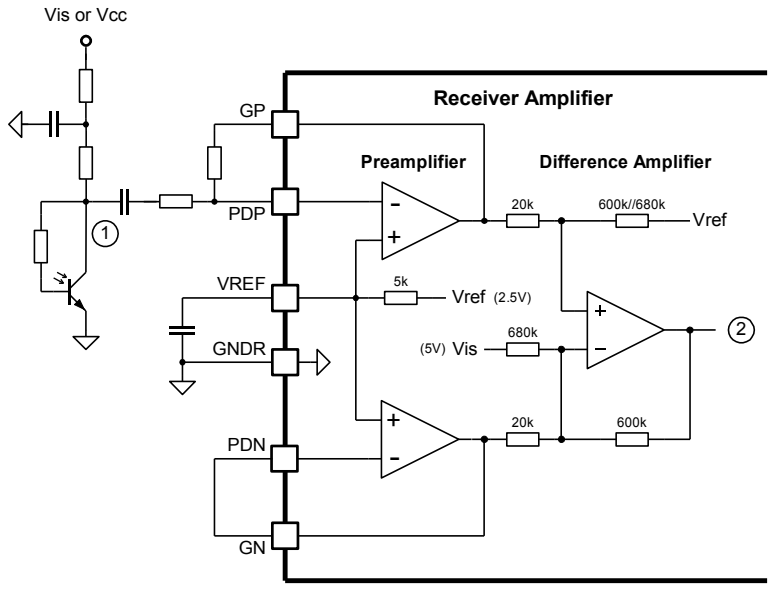


Figure 3: Receiver amplifier with phototransistor input

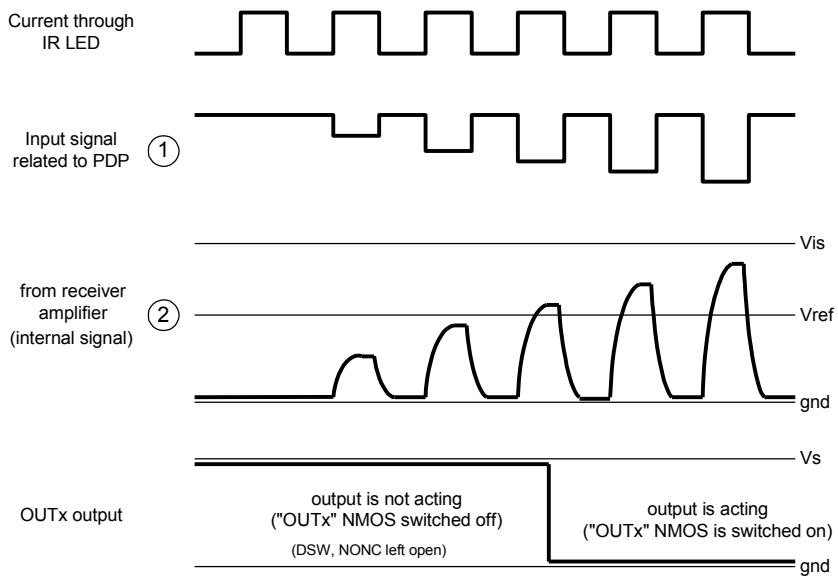


Figure 4: Signals in photoreceiver amplifier

For the use of a position sensitive detector (PSD) a second identical signal amplification channel needs to be wired in the same way as the first channel. The amplified signal at the PDN input is subtracted from the amplified signal at the PDP input. The figure below shows the analog signals at the PDP and PDN inputs in relation to the output.

b) Receiver amplifier with differential inputs:

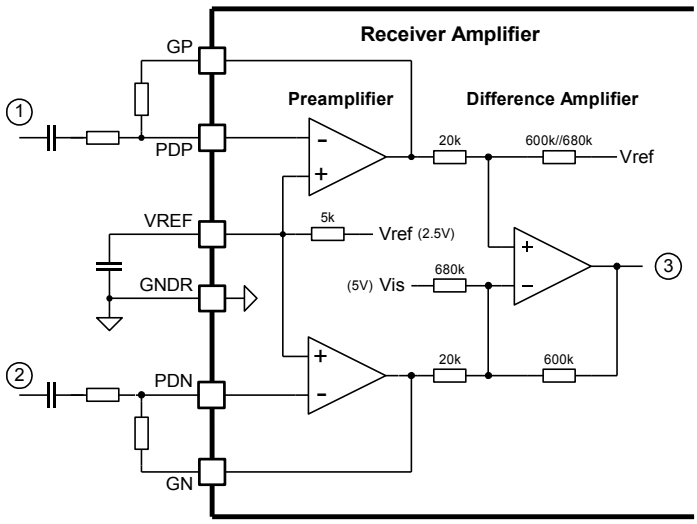


Figure 5: Receiver amplifier with differential input signals

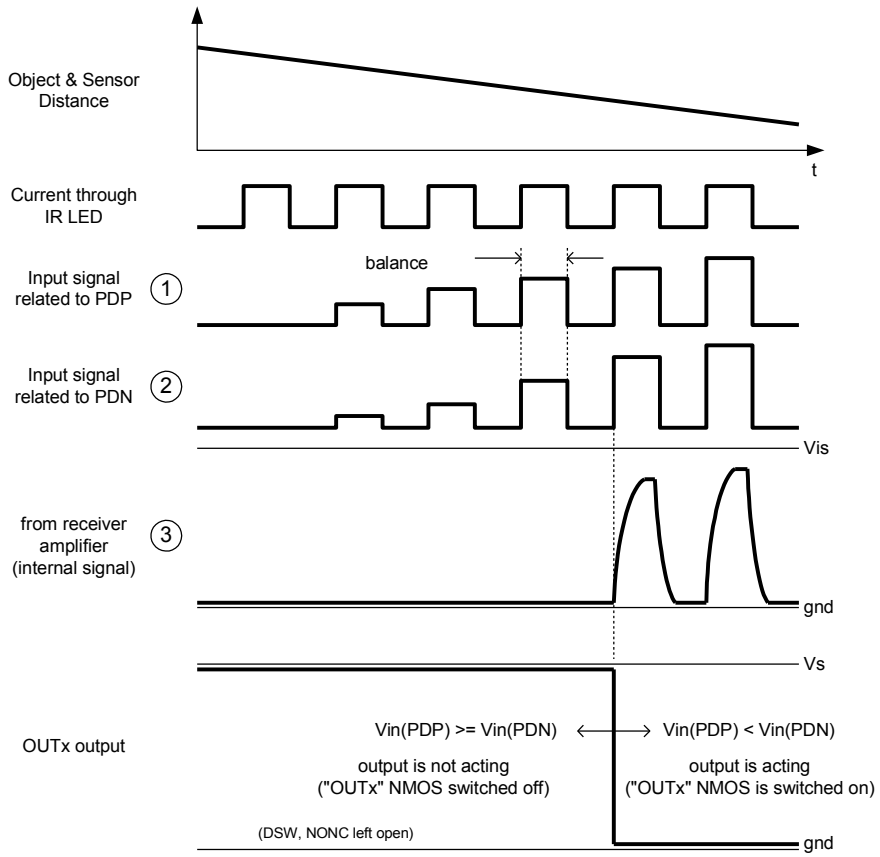


Figure 6: Signal relationship in PSD application

Data Comparator

The fast data comparator compares each amplified (and to the ground line shifted) impulse from the receiver-amplifier output with an internal reference. The reference voltage is equal to the center line of the signal voltage range. The comparator controls the open-drain output DOUT.

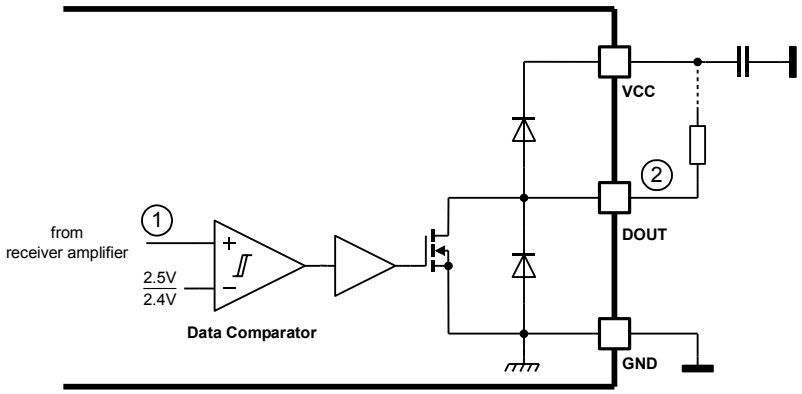


Figure 7: Data comparator

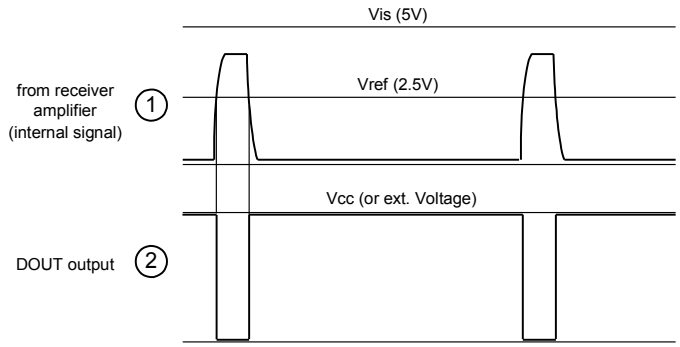


Figure 8: Signals of the data comparator

IR-emitting diode pulse oscillator

The oscillator triggers a monoflop which controls the IR-LED output driver stage. In addition, the delayed oscillator pulses are used to control the peak detector (in clocked mode). The values of the frequency setting capacitor and the pulse-width setting resistor are calculated according to the following formulas:

$$C_{OSC}\,[pF] = 7.6^{*} \times t_{per}\,[\mu s] \qquad R_{pw}\,[k\Omega\,] = 26.5^{*} \times t_{pw}\,[\mu s]$$ wherein

C_{OSC}	Capacitor at COSC pin, sets the oscillator period duration.	
R_{PW}	Resistor at RPW pin, sets the pulse width.	
t_{per}	Oscillator period duration.	t_{per} = 50µs ~ 500µs.
t_{pw}	Pulse width.	t_{pw} = 5µs ~ 30µs.

* The factor in the formulas are based on first sample evaluation.

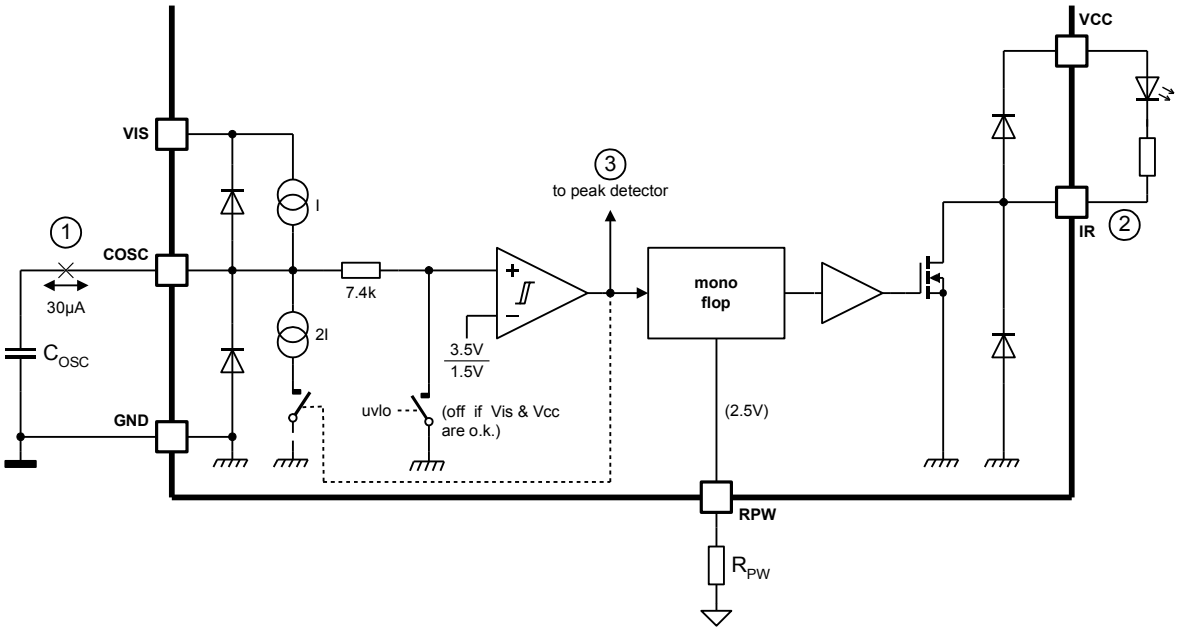


Figure 9: IR-emitting diode pulse oscillator

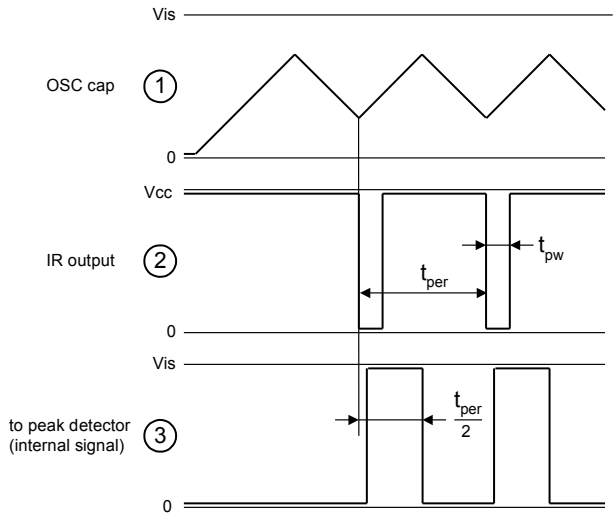


Figure 10: Signals of the oscillator

Peak Detector

The peak detector delivers an output voltage (referring to ground) equivalent to the magnitude of the received pulses.

The peak value of each single received and amplified impulse is stored in a capacitor for the “first” half of the oscillator-period duration. After that the capacitor is discharged to be ready for the next received

impulse. As a result, the peak-detector output signal has always a duty cycle of 0.5 independent of the actual pulse width.

The output signal of the peak detector is available buffered at the LOUT pin. It can be utilized as an input signal for an A/D converter with a conversion time smaller than the half of the oscillator-period duration.

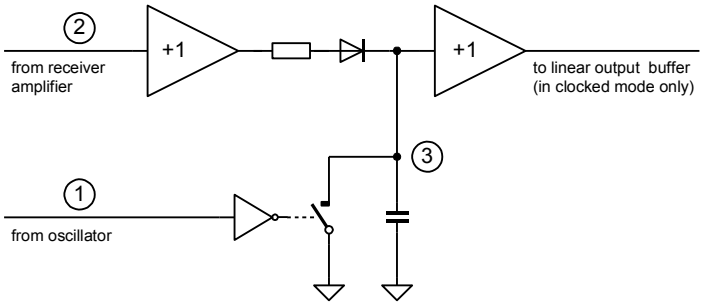


Figure 11: Peak detector

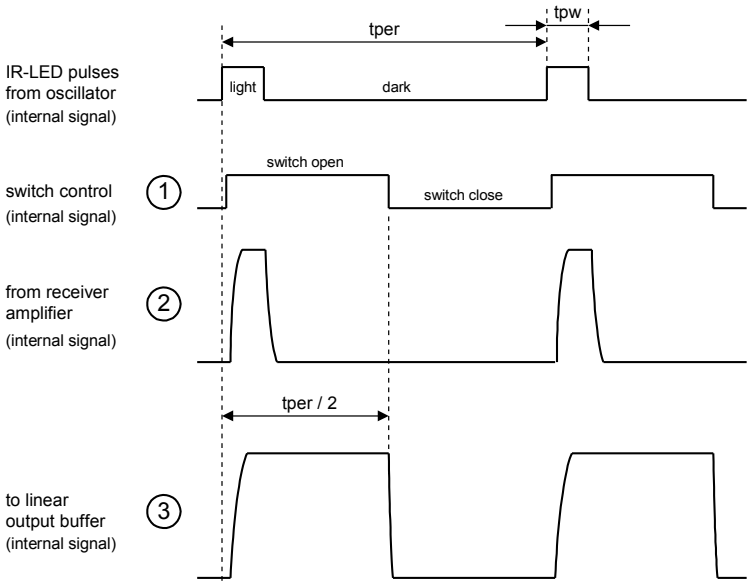


Figure 12: Signals of the peak detector in clocked mode

Linear Output Buffer

The linear output buffer amplifies the signal from the peak detector respectively from the rectifier stage. It “normalizes” the signal values to the voltage range of the V_{CC} rail, i.e. the internal signals are transformed into values from near zero up to near 7V.

In the *clocked mode* the linear output buffer delivers the “normalized” output voltage of the peak detector to the LOUT output. In the *non-clocked mode* the LOUT output presents the amplified output voltage of the rectifier stage.

Rectifier Stage

The rectifier stage “integrates” the incoming pulses and delivers a dc voltage (V_{Cint}, referring to ground) equivalent to the magnitude of the received pulses. This dc voltage is then compared with a reference voltage by the comparator stage.

The external capacitor at the CINT pin (C_{INT}) is charged during each single received pulse with the current I_{CH} until the voltage over the capacitor is equal to the magnitude of the incoming pulses. The external capacitor is discharged with a current I_{DCH} during the pulse pause (off-time after each impulse).

The value of the C_{INT} capacitor determines the rise and the decay of the voltage V_{Cint}.
Therefore the external capacitor C_{INT} sets the response time of the switching outputs (OUT1, OUT2). It also has effect on the ripple of the voltage V_{Cint}.
(Refer to: “Application hints, Dimensioning of the capacitor at CINT”.)

a) Rectifier stage in clocked mode

The incoming pulses are delivered by the peak detector. The C_{INT} charging/ discharging current values are 6µA / 2µA. The ratio of these currents – together with the fixed duty cycle of the input signal of 0.5 – delivers the same rise and decay time constant of the voltage over the capacitor V_{Cint}, independent of the actual duty cycle t_{pw} / t_{per}. Thus the rise and the decay of V_{Cint} is set only by the C_{INT} value.

b) Rectifier stage in non-clocked mode

The incoming pulses are delivered by the receiver amplifier directly, because the peak detector can not operate without a clocking signal. The C_{INT} charging /discharging current values are 30µA / 2µA.

For a given C_{INT} value is valid:
While the decay of the voltage at CINT (V_{Cint}) is fixed, the rise depends on the average charging current (itself a function of the duty cycle t_{pw} / t_{per}). In order to make use of smaller pulse-width values the current ratio is set to 15:1 in the non-clocked mode.

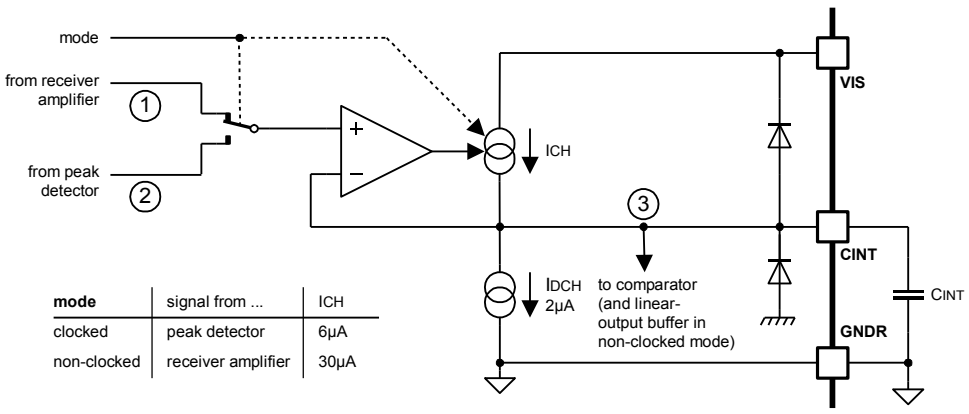


Figure 13: Rectifier stage

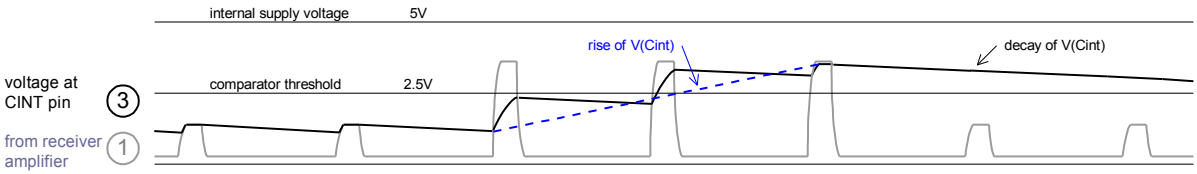


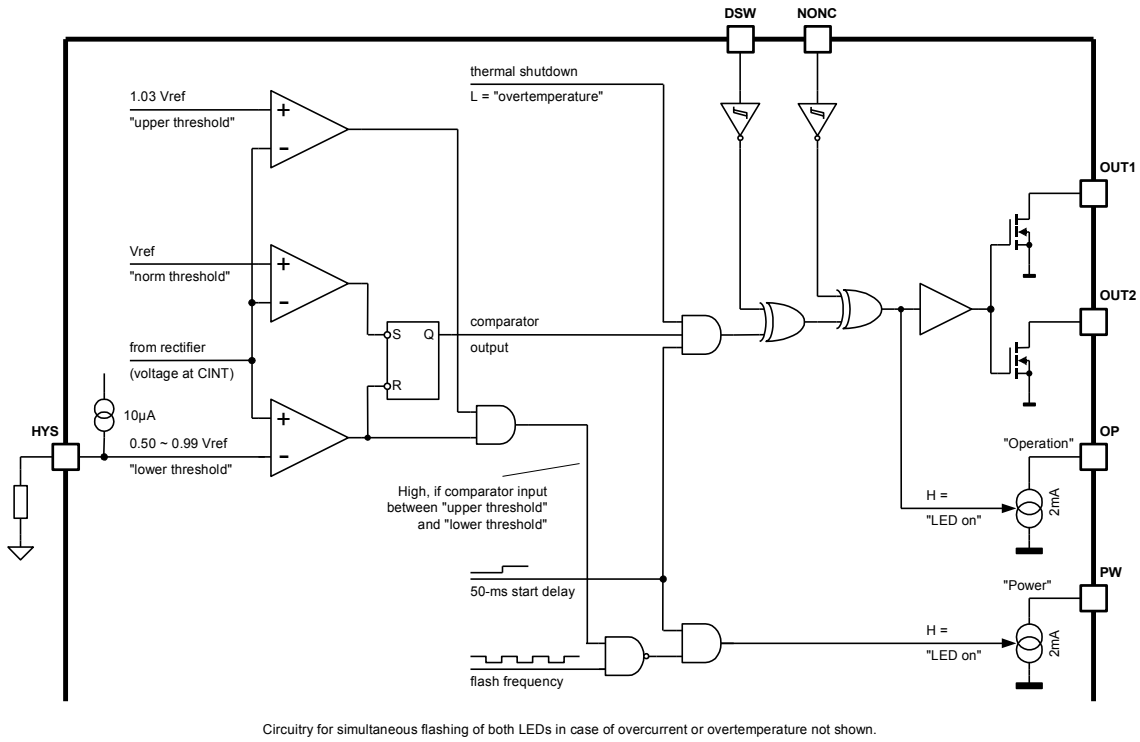
Figure 14: Signals of the rectifier stage in non-clocked mode

Comparator stage

The comparator stage compares the amplified and rectified (“integrated”) pulses with a reference voltage. It can be described as a Schmitt trigger with a positive going threshold (norm threshold) at the middle of the linear output swing, i.e. 3.5V. The negative going threshold (lower threshold) is adjustable externally in the range of 50% up to 99% of the norm threshold.

The Schmitt trigger is formed by two comparator circuits and a RS flip flop controlling the OUT1, OUT2 output stages and the “operation” indicator LED depending on the logical function of the two XOR gates controlled by the DSW and the NONC input.

With the help of a third comparator with a 103% reference, the “power” indicator LED is flashing in the transition region of the Schmitt trigger and slightly (3%) above.
Please refer to figure: “Illustration of indicator LED states”.



Circuitry for simultaneous flashing of both LEDs in case of overcurrent or overtemperature not shown.

Figure 15: Comparator and outputs

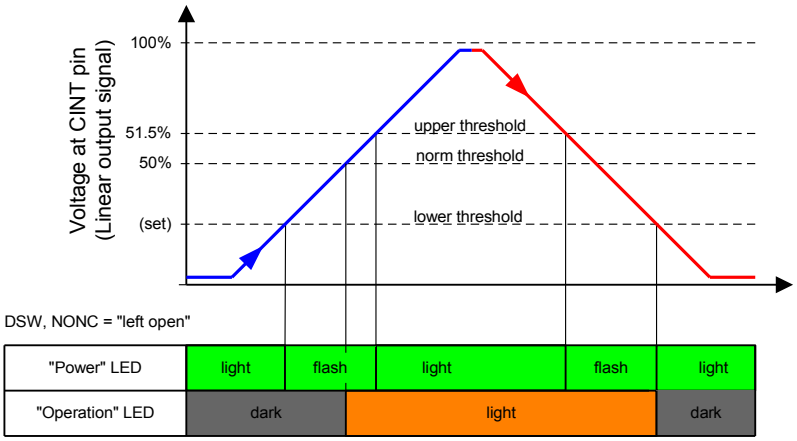


Figure 16: Illustration of indicator LED states

OUTx output driver and overload protection

The OUT1 and OUT2 outputs are controlled by the comparator stage depending on the logical function of the two XOR gates controlled by the DSW and NONC inputs.

The outputs are open-drain outputs. Each output has an on-resistance of typical 2.7Ω and is capable to sink up to 150mA to GND. The outputs can be connected to different loads with different supply voltages. Load currents up to 300mA are possible with both outputs connected together.

Both outputs are equipped with their own overcurrent circuitry. An overcurrent condition is established if a short-circuit current or a load current above the limit is applied at one of the outputs. The overcurrent protection circuitry switches the outputs off if the output current exceeds the limit of 200mA.

After a fixed 1-ms time period the outputs will be renewed switched on for 70µs. This repetitive switching-on behavior delivers an average output current of 14mA (per output). It allows to turn-on capacitive loads without exceeding the allowable power dissipation of the IC.

A overcurrent condition is indicated by the simultaneous flashing of both indicator LEDs. A short single overcurrent event will signalized with at least one flashing cycle (50ms light on, 50ms light off). In case of permanent overload (- repetitive switching-on behavior is active -) the LEDs are flashing as long as the overload condition is applied.

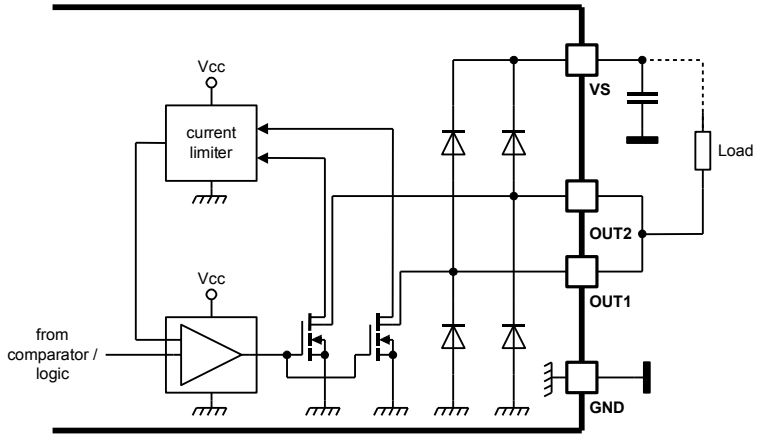


Figure 17: Output driver

Overtemperature detector

If the chip temperature exceeds the thermal shutdown temperature T_{jOT} both open-drain outputs (OUT1, OUT2) will switched off. This state is indicated by simultaneous flashing of the “operation” and the “power” LED. Both outputs are immediately working in the normal operation mode after relaxing of the chip temperature.

Undervoltage detectors and Start delay

There are two undervoltage detectors, one at the internal 5-V voltage rail (V_{IS}) with a 4.3-V threshold, another at the linear regulator’s 7-V rail (V_{CC}) with a 6.5-V threshold.

During powering-up the IC the decoupling capacitors will be charged with the short-circuit limiting

current of each regulator. If the voltages at the VIS and the VCC pin exceed their “power good” thresholds, the oscillator / IR driver start and the photo receiver amplifier is enabled.
Further the flash oscillator starts for one cycle to generate a delay of 50ms (start delay). During this time the OUT1, OUT2 outputs are blocked, and the rectifier stage charges the integration capacitor C_{INT} according the applied input signal level.

Indicator LED constant-current driver

The indicator-LED driver provides a constant current of 2mA to a LED at the output PW respectively OP. The constant current is steered to the V_{CC} rail during the off state of the LED preventing a modulation of V_{CC} when the LED flashes.

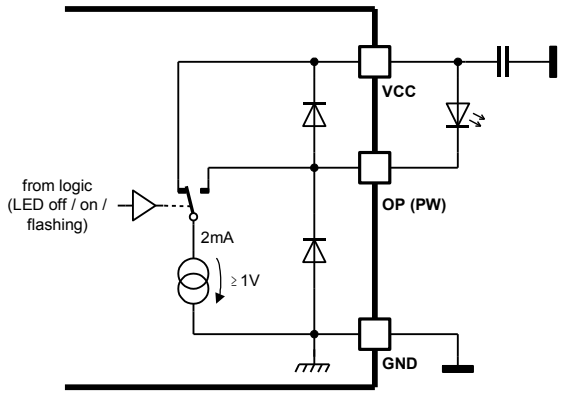
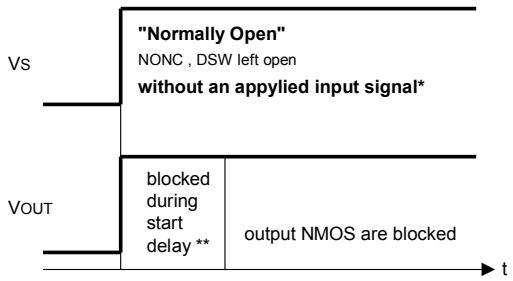
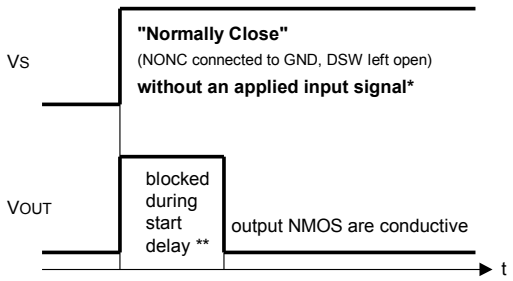


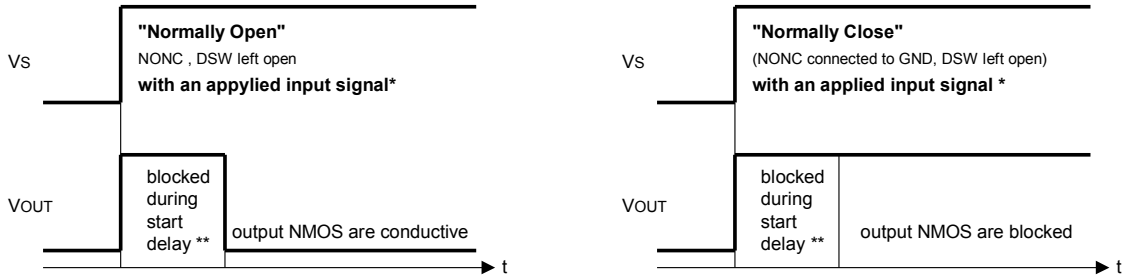
Figure 18: Indicator LED constant-current driver

Behavior of the OUT1, OUT2 outputs during powering up

After reaching the “power good” condition and after the start delay (50ms) OUT1, OUT2 are enabled.
The following four figures are illustrating the output behavior during powering-up the IC:







Note:

*) The case "without an applied input signal" always means an input-signal level that leads to a voltage over the capacitor at the CINT pin (C_{INT}) below the comparator threshold.

The case "with an applied input signal" always means an input-signal level that leads to a C_{INT} voltage above the comparator threshold.

**) "Blocked during start delay" means the blocking of the open-drain output MOSFET at OUT1, OUT2 until the "power good" condition is reached and the subsequent delay (start delay, 50ms) is expired.

6. Operation Modes

The IC can be used in various modes shown in the following table:

Receiver Modes:

Mode	Purpose	Wiring
PSD mode	Differential signal amplification using PSDs using both preamplifiers	Gain set with resistors at PDP, GP and PDN, GN
Phototransistor mode	Signal amplification using a phototransistor using only one preamplifier	Gain set with resistors at PDP, GP

Oscillator Modes:

Mode	Purpose / Function	Pins of interest
clocked mode	Transmitting and receiving light pulses with the same IC. Receiver detectors and pulse driver are synchronized. On-chip oscillator is in operation. The peak detector is clocked. The peak detector measures the peak value of each impulse and stores it for a half of the period duration. Rectifier stage integrates the output signal from peak detector. The resulting dc voltage controls the comparator.	Capacitor at **OSC** pin sets the pulse period duration. Resistor at **RPW** pin sets the pulse width. IR LED connected to **IR** pin. Gain set with resistors at the pins **PDP, GP, PDN, GN** according "receiver mode". Capacitor at **CINT** sets response time of the comparator. **LOUT** delivers an analog output voltage equivalent to the integrated peak value of

		the received pulses. **OUT1**, **OUT2** are controlled by the comparator.
non-clocked mode	Used if receiving light pulses can not be synchronized with the oscillator. On-chip oscillator is not in operation. Rectifier stage integrates the pulse from amplifiers directly. The resulting dc voltage controls the comparator. It is also present at the linear output.	**RPW** pin is wired to the **VIS** pin. **OSC** pin is wired to the **GND** pin. Gain set with resistors at the pins **PDP, GP, PDN, GN** according “receiver mode”. **LOUT** delivers an analog output voltage equivalent to the integrated value of the received pulses. Capacitor at **CINT** sets response time of the comparator. **OUT1**, **OUT2** are controlled by the comparator.

If the IC is only utilized as a data receiver using DOUT, the oscillator should be disabled with connecting the OSC pin to ground.

If the IC is only utilized as a transmitter using the IR output, connect the pins PDP to PG and PDN to GN.

7. Pinning

PIN#	Symbol	Description
1	PDN	Negative photo detector input
2	GN	Negative preamplifier output
3	CINT	Integration capacitor
4	LOUT	Linear output
5	DSW	D-ON/ D-OFF switch
6	NONC	Output status switch
7	VS	Supply voltage, unregulated input voltage
8	OUT1	Sink output 1
9	OUT2	Sink output 2
10	GND	Ground
11	IR	Infrared emitting diode
12	DOUT	Data output
13	PW	Power indicator LED
14	OP	Operation indicator LED
15	COSC	Pulse oscillator capacitor
16	VCC	Supply voltage, regulated output voltage
17	BIAS	Bias current programming resistor
18	RPW	Pulse width resistor
19	HYS	Hysteresis adjustment resistor
20	VIS	Decoupling capacitor for the internal power supply
21	GP	Positive preamplifier output
22	PDP	Positive photo detector input
23	VREF	Receiver reference voltage
24	GNDR	Receiver ground

1)

8. Pin description

VS **Supply voltage,**

9V up to 35V supply voltage, unregulated input voltage of the linear regulator. Decoupling capacitor near VS pin needed. Please select the most suitable capacitor value according to noise level and frequency of power supply.

VCC **Supply voltage, regulated output voltage**

Output voltage of the linear regulator. It must be decoupled to GND externally.

VIS **Decoupling capacitor for the internal power supply**

Output of a second internal linear regulator. It must be decoupled to GNDR externally. This ensures the needed power supply rejection of all receiver stages at the presence of switching noise of IR driver and loads. The output voltage is 5V. A current up to 10mA can be provided to an additional external load under consideration of the IC's total power dissipation.

GND **Ground**

Common ground, ground for IR driver and OUT driver.

GNDR **Receiver reference ground**

Analog ground, return of all receiver stages and components.

VREF **Receiver reference voltage**

2.5-V reference voltage for the receiver input amplifier. It must be decoupled to RGND externally. This ensures the needed power supply rejection of the receiver input amplifier.

IR **Infrared emitting diode**

Open-drain output, cathode terminal of the IR emitting diode.

PDP **Positive photo detector input**

Inverting input of the receiver's preamplifier, phototransistor input.

GP **Positive preamplifier output**

Output of the receiver's preamplifier and terminal for the gain-setting feedback resistor.

PDN **Negative photo detector input**

Inverting input of the receiver's preamplifier. If unused, connect to GN.

GN **Negative preamplifier output**

Output of the receiver's preamplifier and terminal for the gain setting feedback resistor. If unused, connect to PDN.

CINT **Integration capacitor**

Integration capacitor of the rectifier stage.

HYS **Hysteresis adjustment**

Resistor to adjust the lower threshold of the receiver comparator stage.

OUT1 **Sink output 1**

Open drain output, drain of a n-channel power MOSFET, has to be connected with OUT2.

OUT2 **Sink output 2**

Open drain output, drain of a n-channel power MOSFET, has to be connected with OUT1.

COSC **Oscillator capacitor**

Sets the pulse repetition frequency of the IR emitting diode pulses in the “clocked mode”.
Disables the oscillator if connected to ground. Connect to VIS for “non-clocked mode”.

RPW **On-time resistor**

Sets the pulse width of the IR emitting diode pulses.

BIAS **Bias current programming resistor**

Sets the current of the internal bias current generator and influences the oscillator frequency.

LOUT **Linear output**

Output of photo receiver, provides a signal correlated to the input signal level.
In the clocked mode LOUT provides the amplified output of the peak detector, in non-clocked mode it provides the amplified output of the rectifier stage. The output voltage comprises the range between V_{CC} and ground.

DOUT **Data output**

Data output of the photo receiver. Open-drain output, needing a pull-up resistor to V_{CC} or to another logic supply voltage.

DSW **D-ON/ D-OFF switch**

Connect to GND for inverting of the comparator output signal.
Leave open or connect to VCC for passing through of the comparator output signal non-inverted.

NONC **Output mode switch**

“Normally open” mode if left open, or connected to VCC or VS;
“Normally close” mode if connected to ground.

OP **Operation indicator LED, cathode**

Output of a 2-mA current source, connect to cathode terminal of the LED. The “operation” LED

indicates the status of the comparator output (dependent on the inputs DSW and NONC).
For the comparator thresholds and the indicator lighting state see “Detailed Block Description, Comparator stage”.
The “operation” LED flickers in overtemperature condition or in overcurrent condition simultaneously with the “Power” LED.

PW **Power indicator LED, cathode**

Output of a 2-mA current source, connect to cathode terminal of the LED. The “power” LED is controlled by two undervoltage detectors monitoring the voltages at VCC and VIS. A steady-state condition of the power supply after start is indicated with permanent light.

The “power” LED flickers in the transition region of the comparator. For the comparator thresholds and the indicator lighting state see “Detailed Block Description, Comparator stage”.

The “power” LED flickers in overtemperature condition or in overcurrent condition simultaneously with the “operation” LED.

9. Absolute Maximum Ratings

The Absolute Maximum Ratings may not be exceeded under any circumstances.

#	Symbol	Parameter	Min	Max	Unit
1	V_S	Supply voltage, unregulated input voltage	-0.3	36	V
2	V_{OUT1}, V_{OUT2}	Output voltage	-0.3	V_S	V
3	V_{OP}, V_{PW}, V_{IR}	Indicator LED outputs, IR output	-0.3	V_{CC}	V
4	V_{DSW}	Selector switch inputs	-0.3	V_{CC}	V
5	V_{DOUT}	Data output	-0.3	V_{CC}	V
6	V_{LV}	Inputs GP, PDP, GN, PDN, VREF, HYS, BIAS, RPW, OSC, CINT	-0.3	V_{IS}	V
7	V_{NONC}	Output-status switch input	-0.3	V_S	V
8	I_{OUT1}, I_{OUT2}	OUT1, OUT2 output peak current		300	mA
9	I_{IR}	Output peak current		500	mA
10	I_{DOUT}	Data-output peak current		10	mA
11	I_{VCC}	Load current from V_{CC}		50	mA
12	T_{stg}	Storage temperature range	-55	150	°C
13	T_{sold}	Soldering temperature		300	°C
14	T_j **	Junction temperature		150	°C
15	R_{thja} **	Thermal resistance junction to ambient		30	K/W
16	V_{ESD} *	ESD protection rating	-1	1	k V

Note:

* according Human Body Model

** Tj = Rthja x Ptot + Tamb

10. Electrical Characteristics

10.1. Operational Range

#	Symbol	Parameter	Min	Max	Unit
1	V_S	Supply voltage, unregulated input voltage	9	35	V
2	I_{IRpk}	IR-output peak current		400	mA
3	I_{IRavg}	IR-output average current		30	mA
4	$I_{VCCload}$	Allowed load current at VCC	28 ***		mA
5	V_{th_low}	Lower comparator-threshold adjust range	0.50 x V_{th_norm}	0.99 x V_{th_norm}	
6	t_{per}	IR oscillator period duration	50	500	µs
7	t_{pw}	IR oscillator pulse width	5	30	µs
8	T_{amb}	Ambient temperature range	-25	90	°C

Note:

*** The load current is the sum of all variable external load currents. The indicator-LED currents are part of the “operating supply current”, I_{Vop}. External load currents are caused by the IR emitting diode, the phototransistor, currents drawn from the linear output, or any other loads at the VCC pin. The minimum load current value is valid for the specified thermal resistance Rthja.

10.2. DC Characteristics

The typical values, unless otherwise specified, are given with V_S = 24V, T_j = 25°C

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SECTION: General							
1		Operating supply current	no loads, LEDs on	3.6	5.2	7.0	mA
2		Input bias current at inputs NONC, DSW	V_{input} = 0	14	25	40	µA
3		Receiver reference voltage		2.37	2.50	2.63	V
4		Reference voltage for the bias- current programming resistor	R_{BIAS} = 249kΩ		2.50 *		V
5		Internal supply voltage		4.70	5.00	5.30	V

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SECTION: Output stages							
6	$R_{OUT\ (ON)}$	OUTx-output MOSFET on-resistance	I_{OUT} =150mA, OUT1 or OUT2 at 25 °C at 25 °C ~ 140°C	1.9 1.5	2.5 2.5	3.1 5.1	Ω Ω
7	I_{OUT_SC}	Output limiting current of OUT1, OUT2	OUT1 // OUT2	195	220	255	mA
8	$R_{IR\ (ON)}$	IR-output MOSFET on-resistance	I_{IR} =150mA at 25 °C at 25 °C ~ 140°C	1.5 1.3	2.0 2.0	2.5 4.1	Ω Ω
9	I_{LED}	Indicator-LED output current	V_{OP}, V_{PW} = V_{CC}	1.6	2.0	2.4	mA
10	$-I_{LOUTsrc}$	Linear output source current	$V_{CC} - V_{LOUT}$ = 2.5V		1*		mA
11	$I_{LOUTsnk}$	Linear output sink current	V_{LOUT} = 2.5V		1*		mA
12	V_{LOUT_H}	LOUT high level output voltage	$-I_{LOUTsrc}$ = 0.5mA		V_{CC} – 0.7	V_{CC} – 1	V
13	V_{LOUT_L}	LOUT low level output voltage	$I_{LOUTsnk}$ = 0.5mA		0.5	0.8	V
14	V_{DOUT_L}	DOUT low level output voltage	$I_{LOUTsnk}$ = 0.5mA		0.5	0.8	V
SECTION: Under voltage lock-out							
15	V_{CCok}	Turn-on threshold	increasing VS from < 5V	5.7	6.3	7.0	V
16	V_{CCuv}	Lock-out threshold	decreasing VS from > 8V	5.2	5.8	6.3	V
SECTION: Overtemperature							
17	T_{jOT}	thermal shutdown temp.		140	150	160	°C
18	R_{thj-a}	Thermal resistance j-a			42		K/W
SECTION: Photo receiver							
19	$-I_{GXsrc}$	Preamp output source current	$V_{IS} - V_{Gx}$ = 2V	>2 *			mA
20	I_{GXsnk}	Preamp output sink current	V_{Gx} = 2V	>2 *			mA
SECTION: Rectifier stage							
21	$-I_{CH\_clk}$	CINT charging current in clocked mode	V_{CINT} = 2.5V	4.7	6.3	7.9	µA
22	$-I_{CH\_non}$	CINT charging current in non-clocked mode	V_{CINT} = 2.5V	23.6	31.5	39.4	µA
23	I_{DCH}	CINT discharging current	V_{CINT} = 2.5V	1.6	2.1	2.6	µA
SECTION: Comparator							

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
24	V_{th_up}	Upper comparator threshold		1.02 x V_{th_norm}	1.03 x V_{th_norm}	1.04 x V_{th_norm}	V
25	V_{th_norm}	Norm comparator threshold		2.37	2.50 **	2.63	V
26	$-I_{th\_low}$	Lower comparator-threshold setting current (HYS current)	V_{HYS} = 1.0V ~ 2.5V	9	10	11	µA
SECTION: Linear regulator							
27	V_{CC}	Regulated output voltage		6.6	7.0	7.4	V
28	$\lvert \Delta V_{CCline} \rvert$	Line regulation	V_S = 9V to 35V		1	10	mV
29	$\lvert \Delta V_{CCload} \rvert$	Load regulation	I_{VCC} = 0 to 20mA		40	70	mV
30	I_{VCClim}	Regulator limiting current		40	60	80	mA

Note:

*This is an information parameter only. It is not needed to secure IC's function, showed for dimensioning purposes.

**The comparator threshold is the center of the signal range (0 ~ 5V) determined by the internal supply voltage of 5V.
The comparator threshold appears as 3.5V related to the linear output range corresponding to the VCC supply voltage of 7V.

10.3. AC Characteristics

The typical values, unless otherwise specified, are given with V_S = 24V, T_j = 25°C

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SECTION: General							
1		**LED flashing on time**		40	50	60	ms
2		**LED flashing off time**		40	50	0	ms
SECTION: Photo receiver							
3	t_{DOUT}	**DOUT response time**	see test "DOUT response		2.3	3	µs
4	t_{r_DOUT}	Output rise time	time" in test chapter		0.6	1.0	µs
5	t_{f_DOUT}	Output fall time			0.1	0.2	µs
6	BW	Gain bandwidth product of preamplifier			3		MHz
7	A_V	Voltage amplification of preamplifier	see test "Voltage amplification …" in test chapter		90		dB

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
8	A_2	Gain of fixed gain amplifier		29	30	31	-
SECTION: Output stages							
9		LOUT response time	see test “LOUT response time” in test chapter		5	15	µs
10		Comparator-to-output delay	see test “comparator-to-output delay” in test chapter		0.4	0.7	µs
11		Over-all output response time in non-clocked mode	see tests “Over-all output response time”		150 ~ 250	300	µs
12		Over-all output response time in clocked mode	in test chapter		300 ~ 400	500	µs
SECTION: IR pulse oscillator							
13	t_{per3n3}	IR oscillator period duration at C_{OSC} = 3.3nF	C_{OSC} = 3.3nF, R_{Bias} = 249kΩ	365	430	495	µs
14	t_{pw750k}	IR oscillator pulse width at R_{PW} = 750kΩ	R_{PW} = 750kΩ, R_{Bias} = 249kΩ	23	28	33	µs
SECTION: Linear regulator							
15	RR_{VCC}	Ripple rejection at VCC pin	C_{VCC} = 100nF, $f_{VS.SINUS}$ = 10kHz	60			dB
16	RR_{VIS}	Ripple rejection at VIS pin	C_{VIS} . 330nF, $f_{VS.SINUS}$ = 10kHz	60			dB
17	RR_{VREF}	Ripple rejection at VREF pin	C_{VREF} ≥ 330nF, $f_{VS.SINUS}$ = 10kHz	60			dB
18	RR_{CINT}	Ripple rejection at CINT pin	C_{CINT} ≥ 3.3nF, $f_{VS.SINUS}$ = 10kHz	60			dB

Note:

11. Application

11.1. Example Application Circuits

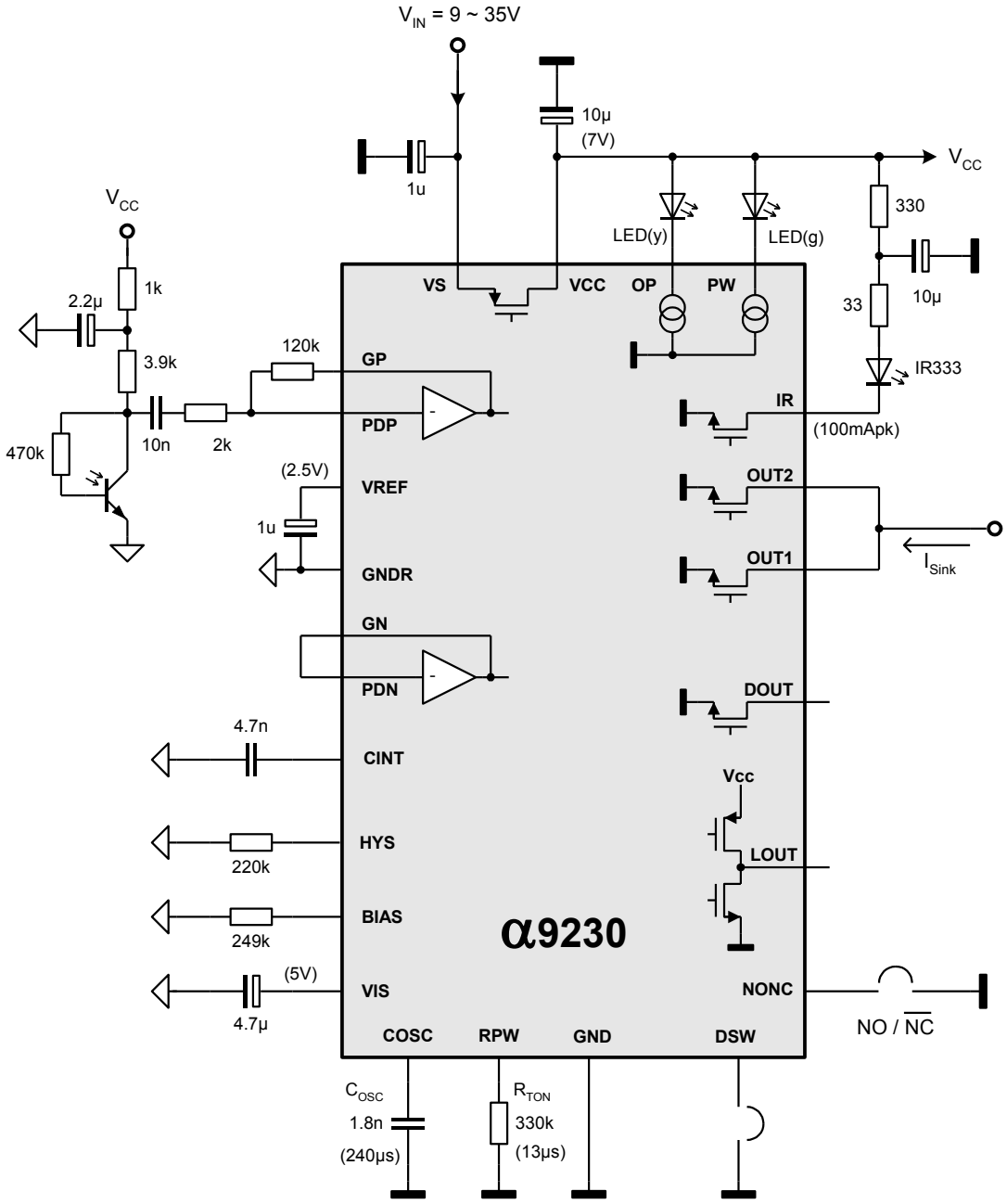


Figure 19: On-off photo detector with fast response (tcmp-OUT < 500µs)using an external non-synchronized pulsed light source

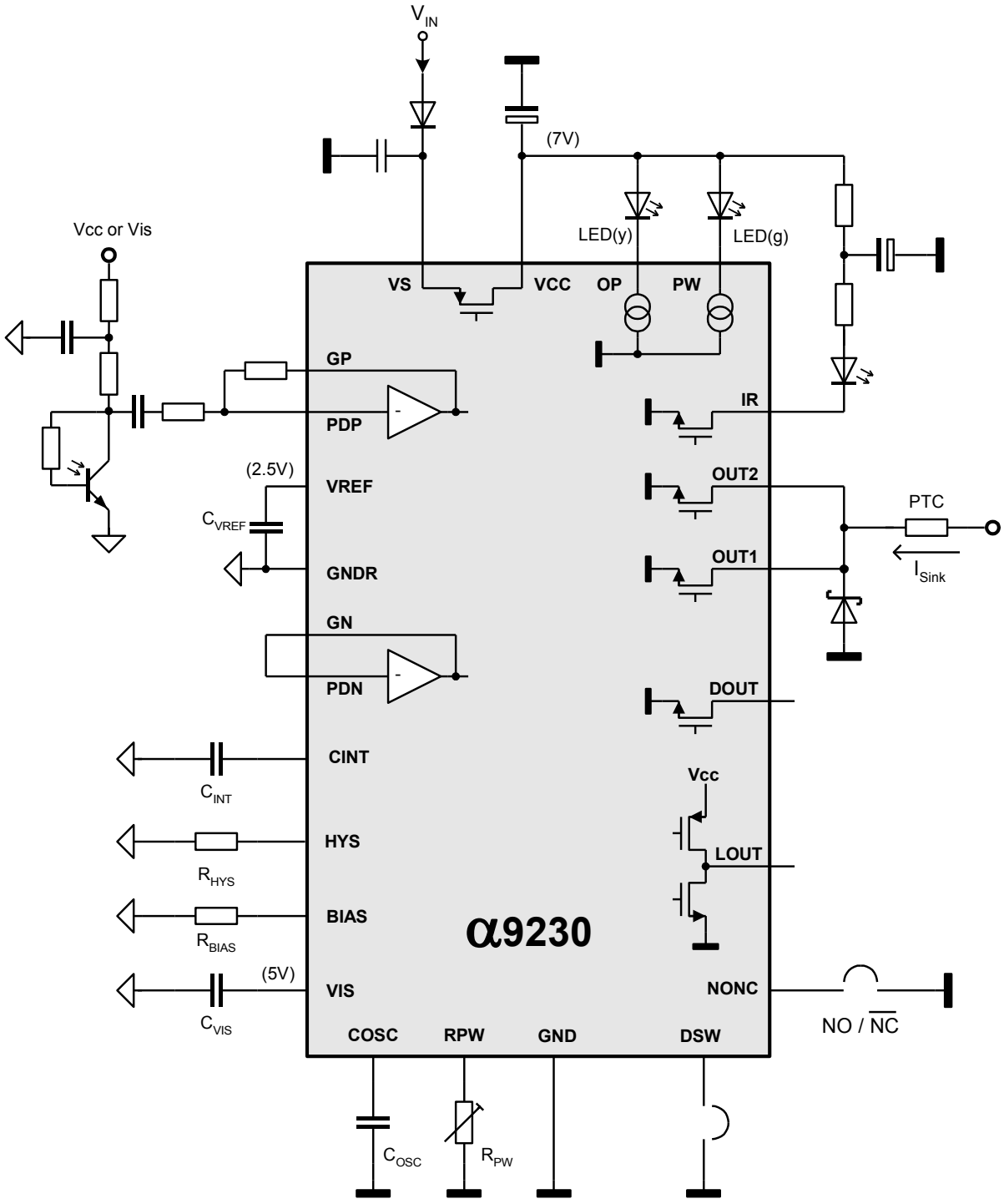


Figure 20: Proximity switch module with reverse polarity protection

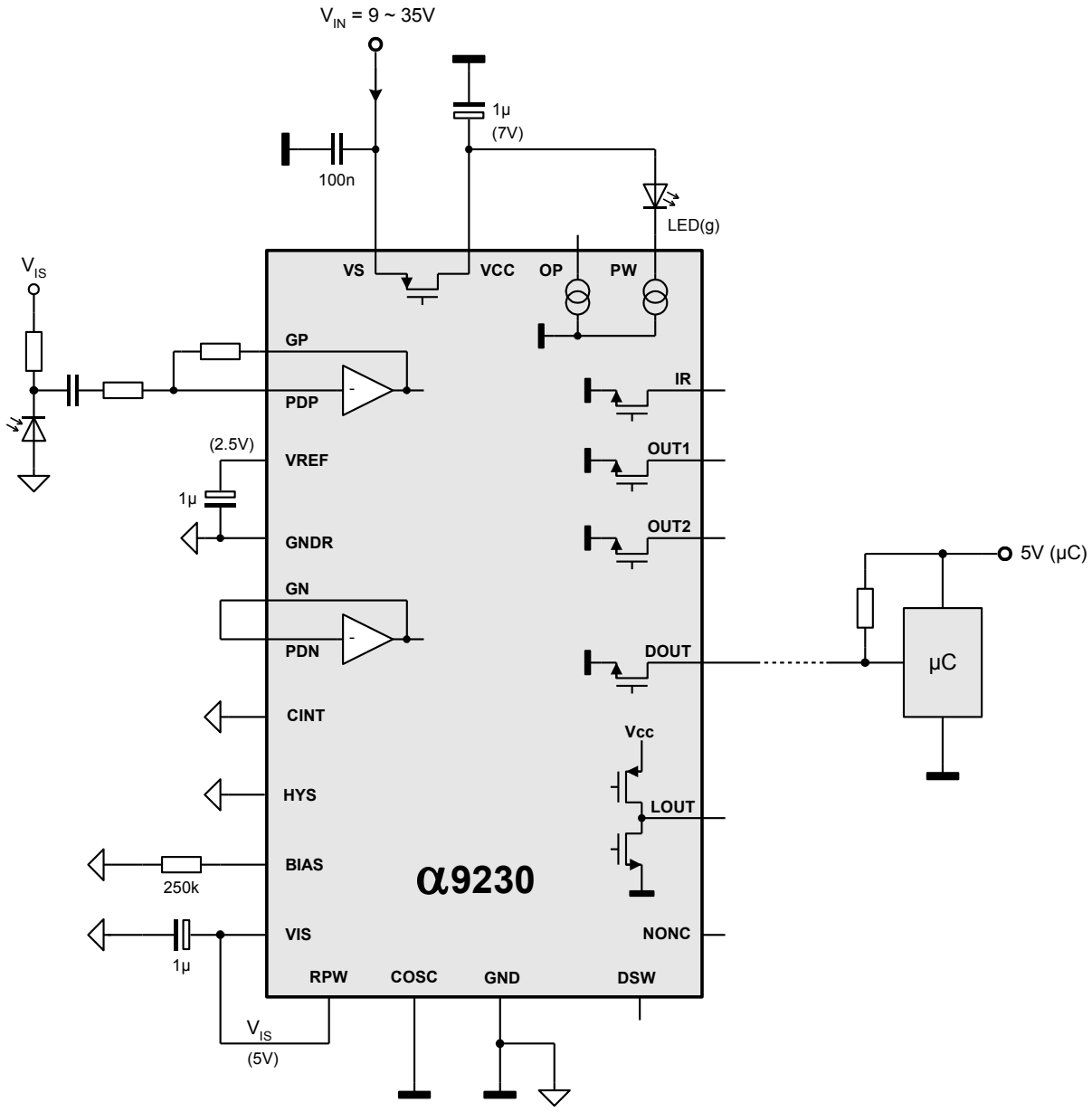


Figure 21: Photo receiver for data communication (other outputs not used)

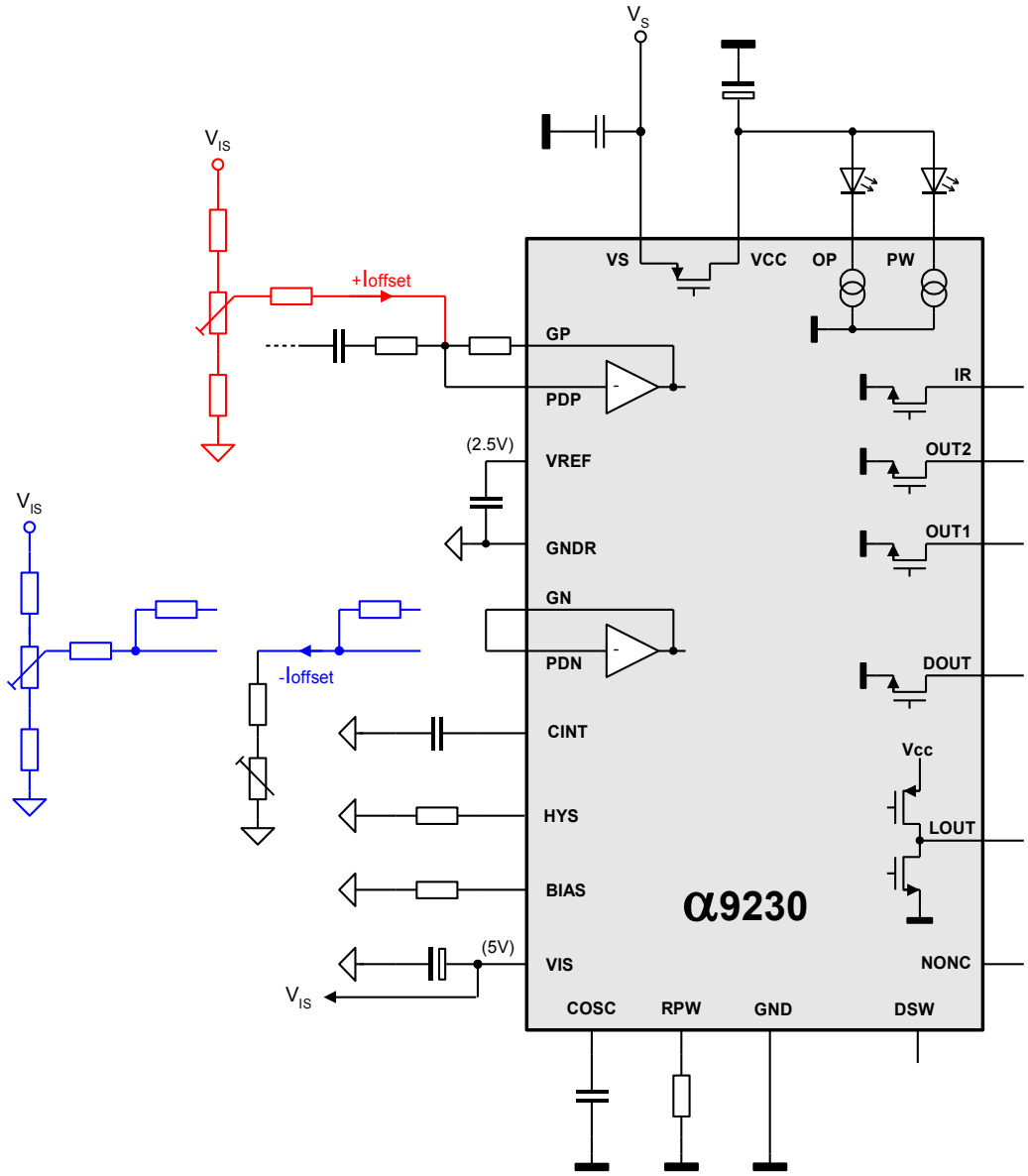


Figure 22: Methods adjusting the "resting voltage" at CINT (offset correction)

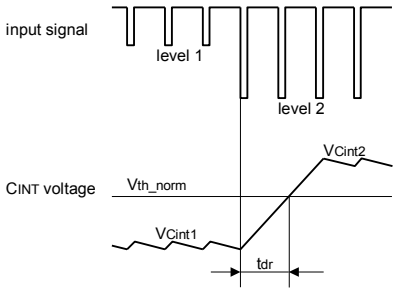
11.2. Application Notes

Dimensioning of the capacitor at CINT / Estimation of output response time

The output response time is defined as the amount of time that is needed for the reaction of the OUT1/ OUT2 output to a large sudden input-signal level change. This time is nearly caused only by the charging / discharging of the C_{INT} capacitor in the rectifier stage. The delays of the following stages (from comparator to output driver) are negligible small (< 2µs). The following shows how the delays caused by the charging / discharging of the C_{INT} can be estimated.

a) at input-signal level increase, in non-clocked mode

C_{INT}	external “integration” capacitor at CINT pin
t_{dr}	delay caused by V_{Cint} rise, time until V_{Cint1} exceeds the norm comparator threshold
I_{CHavg}	average charging current
V_{th_norm}	norm comparator threshold (2.5V)
V_{Cint}	voltage over C_{INT}
V_{Cint1}	C_{INT} voltage # 1 as a result of input-signal level and receiver amplification



$$t_{dr} = \frac{C_{INT} \cdot (V_{th\_norm} - V_{Cint1})}{I_{CHavg}}$$

where

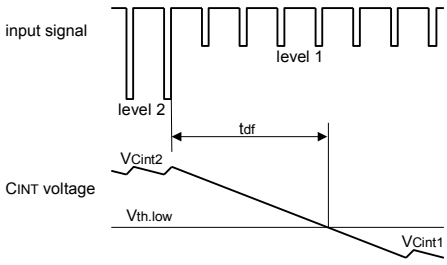
$$I_{CHavg} = (I_{CH} - I_{DCH}) \cdot \frac{t_{pw}}{t_{per}} + I_{DCH}$$

I_{CHavg}	average charging current of rectifier stage, depending on duty cycle
I_{CH}	charging current of rectifier stage (value without sign, I_{CH_non} = 30µA)
I_{DCH}	discharging current of rectifier stage (value without sign, I_{DCH} = 2µA)
t_{pw}	pulse width of received pulses (time during I_{CH} flows is slightly smaller because of receiving delays and pulse shape)
t_{per}	pulse period duration

b) at input-signal level decrease, in non-clocked mode

$$t_{df} = \frac{C_{INT} \cdot (V_{Cint2} - V_{th\_low})}{I_{DCH}}$$

t_{df}	delay caused by V_{Cint} decay, time until V_{Cint2} falls below the lower comparator threshold
C_{INT}	external “integration” capacitor at CINT pin
V_{Cint2}	C_{INT} voltage # 2 as a result of input-signal level and receiver amplification
I_{DCH}	discharging current of rectifier stage (value without sign, I_{DCH} = 2µA)
V_{th_low}	lower comparator threshold (50% ~ 99% of 2.5V set by resistor at HYS pin)



c) in clocked mode

Estimation according to a) and b) with the simplification that the average charging current is - independent of the duty cycle - equal to the discharging current. ($|I_{CHavg}| = |I_{DCH}|$, see also description of *peak detector.*)

General hints to achieve a fast output response time in non-clocked mode

Choose:

- short pulse period duration
- wide pulse to get a high average C_{INT} charging current
- small C_{INT} value
- large comparator hysteresis to be insensitive to the ripple voltage over V_{Cint}

Synchronization with an external oscillator signal

Note if the COSC input is used to synchronize the IC with an external signal:

- the switching thresholds of the COSC inputs are 3.5V / 1.5V.
- the input voltage must not exceed the internal supply voltage V_{IS}.
- the input current is 30µA with alternating sign
- the equivalent input resistance of COSC is about 7.5k during powering up of the IC (until V_{CC} and V_{IS} are reaching their “power good” thresholds).
- the pulsing of the IR output starts one period delayed to the external signal (see figure “signal of the oscillator” in the detailed description chapter).

Improvement of Thermal Resistance

R_{thja} = 30 K/W, based on Four-Layer (2S2=) JEDEC Test Board with 16 vias.

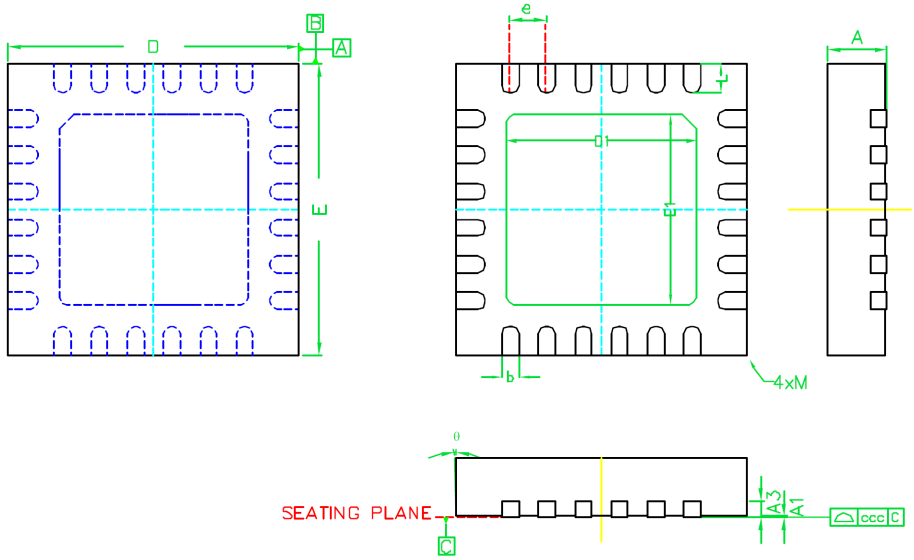
12. Order Information

AMG-SO101-IQN24R (QFN24 - shipment in tape and reel)

13. IC-Package

Package: QFN 24L

Package Outline Drawings



	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
⚠	A	0.80	0.85	0.90
⚠	A1	0	0.010	0.030
	A3	——	0.20REF.	——
	b	0.18	0.23	0.28
⚠	D	3.95	4.00	4.03
⚠	D1	——	2.60BSC	——
⚠	E	3.95	4.00	4.03
⚠	E1	——	2.60BSC	——
	e	——	0.50BSC	——
⚠	L	0.35	0.40	0.45
	θ	−12	——	0
⚠	ccc	——	0.08	——
	M	——	——	0.05
	Burr	0	0.030	0.060

1.ALL DIMENSIONS ARE IN MILLMETERS, θIS IN DEGREES.
2.M : THE MAXIMUM ALLOWABLE CORNER ON THE MOLDED PLASTIC BODY CORNEF
3.DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
4.DIMENSION E DOES NOT INCLUDE INTERTERMINAL MOLD PROTRUSIONS OR TERMINAL PROTRUSIONS.INTERMINAL MOLD PROTRUSIONS AND/OR TERMINAL PROTRUSIONS SHALL NOT EXCEED 0.20mm PER SIDE.
5.DIMENSION b APPLIES TO PLATED TERMINALS. DIMENSION A1 IS PRIMARILY Y TERMINAL PLATING,BUT MAY OR MAY NOT INCLUDE A SMALL PROTRUSION OF TERMINAL BELOW THE BOTTOM SURFACE OF THE PACKAGE.
6.JEDEC STANDARD MO-220

14. IC-Marking

αSO101

4 digit date code

7 digit lot code

15. Notes and Cautions

15.1. ESD Protection

The Requirements for Handling Electrostatic Discharge Sensitive Devices are described in the JEDEC standard JESD625-A. Please note the following recommendations:

- ❑ When handling the device, operators must be grounded by wearing a for the purpose designed grounded wrist strap with at least 1MΩ resistance and direct skin contact.
- ❑ Operators must at all times wear ESD protective shoes or the area should be surrounded by for ESD protection intended floor mats.
- ❑ Opening of the protective ESD package that the device is delivered in must only occur at a properly equipped ESD workbench. The tape with which the package is held together must be cut with a sharp cutting tool, never pulled or ripped off.
- ❑ Any unnecessary contact with the device or any unprotected conductive points should be avoided.
- ❑ Work only with qualified and grounded tools, measuring equipment, casing and workbenches.
- ❑ Outside properly protected ESD-areas the device or any electronic assembly that it may be part of should always be transported in EGB/ESD shielded packaging.

15.2. Storage conditions

The AMG-SO101 corresponds to moisture sensitivity classification ML2, according to JEDEC standard J-STD-020, and should be handled and stored according to J-STD-033.

16. Disclaimer

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