
Analog System Base Chip, I/O PowerStage, OP-Amps

1. Functional Description

The AMG-PU005 has both N-channel and P-channel output drivers, a buck and linear regulator and two OP-AMPs. It is highly suitable as a supply and output stage for many applications such as MCU power stage, I/O and sensor interface.

2. Features

- Supply voltage: 5VDC...36VDC
- 5V/20mA linear regulator
- Adjustable fix frequency buck regulator (8V...34V)
- 100mA P-channel and N-channel over-current & short-circuit protected open drain outputs
- 2 LED current sinks 2mA
- 2 operational amplifiers
- Buck & linear regulator may be connected parallel or in a series
- Package: QFN24 – Body size: 4mm x 4mm x 0.85mm
- RoHS compliant

3. Application

- Inductive Proximity Sensor
- Optical Switch
- Sensor Preamplifier
- LED Driver
- DC Motor Control
- HV Preamplifier
- Level Shifter
- UART – RS232 Converter
- Monoflop
- WDT and VDD Monitor
- Oscillator
- Over current and temperature protection
- Audio Amplifier
- MCU power stage, I/O and sensor interface

3.1. Example Application Schematic

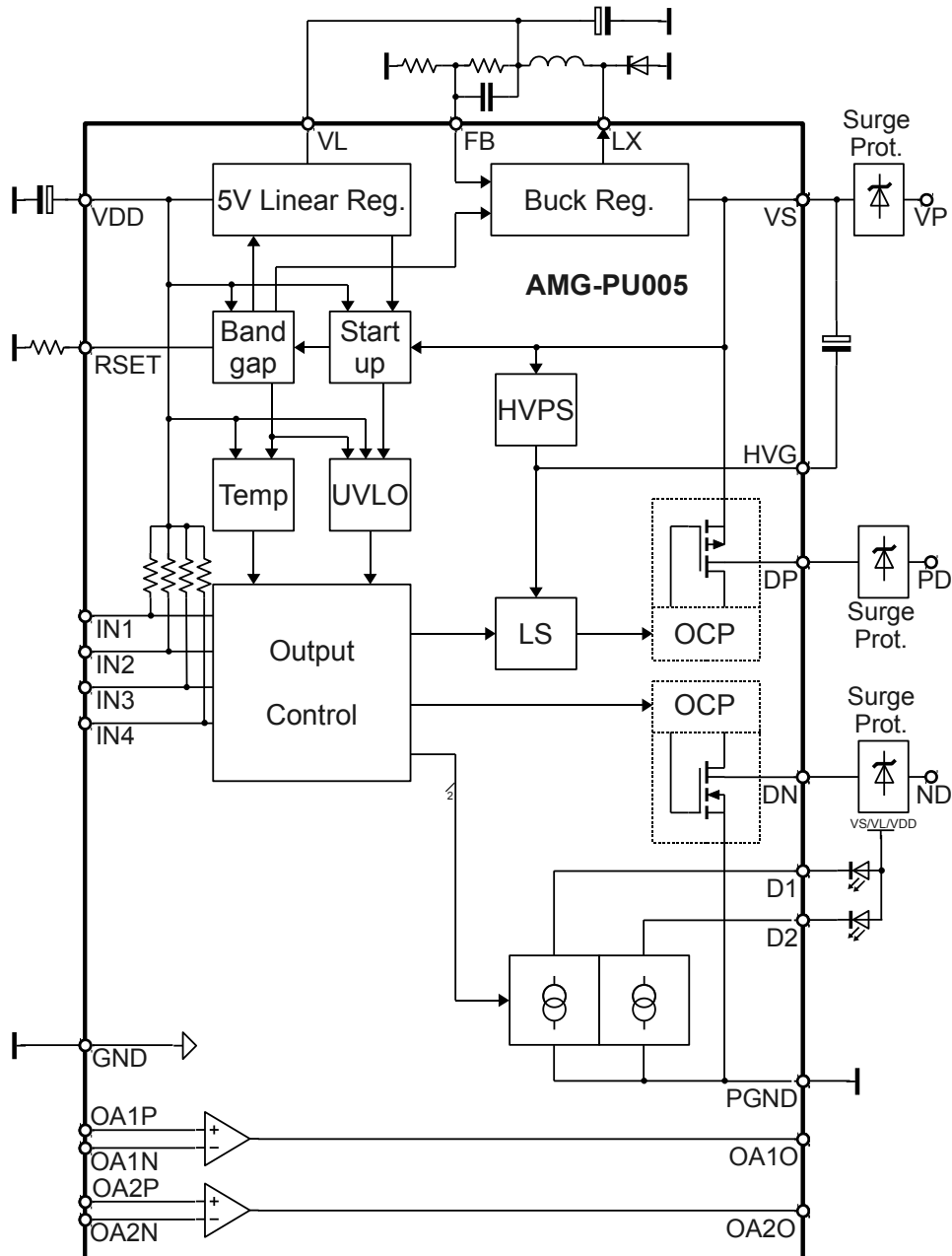


Figure 1: PU005 with basic external circuitry

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4. Block Diagram

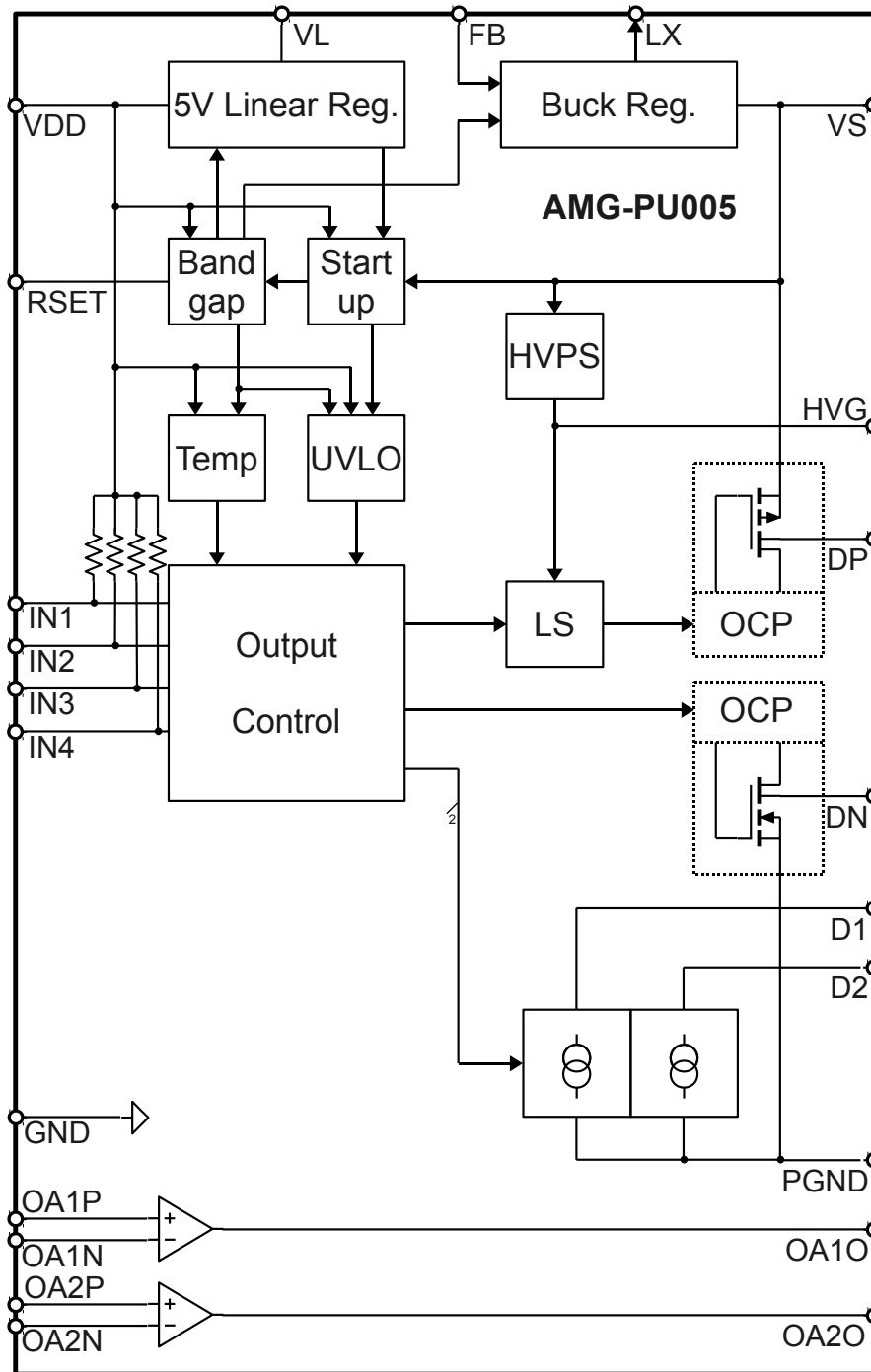


Figure 2: Block Diagram

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5. Block Descriptions

5.1. Output Control - Logic Table

| Inputs | | | | Outputs | | | |
|--------|-----|-----|-----|---------|-----|-----|-----|
| IN1 | IN2 | IN3 | IN4 | LS | HS | LD1 | LD2 |
| 1 | | | | | | | ON |
| 0 | | | | | | | OFF |
| | 1 | | | | ON | | |
| | 0 | | | | OFF | | |
| | | 1 | | ON | | | |
| | | 0 | | OFF | | | |
| | | | 1 | | | ON | |
| | | | 0 | | | OFF | |

5.2. Over Current Protection (OCP) Block

The OCP block prevents the N- and P-Driver open drain outputs from driving disruptive currents.

5.3. Level Shifter (LS)

Internal level shifter to translate switching signals from the low voltage domain to the high voltage domain. It is dedicated to drive the open drain P-Driver gate.

5.4. High Voltage Power Supply (HVPS)

The HVPS supplies the level shifter block with the high voltage needed to drive the open drain P-Driver gate. It supplies even the N-Driver's protection circuit and the buck regulator's driver stage.

5.5. Under Voltage Lock Out (UVLO)

The UVLO block detects under-voltage events on VDD and disables the outputs in case of such event. This prevents the IC from under-voltage driven malfunctions.

5.6. Over-Temperature Protection Block (Temp)

The Temp block prevents the IC from thermal overload. In case of such overload the outputs will be switched off.

5.7. Buck Regulator

This block allows to build an efficient step-down DC-DC converter. Depending on the load it supports continuous current mode, discontinuous current mode and cycle skipping mode. The Buck Regulator is over-current and short circuit protected.

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5.8. 5V Linear Regulator

The 5V Linear Regulator is a shunt regulator which can be used to generate about 5V from voltages up to 36V. It is over-current and short circuit protected.

5.9. Open Drain Drivers

The AMG-PU005 has got a N-Channel and P-Channel Driver with 100mA output current driving capability each. Both Drivers are built in Open Drain configuration. The drivers are over-current and over-temperature protected.

5.10. LED Current-Sink Blocks

The current sink blocks are dedicated to drive LEDs from a supply voltage (5-36V) with a current of 2mA each.

5.11. OP-Amp Blocks

The general purpose OP-Amp blocks allow the customer to built own I/O interfaces. The OP-Amps provide a rail-to-rail input and output.

6. Pinning

| PIN# | Symbol | Description |
|------|--------|---|
| 1 | VDD | Linear regulator output and decoupling output |
| 2 | VL | Linear regulator input voltage |
| 3 | HVG | HV Decoupling |
| 4 | LX | Buck regulator output |
| 5 | VS | Supply voltage |
| 6 | DP | Open drain output of P-Driver |
| 7 | DN | Open drain output of N-Driver |
| 8 | PGND | Power Ground |
| 9 | D1 | LED current sink input 1 |
| 10 | D2 | LED current sink input 2 |
| 11 | GND | Analog GND |
| 12 | RSET | Bias Current Set Resistor |
| 13 | OA1O | OP-AMP 1 output |
| 14 | OA1N | Inverting input of OP-AMP 2 |
| 15 | OA1P | Non inverting input of OP-AMP 1 |
| 16 | OA2P | Non inverting input of OP-AMP 2 |
| 17 | OA2N | Inverting input of OP-AMP 2 |
| 18 | OA2O | OP-AMP 2 output |

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| PIN# | Symbol | Description |
|------|--------|--------------------------------|
| 19 | IN1 | Logic Input |
| 20 | IN2 | Logic Input |
| 21 | IN3 | Logic Input |
| 22 | IN4 | Logic Input |
| 23 | n.c. | Not connected |
| 24 | FB | Buck regulator feed back input |

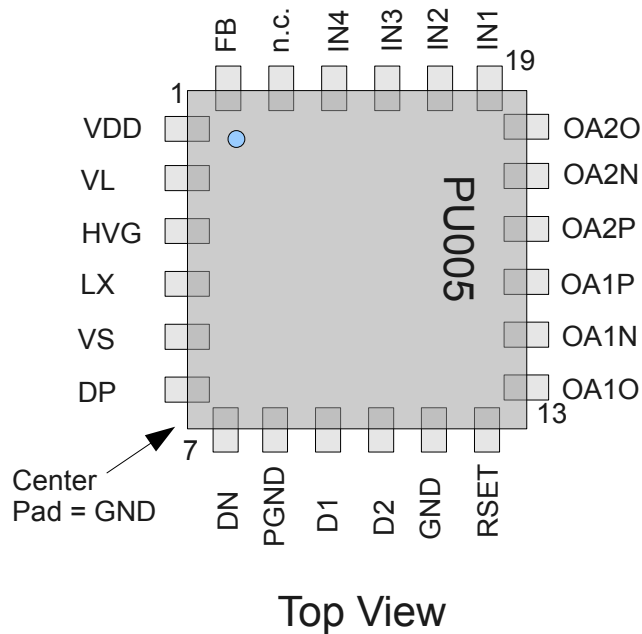


Figure 3: QFN24 Pinout

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7. Absolute Maximum Ratings

The Absolute Maximum Ratings may not be exceeded under any circumstances.

| # | Symbol | Parameter | Min | Max | Unit |
|----|------------------|--|-------|---------------|------|
| 1 | V_{VS} | Supply voltage | | 37.8 | V |
| 2 | V_{pin_hv} | Maximum voltage at pins DP, DN, D1, D2, LX, VL, HVG (high voltage pins) | -0.3 | $V_{VS}+0.3$ | V |
| 3 | V_{VDD} | Maximum analog voltage supply (if applied from external) | | 5.5 | V |
| 4 | V_{pin_lv} | Maximum voltage at all other pins (low voltage pins) | -0.3 | $V_{VDD}+0.3$ | V |
| 5 | I_{DN}, I_{DP} | Drain output current | | 100 | mA |
| 6 | I_{BO} | Buck regulator output current for external loads | | 50 | mA |
| 7 | I_{VDD} | Linear regulator output current for external loads | | 25 | mA |
| 8 | T_{stg} | Storage temperature range (see chapter 14.2) | -55 | 150 | °C |
| 9 | T_J | Junction temperature | -55 | 150 | °C |
| 10 | V_{ESD} | ESD Protection Test voltage (HBM, MIL-STD-883D, Method 3015.7 class 2) ¹⁾ | -2000 | 2000 | V |

Note:

¹⁾ ESD test condition valid for any pin without external protection circuitry

8. Electrical Characteristics

8.1. Operational Range

| # | Symbol | Parameter | Min | Max | Unit |
|---|-------------|--|------|-----|------|
| 1 | $V_{VS,BS}$ | Supply voltage range using buck and linear regulator | 7.5 | 36 | V |
| 2 | $V_{VS,SO}$ | Supply voltage range using linear regulator only | 5.75 | 36 | V |
| 3 | $V_{VS,LX}$ | Supply voltage range using buck regulator only | 6.5 | 36 | V |
| 4 | V_{VDD} | Analog supply voltage range if applied externally | 4.5 | 5.5 | V |
| 5 | T_a | Ambient operating temperature | -25 | 85 | °C |
| 6 | fsw | I/O switching frequency | 400 | 600 | kHz |

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8.2. DC Characteristics

Unless otherwise specified, the minimum and maximum characteristics contain the spread of values guaranteed within the specified operating conditions.

Unless otherwise specified, typical values are given with $V_{VS} = 36V$, $T_J = 25^\circ C$

| # | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------------|----------------|--|--|------------|----------|---------------|---------|
| General Parameters | | | | | | | |
| 1 | I_{VS1} | Supply current w/o external loads, with buck regulator in steady state | $V_{VS}=36V$ | | | 1 | mA |
| 2 | I_{VS2} | Supply current w/o external loads, buck regulator deactivated | $V_{VS}=36V$ | | 260 | | μA |
| 3 | V_{RSET} | Bias current reference voltage | | | 1.25 | | V |
| Buck Regulator | | | | | | | |
| 4 | V_{VL} | Output voltage range (adjustable by external resistor divider) | $V_{VS} \geq 10V$ $I_{LoadExt B}=40mA$ | 4.75 | 8 | $V_{VS}-2$ | V |
| 5 | $V_{Drop B}$ | Saturation voltage drop | $I_{loadextB}=40mA$ | | 2 | | V |
| 6 | V_{FB} | Reference voltage | | | 2.5 | | V |
| 7 | V_{FB_OV} | Overvoltage lockout | | | 2.75 | | V |
| 8 | I_{BUCK} | Operating current | $V_{FB} < V_{FB_OV}$ | | TBD | | mA |
| 9 | V_{FB_BOFF} | Buck switch off input voltage | | | 3.5 | V_{DD} | V |
| 5V Linear Regulator | | | | | | | |
| 10 | V_{VDD} | Output voltage | $6V \leq V_{VL} \leq 16V$ $I_{LoadExt S}=20mA$ | 4.75 | 5 | 5.25 | V |
| 11 | V_{VDDsat} | Output voltage saturated | $5.5V \leq V_{VL} \leq 6.5V$ $I_{LoadExt S}=20mA$ | $V_{VL}-1$ | | | V |
| 12 | $V_{Drop S}$ | Saturation voltage drop | $I_{LoadExt S}=20mA$ | | 1 | | V |
| Open Drain Drivers (FETs) | | | | | | | |
| 13 | $V_{Drop DP}$ | P-channel R_{DSon} voltage drop | $V_{VS}=36V$ $I_{loadP}=-100mA$ | | | 1 | V |
| 14 | $V_{Drop DN}$ | N-channel R_{DSon} voltage drop | $V_{VS}=36V$ $I_{loadN}=100mA$ | | | 1 | V |
| LED current sinks | | | | | | | |
| 15 | I_{Dx} | LED Driver constant current sink | $V_{Dx}=36V$ | 1.8 | 2 | 2.2 | mA |
| OP-AMPS | | | | | | | |
| 16 | $V_{IN,OAx}$ | OP-AMP input voltage range | | 0.5 | | $V_{VDD}-0.5$ | V |
| 17 | $V_{IN,OFFS}$ | Input Offset voltage | $I_{OUT}=0\mu A$ $I_{OUT}=\pm 100\mu A$ | | 10 15 | | mV |
| 18 | $I_{IN,OAx}$ | OP-AMP input current | | | | 200 | nA |
| 19 | $V_{OUT,OAx}$ | OP-AMP output voltage range | | 0 | | V_{VDD} | V |
| 20 | $I_{OUT,OAx}$ | OP-AMP output current driving capability | $V_{OUT,C}=V_{VDD}/2$ | | | ± 1 | mA |

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| # | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----|------------|--------------------------|------------------------|-----------------|-----|-----------------|---------|
| | | Logic inputs | | | | | |
| 21 | $I_{IN,H}$ | Logic HIGH input current | $V_{VDD}=4.5\sim 5.5V$ | -0.1 | | 0.1 | μA |
| 22 | $I_{IN,L}$ | Logic LOW input current | $V_{VDD}=4.5\sim 5.5V$ | -50 | | -10 | μA |
| 23 | $V_{IN,L}$ | Logic LOW input voltage | | 0 | | $0.3^* V_{VDD}$ | V |
| 24 | $V_{IN,H}$ | Logic HIGH input voltage | | $0.5^* V_{VDD}$ | | V_{VDD} | V |

8.3. AC Characteristics

Unless otherwise specified, the minimum and maximum characteristics contain the spread of values guaranteed within the specified operating conditions and the technology process parameter range.

Unless otherwise specified, typical values are given with $V_{VS} = 36V$, $T_J = 25^\circ C$

| # | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|----------|------------------------------|---------------------|-----|-------|-----|------|
| | | Buck regulator | | | | | |
| 1 | fsw | Output switching frequency | | | 500 | | kHz |
| 2 | DC | Duty Cycle | | | | 95 | % |
| | | OP-Amps | | | | | |
| 3 | f_T | Transit frequency | Open loop | 1 | 2.8 | | MHz |
| 4 | gvmax | Max voltage gain | Open loop | | 105 | | dB |
| 5 | gv | Voltage gain | Open loop; 10kHz | 40 | 49.5 | | dB |
| 6 | CMRR | Common mode rejection ratio | 10kHz | TBD | -71 | | dB |
| 7 | PSRR | Power supply rejection ratio | 10kHz | TBD | -51.3 | | dB |
| 8 | M_{PH} | Phase Margin | open loop (f_T) | | 72.7 | | deg |

8.4. Application Notes

8.4.1. Supply concepts

The AMG-PU005 can be used with different supply strategies and ranges. It contains a buck regulator and a linear regulator. The minimum voltage drops of the regulators to be considered are:

- Buck regulator: $V_{DROPB}=2V$ (to be adjusted by external resistor divider)
- Linear regulator: $V_{DROPL}=1V$ (in case of saturation, $V_{VL}\leq 6V$).

Thus none or one or both regulators may be used (see operational voltage range limitations).

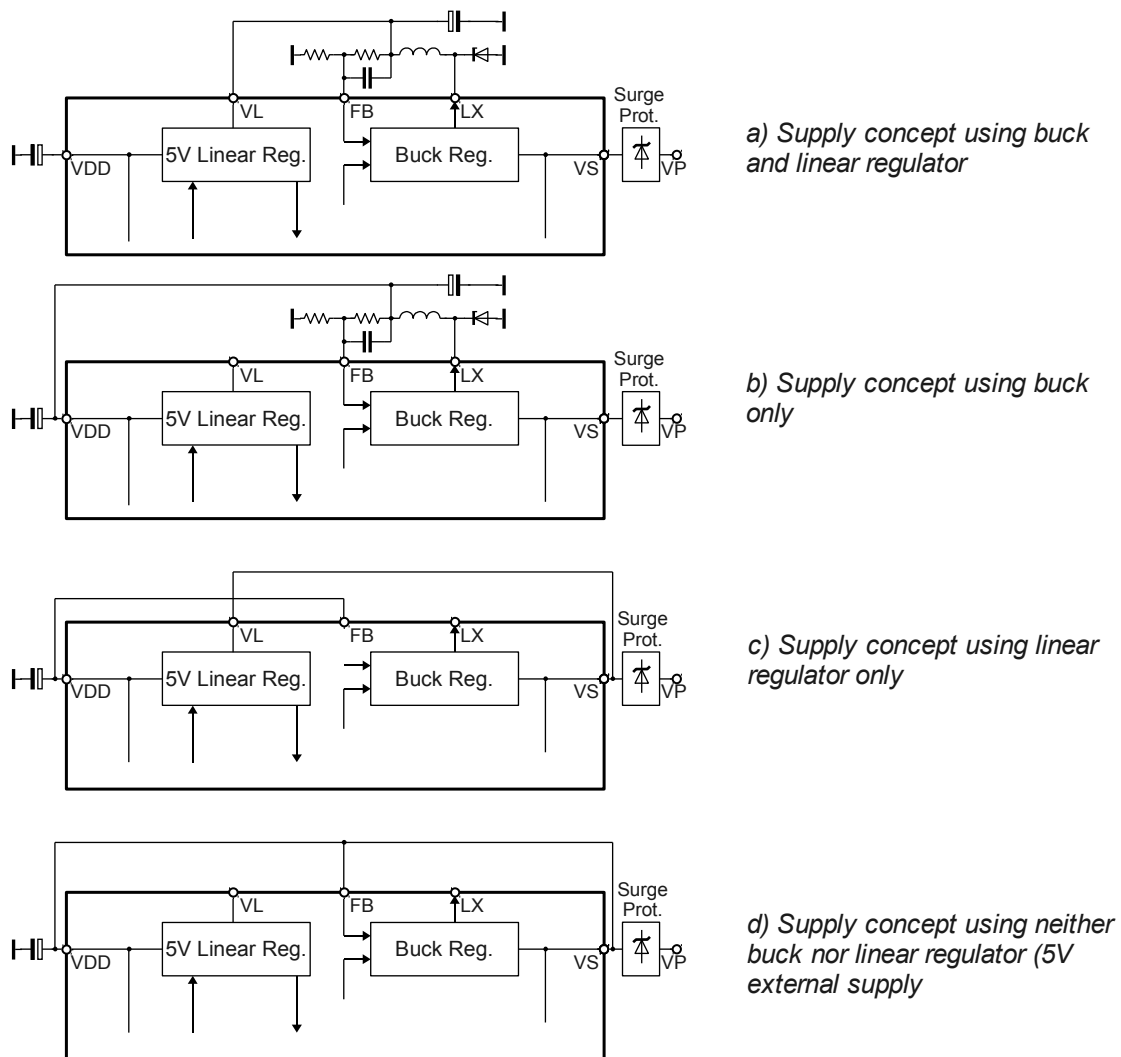


Figure 4: Different supply concepts overview

The buck regulator is able to drive about 40mA external load in total. If it has to supply the linear regulator the maximum external load current will be reduced by the load of the linear regulator (max. 20mA).

The buck regulator's external coil should be larger than 220uH.

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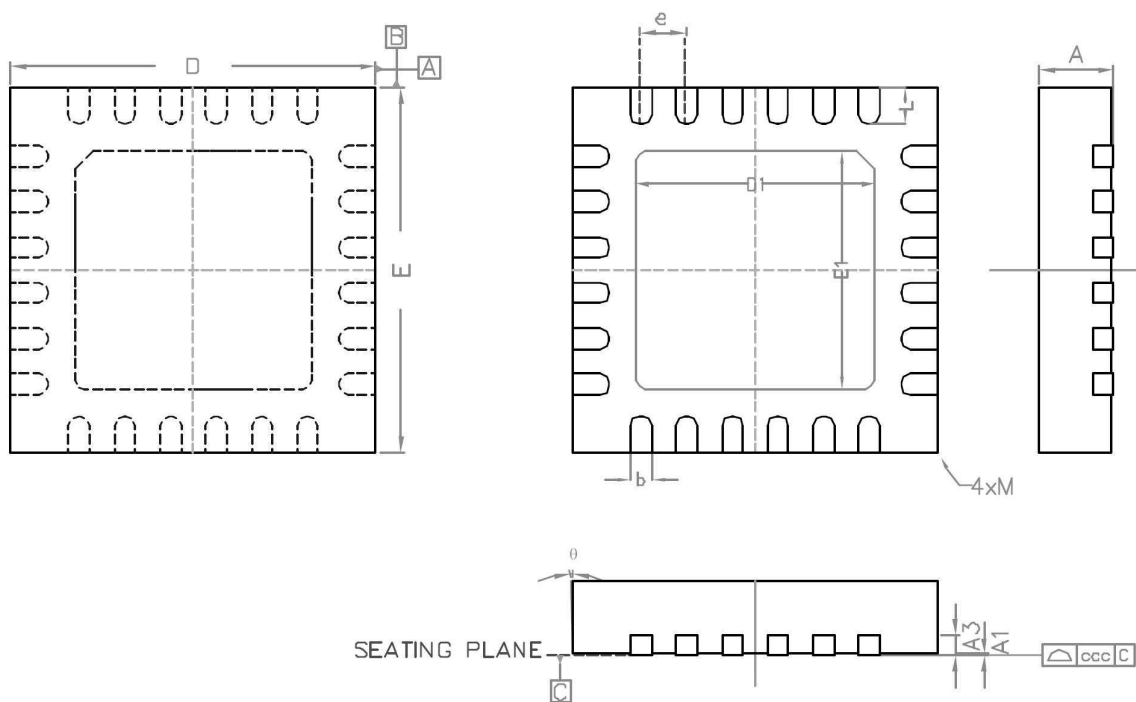
8.4.2. Surge Protection

Pins which are subject to surges need to be adequately protected by external protection devices and appropriate PCB layout. Device functionality might get interrupted during surges.

Alpha microelectronics could give you some layout and circuitry guidelines for good surge protection.

9. IC-Package

9.1. QFN24 – Quad Flat No-leads Package, 24 leads, RoHS compliant



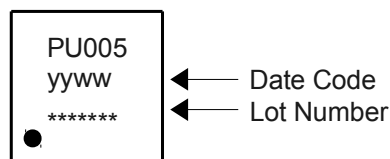
| SYMBOL | Dimensions in mm, angles in deg | | |
|--------|---------------------------------|-------|-------|
| | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0 | 0.010 | 0.030 |
| A3 | - | 0.20 | - |
| b | 0.18 | 0.23 | 0.28 |
| D | 3.95 | 4.00 | 4.03 |
| D1 | - | 2.60 | - |
| E | 3.95 | 4.00 | 4.03 |
| E1 | - | 2.60 | - |

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| | | | |
|----------|------|------|------|
| e | - | 0.50 | - |
| L | 0.35 | 0.4 | 0.45 |
| Θ | -12 | - | 0 |
| ccc | - | 0.08 | - |
| M | - | - | 0.05 |

10. IC-Marking

Top Marking by Laser



11. Ordering Information

AMG-PU005-IQN24R (QFN24, Tape & Reel)

12. Notes and Cautions

12.1. ESD Protection

The Requirements for Handling Electrostatic Discharge Sensitive Devices are described in the JEDEC standard JESD625-A. Please note the following recommendations:

- When handling the device, operators must be grounded by wearing a for the purpose designed grounded wrist strap with at least 1M Ω resistance and direct skin contact.
- Operators must at all times wear ESD protective shoes or the area should be surrounded by for ESD protection intended floor mats.
- Opening of the protective ESD package that the device is delivered in must only occur at a properly equipped ESD workbench. The tape with which the package is held together must be cut with a sharp cutting tool, never pulled or ripped off.
- Any unnecessary contact with the device or any unprotected conductive points should be avoided.
- Work only with qualified and grounded tools, measuring equipment, casing and workbenches.
- Outside properly protected ESD-areas the device or any electronic assembly that it may be part of should always be transported in EGB/ESD shielded packaging.

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12.2. Storage conditions

The AMG-PU005 corresponds to moisture sensitivity classification ML2 , according to JEDEC standard J-STD-020, and should be handled and stored according to J-STD-033.

13. Disclaimer

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